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USB333x

Industry's Smallest Hi-Speed USB Transceiver with Single Supply Operation

PRODUCT FEATURES

- USB-IF Battery Charging 1.2 Specification Compliant
- Link Power Management (LPM) Compliant
- Integrated ESD protection circuits
- Up to ±25kV IEC Air Discharge without external devices
- Over-Voltage Protection circuit (OVP) protects the VBUS pin from continuous DC voltages up to 30V
- Integrated USB Switch (USB3331, USB3336, and USB3338)
  — No degradation of Hi-Speed electrical characteristics
  — Allows single USB port of connection by providing switching function for:
    – Battery charging
    – Stereo and mono/mic audio
    – USB Full-Speed/Low-Speed data
- SMSC RapidCharge Anywhere™ Provides:
  — 3-times the charging current through a USB port over traditional solutions
  — USB-IF Battery Charging 1.2 compliance to any portable device
  — Charging current up to 1.5Amps via compatible USB host or dedicated charger
  — Dedicated Charging Port (DCP), Charging (CDP) & Standard (SDP) Downstream Port support
- flexPWR® Technology
  — Extremely low current design ideal for battery powered applications
  — "Sleep" mode tri-states all ULPI pins and places the part in a low current state
  — 1.8V to 3.3V IO Voltage (USB3333)
- Single Power Supply Operation
  — Integrated 1.8V regulator
  — Integrated battery to 3.3V regulator
    – 100mV dropout voltage
- PHYBoost
  — Programmable USB transceiver drive strength for recovering signal integrity
- VariSense™
  — Programmable USB receiver sensitivity
- "Wrapper-less" design for optimal timing performance and design ease
  — Low Latency Hi-Speed Receiver (43 Hi-Speed clocks Max) allows use of legacy UTMI Links with a ULPI bridge

- External Reference Clock operation available
  — ULPI Clock In Mode (60MHz sourced by Link)
  — 0 to 3.6V input drive tolerant
  — Able to accept "noisy" clock sources as reference to internal, low-jitter PLL
  — USB3330 and USB3333 support multiple frequencies
- Smart detection circuits allow identification of USB charger, headset, or data cable insertion
- Includes full support for the optional On-The-Go (OTG) protocol detailed in the On-The-Go Supplement Revision 2.0 specification
- Supports the OTG Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- UART mode for non-USB serial data transfers
- Internal 5V cable short-circuit protection of ID, DP and DM lines to VBUS or ground
- Industrial Operating Temperature -40°C to +85°C
- 25 ball, WLCSP lead-free RoHS Compliant package (1.97 x 1.97 x 0.53 mm height)

Applications

The USB333x is the solution of choice for any application where a Hi-Speed USB connection is desired and when board space, power, and interface pins must be minimized.

- Cell Phones
- PDAs
- MP3 Players
- GPS Personal Navigation
- Scanners
- External Hard Drives
- Digital Still and Video Cameras
- Portable Media Players
- Entertainment Devices
- Printers
- Set Top Boxes
- Video Record/Playback Systems
- IP and Video Phones
- Gaming Consoles

DATASHEET

Order Numbers:

ORDER NUMBER	REFCLK FREQUENCY (Note 0.1)	PACKAGE TYPE	REEL SIZE
USB3330E-GL-TR	Selectable See Table 5.2	25 Ball, WLCSP Lead-Free RoHS Compliant Package (tape and reel)	3,000 pieces
USB3331E-GL-TR	26MHz		
USB3333E-GL-TR	Selectable See Table 5.3		
USB3336E-GL-TR	19.2MHz		
USB3338E-GL-TR	38.4MHz		

Note 0.1 All versions support ULPI Clock Input Mode (60MHz input at REFCLK)

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.

0.1 Reference Documents

UTMI+ Low Pin Interface (ULPI) Specification, Revision 1.1

Universal Serial Bus Specification, Revision 2.0

On-The-Go Supplement to the USB2.0 Specification, Revision 1.3

On-The-Go Supplement to the USB2.0 Specification, Revision 2.0

USB Battery Charging Specification, Revision 1.2

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Chapter 1 General Description

SMSC's USB333x is a family of High Speed USB 2.0 Transceivers that provides a physical layer (PHY) solution well-suited for portable electronic devices. Both commercial and industrial temperature applications are supported.

Each model in the USB333x family may use a 60MHz reference clock or the model-number specific reference clock shown in Order Numbers: on page 2. The USB3330 and USB3333 can support several different frequencies driven on the **REFCLK** pin. The configuration of the frequency selection pins set the desired reference frequency.

Several advanced features make the USB333x the transceiver of choice by reducing both eBOM part count and printed circuit board (PCB) area. Outstanding ESD robustness eliminates the need for external ESD protection devices in typical applications. The internal Over-Voltage Protection circuit (OVP) protects the USB333x from voltages up to 30V on the **VBUS** pin. By using a reference clock from the Link, the USB333x removes the cost of a dedicated crystal reference from the design. The USB333x includes integrated 3.3V and 1.8V regulators, making it possible to operate the device from a single power supply.

The USB333x is optimized for use in portable applications where a low operating current and standby current is essential. The USB333x also supports the Link Power Management protocol (LPM) to further reduce USB operating currents.

The USB333x also includes integrated battery charger detection circuitry. These circuits are used to detect the attachment of a USB Charger as described in Section 5.8. By sensing the attachment to a USB Charger, a product using the USB333x can draw more than 500mA from the USB connector.

The USB333x meets all of the electrical requirements for a High Speed USB Host, Device, or an On-the-Go (OTG) transceiver. In addition to the supporting USB signaling, the USB333x also provides USB UART mode and, in versions with the integrated USB switch, USB Audio mode.

USB333x uses the industry standard UTMI+ Low Pin Interface (ULPI) to connect the USB PHY to the Link. ULPI uses a method of in-band signaling and status byte transfers between the Link and PHY to facilitate a USB session with only twelve pins.

The USB333x uses SMSC's "wrapper-less" technology to implement the ULPI interface. This "wrapper-less" technology allows the PHY to achieve a low latency transmit and receive time. SMSC's low latency transceiver allows an existing UTMI Link to be reused by adding a UTMI to ULPI bridge. By adding a bridge to the ASIC the existing and proven UTMI Link IP can be reused.

Versions of the USB333x with the integrated USB switch enable a single USB port of connection.
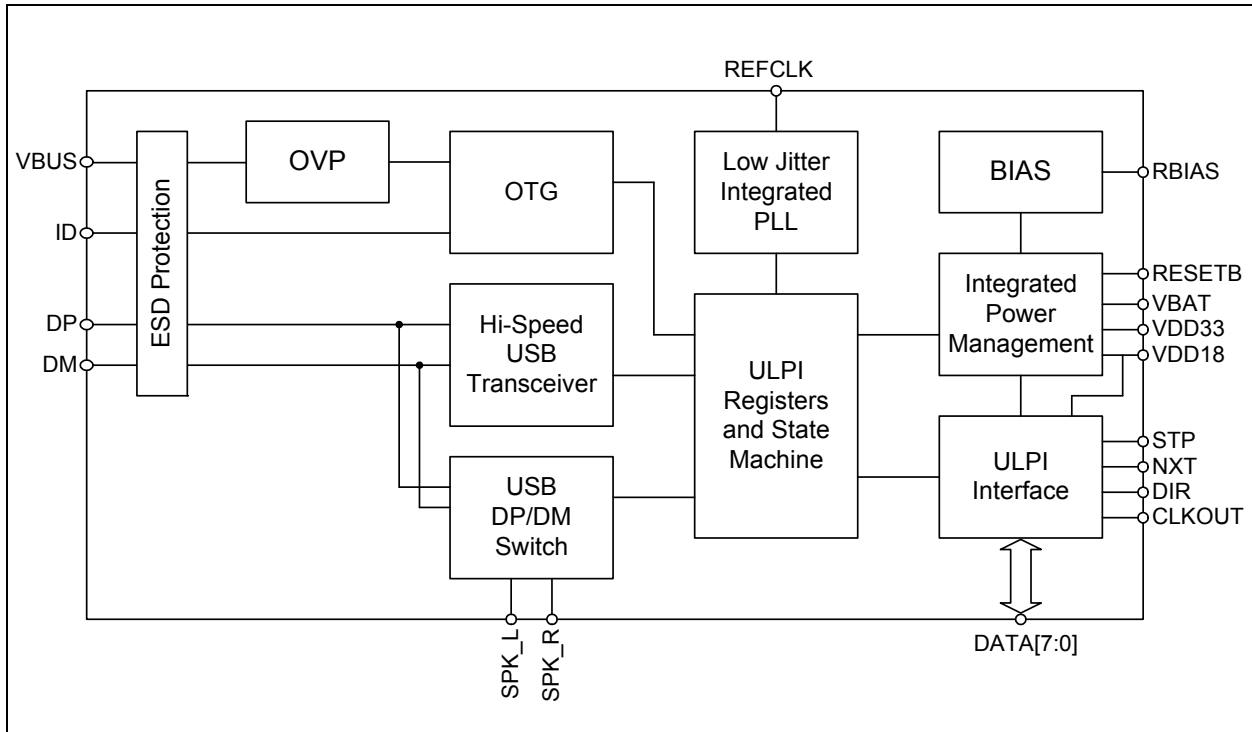
Figure 1.1 Block Diagram (USB3331, USB3336, and USB3338)

In USB Audio mode, a switch connects the **DP** pin to the **SPK_R** pin, and another switch connects he **DM** pin to the **SPK_L** pin. These switches are shown in the lower left-hand corner of Figure 5.1.The USB333x can be configured to enter USB Audio mode as described in Section 6.7.2. In addition, these switches are on when the **RESETB** pin of the USB333x is asserted. The USB Audio mode enables audio signaling from a single USB port of connection, and the switches may also be used to connect Full Speed USB from another transceiver to the USB connector.
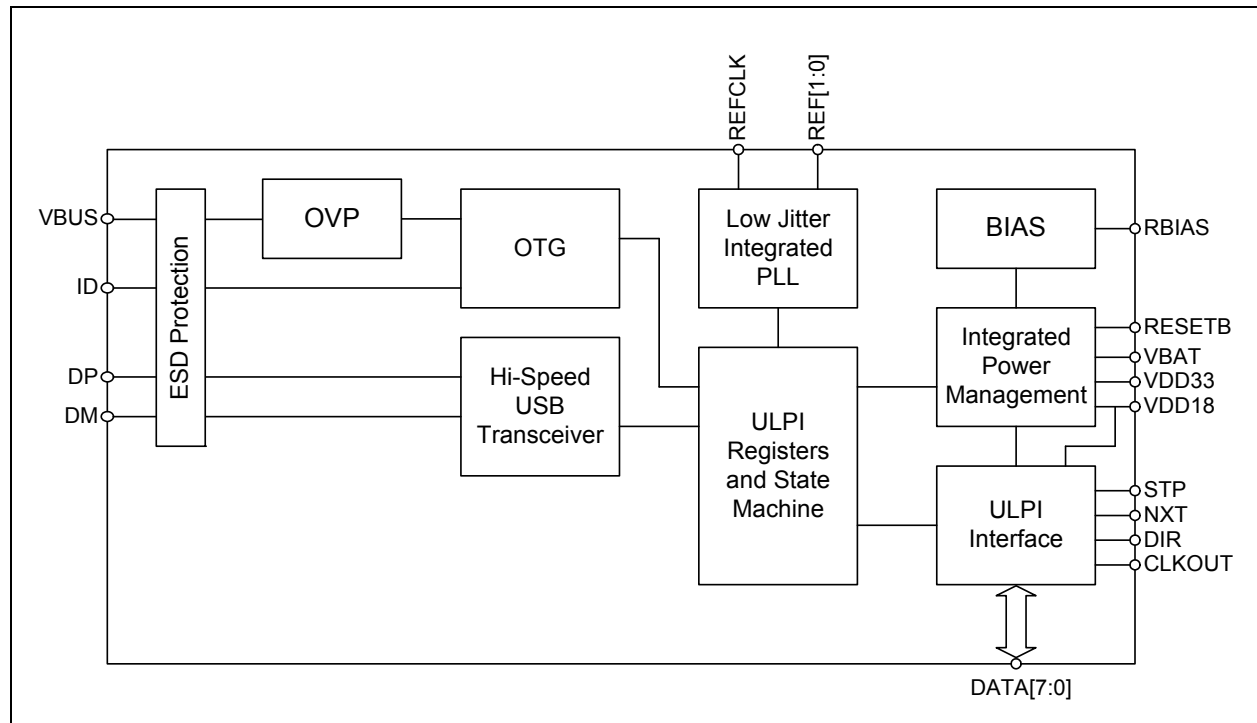
Figure 1.2 Block Diagram (USB3330)
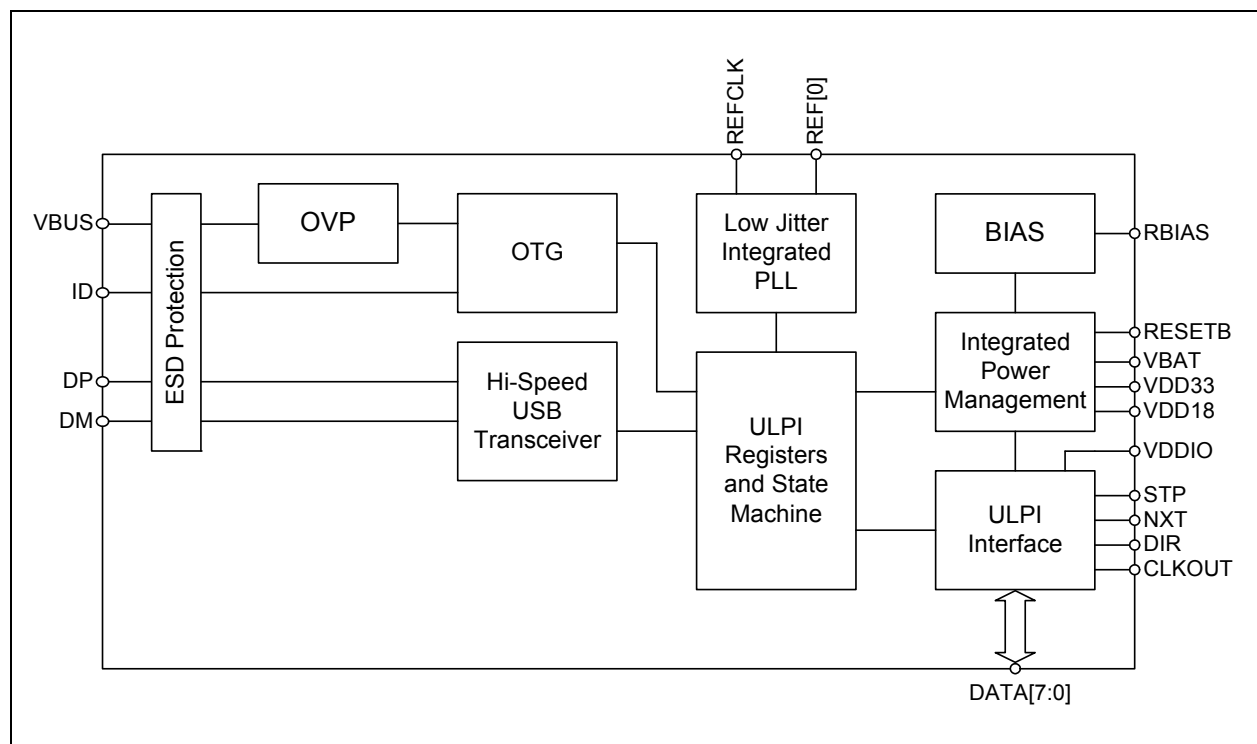
Figure 1.3 Block Diagram (USB3333)

The USB333x includes an integrated 3.3V LDO regulator that is used to generate 3.3V from power applied to the **VBAT** pin. The voltage on the **VBAT** pin can range from 3.0 to 5.5V. The regulator dropout voltage is less than 100mV which allows the PHY to continue USB signaling when the voltage on **VBAT** drops to 3.0V. The USB transceiver will continue to operate at lower voltages, although some parameters may be outside the limits of the USB-IF specification for Full Speed USB operation. The **VBAT** and **VDD33** pins should *never* be connected together.

In USB UART mode, the USB333x **DP** and **DM** pins are redefined to enable pass-through of asynchronous serial data. The USB333x will enter UART mode when programmed, as described in Section 6.7.1.

Chapter 2 USB333x Pin Locations and Definitions

2.1 USB333x Ball Locations and Descriptions

2.1.1 Package Diagram with Ball Locations

The illustration below is viewed from the top of the package.
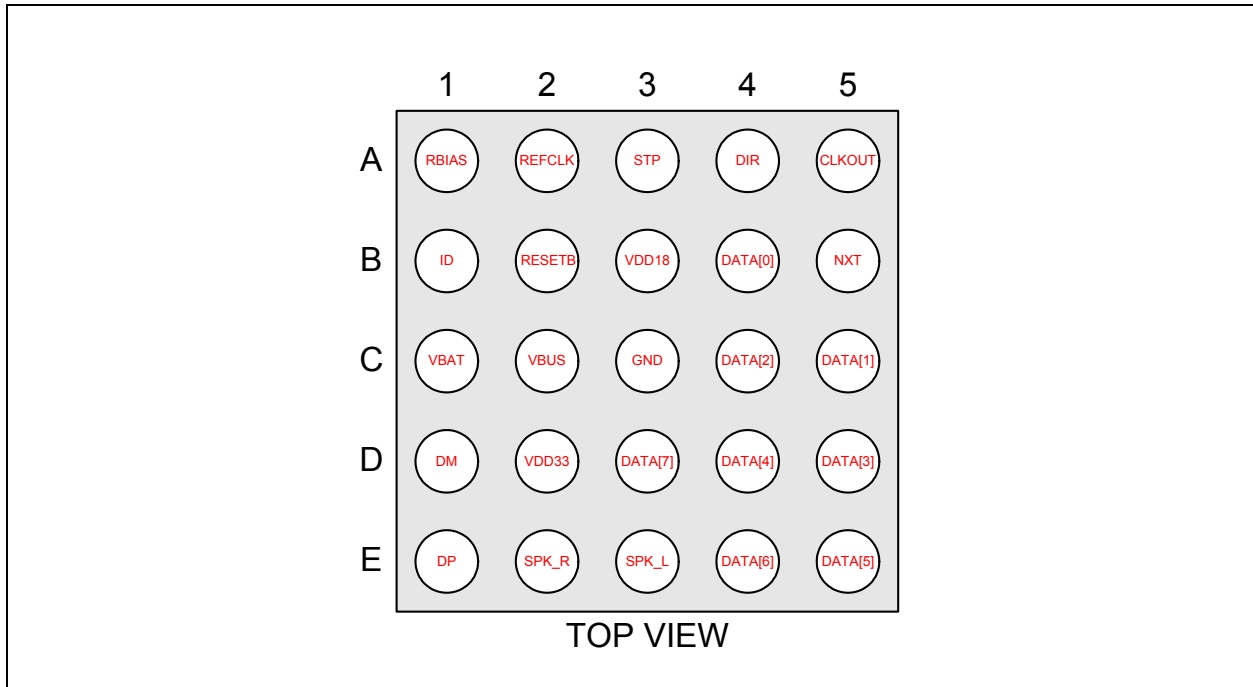
Figure 2.1 USB3331, USB3336, and USB3338 Ball Locations - Top View
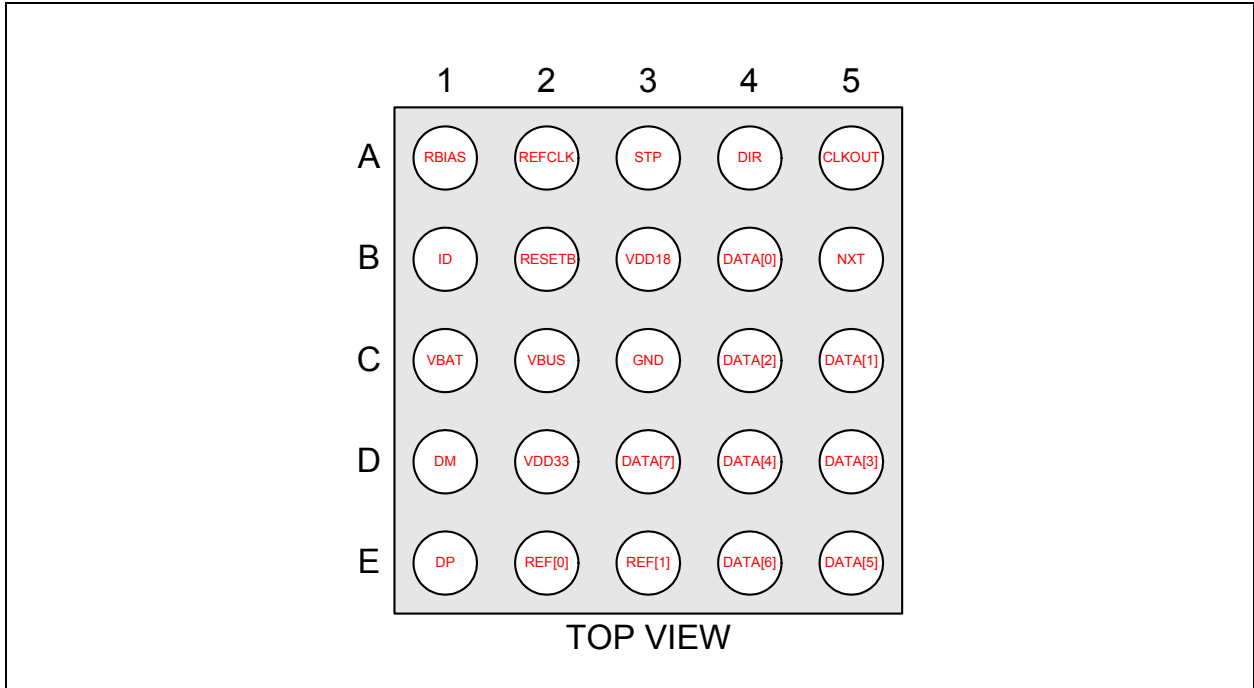
Figure 2.2 USB3330 Ball Locations - Top View
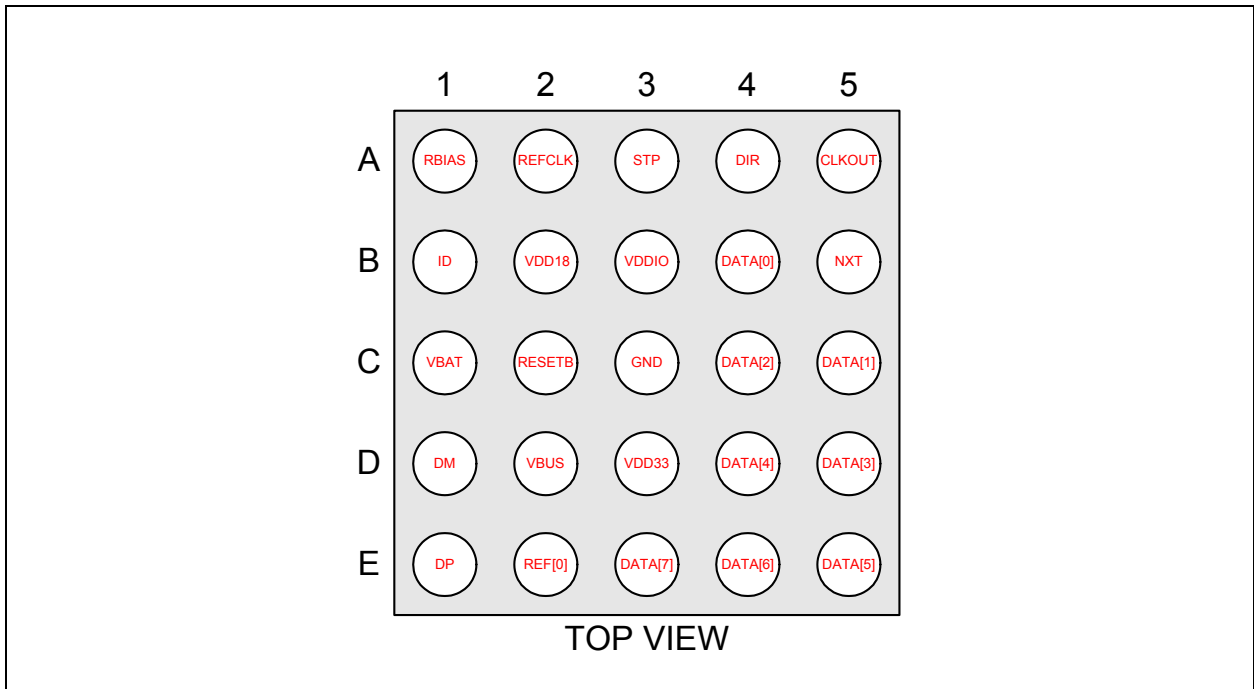
Figure 2.3 USB3333 Ball Locations - Top View

2.1.2   Ball Definitions

The following table details the ball definitions for the figure above.

Table 2.1 USB3331, USB3336, and USB3338 Pin Description

BALL	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
B1	ID	Input, Analog	N/A	For device applications the **ID** pin is connected to **VDD33**. For Host applications **ID** is grounded. For OTG applications the **ID** pin is connected to the USB connector.
C2	VBUS	I/O, Analog	N/A	This pin is used for the VBUS comparator inputs and for VBUS pulsing during session request protocol. An external resistor, R_{VBUS}, is required between this pin and the USB connector.
C1	VBAT	Power	N/A	Regulator input. The regulator supply can be from 5.5V to 3.0V.
D2	VDD33	Power	N/A	3.3V Regulator Output. A 1.0uF (<1 ohm ESR) bypass capacitor to ground is required for regulator stability. The bypass capacitor should be placed as close as possible to the USB333x.
D1	DM	I/O, Analog	N/A	D- pin of the USB cable.
E1	DP	I/O, Analog	N/A	D+ pin of the USB cable.
E2	SPK_R	I/O, Analog	N/A	USB switch in/out for **DP** signals.
E3	SPK_L	I/O, Analog	N/A	USB switch in/out for **DM** signals.
D3	DATA[7]	I/O, CMOS	N/A	ULPI bi-directional data bus. **DATA[7]** is the MSB.
E4	DATA[6]	I/O, CMOS	N/A	ULPI bi-directional data bus.
E5	DATA[5]	I/O, CMOS	N/A	ULPI bi-directional data bus.
D4	DATA[4]	I/O, CMOS	N/A	ULPI bi-directional data bus.
A5	CLKOUT	Output, CMOS	N/A	**ULPI Clock Out Mode:** 60MHz ULPI clock output. All ULPI signals are driven synchronous to the rising edge of this clock. **ULPI Clock In Mode:** Connect this pin to **VDD18** to configure 60MHz ULPI Clock IN mode as described in Section 5.4.1.
D5	DATA[3]	I/O, CMOS	N/A	ULPI bi-directional data bus.
C4	DATA[2]	I/O, CMOS	N/A	ULPI bi-directional data bus.
C5	DATA[1]	I/O, CMOS	N/A	ULPI bi-directional data bus.

Table 2.1 USB3331, USB3336, and USB3338 Pin Description (continued)

BALL	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
B4	DATA[0]	I/O, CMOS	N/A	ULPI bi-directional data bus. **DATA[0]** is the LSB.
B5	NXT	Output, CMOS	High	The PHY asserts **NXT** to throttle the data. When the Link is sending data to the PHY, **NXT** indicates when the current byte has been accepted by the PHY.
A4	DIR	Output, CMOS	N/A	Controls the direction of the data bus. When the PHY has data to transfer to the Link, it drives **DIR** high to take ownership of the bus. When the PHY has no data to transfer it drives **DIR** low and monitors the bus for commands from the Link.
A3	STP	Input, CMOS	High	The Link asserts **STP** for one clock cycle to stop the data stream currently on the bus. If the Link is sending data to the PHY, **STP** indicates the last byte of data was on the bus in the previous cycle.
B3	VDD18	Power	N/A	1.8V Regulator Output. A 1.0uF (<1 ohm ESR) bypass capacitor to ground is required for regulator stability. The bypass capacitor should be placed as close as possible to the USB333x.
B2	RESETB	Input, CMOS,	Low	When low, the part is suspended and the 3.3V and 1.8V regulators are disabled. When high, the USB333x will operate as a normal ULPI device, as described in Section 5.5.1. The state of this pin may be changed asynchronously to the clock signals. When asserted for a minimum of 1 microsecond and then de-asserted, the ULPI registers are reset to their default state and all internal state machines are reset.
A2	REFCLK	Input, CMOS	N/A	**ULPI Clock Out Mode:** Model-specific reference clock. See Order Numbers: on page 2. **ULPI Clock In Mode:** 60MHz ULPI clock input.
A1	RBIAS	Analog, CMOS	N/A	Bias Resistor pin. This pin requires an 8.06kΩ (±1%) resistor to ground, placed as close as possible to the USB333x. Nominal voltage during ULPI operation is 0.8V.
C3	GND	Ground	N/A	Ground.

Table 2.2 USB3330 Pin Description

BALL	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
B1	ID	Input, Analog	N/A	For device applications the **ID** pin is connected to **VDD33**. For Host applications **ID** is grounded. For OTG applications the **ID** pin is connected to the USB connector.
C2	VBUS	I/O, Analog	N/A	This pin is used for the VBUS comparator inputs and for VBUS pulsing during session request protocol. An external resistor, R_{VBUS}, is required between this pin and the USB connector.

Table 2.2 USB3330 Pin Description (continued)

BALL	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
C1	VBAT	Power	N/A	Regulator input. The regulator supply can be from 5.5V to 3.0V.
D2	VDD33	Power	N/A	3.3V Regulator Output. A 1.0uF (<1 ohm ESR) bypass capacitor to ground is required for regulator stability. The bypass capacitor should be placed as close as possible to the USB333x.
D1	DM	I/O, Analog	N/A	D- pin of the USB cable.
E1	DP	I/O, Analog	N/A	D+ pin of the USB cable.
E2	REF[0]	I/O, Digital 3.3V	N/A	Used to select REFCLK frequency. Connect to ground or VDD33. Refer to Table 5.1 for frequency selection options.
E3	REF[1]	I/O, Digital 3.3V	N/A	Used to select REFCLK frequency. Connect to ground or VDD33. Refer to Table 5.1 for frequency selection options.
D3	DATA[7]	I/O, CMOS	N/A	ULPI bi-directional data bus. **DATA[7]** is the MSB.
E4	DATA[6]	I/O, CMOS	N/A	ULPI bi-directional data bus.
E5	DATA[5]	I/O, CMOS	N/A	ULPI bi-directional data bus.
D4	DATA[4]	I/O, CMOS	N/A	ULPI bi-directional data bus.
A5	CLKOUT	Output, CMOS	N/A	**ULPI Clock Out Mode:** 60MHz ULPI clock output. All ULPI signals are driven synchronous to the rising edge of this clock. **ULPI Clock In Mode:** Connect this pin to **VDD18** to configure 60MHz ULPI Clock IN mode as described in Section 5.4.1.
D5	DATA[3]	I/O, CMOS	N/A	ULPI bi-directional data bus.
C4	DATA[2]	I/O, CMOS	N/A	ULPI bi-directional data bus.
C5	DATA[1]	I/O, CMOS	N/A	ULPI bi-directional data bus.
B4	DATA[0]	I/O, CMOS	N/A	ULPI bi-directional data bus. **DATA[0]** is the LSB.
B5	NXT	Output, CMOS	High	The PHY asserts **NXT** to throttle the data. When the Link is sending data to the PHY, **NXT** indicates when the current byte has been accepted by the PHY.
A4	DIR	Output, CMOS	N/A	Controls the direction of the data bus. When the PHY has data to transfer to the Link, it drives **DIR** high to take ownership of the bus. When the PHY has no data to transfer it drives **DIR** low and monitors the bus for commands from the Link.

Table 2.2 USB3330 Pin Description (continued)

BALL	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
A3	STP	Input, CMOS	High	The Link asserts **STP** for one clock cycle to stop the data stream currently on the bus. If the Link is sending data to the PHY, **STP** indicates the last byte of data was on the bus in the previous cycle.
B3	VDD18	Power	N/A	1.8V Regulator Output. A 1.0uF (<1 ohm ESR) bypass capacitor to ground is required for regulator stability. The bypass capacitor should be placed as close as possible to the USB333x.
B2	RESETB	Input, CMOS,	Low	When low, the part is suspended and the 3.3V and 1.8V regulators are disabled. When high, the USB333x will operate as a normal ULPI device, as described in Section 5.5.1. The state of this pin may be changed asynchronously to the clock signals. When asserted for a minimum of 1 microsecond and then de-asserted, the ULPI registers are reset to their default state and all internal state machines are reset.
A2	REFCLK	Input, CMOS	N/A	**ULPI Clock Out Mode:** Frequency set by **REF[1:0]** pins. **ULPI Clock In Mode:** 60MHz ULPI clock input.
A1	RBIAS	Analog, CMOS	N/A	Bias Resistor pin. This pin requires an 8.06kΩ (±1%) resistor to ground, placed as close as possible to the USB333x. Nominal voltage during ULPI operation is 0.8V.
C3	GND	Ground	N/A	Ground.

Table 2.3 USB3333 Pin Description

BALL	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
B1	ID	Input, Analog	N/A	For device applications the **ID** pin is connected to **VDD33**. For Host applications **ID** is grounded. For OTG applications the **ID** pin is connected to the USB connector.
D2	VBUS	I/O, Analog	N/A	This pin is used for the VBUS comparator inputs and for VBUS pulsing during session request protocol. An external resistor, R_{VBUS}, is required between this pin and the USB connector.
C1	VBAT	Power	N/A	Regulator input. The regulator supply can be from 5.5V to 3.0V.
D3	VDD33	Power	N/A	3.3V Regulator Output. A 1.0uF (<1 ohm ESR) bypass capacitor to ground is required for regulator stability. The bypass capacitor should be placed as close as possible to the USB333x.
D1	DM	I/O, Analog	N/A	D- pin of the USB cable.
E1	DP	I/O, Analog	N/A	D+ pin of the USB cable.

Table 2.3 USB3333 Pin Description (continued)

BALL	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
E2	REF[0]	I/O, Digital 3.3V	N/A	Used to select REFCLK frequency. Connect to ground or VDD33. Refer to Table 5.2 for frequency selection options.
B3	VDDIO	Power	N/A	ULPI interface supply voltage. When RESETB is low and VDDIO is powered on, ULPI pins will tri-state.
E3	DATA[7]	I/O, CMOS	N/A	ULPI bi-directional data bus. **DATA[7]** is the MSB.
E4	DATA[6]	I/O, CMOS	N/A	ULPI bi-directional data bus.
E5	DATA[5]	I/O, CMOS	N/A	ULPI bi-directional data bus.
D4	DATA[4]	I/O, CMOS	N/A	ULPI bi-directional data bus.
A5	CLKOUT	Output, CMOS	N/A	**ULPI Clock Out Mode:** 60MHz ULPI clock output. All ULPI signals are driven synchronous to the rising edge of this clock. **ULPI Clock In Mode:** Connect this pin to **VDDIO** to configure 60MHz ULPI Clock IN mode as described in Section 5.4.1.
D5	DATA[3]	I/O, CMOS	N/A	ULPI bi-directional data bus.
C4	DATA[2]	I/O, CMOS	N/A	ULPI bi-directional data bus.
C5	DATA[1]	I/O, CMOS	N/A	ULPI bi-directional data bus.
B4	DATA[0]	I/O, CMOS	N/A	ULPI bi-directional data bus. **DATA[0]** is the LSB.
B5	NXT	Output, CMOS	High	The PHY asserts **NXT** to throttle the data. When the Link is sending data to the PHY, **NXT** indicates when the current byte has been accepted by the PHY.
A4	DIR	Output, CMOS	N/A	Controls the direction of the data bus. When the PHY has data to transfer to the Link, it drives **DIR** high to take ownership of the bus. When the PHY has no data to transfer it drives **DIR** low and monitors the bus for commands from the Link.
A3	STP	Input, CMOS	High	The Link asserts **STP** for one clock cycle to stop the data stream currently on the bus. If the Link is sending data to the PHY, **STP** indicates the last byte of data was on the bus in the previous cycle.
B2	VDD18	Power	N/A	1.8V Regulator Output. A 1.0uF (<1 ohm ESR) bypass capacitor to ground is required for regulator stability. The bypass capacitor should be placed as close as possible to the USB333x.

Table 2.3 USB3333 Pin Description (continued)

BALL	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
C2	**RESETB**	Input, CMOS,	Low	When low, the part is suspended and the 3.3V and 1.8V regulators are disabled. When high, the USB333x will operate as a normal ULPI device, as described in Section 5.5.1. The state of this pin may be changed asynchronously to the clock signals. When asserted for a minimum of 1 microsecond and then de-asserted, the ULPI registers are reset to their default state and all internal state machines are reset.
A2	**REFCLK**	Input, CMOS	N/A	**ULPI Clock Out Mode:** Frequency set by **REF[0]** pin. **ULPI Clock In Mode:** 60MHz ULPI clock input.
A1	**RBIAS**	Analog, CMOS	N/A	Bias Resistor pin. This pin requires an 8.06kΩ (±1%) resistor to ground, placed as close as possible to the USB333x. Nominal voltage during ULPI operation is 0.8V.
C3	**GND**	Ground	N/A	Ground.

Chapter 3 Limiting Values

3.1 Absolute Maximum Ratings

Table 3.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VBUS, **VBAT**, **ID**, **DP**, **DM**, **SPK_L**, and **SPK_R** voltage to **GND**	V_{MAX_5V}	Voltage measured at pin. **VBUS** tolerant to 30V with external R_{VBUS}.	-0.5		+6.0	V
Maximum **VDD18** voltage to Ground	V_{MAX_18V}		-0.5		2.5	V
Maximum **VDD33** voltage to Ground	V_{MAX_33V}		-0.5		4.0	V
Maximum **VDDIO** voltage to Ground (USB3333)	V_{MAX_IOV}		-0.5		4.0	
Maximum I/O voltage to Ground (USB3330, USB3331, USB3336, and USB3338)	V_{MAX_IN}		-0.5		2.5	V
Maximum I/O voltage to Ground (USB3333)	V_{MAX_IN}		-0.5		V_{DDIO} + 0.7	
Operating Temperature	T_{MAX_OP}		-40		85	C
Storage Temperature	T_{MAX_STG}		-55		150	C

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.2 Recommended Operating Conditions

Table 3.2 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VBAT to **GND**	V_{BAT}		3.0		5.5	V
VDD33 to **GND**	V_{DD33}		3.0	3.3	3.6	V
VDD18 to **GND**	V_{DD18}		1.6	1.8	2.0	V
VDDIO to **GND**	V_{DDIO}		1.6	1.8-3.3	3.6	V
Input Voltage on Digital Pins (**RESETB**, **STP**, **DIR**, **NXT**, **DATA[7:0]**) (USB3330, USB3331, USB3336, and USB3338)	V_I		0.0		V_{DD18}	V

Table 3.2 Recommended Operating Conditions (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage on Digital Pins (**RESETB**, **STP**, **DIR**, **NXT**, **DATA[7:0]**) (USB3333)	V_I		0.0		V_{DDIO}	V
Voltage on Analog I/O Pins (**DP**, **DM**, **ID**, **SPK_L**, **SPK_R**)	$V_{I(I/O)}$		0.0		V_{DD33}	V
VBUS to **GND**	V_{VMAX}		0.0		5.5	
Ambient Temperature	T_A		-40		85	C

Chapter 4 Electrical Characteristics

The following conditions are assumed unless otherwise specified:

V_{BAT} = 3.0 to 5.5V; V_{DDIO} = 1.6 to 3.6V; V_{SS} = 0V; T_A = -40C to +85C

4.1 Operating Current

Table 4.1 Operating Current (USB3330, USB3331, USB3336, and USB3338)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Synchronous Mode Current (Default Configuration)	$I_{VBAT(SYNC)}$	USB Idle	21	22	26	mA
Synchronous Mode Current (HS USB operation)	$I_{VBAT(HS)}$	Active USB Transfer	33	36	40	mA
Synchronous Mode Current (FS/LS USB operation)	$I_{VBAT(FS)}$	Active USB Transfer	27	28	32	mA
Serial Mode Current (FS/LS USB) Note 4.1	$I_{VBAT(FS\_S)}$		5	7	8	mA
USB UART Current Note 4.1	$I_{VBAT(UART)}$		6	7	8	mA
USB Audio Mode Note 4.2	$I_{VBAT(AUDIO)}$	V_{VBAT} = 4.2V	58	68	114	uA
Low Power Mode Note 4.2	$I_{VBAT(SUSPEND)}$	V_{VBAT} = 4.2V	27	31	71	uA
RESET Mode	$I_{VBAT(RSTB)}$	**RESETB** = 0 V_{VBAT} = 4.2V	0.1	1.5	10	uA

Note 4.1 *ClockSuspendM* bit = 0.

Note 4.2 SessEnd, VbusVld, and IdFloat comparators disabled. **STP** Interface protection disabled.

Table 4.2 Operating Current (USB3333)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Synchronous Mode Current (Default Configuration)	$I_{VBAT(SYNC)}$	USB Idle	20	22	24	mA
	$I_{VIO(SYNC)}$		2	3	8.5	mA
Synchronous Mode Current (HS USB operation)	$I_{VBAT(HS)}$	Active USB Transfer	29	31	35	mA
	$I_{VIO(HS)}$		5	8	17	mA
Synchronous Mode Current (FS/LS USB operation)	$I_{VBAT(FS)}$	Active USB Transfer	22	23	30	mA
	$I_{VIO(FS)}$		5	9	16	mA
Serial Mode Current (FS/LS USB) Note 4.1	$I_{VBAT(FS\_S)}$		6	7	8	mA
	$I_{VIO(FS\_S)}$		0	0.1	0.5	mA

Table 4.2 Operating Current (USB3333) (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
USB UART Current Note 4.1	$I_{VBAT(UART)}$		6	7	8	mA
	$I_{VIO(UART)}$		0	0.1	0.5	mA
Low Power Mode Note 4.2 Note 4.3	$I_{VBAT(SUSPEND)}$	V_{VBAT} = 4.2V V_{VDDIO} = 1.8V	28	32	60	uA
	$I_{VIO(SUSPEND)}$		0	0	2	uA
RESET Mode Note 4.3	$I_{VBAT(RSTB)}$	**RESETB** = 0 V_{VBAT} = 4.2V V_{VDDIO} = 1.8V	0.1	1.6	7	uA
	$I_{VIO(RSTB)}$		0	0.1	3	uA

Note 4.3   REFCLK is OFF.

4.2   Clock Specifications

The model number for each frequency of REFCLK is provided in Order Numbers: on page 2.

Table 4.3 Clock Specifications

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Suspend Recovery Time	T_{START}	*LPM Enable* = 0	1.0	1.1	1.2	ms
	T_{START_LPM}	*LPM Enable* = 1	125		150	uS
PHY Preparation Time 60MHz **REFCLK**	T_{PREP}	*LPM Enable* = 0	1.0	1.1	1.2	ms
	T_{PREP_LPM}	*LPM Enable* = 1	125		150	uS
CLKOUT Duty Cycle	DC_{CLKOUT}		45		55	%
REFCLK Duty Cycle	DC_{REFCLK}		20		80	%
REFCLK Frequency Accuracy	F_{REFCLK}		-500		+500	PPM

Note: T_{START} and T_{PREP} are measured from the time when **REFCLK** and **RESETB** are both valid to when the USB333x de-asserts **DIR**.

Note: The USB333x uses the *AutoResume* feature, Section 6.4.1.4, to allow a host start-up time of less than 1ms

4.3   ULPI Interface Timing

Table 4.4 ULPI Interface Timing (USB333x)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
60MHz ULPI Output Clock Note 4.4					
Setup time (**STP**, data in)	T_{SC}, T_{SD}	Model-specific **REFCLK**	5.0		ns
Hold time (**STP**, data in)	T_{HC}, T_{HD}	Model-specific **REFCLK**	0.0		ns
Output delay (control out, 8-bit data out)	T_{DC}, T_{DD}	Model-specific **REFCLK**		6.0	ns

Table 4.4 ULPI Interface Timing (USB333x) (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
60MHz ULPI Input Clock					
Setup time (**STP**, data in)	T_{SC}, T_{SD}	60MHz **REFCLK**	3.0		ns
Hold time (**STP**, data in)	T_{HC}, T_{HD}	60MHz **REFCLK**	0.0		ns
Output delay (control out, 8-bit data out)	T_{DC}, T_{DD}	60Mhz **REFCLK**		6.0	ns

Note: C_{Load} = 10pF.

Note 4.4   **REFCLK** does not need to be aligned in any way to the ULPI signals.

4.4   Digital IO Pins

Table 4.5 Digital IO Characteristics: RESETB, STP, DIR, NXT, DATA[7:0], and REFCLK Pins

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low-Level Input Voltage (USB3330, USB3331, USB3336, and USB3338)	V_{IL}		V_{SS}		0.4 * V_{DD18}	V
Low-Level Input Voltage (USB3333)	V_{IL}	Note 4.5	V_{SS}		0.4 * V_{DDIO}	V
High-Level Input Voltage (USB3330, USB3331, USB3336, and USB3338)	V_{IH}		0.68 * V_{DD18}		V_{DD18}	V
High-Level Input Voltage (USB3333)	V_{IH}		0.68 * V_{DDIO}		V_{DDIO}	V
High-Level Input Voltage **REFCLK** and **RESETB** (USB3330, USB3331, USB3336, and USB3338)	V_{IH_REF}		0.68 * V_{DD18}		V_{DD33}	V
High-Level Input Voltage **REFCLK** and **RESETB** (USB3333)	V_{IH_REF}		0.68 * V_{DDIO}		V_{DD33}	V
Low-Level Output Voltage	V_{OL}	I_{OL} = 8mA			0.4	V
High-Level Output Voltage (USB3330, USB3331, USB3336, and USB3338)	V_{OH}	I_{OH} = -8mA	V_{DD18} - 0.4			V
High-Level Output Voltage (USB3333)	V_{OH}	I_{OH} = -8mA	V_{DDIO} - 0.4			V
Output rise time	T_{IORISE}	C_{LOAD} = 10pF		1.19		nS
Output fall time	T_{IOFALL}	C_{LOAD} = 10pF		1.56		nS
Input Leakage Current	I_{LI}				±10	uA
Pin Capacitance	Cpin				2	pF
STP pull-up resistance	R_{STP}	*InterfaceProtectDisable* = 0	55	67	77	kΩ

Table 4.5 Digital IO Characteristics: RESETB, STP, DIR, NXT, DATA[7:0], and REFCLK Pins (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DATA[7:0] pull-down resistance	R_{DATA_PD}	*ULPI Synchronous Mode*	55	67	80	kΩ
CLKOUT External Drive (USB3330, USB3331, USB3336, and USB3338)	V_{IH_ED}	At start-up or following reset			0.4 * V_{DD18}	V
CLKOUT External Drive (USB3333)	V_{IH_ED}	At start-up or following reset			0.4 * V_{DDIO}	V

Note 4.5   MAX V_{IL} for USB3333 not to exceed 0.8V.

4.5   DC Characteristics: Analog I/O Pins

Table 4.6 DC Characteristics: Analog I/O Pins (DP/DM)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LS/FS FUNCTIONALITY						
Input levels						
Differential Receiver Input Sensitivity	V_{DIFS}	| V(DP) - V(DM) |	0.2			V
Differential Receiver Common-Mode Voltage	V_{CMFS}		0.8		2.5	V
Single-Ended Receiver Low Level Input Voltage	V_{ILSE}	Note 4.7			0.8	V
Single-Ended Receiver High Level Input Voltage	V_{IHSE}	Note 4.7	2.0			V
Single-Ended Receiver Hysteresis	V_{HYSSE}		0.050		0.150	V
Output Levels						
Low Level Output Voltage	V_{FSOL}	Pull-up resistor on DP; R_L = 1.5kΩ to V_{DD33}			0.3	V
High Level Output Voltage	V_{FSOH}	Pull-down resistor on DP, DM; Note 4.7 R_L = 15kΩ to GND	2.8		3.6	V
Termination						
Driver Output Impedance for HS	Z_{HSDRV}	Steady state drive	40.5	45	49.5	Ω
Input Impedance	Z_{INP}	RX, RPU, RPD disabled	1.0			MΩ
Pull-up Resistor Impedance	R_{PU}	Bus Idle, Note 4.6	0.900	1.24	1.575	kΩ
Pull-up Resistor Impedance	R_{PU}	Device Receiving, Note 4.6	1.425	2.26	3.09	kΩ
Pull-dn Resistor Impedance	R_{PD}	Note 4.6	14.25	16.9	20	kΩ