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MICROCHIP

USB3340

Enhanced Single Supply Hi-Speed USB ULPI Transceiver

PRODUCT FEATURES

Datasheet

- USB-IF Battery Charging 1.2 Specification Compliant
- Link Power Management (LPM) Specification Compliant
- Integrated ESD protection circuits
  - — Up to ±25kV IEC Air Discharge without external devices
- Over-Voltage Protection circuit (OVP) protects the VBUS pin from continuous DC voltages up to 30V
- Integrated USB Switch
  - — Allows single USB port of connection by providing switching function for:
    - – Battery charging
    - – Stereo and mono/mic audio
    - – USB Full-Speed/Low-Speed data
- RapidCharge Anywhere™ Provides:
  - — 3-times the charging current through a USB port over traditional solutions
  - — USB-IF Battery Charging 1.2 compliance to any portable device
  - — Charging current up to 1.5Amps via compatible USB host or dedicated charger
  - — Dedicated Charging Port (DCP), Charging (CDP) & Standard (SDP) Downstream Port support
- flexPWR® Technology
  - — Extremely low current design ideal for battery powered applications
  - — “Sleep” mode tri-states all ULPI pins and places the part in a low current state
  - — 1.8V to 3.3V IO Voltage
- Single Power Supply Operation
  - — Integrated 1.8V regulator
  - — Integrated 3.3V regulator
    - – 100mV dropout voltage
- PHYBoost
  - — Programmable USB transceiver drive strength for recovering signal integrity
- VariSense™
  - — Programmable USB receiver sensitivity
- “Wrapper-less” design for optimal timing performance and design ease
  - — Low Latency Hi-Speed Receiver (43 Hi-Speed clocks Max) allows use of legacy UTMI Links with a ULPI bridge
- External Reference Clock operation available
  - — ULPI Clock Input Mode (60MHz sourced by Link)
  - — 0 to 3.6V input drive tolerant
  - — Able to accept “noisy” clock sources as reference to internal, low-jitter PLL
  - — Crystal support available
- Smart detection circuits allow identification of USB charger, headset, or data cable insertion
- Includes full support for the optional On-The-Go (OTG) protocol detailed in the On-The-Go Supplement Revision 2.0 specification
- Supports the OTG Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- UART mode for non-USB serial data transfers
- Internal 5V cable short-circuit protection of ID, DP and DM lines to VBUS or ground
- Industrial Operating Temperature -40°C to +85°C
- 32 pin, QFN RoHS Compliant package (5 x 5 x 0.90 mm height)

Applications

The USB3340 is the solution of choice for any application where a Hi-Speed USB connection is desired and when board space, power, and interface pins must be minimized.

- Cell Phones
- PDAs
- MP3 Players
- GPS Personal Navigation
- Scanners
- External Hard Drives
- Digital Still and Video Cameras
- Portable Media Players
- Entertainment Devices
- Printers
- Set Top Boxes
- Video Record/Playback Systems
- IP and Video Phones
- Gaming Consoles

Order Number(s):

ORDER NUMBER	REFCLK FREQUENCY (Note 0.1)	PACKAGE TYPE	REEL SIZE
USB3340-EZK-TR	Selectable See Table 5.2	32 Pin, QFN RoHS Compliant Package (tape and reel)	4,000 pieces

Note 0.1 All versions support ULPI Clock In Mode (60MHz input at REFCLK)

This product meets the halogen maximum concentration values per IEC61249-2-21

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0.1 Reference Documents

UTMI+ Low Pin Interface (ULPI) Specification, Revision 1.1

Universal Serial Bus Specification, Revision 2.0

On-The-Go Supplement to the USB2.0 Specification, Revision 1.3

On-The-Go Supplement to the USB2.0 Specification, Revision 2.0

USB Battery Charging Specification, Revision 1.2

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Chapter 1 General Description

Microchip's USB3340 is a Hi-Speed USB 2.0 Transceiver that provides a physical layer (PHY) solution well-suited for portable electronic devices. Both commercial and industrial temperature applications are supported.

Several advanced features make the USB3340 the transceiver of choice by reducing both eBOM part count and printed circuit board (PCB) area. Outstanding ESD robustness eliminates the need for external ESD protection devices in typical applications. The internal Over-Voltage Protection circuit (OVP) protects the USB3340 from voltages up to 30V on the **VBUS** pin. By using a reference clock from the Link, the USB3340 removes the cost of a dedicated crystal reference from the design. The USB3340 includes integrated 3.3V and 1.8V regulators, making it possible to operate the device from a single power supply.

The USB3340 is optimized for use in portable applications where a low operating current and standby currents are essential. The USB3340 operates from a single supply and includes integrated regulators for its supplies. The USB3340 also supports the USB Link Power Management protocol (LPM) to further reduce USB operating currents.

The USB3340 also includes RapidCharge Anywhere™ which supports USB-IF Battery Charging 1.2 for any portable device. RapidCharge Anywhere™ provides three times the charging current through a USB port over traditional solutions which translate up to 1.5Amps via compatible USB host or dedicated charger. In addition, this provides a complete USB charging ecosystem between device and host ports such as Dedicated Charging Port (DCP), Charging (CDP) and Standard (SDP) Downstream Ports. Section 5.9 describes this is further detail.

The USB3340 meets all of the electrical requirements for a Hi-Speed USB Host, Device, or an On-the-Go (OTG) transceiver. In addition to the supporting USB signaling, the USB3340 also provides USB UART mode and, in versions with the integrated USB switch, USB Audio mode.

USB3340 uses the industry standard UTMI+ Low Pin Interface (ULPI) to connect the USB transceiver to the Link. ULPI uses a method of in-band signaling and status byte transfers between the Link and PHY to facilitate a USB session with only twelve pins.

The USB3340 uses "wrapper-less" technology to implement the ULPI interface. This "wrapper-less" technology allows the PHY to achieve a low latency transmit and receive time. Microchip's low latency transceiver allows an existing UTMI Link to be reused by adding a UTMI to ULPI bridge. By adding a bridge to the ASIC the existing and proven UTMI Link IP can be reused.

The integrated USB switch enables a single USB port of connection.

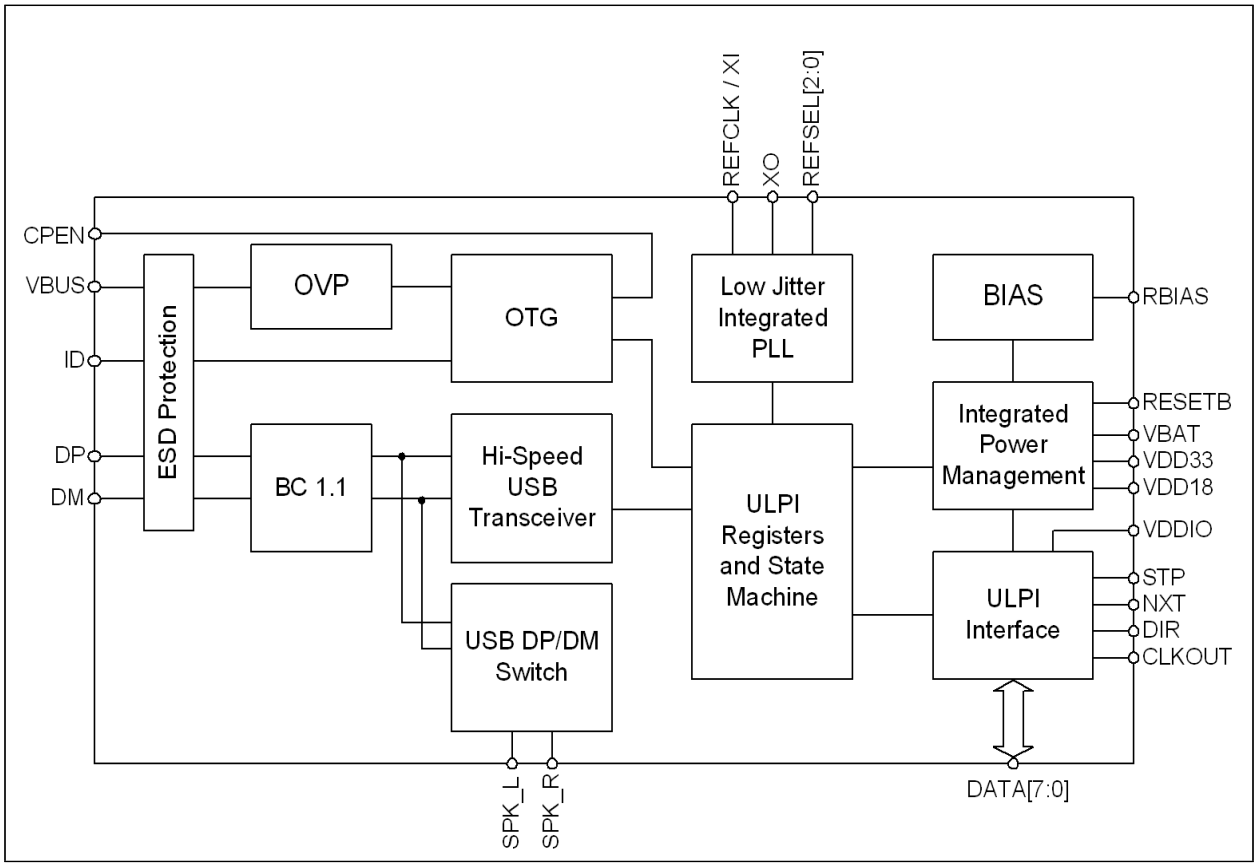

Figure 1.1 Block Diagram USB3340

In USB audio mode, a switch connects the **DP** pin to the **SPK_R** pin, and another switch connects he **DM** pin to the **SPK_L** pin. These switches are shown in the lower left-hand corner of .The USB3340 can be configured to enter USB audio mode as described in Section 6.7.2. In addition, these switches are on when the **RESETB** pin of the USB3340 is asserted. The USB audio mode enables audio signaling from a single USB port of connection, and the switches may also be used to connect Full Speed USB from another transceiver to the USB connector.

The USB3340 includes an integrated 3.3V LDO regulator that is used to generate 3.3V from power applied to the **VBAT** pin. The voltage on the **VBAT** pin can range from 3.0 to 5.5V. The regulator dropout voltage is less than 100mV which allows the PHY to continue USB signaling when the voltage on **VBAT** drops to 3.0V. The USB transceiver will continue to operate at lower voltages, although some parameters may be outside the limits of the USB specifications. The **VBAT** and **VDD33** pins should *never* be connected together.

In USB UART mode, the USB3340 **DP** and **DM** pins are redefined to enable pass-through of asynchronous serial data. The USB3340 will enter UART mode when programmed, as described in Section 6.7.1.

Chapter 2 Pin Locations and Definitions

2.1 USB3340 Pin Locations and Descriptions

2.1.1 USB3340 Pin Diagram and Pin Definitions

The illustration below is viewed from the top of the package.

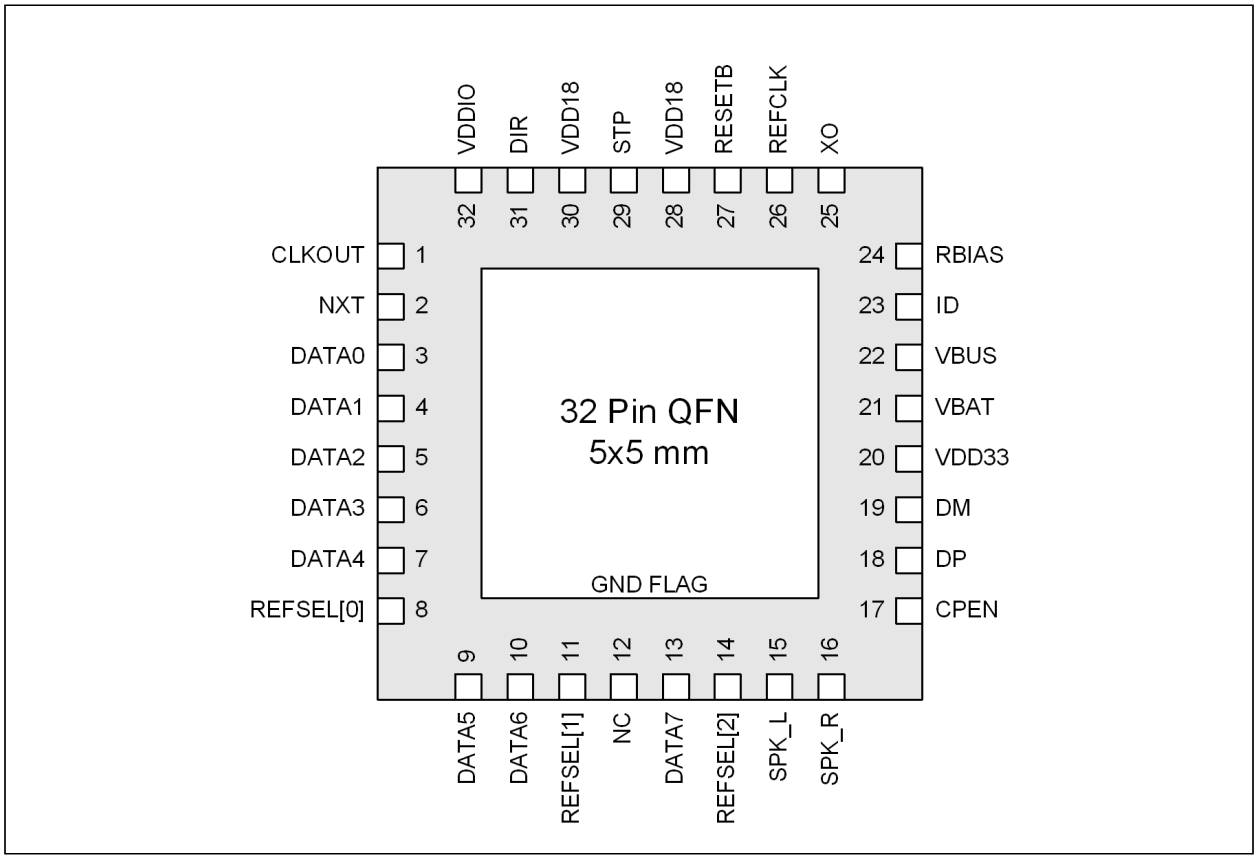

Figure 2.1 USB3340 Pin Locations - Top View

The following table details the pin definitions for the figure above.

Table 2.1 USB3340 Pin Descriptions

PIN	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
1	**CLKOUT**	Output, CMOS	N/A	**ULPI Clock Out Mode:** 60MHz ULPI clock output. All ULPI signals are driven synchronous to the rising edge of this clock. **ULPI Clock In Mode:** Connect this pin to **VDDIO** to configure 60MHz ULPI Clock IN mode as described in Section 5.5.1.
2	**NXT**	Output, CMOS	High	The PHY asserts **NXT** to throttle the data. When the Link is sending data to the PHY, **NXT** indicates when the current byte has been accepted by the PHY.

Table 2.1 USB3340 Pin Descriptions (continued)

PIN	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
3	**DATA[0]**	I/O, CMOS	N/A	ULPI bi-directional data bus. **DATA[0]** is the LSB.
4	**DATA[1]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
5	**DATA[2]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
6	**DATA[3]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
7	**DATA[4]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
8	**REFSEL[0]**	Input	N/A	Used to select xtal/reference frequency. This pad is connected to **VDDIO** or **GND**.
9	**DATA[5]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
10	**DATA[6]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
11	**REFSEL[1]**	Input	N/A	Used to select xtal/reference frequency. This pad is connected to **VDDIO** or **GND**.
12	**NC**	N/A	N/A	No connect. Leave pin floating.
13	**DATA[7]**	I/O, CMOS	N/A	ULPI bi-directional data bus. **DATA[7]** is the MSB.
14	**REFSEL[2]**	Input	N/A	Used to select xtal/reference frequency. This pad is connected to **VDDIO** or **GND**.
15	**SPK_L**	I/O, Analog	N/A	USB switch in/out for **DM** signals.
16	**SPK_R**	I/O, Analog	N/A	USB switch in/out for **DP** signals.
17	**CPEN**	Output, CMOS	High	External 5 volt supply enable. This pin is used to enable the external Vbus power supply. The **CPEN** pin is low on POR. This pad uses VDD33 logic level.
18	**DP**	I/O, Analog	N/A	D+ pin of the USB cable.
19	**DM**	I/O, Analog	N/A	D- pin of the USB cable.
20	**VDD33**	Power	N/A	3.3V Regulator Output. A 1.0uF (<1 ohm ESR) bypass capacitor to ground is required for regulator stability. The bypass capacitor should be placed as close as possible to the USB3340.
21	**VBAT**	Power	N/A	Regulator input. The regulator supply can be from 5.5V to 3.0V.
22	**VBUS**	I/O, Analog	N/A	This pin is used for the VBUS comparator inputs and for VBUS pulsing during session request protocol. An external resistor, R_{VBUS}, is required between this pin and the USB connector.

Table 2.1 USB3340 Pin Descriptions (continued)

PIN	NAME	DIRECTION/ TYPE	ACTIVE LEVEL	DESCRIPTION
23	**ID**	Input, Analog	N/A	For device applications the **ID** pin is connected to **VDD33**. For Host applications **ID** is grounded. For OTG applications the **ID** pin is connected to the USB connector.
24	**RBIAS**	Analog, CMOS	N/A	Bias Resistor pin. This pin requires an 8.06kΩ (±1%) resistor to ground, placed as close as possible to the USB3340. Nominal voltage during ULPI operation is 0.8V.
25	**XO**	Output, Analog	N/A	Crystal pin. If using an external clock on XI this pin should be floated.
26	**REFCLK**	Input, CMOS	N/A	**ULPI Clock Out Mode:** Model-specific reference clock or XI (crystal in) pin. See on page 2. **ULPI Clock In Mode:** 60MHz ULPI clock input.
27	**RESETB**	Input, CMOS,	Low	When low, the part is suspended and the 3.3V and 1.8V regulators are disabled. When high, the USB3340 will operate as a normal ULPI device, as described in Section 5.6.2. The state of this pin may be changed asynchronously to the clock signals. When asserted for a minimum of 1 microsecond and then de-asserted, the ULPI registers are reset to their default state and all internal state machines are reset.
28	**VDD18**	Power	N/A	1.8V Regulator Output. A 1.0uF (<1 ohm ESR) bypass capacitor to ground is required for regulator stability. The bypass capacitor should be placed as close as possible to the USB3340. Pin 28 and Pin 30 must be tied together. Only one bypass capacitor is required between Pin 28 and Pin 30.
29	**STP**	Input, CMOS	High	The Link asserts **STP** for one clock cycle to stop the data stream currently on the bus. If the Link is sending data to the PHY, **STP** indicates the last byte of data was on the bus in the previous cycle.
30	**VDD18**	Power	N/A	1.8V Regulator Output. A 1.0uF (<1 ohm ESR) bypass capacitor to ground is required for regulator stability. The bypass capacitor should be placed as close as possible to the USB3340. Pin 28 and Pin 30 must be tied together. Only one bypass capacitor is required between Pin 28 and Pin 30.
31	**DIR**	Output, CMOS	N/A	Controls the direction of the data bus. When the PHY has data to transfer to the Link, it drives **DIR** high to take ownership of the bus. When the PHY has no data to transfer it drives **DIR** low and monitors the bus for commands from the Link.
32	**VDDIO**	Power	N/A	ULPI interface supply voltage. When RESETB is low and VDDIO is powered on, ULPI pins will tri-state.
FLAG	**GND**	Ground	N/A	Ground.

Chapter 3 Limiting Values

3.1 Absolute Maximum Ratings

Table 3.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VBUS, **VBAT**, **ID**, **DP**, **DM**, **SPK_L**, and **SPK_R** voltage to **GND**	V_{MAX_5V}	Voltage measured at pin. **VBUS** tolerant to 30V with external R_{VBUS}.	-0.5		+6.0	V
Maximum **VDD18** voltage to Ground	V_{MAX_18V}		-0.5		2.5	V
Maximum **VDD33** voltage to Ground	V_{MAX_33V}		-0.5		4.0	V
Maximum **VDDIO** voltage to Ground	V_{MAX_IOV}		-0.5		4.0	V
Maximum I/O voltage to Ground	V_{MAX_IN}		-0.5		V_{DDIO} + 0.7	
Operating Temperature	T_{MAX_OP}		-40		85	C
Storage Temperature	T_{MAX_STG}		-55		150	C

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.2 Recommended Operating Conditions

Table 3.2 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VBAT to **GND**	V_{BAT}		3.0		5.5	V
VDD33 to **GND**	V_{DD33}		3.0	3.3	3.6	V
VDD18 to **GND**	V_{DD18}		1.6	1.8	2.0	V
VDDIO to **GND**	V_{DDIO}		1.6	1.8-3.3	3.6	V
Input Voltage on Digital Pins (**RESETB**, **STP**, **DIR**, **NXT**, **DATA[7:0]**)	V_I		0.0		V_{DDIO}	V
Voltage on Analog I/O Pins (**DP**, **DM**, **ID**, **CPEN**, **SPK_L**, **SPK_R**)	$V_{I(I/O)}$		0.0		V_{DD33}	V
VBUS to **GND**	V_{VMAX}		0.0		5.5	V
Ambient Temperature	T_A		-40		85	C

Chapter 4 Electrical Characteristics

The following conditions are assumed unless otherwise specified:

V_{DD33} = 3.0 to 3.6V; VDD18 = 1.6 to 2.0V; V_{SS} = 0V; T_A = -40C to +85C

4.1 Operating Current

Table 4.1 Operating Current

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Synchronous Mode Current (Default Configuration)	$I_{VBAT(SYNC)}$	USB Idle	18	22	24	mA
	$I_{VIO(SYNC)}$		1	2	5	mA
Synchronous Mode Current (HS USB operation)	$I_{VBAT(HS)}$	Active USB Transfer	33	35	37	mA
	$I_{VIO(HS)}$		5	6	14	mA
Synchronous Mode Current (FS/LS USB operation)	$I_{VBAT(FS)}$	Active USB Transfer	25	28.5	30	mA
	$I_{VIO(FS)}$		4	5	13	mA
Serial Mode Current (FS/LS USB) Note 4.1	$I_{VBAT(FS\_S)}$		7	8	9	mA
	$I_{VIO(FS\_S)}$		0	0.1	0.7	mA
USB UART Current Note 4.1	$I_{VBAT(UART)}$		7	8	9	mA
	$I_{VIO(UART)}$		0	0.1	0.7	mA
Low Power Mode Note 4.2 Note 4.3	$I_{VBAT(SUSPEND)}$	V_{VBAT} = 4.2V V_{VDDIO} = 1.8V	29	32	83	uA
	$I_{VIO(SUSPEND)}$		0	0	2	uA
RESET Mode Note 4.3	$I_{VBAT(RSTB)}$	**RESETB** = 0 V_{VBAT} = 4.2V V_{VDDIO} = 1.8V	0.1	1	12	uA
	$I_{VIO(RSTB)}$		0	0	7	uA

Note 4.1 *ClockSuspendM* bit = 0.

Note 4.2 SessEnd, VbusVld, and IdFloat comparators disabled. **STP** Interface protection disabled.

Note 4.3 REFCLK is OFF

4.2 Clock Specifications

The model number for each frequency of REFCLK is provided in on page 2.

Table 4.2 Clock Specifications

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Suspend Recovery Time	T_{START}	LPM Enable = 0	1.0	1.1	1.2	ms
	T_{START_LPM}	LPM Enable = 1	125		150	uS

Table 4.2 Clock Specifications (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PHY Preparation Time 60MHz **REFCLK**	T_{PREP}	LPM Enable = 0	1.0	1.1	1.2	ms
	T_{PREP_LPM}	LPM Enable = 1	125		150	uS
CLKOUT Duty Cycle	DC_{CLKOUT}	**ULPI Clock Input Mode**	45		55	%
REFCLK Duty Cycle	DC_{REFCLK}		20		80	%
REFCLK Frequency Accuracy	F_{REFCLK}		-500		+500	PPM

Note: T_{START} and T_{PREP} are measured from the time when **REFCLK** and **RESETB** are both valid to when the USB3340 de-asserts **DIR**.

Note: The USB3340 uses the *AutoResume* feature, Section 6.4.1.4, to allow a host start-up time of less than 1ms.

4.3 ULPI Interface Timing

Table 4.3 ULPI Interface Timing

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
60MHz ULPI Output Clock Note 4.4					
Setup time (**STP**, data in)	T_{SC}, T_{SD}	Model-specific **REFCLK**	5.0		ns
Hold time (**STP**, data in)	T_{HC}, T_{HD}	Model-specific **REFCLK**	0.0		ns
Output delay (control out, 8-bit data out)	T_{DC}, T_{DD}	Model-specific **REFCLK**	1.5	6	ns
60MHz ULPI Input Clock					
Setup time (**STP**, data in)	T_{SC}, T_{SD}	60MHz **REFCLK**	3		ns
Hold time (**STP**, data in)	T_{HC}, T_{HD}	60MHz **REFCLK**	0		ns
Output delay (control out, 8-bit data out)	T_{DC}, T_{DD}	60Mhz **REFCLK**	0.5	6.0	ns

Note: C_{Load} = 10pF.

Note 4.4 **REFCLK** does not need to be aligned in any way to the ULPI signals.

4.4 Digital IO Pins

Table 4.4 Digital IO Characteristics: RESETB, CPEN, STP, DIR, NXT, DATA[7:0], and REFCLK Pins

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low-Level Input Voltage	V_{IL}		V_{SS}		0.8	V
High-Level Input Voltage	V_{IH}		0.68 * V_{DDIO}		V_{DDIO}	V
High-Level Input Voltage **REFCLK** and **RESETB**	V_{IH_REF}		0.68 * V_{DDIO}		V_{DD33}	V
Low-Level Output Voltage	V_{OL}	I_{OL} = 8mA			0.4	V

Table 4.4 Digital IO Characteristics: RESETB, CPEN, STP, DIR, NXT, DATA[7:0], and REFCLK Pins (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High-Level Output Voltage	V_{OH}	I_{OH} = -8mA	V_{DDIO} - 0.4			V
High-Level Output Voltage **CPEN**	V_{OH}	I_{OH} = -8mA	V_{DD33} - 0.4			V
Output rise time	T_{IORISE}	C_{LOAD} = 10pF		1.19		nS
Output fall time	T_{IOFALL}	C_{LOAD} = 10pF		1.56		nS
Input Leakage Current	I_{LI}				±10	uA
Pin Capacitance	Cpin				4	pF
STP pull-up resistance	R_{STP}	InterfaceProtectDisable = 0	55	67	80	kΩ
DATA[7:0] pull-down resistance	R_{DATA_PD}	ULPI Synchronous Mode	55	67	77	kΩ
CLKOUT External Drive	V_{IH_ED}	At start-up or following reset			0.4 * V_{DDIO}	V

4.5 DC Characteristics: Analog I/O Pins

Table 4.5 DC Characteristics: Analog I/O Pins (DP/DM)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LS/FS FUNCTIONALITY						
Input levels						
Differential Receiver Input Sensitivity	V_{DIFS}	| V(DP) - V(DM) |	0.2			V
Differential Receiver Common-Mode Voltage	V_{CMFS}		0.8		2.5	V
Single-Ended Receiver Low Level Input Voltage	V_{ILSE}	Note 4.6			0.8	V
Single-Ended Receiver High Level Input Voltage	V_{IHSE}	Note 4.6	2.0			V
Single-Ended Receiver Hysteresis	V_{HYSSE}		0.050		0.150	V
Output Levels						
Low Level Output Voltage	V_{FSOL}	Pull-up resistor on DP; R_L = 1.5kΩ to V_{DD33}			0.3	V
High Level Output Voltage	V_{FSOH}	Pull-down resistor on DP, DM; Note 4.6 R_L = 15kΩ to GND	2.8		3.6	V
Termination						
Driver Output Impedance for HS	Z_{HSDRV}	Steady state drive	40.5	45	49.5	Ω

Table 4.5 DC Characteristics: Analog I/O Pins (DP/DM) (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Impedance	Z_{INP}	RX, RPU, RPD disabled	1.0			MΩ
Pull-up Resistor Impedance	R_{PU}	Bus Idle, Note 4.5	0.900	1.24	1.575	kΩ
Pull-up Resistor Impedance	R_{PU}	Device Receiving, Note 4.5	1.425	2.26	3.09	kΩ
Pull-dn Resistor Impedance	R_{PD}	Note 4.5	14.25	16.9	20	kΩ
HS FUNCTIONALITY						
Input levels						
HS Differential Input Sensitivity	V_{DIHS}	| V(DP) - V(DM) |	100			mV
HS Data Signaling Common Mode Voltage Range	V_{CMHS}		-50		500	mV
HS Squelch Detection Threshold (Differential)	V_{HSSQ}	*VariSense[1:0]* = 00b Note 4.7	100		150	mV
HS Disconnect Threshold	V_{HSDSC}		525		625	mV
Output Levels						
High Speed Low Level Output Voltage (DP/DM referenced to GND)	V_{HSOL}	45Ω load	-10		10	mV
High Speed High Level Output Voltage (DP/DM referenced to GND)	V_{HSOH}	45Ω load	360		440	mV
High Speed IDLE Level Output Voltage (DP/DM referenced to GND)	V_{OLHS}	45Ω load	-10		10	mV
Chirp-J Output Voltage (Differential)	V_{CHIRPJ}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	700		1100	mV
Chirp-K Output Voltage (Differential)	V_{CHIRPK}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	-900		-500	mV
Leakage Current						
OFF-State Leakage Current	I_{LZ}				±10	uA
Port Capacitance						
Transceiver Input Capacitance	C_{IN}	Pin to GND		5	10	pF

Note 4.5 The resistor value follows the 27% Resistor ECN published by the USB-IF.

Note 4.6 The values shown are valid when the *USB RegOutput* bits in the USB IO & Power Management register are set to the default value.

Note 4.7 An automatic waiver up to 200mV is granted to accommodate system-level elements such as measurement/test fixtures, captive cables, EMI components, and ESD suppression. This parameter can be tuned using VariSense technology, as defined in Section 7.1.3.1of Chapter 7.

4.6 Dynamic Characteristics: Analog I/O Pins

Table 4.6 Dynamic Characteristics: Analog I/O Pins (DP/DM)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FS Output Driver Timing						
FS Rise Time	T_{FR}	C_L = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
FS Fall Time	T_{FF}	C_L = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
Output Signal Crossover Voltage	V_{CRS}	Excluding the first transition from IDLE state	1.3		2.0	V
Differential Rise/Fall Time Matching	T_{FRFM}	Excluding the first transition from IDLE state	90		111.1	%
LS Output Driver Timing						
LS Rise Time	T_{LR}	C_L = 50-600pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	75		300	ns
LS Fall Time	T_{LF}	C_L = 50-600pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	75		300	ns
Differential Rise/Fall Time Matching	T_{LRFM}	Excluding the first transition from IDLE state	80		125	%
HS Output Driver Timing						
Differential Rise Time	T_{HSR}		500			ps
Differential Fall Time	T_{HSF}		500			ps
Driver Waveform Requirements		Eye pattern of Template 1 in USB 2.0 specification				
High Speed Mode Timing						
Receiver Waveform Requirements		Eye pattern of Template 4 in USB 2.0 specification				
Data Source Jitter and Receiver Jitter Tolerance		Eye pattern of Template 4 in USB 2.0 specification				

4.7 VBUS Electrical Characteristics

Table 4.7 VBUS Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SessEnd trip point	$V_{SessEnd}$		0.2	0.5	0.8	V
SessVld trip point	$V_{SessVld}$		0.8	1.4	2.0	V
VbusVld trip point	$V_{VbusVld}$		4.4	4.58	4.75	V
VBUS Pull-Up	R_{VPU}	**VBUS** to **VDD33** Note 4.8 (*ChargeVbus* = 1)	1.29	1.34	1.45	kΩ

Table 4.7 VBUS Electrical Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VBUS Pull-down	R_{VPD}	**VBUS** to **GND** Note 4.8 (*DisChargeVbus* = 1)	1.55	1.7	1.85	kΩ
VBUS Impedance	R_{VB}	**VBUS** to **GND**	40	75	100	kΩ
A-Device Impedance to ground	R_{IdGnd}	Maximum Impedance to ground on **ID** pin			100	kΩ

Note 4.8 The R_{VPD} and R_{VPU} values include the required 1kΩ external R_{VBUS} resistor.

4.8 ID Electrical Characteristics

Table 4.8 ID Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ID Ground Trip Point	V_{IdGnd}		0.4	0.7	0.9	V
ID Float Trip Point	$V_{IdFloat}$		1.6	2.2	2.5	V
ID pull-up resistance	R_{ID}	IdPullup = 1	80	100	120	kΩ
ID weak pull-up resistance	R_{IDW}	IdPullup = 0	1			MΩ
ID pull-dn resistance	R_{IDPD}	IdGndDrv = 1			1000	Ω

4.9 USB Audio Switch Characteristics

Table 4.9 USB Audio Switch Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum “ON” Resistance	R_{ON_Min}	$0 < V_{switch} < V_{DD33}$	2.7	5	5.8	Ω
Maximum “ON” Resistance	R_{ON_Max}	$0 < V_{switch} < V_{DD33}$	4.5	7	13	Ω
Minimum “OFF” Resistance	R_{OFF_Min}	$0 < V_{switch} < V_{DD33}$	1			MΩ

4.10 USB Charger Detection Characteristics

Table 4.10 USB Charger Detection Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Source Voltage	V_{DAT_SRC}	$I_{DAT\_SRC} < 250uA$	0.5		0.7	V
Data Detect Voltage	V_{DAT_REF}		0.25		0.4	V
Data Source Current	I_{DAT_SRC}		250			uA
Data Sink Current	I_{DAT_SINK}		50		150	uA

Table 4.10 USB Charger Detection Characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Connect Current	I_{DP_SRC}		7		13	uA
Weak Pull-up Resistor Impedance	R_{CD}	Configured by bits 4 and 5 in USB IO & Power Management register.	128	170	212	kΩ

4.11 Regulator Output Voltages and Capacitor Requirement

Table 4.11 Regulator Output Voltages and Capacitor Requirement

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Regulator Output Voltage	V_{DD33}	5.5V > **VBAT** > 3.0V	2.8	3.3	3.6	V
		USB UART Mode & UART RegOutput[1:0] = 01 6V > VBAT > 3.0V	2.7	3.0	3.3	V
		USB UART Mode & UART RegOutput[1:0] = 10 6V > VBAT > 3.0V	2.47	2.75	3.03	V
		USB UART Mode & UART RegOutput[1:0] = 11 6V > VBAT > 3.0V	2.25	2.5	2.75	V
Regulator Bypass Capacitor	C_{OUT33}		1.0			uF
Bypass Capacitor ESR	C_{ESR33}				1	Ω
Regulator Output Voltage	V_{DD18}	3.6V > **VDD33** > 2.25V	1.6	1.8	2.0	V
Regulator Bypass Capacitor	C_{OUT18}		1.0			uF
Bypass Capacitor ESR	C_{ESR18}				1	Ω

4.12 Piezoelectric Resonator for Internal Oscillator

The internal oscillator may be used with an external quartz crystal or ceramic resonator as described in Section 5.4. See Table 4.12 for the recommended crystal specifications.

Table 4.12 USB3340 Quartz Crystal Specifications

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS	NOTES
Crystal Cut	AT, typ					
Crystal Oscillation Mode	Fundamental Mode					
Crystal Calibration Mode	Parallel Resonant Mode					
Frequency	F_{fund}	-	See on page 2	-	MHz	
Total Allowable PPM Budget		-	-	±500	PPM	Note 4.9
Shunt Capacitance	C_O	-	7 typ	-	pF	
Load Capacitance	C_L	-	20 typ	-	pF	
Drive Level	P_W	0.1	-	-	mW	
Equivalent Series Resistance	R_1	-	-	30	Ohm	
USB3340 **REFCLK** Pin Capacitance		-	3 typ	-	pF	Note 4.10
USB3340 **XO** Pin Capacitance		-	3 typ	-	pF	Note 4.10

Note 4.9 The required bit rate accuracy for Hi-Speed USB applications is ±500 ppm as provided in the USB 2.0 Specification. This takes into account the effect of voltage, temperature, aging, etc.

Note 4.10 This number includes the pad, the bond wire and the lead frame. Printed Circuit Board (PCB) capacitance is not included in this value. The PCB capacitance value and the capacitance value of the **XO** and **REFCLK** pins are required to accurately calculate the value of the two external load capacitors.

4.13 ESD and Latch-Up Performance

Table 4.13 ESD and Latch-Up Performance

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	COMMENTS
ESD PERFORMANCE						
Note 4.11 Note 4.12	Human Body Model			±8	kV	Device
System	EN/IEC 61000-4-2 Contact Discharge			±25	kV	3rd party system test
System	EN/IEC 61000-4-2 Air-gap Discharge			±25	kV	3rd party system test
LATCH-UP PERFORMANCE						
All Pins	EIA/JESD 78, Class II		150		mA	

Note 4.11 **REFCLK**, **XO**, **ID, RESETB**, **SPK_L** and **SPK_R** pins: ±5kV Human Body Model.

Note 4.12 The **REFSEL[2:0]** pins only tested to ±2kV Human Body Model.

Chapter 5 Architecture Overview

The USB3340 consists of the blocks shown in the diagram below.

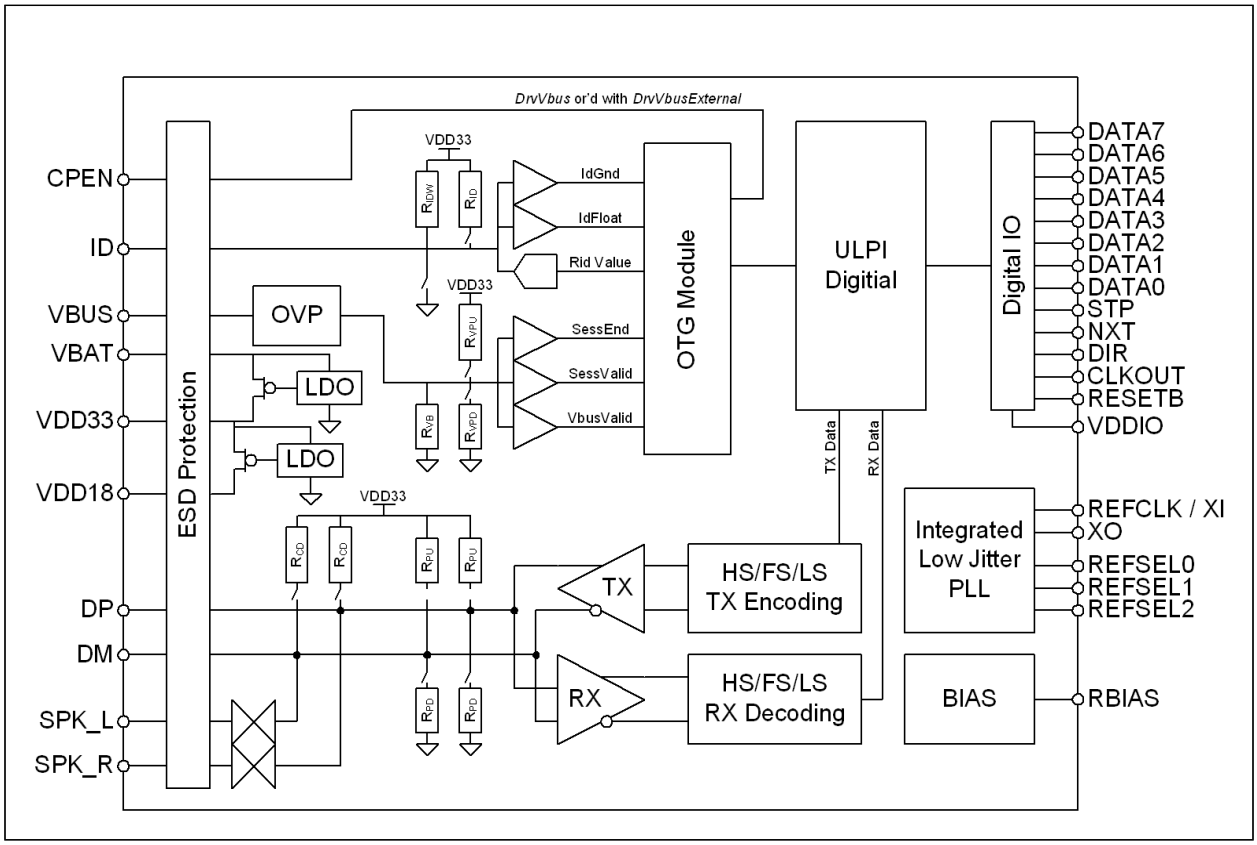

Figure 5.1 USB3340 System Diagram

5.1 ULPI Digital Operation and Interface

This section of the USB3340 is covered in detail in Chapter 6, ULPI Operation.

5.2 USB 2.0 Hi-Speed Transceiver

The blocks in the lower left-hand corner of interface to the DP/DM pins.

5.2.1 USB Transceiver

The USB3340 transceiver includes a Universal Serial Bus Specification Rev 2.0 compliant receiver and transmitter. The DP/DM signals in the USB cable connect directly to the receivers and transmitters.

The receiver consists of receivers for HS and FS/LS mode. Depending on the mode, the selected receiver provides the serial data stream through the multiplexer to the RX Logic block. For HS mode support, the HS RX block contains a squelch circuit to insure that noise is not interpreted as data. The RX block also includes a single-ended receiver on each of the data lines to determine the correct FS linestate.

Data from the Link is encoded, bit stuffed, serialized and transmitted onto the USB cable by the transmitter. Separate differential FS/LS and HS transmitters are included to support all modes.

The USB3340 TX block meets the HS signalling level requirements in the USB 2.0 Specification when the PCB traces from the **DP** and **DM** pins to the USB connector are correctly designed. In some systems the proper 90 ohm differential impedance can not be maintained and it may be desirable to compensate for loss by adjusting the HS transmitter amplitude and this HS squelch threshold. The *PHYBoost* bits in the HS Compensation Register may be configured to adjust the HS transmitter amplitude at the **DP** and **DM** pins. The *VariSense* bits in the HS Compensation Register can also be used to lower the squelch threshold to compensate for losses on the PCB.

To ensure proper operation of the USB transceiver the settings of Table 5.1 must be followed.

5.2.2 Termination Resistors

The USB3340 transceiver fully integrates all of the USB termination resistors on both **DP** and **DM**. This includes 1.5kΩ pull-up resistors, 15kΩ pull-down resistors and the 45Ω High Speed termination resistors. These resistors require no tuning or trimming by the Link. The state of the resistors is determined by the operating mode of the transceiver when operating in synchronous mode.

The *XcvrSelect[1:0]*, *TermSelect* and *OpMode[1:0]* bits in the Function Control register, and the *DpPulldown* and *DmPulldown* bits in the OTG Control register control the configuration of the termination resistors. All possible valid resistor combinations are shown in Table 5.1, and operation is guaranteed in only the configurations shown. If a ULPI Register Setting is configured that does not match a setting in the table, the transceiver operation is not guaranteed and the settings in the last row of Table 5.1 will be used.

- RPU_DP_EN activates the 1.5kΩ DP pull-up resistor
- RPU_DM_EN activates the 1.5kΩ DM pull-up resistor
- RPD_DP_EN activates the 15kΩ DP pull-down resistor
- RPD_DM_EN activates the 15kΩ DM pull-down resistor
- HSTERM_EN activates the 45Ω DP and DM High Speed termination resistors

Table 5.1 DP/DM Termination vs. Signaling Mode

	ULPI REGISTER SETTINGS					USB3340 TERMINATION RESISTOR SETTINGS				
SIGNALING MODE	***XcvrSelect[1:0]***	***TermSelect***	***OpMode[1:0]***	***DpPulldown***	***DmPulldown***	**RPU_DP_EN**	**RPU_DM_EN**	**RPD_DP_EN**	**RPD_DM_EN**	**HSTERM_EN**
General Settings										
Tri-State Drivers, Note 5.1	XXb	Xb	01b	Xb	Xb	0b	0b	0b	0b	0b
Power-up or VBUS < $V_{SESSEND}$	01b	0b	00b	1b	1b	0b	0b	1b	1b	0b
Host Settings										
Host Chirp	00b	0b	10b	1b	1b	0b	0b	1b	1b	1b
Host High Speed	00b	0b	00b	1b	1b	0b	0b	1b	1b	1b
Host Full Speed	X1b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host HS/FS Suspend	01b	1b	00b	1b	1b	0b	0b	1b	1b	0b

Table 5.1 DP/DM Termination vs. Signaling Mode (continued)

SIGNALING MODE	ULPI REGISTER SETTINGS					USB3340 TERMINATION RESISTOR SETTINGS				
	XcvrSelect[1:0]	*TermSelect*	*OpMode[1:0]*	*DpPulldown*	*DmPulldown*	RPU_DP_EN	RPU_DM_EN	RPD_DP_EN	RPD_DM_EN	HSTERM_EN
Host HS/FS Resume	01b	1b	10b	1b	1b	0b	0b	1b	1b	0b
Host Low Speed	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host LS Suspend	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host LS Resume	10b	1b	10b	1b	1b	0b	0b	1b	1b	0b
Host Test J/Test_K	00b	0b	10b	1b	1b	0b	0b	1b	1b	1b
Peripheral Settings										
Peripheral Chirp	00b	1b	10b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS	00b	0b	00b	0b	0b	0b	0b	0b	0b	1b
Peripheral FS	01b	1b	00b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Suspend	01b	1b	00b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Resume	01b	1b	10b	0b	0b	1b	0b	0b	0b	0b
Peripheral LS	10b	1b	00b	0b	0b	0b	1b	0b	0b	0b
Peripheral LS Suspend	10b	1b	00b	0b	0b	0b	1b	0b	0b	0b
Peripheral LS Resume	10b	1b	10b	0b	0b	0b	1b	0b	0b	0b
Peripheral Test J/Test K	00b	0b	10b	0b	0b	0b	0b	0b	0b	1b
OTG device, Peripheral Chirp	00b	1b	10b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS	00b	0b	00b	0b	1b	0b	0b	0b	1b	1b
OTG device, Peripheral FS	01b	1b	00b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS/FS Suspend	01b	1b	00b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS/FS Resume	01b	1b	10b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral Test J/Test K	00b	0b	10b	0b	1b	0b	0b	0b	1b	1b
Charger Detection										
Connect Detect	01b	0b	00b	0b	1b	0b	0b	0b	1b	0b
Any combination not defined above, Note 5.2						0b	0b	1b	1b	0b

Note: This is equivalent to Table 40, Section 4.4 of the ULPI 1.1 specification.

Note: USB3340 does not support operation as an upstream hub port. See Chapter 6.4.1.3.

Note 5.1 When **RESETB** = 0 The HS termination will tri-state the USB drivers