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USB3370

Enhanced Single Supply Hi-Speed USB ULPI Transceiver

Highlights

- USB-IF Battery Charging 1.1 Specification Compliant
- Link Power Management (LPM) Specification Compliant
- Integrated ESD protection circuits
  - Up to ±25kV IEC Air Discharge without external devices
- Over-Voltage Protection circuit (OVP) protects the VBUS pin from continuous DC voltages up to 30V
- Microchip RapidCharge Anywhere™ Provides:
  - 3-times the charging current through a USB port over traditional solutions
  - USB-IF Battery Charging 1.1 compliance to any portable device
  - Charging current up to 1.5Amps via compatible USB host or dedicated charger
  - Dedicated Charging Port (DCP), Charging (CDP) & Standard (SDP) Downstream Port support
- flexPWR® Technology
  - Extremely low current design ideal for battery powered applications
  - “Sleep” mode tri-states all ULPI pins and places the part in a low current state
  - 1.8V to 3.3V IO Voltage
- Single Power Supply Operation
  - Integrated 1.8V regulator
  - Integrated 3.3V regulator
    - 100mV dropout voltage
- PHYBoost
  - Programmable USB transceiver drive strength for recovering signal integrity
- VariSense™
  - Programmable USB receiver sensitivity
- “Wrapper-less” design for optimal timing performance and design ease
  - Low Latency Hi-Speed Receiver (43 Hi-Speed clocks Max) allows use of legacy UTMI Links with a ULPI bridge
- External Reference Clock operation available
  - 19.2MHz Reference Clock needed
  - ULPI Clock Input Mode (60MHz sourced by Link)
  - 0 to 3.6V input drive tolerant
  - Able to accept “noisy” clock sources as reference to internal, low-jitter PLL
  - Crystal support available
- Smart detection circuits allow identification of USB charger, headset, or data cable insertion
- Includes full support for the optional On-The-Go (OTG) protocol detailed in the On-The-Go Supplement Revision 2.0 specification
- Supports the OTG Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- UART mode for non-USB serial data transfers
- Internal 5V cable short-circuit protection of ID, DP and DM lines to VBUS or ground
- Industrial Operating Temperature -40°C to +85°C
- 32 pin, QFN RoHS Compliant package (5 x 5x 0.90 mm height)

Applications

The USB3370 is the solution of choice for any application where a Hi-Speed USB connection is desired and when board space, power, and interface pins must be minimized.

- Cell Phones
- PDAs
- MP3 Players
- GPS Personal Navigation
- Scanners
- External Hard Drives
- Digital Still and Video Cameras
- Portable Media Players
- Entertainment Devices
- Printers
- Set Top Boxes
- Video Record/Playback Systems
- IP and Video Phones
- Gaming Consoles

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1.0 INTRODUCTION

Microchip's USB3370 is a family of Hi-Speed USB 2.0 Transceivers that provide a physical layer (PHY) solution well-suited for portable electronic devices. Both commercial and industrial temperature applications are supported.

Several advanced features make the USB3370 the transceiver of choice by reducing both eBOM part count and printed circuit board (PCB) area. Outstanding ESD robustness eliminates the need for external ESD protection devices in typical applications. The internal Over-Voltage Protection circuit (OVP) protects the USB3370 from voltages up to 30V on the **VBUS** pin. By using a reference clock from the Link, the USB3370 removes the cost of a dedicated crystal reference from the design. The USB3370 includes integrated 3.3V and 1.8V regulators, making it possible to operate the device from a single power supply.

The USB3370 is optimized for use in portable applications where a low operating current and standby currents are essential. The USB3370 operates from a single supply and includes integrated regulators for its supplies. The USB3370 also supports the USB Link Power Management protocol (LPM) to further reduce USB operating currents.

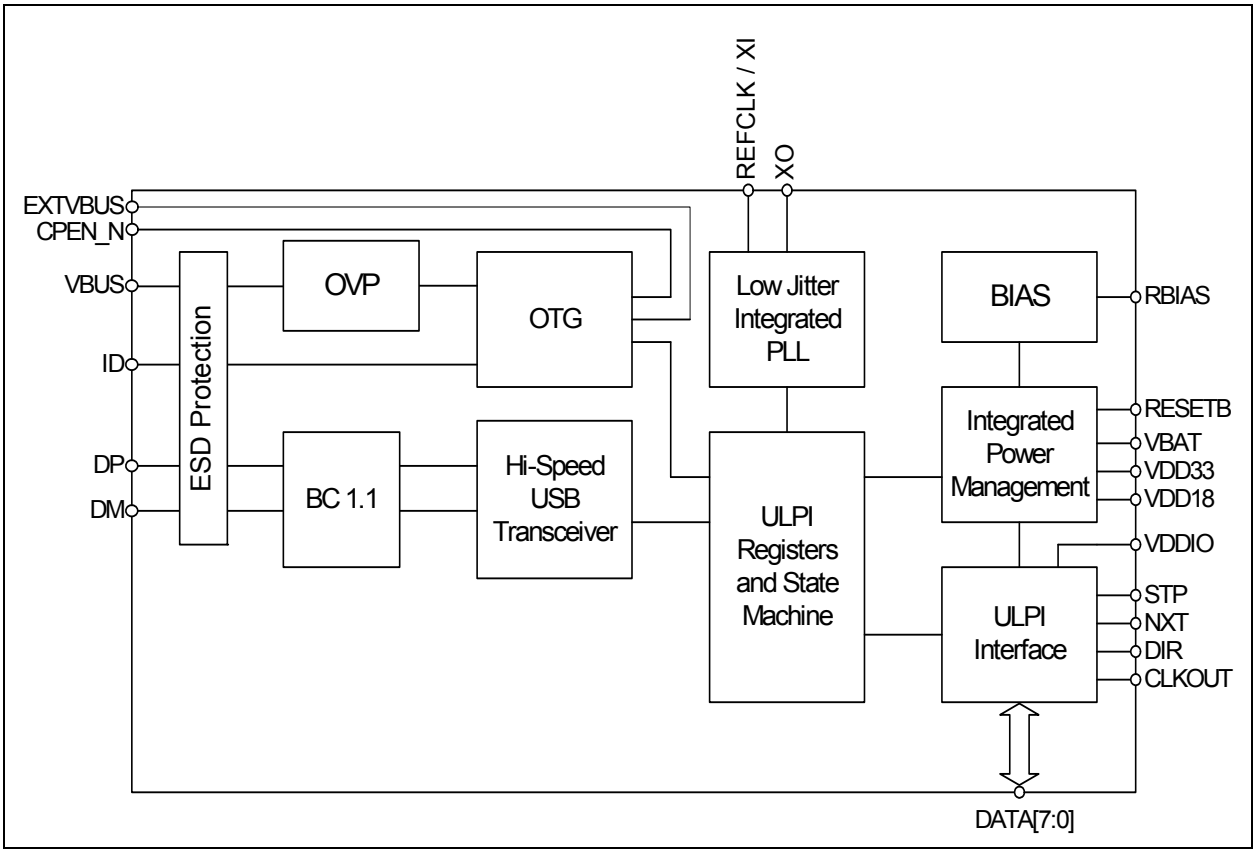
The USB3370 also includes family is enabled with Microchip's RapidCharge Anywhere™ which supports USB-IF Battery Charging 1.1 for any portable device. RapidCharge Anywhere™ provides three times the charging current through a USB port over traditional solutions which translate up to 1.5Amps via compatible USB host or dedicated charger. In addition, this provides a complete USB charging ecosystem between device and host ports such as Dedicated Charging Port (DCP), Charging (CDP) and Standard (SDP) Downstream Ports. Section 5.9 describes this is further detail.

The USB3370 meets all of the electrical requirements for a Hi-Speed USB Host, Device, or an On-the-Go (OTG) transceiver. In addition to the supporting USB signaling, the USB3370 also provides USB UART mode.

USB3370 uses the industry standard UTMI+ Low Pin Interface (ULPI) to connect the USB transceiver to the Link. ULPI uses a method of in-band signaling and status byte transfers between the Link and PHY to facilitate a USB session with only twelve pins.

The USB3370 uses Microchip's "wrapper-less" technology to implement the ULPI interface. This "wrapper-less" technology allows the PHY to achieve a low latency transmit and receive time. Microchip's low latency transceiver allows an existing UTMI Link to be reused by adding a UTMI to ULPI bridge. By adding a bridge to the ASIC the existing and proven UTMI Link IP can be reused.

FIGURE 1-1: BLOCK DIAGRAM USB3370



The USB3370 includes an integrated 3.3V LDO regulator that is used to generate 3.3V from power applied to the **VBAT** pin. The voltage on the **VBAT** pin can range from 3.0 to 5.5V. The regulator dropout voltage is less than 100mV which allows the PHY to continue USB signaling when the voltage on **VBAT** drops to 3.0V. The USB transceiver will continue to operate at lower voltages, although some parameters may be outside the limits of the USB specifications. The **VBAT** and **VDD33** pins should *never* be connected together.

In USB UART mode, the USB3370 **DP** and **DM** pins are redefined to enable pass-through of asynchronous serial data. The USB3370 will enter UART mode when programmed, as described in Section 6.7.1.

1.1 Reference Documents

UTMI+ Low Pin Interface (ULPI) Specification, Rev. 1.1

Universal Serial Bus Specification, Revision 2.0

On-The-Go Supplement to the USB2.0 Specification, Rev. 1.3

On-The-Go Supplement to the USB2.0 Specification, Rev. 2.0

USB Battery Charging Specification, Rev. 1.1

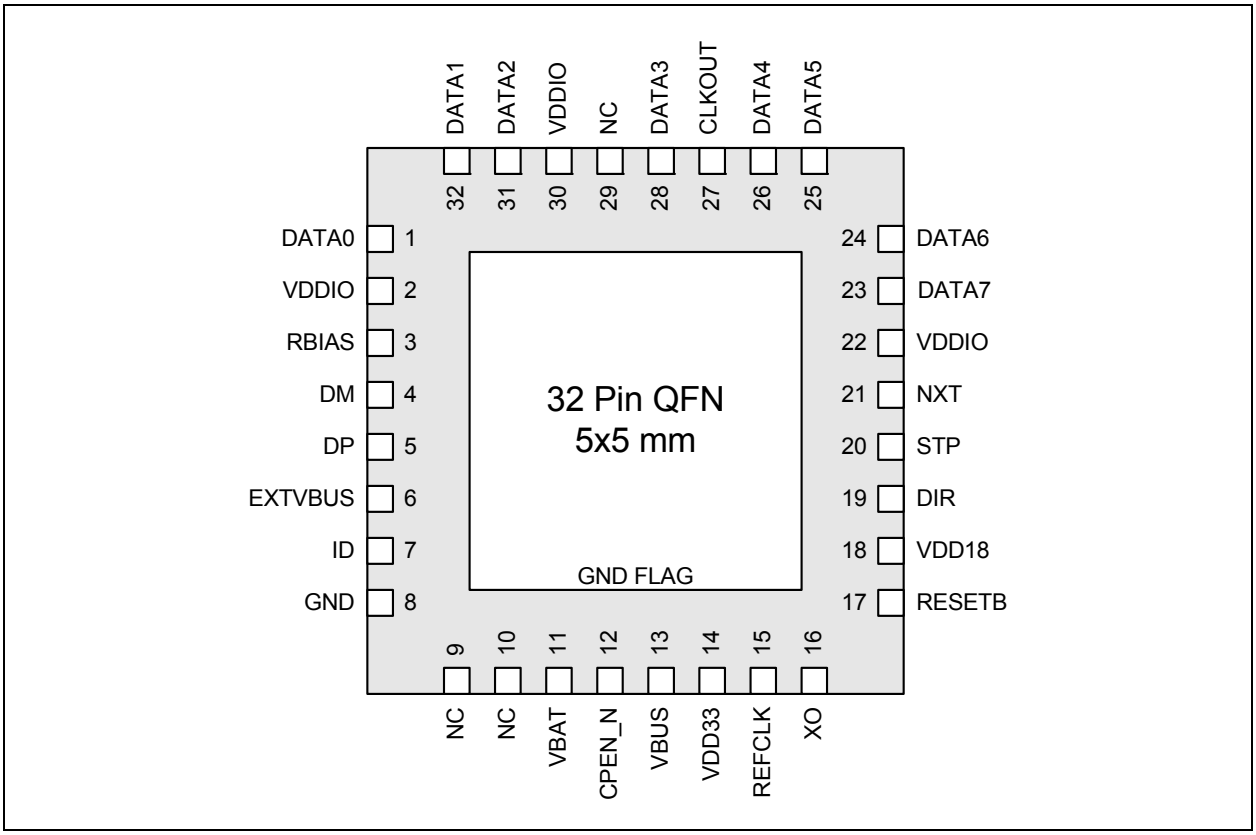
2.0 USB3370 PIN LOCATIONS AND DEFINITIONS

2.1 USB3370 Pin Locations and Descriptions

2.1.1 USB3370 PIN DIAGRAM AND PIN DEFINITIONS

The illustration below is viewed from the top of the package.

FIGURE 2-1: USB3370 PIN LOCATIONS - TOP VIEW



The following table details the pin definitions for the figure above.

TABLE 2-1: USB3370 PIN DESCRIPTIONS

Pin	Name	Direction/ Type	Active Level	Description
27	**CLKOUT**	Output, CMOS	N/A	**ULPI Clock Out Mode:** 60MHz ULPI clock output. All ULPI signals are driven synchronous to the rising edge of this clock. **ULPI Clock In Mode:** Connect this pin to **VDDIO** to configure 60MHz ULPI Clock IN mode as described in Section 5.5.1.
21	**NXT**	Output, CMOS	High	The PHY asserts **NXT** to throttle the data. When the Link is sending data to the PHY, **NXT** indicates when the current byte has been accepted by the PHY.
1	**DATA[0]**	I/O, CMOS	N/A	ULPI bi-directional data bus. **DATA[0]** is the LSB.
32	**DATA[1]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
31	**DATA[2]**	I/O, CMOS	N/A	ULPI bi-directional data bus.

TABLE 2-1: USB3370 PIN DESCRIPTIONS (CONTINUED)

Pin	Name	Direction/ Type	Active Level	Description
28	**DATA[3]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
26	**DATA[4]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
6	**EXTVBUS**	Input, CMOS	High	External Vbus Detect. Connect to fault output of an external USB power switch or an external Vbus Valid comparator. See Section 5.7.5, "External Vbus Indicator," on page 29 for details. This pin has a pull down resistor to prevent it from floating when the ULPI bit *UseExternalVbusIndicator* is set to 0.
25	**DATA[5]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
24	**DATA[6]**	I/O, CMOS	N/A	ULPI bi-directional data bus.
9 10 29	**NC**	N/A	N/A	No connect. Leave pin floating.
23	**DATA[7]**	I/O, CMOS	N/A	ULPI bi-directional data bus. **DATA[7]** is the MSB.
12	**CPEN_N**	Output, Open Drain	Low	External 5 volt supply enable. This pin is used to enable the external Vbus power supply. The **CPEN_N** pin is tri-stated on POR.
5	**DP**	I/O, Analog	N/A	D+ pin of the USB cable.
4	**DM**	I/O, Analog	N/A	D- pin of the USB cable.
14	**VDD33**	Power	N/A	3.3V Regulator Output. A 1.0uF (<1 ohm ESR) bypass capacitor to ground is required for regulator stability. The bypass capacitor should be placed as close as possible to the USB3370.
11	**VBAT**	Power	N/A	Regulator input. The regulator supply can be from 5.5V to 3.0V.
13	**VBUS**	I/O, Analog	N/A	This pin is used for the VBUS comparator inputs and for VBUS pulsing during session request protocol. An external resistor, R_{VBUS}, is required between this pin and the USB connector.
7	**ID**	Input, Analog	N/A	For device applications the **ID** pin is connected to **VDD33**. For Host applications **ID** is grounded. For OTG applications the **ID** pin is connected to the USB connector.
3	**RBIAS**	Analog, CMOS	N/A	Bias Resistor pin. This pin requires an 10kΩ (±1%) resistor to ground, placed as close as possible to the USB3370. Nominal voltage during ULPI operation is 0.8V.
16	**XO**	Output, Analog	N/A	Crystal pin. If using an external clock on XI this pin should be floated.
15	**REFCLK**	Input, CMOS	N/A	**ULPI Clock Out Mode:** Reference clock or XI (crystal in) pin. **ULPI Clock In Mode:** 60MHz ULPI clock input.

TABLE 2-1: USB3370 PIN DESCRIPTIONS (CONTINUED)

Pin	Name	Direction/ Type	Active Level	Description
17	**RESETB**	Input, CMOS,	Low	When low, the part is suspended and the 3.3V and 1.8V regulators are disabled. When high, the USB3370 will operate as a normal ULPI device, as described in Section 5.6.2. The state of this pin may be changed asynchronously to the clock signals. When asserted for a minimum of 1 microsecond and then de-asserted, the ULPI registers are reset to their default state and all internal state machines are reset.
18	**VDD18**	Power	N/A	1.8V Regulator Output. A 1.0uF (<1 ohm ESR) bypass capacitor to ground is required for regulator stability. The bypass capacitor should be placed as close as possible to the USB3370.
20	**STP**	Input, CMOS	High	The Link asserts **STP** for one clock cycle to stop the data stream currently on the bus. If the Link is sending data to the PHY, **STP** indicates the last byte of data was on the bus in the previous cycle.
19	**DIR**	Output, CMOS	N/A	Controls the direction of the data bus. When the PHY has data to transfer to the Link, it drives **DIR** high to take ownership of the bus. When the PHY has no data to transfer it drives **DIR** low and monitors the bus for commands from the Link.
2 22 30	**VDDIO**	Power	N/A	1.8V to 3.3V ULPI interface supply voltage.
FLAG 8	**GND**	Ground	N/A	Ground.

3.0 LIMITING VALUES

3.1 Absolute Maximum Ratings

TABLE 3-1: ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
VBUS, **VBAT**, and **ID**, voltage to **GND**	V_{MAX_USB}	Voltage measured at pin. **VBUS** tolerant to 30V with external R_{VBUS}.	-0.5		6.0	V
DP and **DM** voltage to **GND**	V_{MAX_DPDM}		-0.5		5.0	V
Maximum **VDD18** voltage to Ground	V_{MAX_18V}		-0.5		2.5	V
Maximum **VDD33** voltage to Ground	V_{MAX_33V}		-0.5		4.0	V
Maximum **VDDIO** voltage to Ground	V_{MAX_IOV}		-0.5		4.0	
Maximum I/O voltage to Ground	V_{MAX_IN}		-0.5		V_{DDIO} + 0.7	
Maximum I/O voltage to Ground (**EXTVBUS**, **CPEN_N**)	V_{MAX_IN}		-0.5		5.5V	
Operating Temperature	T_{MAX_OP}		-40		85	C
Storage Temperature	T_{MAX_STG}		-55		150	C

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.2 Recommended Operating Conditions

TABLE 3-2: RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
VBAT to **GND**	V_{BAT}		3.0		5.5	V
VDD33 to **GND**	V_{DD33}		3.0	3.3	3.6	V
VDD18 to **GND**	V_{DD18}		1.6	1.8	2.0	V
VDDIO to **GND**	V_{DDIO}		1.6	1.8-3.3	3.6	V
Input Voltage on Digital Pins (**RESETB**, **STP**, **DIR**, **NXT**, **DATA[7:0]**)	V_I		0.0		V_{DDIO}	V
Input Voltage on Digital Pins (**EXTVBUS, CPEN_N**)	V_I		0.0		5.0	V
Voltage on Analog I/O Pins (**DP**, **DM**, **ID**)	$V_{I(I/O)}$		0.0		V_{DD33}	V
VBUS to **GND**	V_{VMAX}		0.0		5.5	
Ambient Temperature	T_A		-40		85	C

4.0 ELECTRICAL CHARACTERISTICS

The following conditions are assumed unless otherwise specified:

V_{DD33} = 3.0 to 3.6V; VDD18 = 1.6 to 2.0V; V_{SS} = 0V; T_A = -40C to +85C

4.1 Operating Current

TABLE 4-1: OPERATING CURRENT

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
Synchronous Mode Current (Default Configuration)	$I_{VBAT(SYNC)}$	USB Idle	24	27	29	mA
	$I_{VIO(SYNC)}$		2	3	7	mA
Synchronous Mode Current (HS USB operation)	$I_{VBAT(HS)}$	Active USB Transfer	33	35	37	mA
	$I_{VIO(HS)}$		5	6	14	mA
Synchronous Mode Current (FS/LS USB operation)	$I_{VBAT(FS)}$	Active USB Transfer	25	28.5	30	mA
	$I_{VIO(FS)}$		4	5	13	mA
Serial Mode Current (FS/LS USB) Note 4-1	$I_{VBAT(FS\_S)}$		7	8	9	mA
	$I_{VIO(FS\_S)}$		0	0.1	0.7	mA
USB UART Current Note 4-1	$I_{VBAT(UART)}$		7	8	9	mA
	$I_{VIO(UART)}$		0	0.1	0.7	mA
Low Power Mode Note 4-2 Note 4-3	$I_{VBAT(SUSPEND)}$	V_{VBAT} = 4.2V V_{VDDIO} = 1.8V	29	32	83	uA
	$I_{VIO(SUSPEND)}$		0	0	2	uA
RESET Mode Note 4-3	$I_{VBAT(RSTB)}$	**RESETB** = 0 V_{VBAT} = 4.2V V_{VDDIO} = 1.8V	0.1	1	12	uA
	$I_{VIO(RSTB)}$		0	0	7	uA

Note 4-1 *ClockSuspendM* bit = 0.

Note 4-2 SessEnd, VbusVld, and IdFloat comparators disabled. **STP** Interface protection disabled.

Note 4-3 REFCLK is OFF

4.2 Clock Specifications

The model number for each frequency of REFCLK is provided in Product Identification System on page 73.

TABLE 4-2: CLOCK SPECIFICATIONS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
Suspend Recovery Time	T_{START}	LPM Enable = 0	1.0	1.1	1.32	ms
	T_{START_LPM}	LPM Enable = 1	125		150	uS
PHY Preparation Time 60MHz **REFCLK**	T_{PREP}	LPM Enable = 0	1.0	1.1	1.32	ms
	T_{PREP_LPM}	LPM Enable = 1	125		150	uS
CLKOUT Duty Cycle	DC_{CLKOUT}	**ULPI Clock Input Mode**	45		55	%
REFCLK Duty Cycle	DC_{REFCLK}		20		80	%
REFCLK Frequency Accuracy	F_{REFCLK}		-500		+500	PPM

Note 1: T_{START} and T_{PREP} are measured from the time when **REFCLK** and **RESETB** are both valid to when the USB3370 de-asserts **DIR**.

2: The USB3370 uses the *AutoResume* feature, Section 6.4.1.4, to allow a host start-up time of less than 1ms.

Note 4-4 REFCLK with oscillator Input

Note 4-5 Crystal Input

4.3 ULPI Interface Timing

TABLE 4-3: ULPI INTERFACE TIMING

Parameter	Symbol	Conditions	MIN	MAX	Units
60MHz ULPI Output Clock Note 4-6					
Setup time (**STP**, data in)	T_{SC}, T_{SD}	Model-specific **REFCLK**	5.0		ns
Hold time (**STP**, data in)	T_{HC}, T_{HD}	Model-specific **REFCLK**	0.0		ns
Output delay (control out, 8-bit data out)	T_{DC}, T_{DD}	Model-specific **REFCLK**	1.5	6	ns
60MHz ULPI Input Clock					
Setup time (**STP**, data in)	T_{SC}, T_{SD}	60MHz **REFCLK**	3		ns
Hold time (**STP**, data in)	T_{HC}, T_{HD}	60MHz **REFCLK**	0		ns
Output delay (control out, 8-bit data out)	T_{DC}, T_{DD}	60Mhz **REFCLK**	0.5	6.0	ns

Note: C_{Load} = 10pF.

Note 4-6 **REFCLK** does not need to be aligned in any way to the ULPI signals.

4.4 Digital IO Pins

TABLE 4-4: DIGITAL IO CHARACTERISTICS: RESETB, STP, DIR, NXT, DATA[7:0], AND REFCLK PINS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
Low-Level Input Voltage	V_{IL}		V_{SS}		0.8	V
High-Level Input Voltage	V_{IH}		0.68 * V_{DDIO}		V_{DDIO}	V
High-Level Input Voltage **REFCLK** and **RESETB**	V_{IH_REF}		0.68 * V_{DDIO}		V_{DD33}	V
Low-Level Output Voltage	V_{OL}	I_{OL} = 8mA			0.4	V
High-Level Output Voltage	V_{OH}	I_{OH} = -8mA	V_{DDIO} - 0.4			V
Output rise time	T_{IORISE}	C_{LOAD} = 10pF		1.19		nS
Output fall time	T_{IOFALL}	C_{LOAD} = 10pF		1.56		nS
Input Leakage Current	I_{LI}				±10	uA
Pin Capacitance	Cpin				4	pF
STP pull-up resistance	R_{STP}	InterfaceProtectDisable = 0	55	67	80	kΩ
DATA[7:0] pull-down resistance	R_{DATA_PD}	ULPI Synchronous Mode	55	67	77	kΩ
CLKOUT External Drive	V_{IH_ED}	At start-up or following reset			0.4 * V_{DDIO}	V

4.5 DC Characteristics: Analog I/O Pins

TABLE 4-5: DC CHARACTERISTICS: ANALOG I/O PINS (DP/DM)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
LS/FS FUNCTIONALITY						
Input levels						
Differential Receiver Input Sensitivity	V_{DIFS}	| V(DP) - V(DM) |	0.2			V
Differential Receiver Common-Mode Voltage	V_{CMFS}		0.8		2.5	V
Single-Ended Receiver Low Level Input Voltage	V_{ILSE}	Note 4-8			0.8	V
Single-Ended Receiver High Level Input Voltage	V_{IHSE}	Note 4-8	2.0			V
Single-Ended Receiver Hysteresis	V_{HYSSE}		0.050		0.150	V
Output Levels						
Low Level Output Voltage	V_{FSOL}	Pull-up resistor on DP; R_L = 1.5kΩ to V_{DD33}			0.3	V
High Level Output Voltage	V_{FSOH}	Pull-down resistor on DP, DM; Note 4-8 R_L = 15kΩ to GND	2.8		3.6	V
Termination						
Driver Output Impedance for HS	Z_{HSDRV}	Steady state drive	40.5	45	49.5	Ω
Input Impedance	Z_{INP}	RX, RPU, RPD disabled	1.0			MΩ
Pull-up Resistor Impedance	R_{PU}	Bus Idle, Note 4-7	0.900	1.24	1.575	kΩ
Pull-up Resistor Impedance	R_{PU}	Device Receiving, Note 4-7	1.425	2.26	3.09	kΩ
Pull-dn Resistor Impedance	R_{PD}	Note 4-7	14.25	16.9	20	kΩ
HS FUNCTIONALITY						
Input levels						
HS Differential Input Sensitivity	V_{DIHS}	| V(DP) - V(DM) |	100			mV
HS Data Signaling Common Mode Voltage Range	V_{CMHS}		-50		500	mV
HS Squelch Detection Threshold (Differential)	V_{HSSQ}	*VariSense[1:0]* = 00b Note 4-9	100		150	mV
HS Disconnect Threshold	V_{HSDSC}		525		625	mV
Output Levels						
High Speed Low Level Output Voltage (DP/DM referenced to GND)	V_{HSOL}	45Ω load	-10		10	mV
High Speed High Level Output Voltage (DP/DM referenced to GND)	V_{HSOH}	45Ω load	360		440	mV
High Speed IDLE Level Output Voltage (DP/DM referenced to GND)	V_{OLHS}	45Ω load	-10		10	mV
Chirp-J Output Voltage (Differential)	V_{CHIRPJ}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	700		1100	mV
Chirp-K Output Voltage (Differential)	V_{CHIRPK}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	-900		-500	mV

TABLE 4-5: DC CHARACTERISTICS: ANALOG I/O PINS (DP/DM) (CONTINUED)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
Leakage Current						
OFF-State Leakage Current	I_{LZ}				±10	uA
Port Capacitance						
Transceiver Input Capacitance	C_{IN}	Pin to GND		5	10	pF

Note 4-7 The resistor value follows the 27% Resistor ECN published by the USB-IF.

Note 4-8 The values shown are valid when the *USB RegOutput* bits in the USB IO & Power Management register are set to the default value.

Note 4-9 An automatic waiver up to 200mV is granted to accommodate system-level elements such as measurement/test fixtures, captive cables, EMI components, and ESD suppression. This parameter can be tuned using VariSense technology, as defined in Section 7.1.3.1 of Section 7.0, "ULPI Register Map".

4.6 Dynamic Characteristics: Analog I/O Pins

TABLE 4-6: DYNAMIC CHARACTERISTICS: ANALOG I/O PINS (DP/DM)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
FS Output Driver Timing						
FS Rise Time	T_{FR}	C_L = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
FS Fall Time	T_{FF}	C_L = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
Output Signal Crossover Voltage	V_{CRS}	Excluding the first transition from IDLE state	1.3		2.0	V
Differential Rise/Fall Time Matching	T_{FRFM}	Excluding the first transition from IDLE state	90		111.1	%
LS Output Driver Timing						
LS Rise Time	T_{LR}	C_L = 50-600pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	75		300	ns
LS Fall Time	T_{LF}	C_L = 50-600pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	75		300	ns
Differential Rise/Fall Time Matching	T_{LRFM}	Excluding the first transition from IDLE state	80		125	%
HS Output Driver Timing						
Differential Rise Time	T_{HSR}		500			ps
Differential Fall Time	T_{HSF}		500			ps
Driver Waveform Requirements		Eye pattern of Template 1 in USB 2.0 specification				
High Speed Mode Timing						
Receiver Waveform Requirements		Eye pattern of Template 4 in USB 2.0 specification				
Data Source Jitter and Receiver Jitter Tolerance		Eye pattern of Template 4 in USB 2.0 specification				

4.7 VBUS Electrical Characteristics

TABLE 4-7: VBUS ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
SessEnd trip point	$V_{SessEnd}$		0.2	0.5	0.8	V
SessVld trip point	$V_{SessVld}$		0.8	1.4	2.0	V
VbusVld trip point	$V_{VbusVld}$		4.4	4.58	4.75	V
VBUS Pull-Up	R_{VPU}	**VBUS** to **VDD33** Note 4-10 (*ChargeVbus* = 1)	1.29	1.34	1.45	kΩ
VBUS Pull-down	R_{VPD}	**VBUS** to **GND** Note 4-10 (*DisChargeVbus* = 1)	1.55	1.7	1.85	kΩ
VBUS Impedance	R_{VB}	**VBUS** to **GND**	40	75	100	kΩ
A-Device Impedance to ground	R_{IdGnd}	Maximum Impedance to ground on **ID** pin			100	kΩ

Note 4-10 The R_{VPD} and R_{VPU} values include the required 1kΩ external R_{VBUS} resistor.

4.8 ID Electrical Characteristics

TABLE 4-8: ID ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
ID Ground Trip Point	V_{IdGnd}		0.4	0.7	0.9	V
ID Float Trip Point	$V_{IdFloat}$		1.6	2.2	2.5	V
ID pull-up resistance	R_{ID}	IdPullup = 1	80	100	120	kΩ
ID weak pull-up resistance	R_{IDW}	IdPullup = 0	1			MΩ
ID pull-dn resistance	R_{IDPD}	IdGndDrv = 1			1000	Ω

4.9 USB Charger Detection Characteristics

TABLE 4-9: USB CHARGER DETECTION CHARACTERISTICS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
Data Source Voltage	V_{DAT_SRC}	I_{DAT_SRC} < 250uA	0.5		0.7	V
Data Detect Voltage	V_{DAT_REF}		0.25		0.4	V
Data Source Current	I_{DAT_SRC}		250			uA
Data Sink Current	I_{DAT_SINK}		50		150	uA
Data Connect Current	I_{DP_SRC}		7		13	uA
Weak Pull-up Resistor Impedance	R_{CD}	Configured by bits 4 and 5 in USB IO & Power Management register.	128	170	212	kΩ

4.10 Regulator Output Voltages and Capacitor Requirement

TABLE 4-10: REGULATOR OUTPUT VOLTAGES AND CAPACITOR REQUIREMENT

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
Regulator Output Voltage	V_{DD33}	5.5V > **VBAT** > 3.0V	2.8	3.3	3.6	V
		USB UART Mode & UART RegOutput[1:0] = 01 6V > VBAT > 3.0V	2.7	3.0	3.3	V
		USB UART Mode & UART RegOutput[1:0] = 10 6V > VBAT > 3.0V	2.47	2.75	3.03	V
		USB UART Mode & UART RegOutput[1:0] = 11 6V > VBAT > 3.0V	2.25	2.5	2.75	V
Regulator Bypass Capacitor	C_{OUT33}		1.0			uF
Bypass Capacitor ESR	C_{ESR33}				1	Ω
Regulator Output Voltage	V_{DD18}	3.6V > **VDD33** > 2.25V	1.6	1.8	2.0	V
Regulator Bypass Capacitor	C_{OUT18}		1.0			uF
Bypass Capacitor ESR	C_{ESR18}				1	Ω

4.11 Piezoelectric Resonator for Internal Oscillator

The internal oscillator may be used with an external quartz crystal or ceramic resonator as described in Section 5.4. See Table 4-11 for the recommended crystal specifications.

TABLE 4-11: USB3370 QUARTZ CRYSTAL SPECIFICATIONS

Parameter	Symbol	MIN	NOM	MAX	Units	Notes
Crystal Cut	AT, typ					
Crystal Oscillation Mode	Fundamental Mode					
Crystal Calibration Mode	Parallel Resonant Mode					
Frequency	F_{fund}	-	See Product Identification System on page 73	-	MHz	
Total Allowable PPM Budget		-	-	±500	PPM	Note 4-11
Shunt Capacitance	C_O	-	7 typ	-	pF	
Load Capacitance	C_L	-	20 typ	-	pF	
Drive Level	P_W	0.1	-	-	mW	
Equivalent Series Resistance	R_1	-	-	30	Ohm	
USB3370 **REFCLK** Pin Capacitance		-	3 typ	-	pF	Note 4-12
USB3370 **XO** Pin Capacitance		-	3 typ	-	pF	Note 4-12
Recommended Resistance between XI and XO		1M	-	-	Ohm	Note 4-13

Note 4-11 The required bit rate accuracy for Hi-Speed USB applications is ±500 ppm as provided in the USB 2.0 Specification. This takes into account the effect of voltage, temperature, aging, etc.

Note 4-12 This number includes the pad, the bond wire and the lead frame. Printed Circuit Board (PCB) capacitance is not included in this value. The PCB capacitance value and the capacitance value of the **XO** and **REFCLK** pins are required to accurately calculate the value of the two external load capacitors.

Note 4-13 Refer to Section 5.4 and Figure 8-1 for more information.

4.12 ESD and Latch-Up Performance

TABLE 4-12: ESD AND LATCH-UP PERFORMANCE

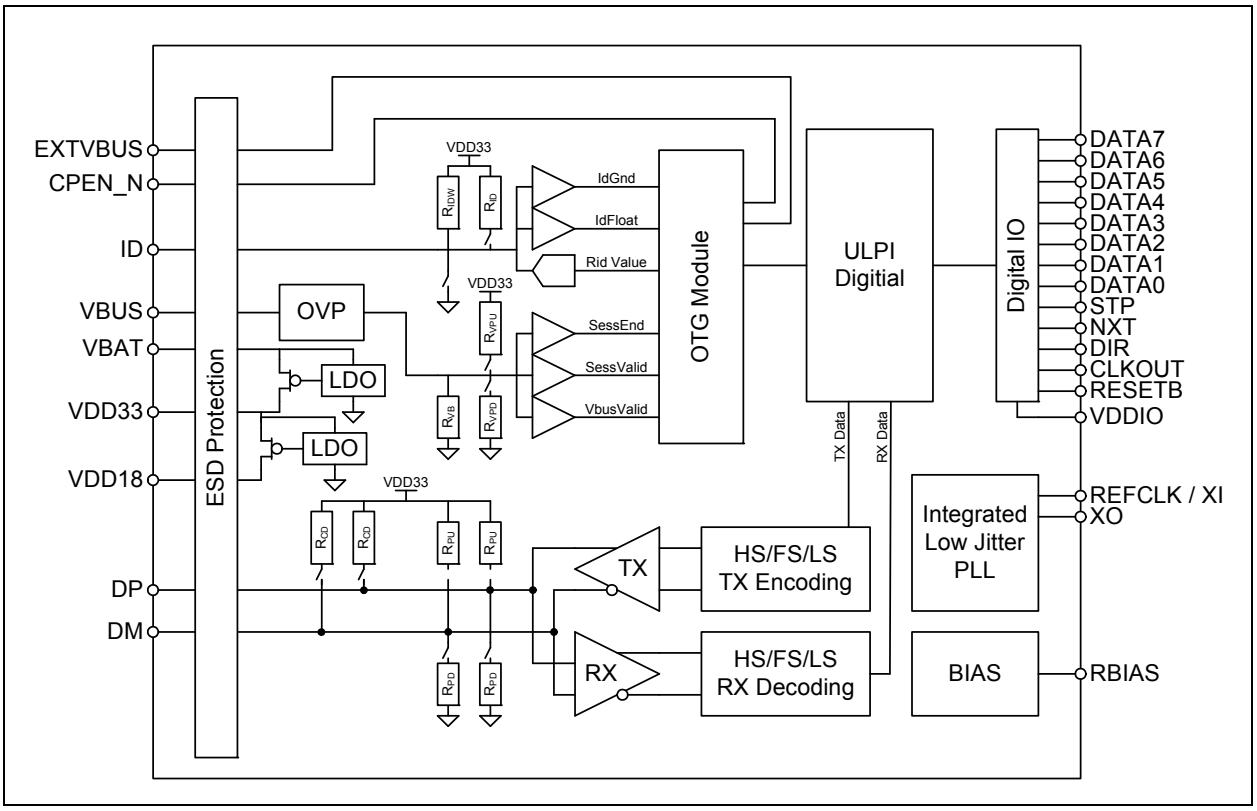
Parameter	Conditions	MIN	TYP	MAX	Units	Comments
ESD PERFORMANCE						
Note 4-14	Human Body Model			±8	kV	Device
System	EN/IEC 61000-4-2 Contact Discharge			±25	kV	3rd party system test
System	EN/IEC 61000-4-2 Air-gap Discharge			±25	kV	3rd party system test
LATCH-UP PERFORMANCE						
All Pins	EIA/JESD 78, Class II		150		mA	

Note 4-14 **REFCLK**, **XO**, **ID,** and **RESETB** pins: ±5kV Human Body Model.

5.0 ARCHITECTURE OVERVIEW

The USB3370 consists of the blocks shown in the diagram below.

FIGURE 5-1: USB3370 SYSTEM DIAGRAM



5.1 ULPI Digital Operation and Interface

This section of the USB3370 is covered in detail in Section 6.0, "ULPI Operation".

5.2 USB 2.0 Hi-Speed Transceiver

The blocks in the lower left-hand corner of Figure 6-1 interface to the DP/DM pins.

5.2.1 USB TRANSCEIVER

The USB3370 transceiver includes a Universal Serial Bus Specification Rev 2.0 compliant receiver and transmitter. The DP/DM signals in the USB cable connect directly to the receivers and transmitters.

The receiver consists of receivers for HS and FS/LS mode. Depending on the mode, the selected receiver provides the serial data stream through the multiplexer to the RX Logic block. For HS mode support, the HS RX block contains a squelch circuit to insure that noise is not interpreted as data. The RX block also includes a single-ended receiver on each of the data lines to determine the correct FS linestate.

Data from the Link is encoded, bit stuffed, serialized and transmitted onto the USB cable by the transmitter. Separate differential FS/LS and HS transmitters are included to support all modes.

The USB3370 TX block meets the HS signaling level requirements in the USB 2.0 Specification when the PCB traces from the **DP** and **DM** pins to the USB connector are correctly designed. In some systems the proper 90 ohm differential impedance can not be maintained and it may be desirable to compensate for loss by adjusting the HS transmitter amplitude and this HS squelch threshold. The *PHYBoost* bits in the HS Compensation Register may be configured to adjust the HS transmitter amplitude at the **DP** and **DM** pins. The *VariSense* bits in the HS Compensation Register can also be used to lower the squelch threshold to compensate for losses on the PCB.

To ensure proper operation of the USB transceiver the settings of Table 5-1 must be followed.

5.2.2 TERMINATION RESISTORS

The USB3370 transceiver fully integrates all of the USB termination resistors on both **DP** and **DM**. This includes 1.5kΩ pull-up resistors, 15kΩ pull-down resistors and the 45Ω High Speed termination resistors. These resistors require no tuning or trimming by the Link. The state of the resistors is determined by the operating mode of the transceiver when operating in synchronous mode.

The *XcvrSelect[1:0]*, *TermSelect* and *OpMode[1:0]* bits in the Function Control register, and the *DpPulldown* and *DmPulldown* bits in the OTG Control register control the configuration of the termination resistors. All possible valid resistor combinations are shown in Table 5-1, and operation is ensured in only the configurations shown. If a ULPI Register Setting is configured that does not match a setting in the table, the transceiver operation is not guaranteed and the settings in the last row of Table 5-1 will be used.

- RPU_DP_EN activates the 1.5kΩ DP pull-up resistor
- RPU_DM_EN activates the 1.5kΩ DM pull-up resistor
- RPD_DP_EN activates the 15kΩ DP pull-down resistor
- RPD_DM_EN activates the 15kΩ DM pull-down resistor
- HSTERM_EN activates the 45Ω DP and DM High Speed termination resistors

TABLE 5-1: DP/DM TERMINATION VS. SIGNALING MODE

Signaling Mode	ULPI Register Settings					USB3370 Termination Resistor Settings				
	XcvrSelect[1:0]	*TermSelect*	*OpMode[1:0]*	*DpPulldown*	*DmPulldown*	RPU_DP_EN	RPU_DM_EN	RPD_DP_EN	RPD_DM_EN	HSTERM_EN
General Settings										
Tri-State Drivers, Note 5-1	XXb	Xb	01b	Xb	Xb	0b	0b	0b	0b	0b
Power-up or VBUS < $V_{SESSEND}$	01b	0b	00b	1b	1b	0b	0b	1b	1b	0b
Host Settings										
Host Chirp	00b	0b	10b	1b	1b	0b	0b	1b	1b	1b
Host High Speed	00b	0b	00b	1b	1b	0b	0b	1b	1b	1b
Host Full Speed	X1b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host HS/FS Suspend	01b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host HS/FS Resume	01b	1b	10b	1b	1b	0b	0b	1b	1b	0b
Host Low Speed	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host LS Suspend	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host LS Resume	10b	1b	10b	1b	1b	0b	0b	1b	1b	0b
Host Test J/Test_K	00b	0b	10b	1b	1b	0b	0b	1b	1b	1b
Peripheral Settings										
Peripheral Chirp	00b	1b	10b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS	00b	0b	00b	0b	0b	0b	0b	0b	0b	1b
Peripheral FS	01b	1b	00b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Suspend	01b	1b	00b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Resume	01b	1b	10b	0b	0b	1b	0b	0b	0b	0b
Peripheral LS	10b	1b	00b	0b	0b	0b	1b	0b	0b	0b
Peripheral LS Suspend	10b	1b	00b	0b	0b	0b	1b	0b	0b	0b
Peripheral LS Resume	10b	1b	10b	0b	0b	0b	1b	0b	0b	0b
Peripheral Test J/Test K	00b	0b	10b	0b	0b	0b	0b	0b	0b	1b
OTG device, Peripheral Chirp	00b	1b	10b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS	00b	0b	00b	0b	1b	0b	0b	0b	1b	1b

TABLE 5-1: DP/DM TERMINATION VS. SIGNALING MODE (CONTINUED)

Signaling Mode	ULPI Register Settings					USB3370 Termination Resistor Settings				
	XcvrSelect[1:0]	*TermSelect*	*OpMode[1:0]*	*DpPulldown*	*DmPulldown*	RPU_DP_EN	RPU_DM_EN	RPD_DP_EN	RPD_DM_EN	HSTERM_EN
OTG device, Peripheral FS	01b	1b	00b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS/FS Suspend	01b	1b	00b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS/FS Resume	01b	1b	10b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral Test J/Test K	00b	0b	10b	0b	1b	0b	0b	0b	1b	1b
Charger Detection										
Connect Detect	01b	0b	00b	0b	1b	0b	0b	0b	1b	0b
Any combination not defined above, Note 5-2						0b	0b	1b	1b	0b

Note 1: This is equivalent to Table 40, Section 4.4 of the ULPI 1.1 specification.

2: USB3370 does not support operation as an upstream hub port. See Section 6.4.1.3.

Note 5-1 When **RESETB** = 0 The HS termination will tri-state the USB drivers

Note 5-2 The transceiver operation is not guaranteed in a combination that is not defined.

The USB3370 uses the 27% resistor ECN resistor tolerances. The resistor values are shown in Table 4-5.

5.3 Bias Generator

This block consists of an internal bandgap reference circuit used for generating the driver current and the biasing of the analog circuits. This block requires an external 10KΩ, 1% tolerance, reference resistor connected from **RBIAS** to ground. This resistor should be placed as close as possible to the USB3370 to minimize the trace length. The nominal voltage at **RBIAS** is 0.8V +/- 10% and therefore the resistor will dissipate approximately 80µW of power.

5.4 Crystal Reference Support

The USB3370 provides support for a crystal to provide the reference frequency required by the device in place of a clock oscillator. The crystal should be connected to the REFCLK/XI and XO pins. If a clock oscillator is used in place of a crystal, it should be driven into the REFCLK/XI pin, and the XO pin should be left floating. Proper care should be taken to ensure that a crystal is selected with appropriate power dissipation characteristics.

5.5 Integrated Low Jitter PLL

The USB3370 uses an integrated low jitter phase locked loop (PLL) to provide a clean 480MHz clock required for HS USB signal quality. This clock is used by the PHY during both transmit and receive. The USB3370 PLL requires an accurate frequency reference to be driven on the **REFCLK** pin.

5.5.1 REFCLK FREQUENCY SELECTION

The USB3370 PLL is designed to operate in one of two reference clock modes. In the first mode, the 60MHz ULPI clock is driven on the **REFCLK** pin. In the second mode a reference clock is driven on the **REFCLK** pin. The Link is driving the ULPI clock, in the first mode, and this is referred to as **ULPI Clock Input Mode**. In the second mode, the USB3370 generates the ULPI clock, and this is referred to as **ULPI Clock Output Mode**.

During start-up, the USB3370 monitors the **CLKOUT** pin. If a connection to **VDDIO** is detected, the USB3370 is configured for a 60MHz ULPI reference clock driven on the **REFCLK** pin. Section 5.5.1.1 and Section 5.5.1.2 describe how to configure the USB3370 for either ULPI Clock Input Mode or ULPI Clock Output Mode.

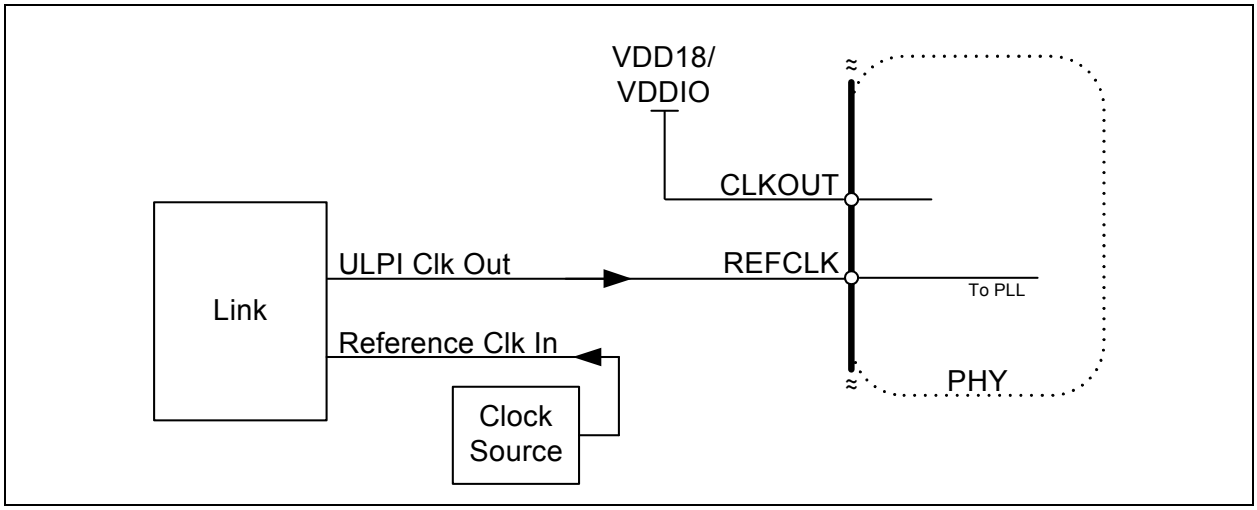
5.5.1.1 ULPI Clock Input Mode (60MHz REFCLK Mode)

When using ULPI Clock Input Mode, the Link must supply the 60MHz ULPI clock to the USB3370. In this mode the 60MHz ULPI Clock is connected to the **REFCLK** pin, and the **CLKOUT** pin is tied high to **VDDIO**.

After the PLL has locked to the correct frequency, the USB3370 will de-assert **DIR** and the Link can begin using the ULPI interface. The USB3370 is ensured to start the clock within the time specified in Table 4-2. For Host applications, the ULPI *AutoResume* bit should be enabled. This is described in Section 6.4.1.4.

For the USB3370, the REF pins should be tied to ground.

FIGURE 5-2: CONFIGURING THE USB3370 FOR ULPI CLOCK INPUT MODE (60 MHZ)



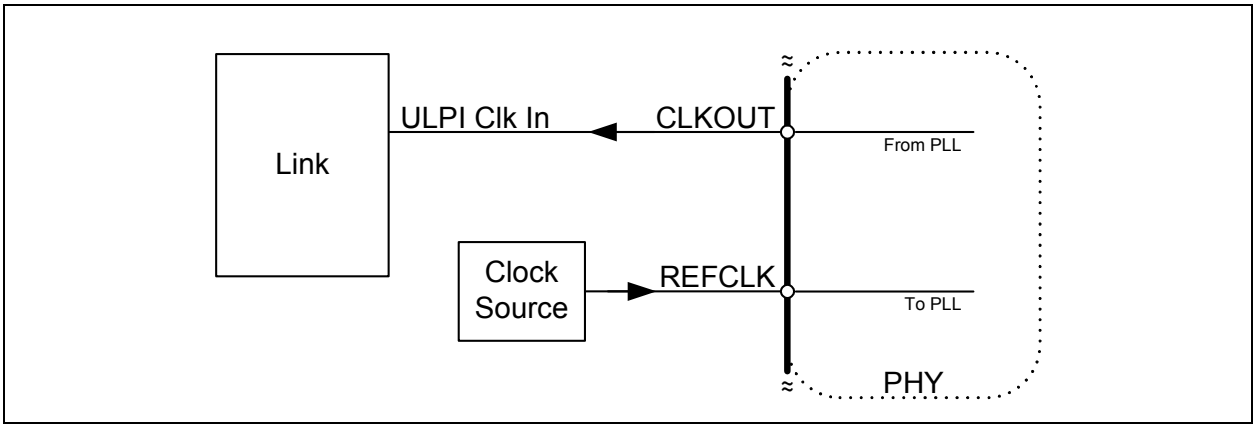
5.5.1.2 ULPI Clock Output Mode

When using ULPI Clock Output Mode, the USB3370 generates the 60MHz ULPI clock used by the Link. In this mode, the **REFCLK** pin must be driven with the model-specific frequency, and the **CLKOUT** pin sources the 60MHz ULPI clock to the Link. When using ULPI Clock Output Mode, the system must not drive the **CLKOUT** pin following POR or hardware reset with a voltage that exceeds the value of V_{IH_ED} provided in Table 4-3. An example of ULPI Clock Output Mode is shown in Figure 8-1

After the PLL has locked to the correct frequency, the USB3370 generates the 60MHz ULPI clock on the **CLKOUT** pin, and de-asserts **DIR** to indicate that the PLL is locked. The USB3370 is ensured to start the clock within the time specified in Table 4-2, and it will be accurate to within ±500ppm. For Host applications the ULPI *AutoResume* bit should be enabled. This is described in Section 6.4.1.4.

When using ULPI Clock Output Mode, the edges of the reference clock do not need to be aligned in any way to the ULPI interface signals. There is no need to align the phase of the **REFCLK** and the **CLKOUT**.

FIGURE 5-3: CONFIGURING THE USB3370 FOR ULPI CLOCK OUTPUT MODE



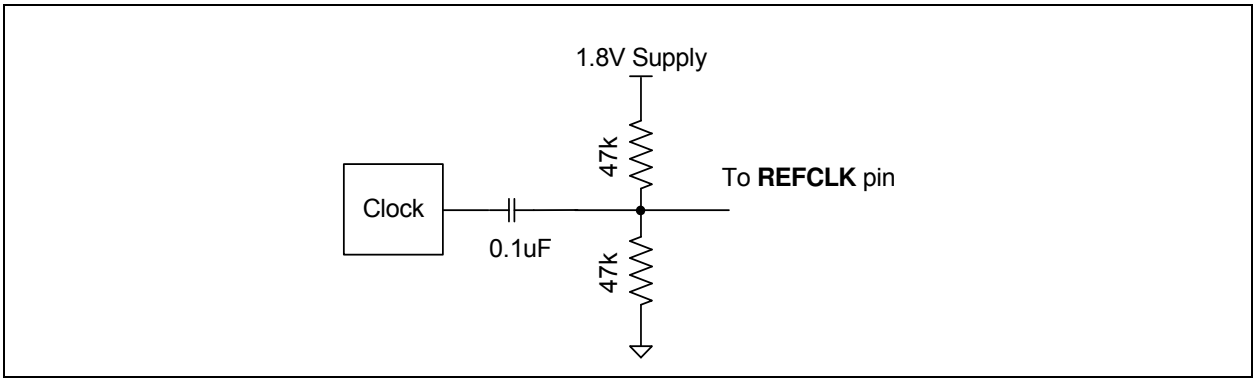
5.5.2 REFCLK AMPLITUDE

The reference clock should be connected to the **REFCLK** pin as shown in the application diagrams, Figure 8-1. The **REFCLK** pin is designed to be driven with a square wave from 0V to **VDDIO**, but can be driven with a square wave from 0V to as high as 3.6V. The USB3370 uses only the positive edge of the **REFCLK**.

If a digital reference is not available, the **REFCLK** pin can be driven by an analog sine wave that is AC coupled into the **REFCLK** pin. If using an analog clock the DC bias should be set at the mid-point of the **VDD18** supply using a bias circuit as shown in Figure 5-4. The amplitude must be greater than 300mV peak to peak. The component values provided in Figure 5-4 are for example only. The actual values should be selected to satisfy system requirements.

The **REFCLK** amplitude must comply with the signal amplitudes shown in Table 4-4 and the duty cycle in Table 4-2.

FIGURE 5-4: EXAMPLE OF CIRCUIT USED TO SHIFT A REFERENCE CLOCK COMMON-MODE VOLTAGE LEVEL



5.5.3 REFCLK JITTER

The USB3370 is tolerant to jitter on the reference clock. The **REFCLK** jitter should be limited to a peak to peak jitter of less than 1nS over a 10uS time interval. If this level of jitter is exceeded when configured for either ULPI Clock Input Mode or ULPI Clock Output Mode, the USB3370 High Speed eye diagram may be degraded.

The frequency accuracy of the REFCLK must meet the +/- 500ppm requirement as shown in Table 4-2.

5.5.4 REFCLK ENABLE/DISABLE

The **REFCLK** should be enabled when the **RESETB** pin is brought high. The ULPI interface will start running after the time specified in Table 4-2. If the reference clock enable is delayed relative to the **RESETB** pin, the ULPI interface will start operation delayed by the same amount. The reference clock can be run at anytime the **RESETB** pin is low without causing the USB3370 to start-up or draw current.

When the USB3370 is placed in Low Power Mode or Carkit Mode, the reference clock can be stopped after the final ULPI register write is complete. The **STP** pin is asserted to bring the USB3370 out of Low Power Mode. The reference clock should be started at the same time **STP** is asserted to minimize the USB3370 start-up time.

If the reference clock is stopped while in ULPI Synchronous mode the PLL will come out of lock and the frequency of oscillation will decrease to the minimum allowed by the PLL design. If the reference clock is stopped during a USB session, the session may drop.

5.6 Internal Regulators and POR

The USB3370 includes integrated power management functions, including a Low-Dropout regulator that can be used to generate the 3.3V USB supply, an integrated 1.8V regulator, and a POR generator described in Section 5.6.2.

5.6.1 INTEGRATED LOW DROPOUT REGULATORS

The USB3370 includes two integrated linear regulators. Power sourced at the **VBAT** pin is regulated to 3.3V and 1.8V output on the **VDD33** and **VDD18** pins. To ensure stability, both regulators require an external bypass capacitor as specified in Table 4-10 placed as close to the pin as possible.

The USB3370 regulators are designed to generate the 3.3 Volt and 1.8 Volt supplies for the USB3370 only. Using the regulators to provide current for other circuits is not recommended and Microchip does not guarantee USB performance or regulator stability.

During USB UART mode the 3.3V regulator output voltage can be changed to allow the USB3370 to work with UARTs operating at different operating voltages. The 3.3V regulator output is configured to the voltages shown in Table 4-10 with the *UART RegOutput[1:0]* bits in the USB IO & Power Management register.

The regulators are enabled by the **RESETB** pin. When **RESETB** pin is low both regulators are disabled and the regulator outputs are pulled low by weak pull-down. The **RESETB** pin must be brought high to enable the regulators.

For peripheral-only or host-only bus-powered applications, the input to **VBAT** may be derived from the VBUS pin of the USB connector. In this configuration, the supply must be capable of withstanding any transient voltage present at the VBUS pin of the USB connector. Microchip does not recommend connecting the **VBAT** pin to the VBUS terminal of the USB connector.

5.6.2 POWER ON RESET (POR)

The USB3370 provides a POR circuit that generates an internal reset pulse after the **VDD18** supply is stable. After the internal POR goes high the USB3370 will release from reset and begin normal ULPI operation as described in Section 5.6.4.

The ULPI registers will power up in their default state summarized in Table 7-1 when the 1.8V supply comes up. Cycling the **RESETB** pin can also be used to reset the ULPI registers to their default state (and reset all internal state machines) by bringing the pin low for a minimum of 1 microsecond and then high. It is not necessary to wait for the **VDD33** and **VDD18** pins to discharge to 0 volts to reset the part.

The **RESETB** pin must be pulled high to enable the 3.3V and 1.8V regulators. A pull-down resistor is not present on the **RESETB** pin and therefore the system should drive the **RESETB** pin to the desired state at all times. If the system does not need to place the USB3370 into reset mode the **RESETB** pin can be connected to a supply between 1.8V and 3.3V.

5.6.3 RECOMMENDED POWER SUPPLY SEQUENCE

For USB operation, the USB3370 requires a valid voltage on the **VBAT** and **VDDIO** pins. The **VDD33** and **VDD18** regulators are automatically enabled when the **RESETB** pin is brought high. For the USB3343, Table 5-2 presents the power supply configurations in more detail.

The **RESETB** pin can be held low until the **VBAT** supply is stable. If the Link is not ready to interface the USB3370, the Link may choose to hold the **RESETB** pin low until it is ready to control the ULPI interface.

TABLE 5-2: OPERATING MODE VS. POWER SUPPLY CONFIGURATION

VBAT	VDDIO	RESETB	Operating Modes Available
0	0	0	Powered Off
1	X	0	RESET Mode. (Note 5-3)
1	1	1	Full USB operation as described in Section 6.0.

Note 5-3 **VDDIO** must be present for ULPI pins to tri-state.

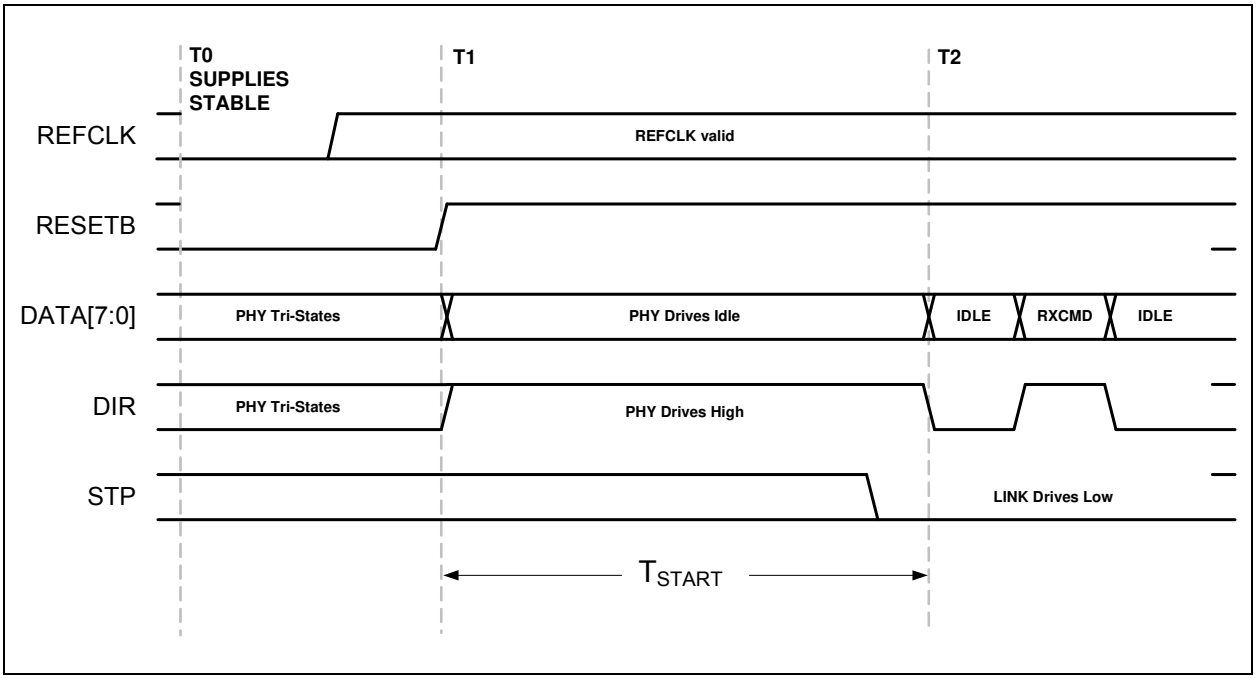
5.6.4 START-UP

The power on default state of the USB3370 is ULPI Synchronous mode. The USB3370 requires the following conditions to begin operation: the power supplies must be stable, the **REFCLK** must be present and the **RESETB** pin must be high. After these conditions are met, the USB3370 will begin ULPI operation that is described in Section 6.0.

Figure 5-5 below shows a timing diagram to illustrate the start-up of the USB3370. At T0, the supplies are stable and the USB3370 is held in reset mode. At T1, the Link drives **RESETB** high after the **REFCLK** has started. The **RESETB** pin may be brought high asynchronously to **REFCLK**. Once, the 3.3V and 1.8V internal supplies become stable the USB3370 will apply the 15Kohm pull downs to the data bus and assert **DIR** until the internal PLL has locked. After the PLL has locked, the USB3370 will check that the Link has de-asserted **STP** and at T2 it will de-assert **DIR** and begin ULPI operation.

The ULPI bus will be available as shown in Figure 5-5 in the time defined as T_{START} given in Table 4-2. If the **REFCLK** signal starts after the **RESETB** pin is brought high, then time T0 will begin when **REFCLK** starts. T_{START} also assumes that the Link has de-asserted **STP**. If the Link has held **STP** high the USB3370 will hold **DIR** high until **STP** is de-asserted. When the LINK de-asserts **STP**, it must be ready drive the ULPI data bus to idle (00h) for a minimum of one clock cycle after **DIR** de-asserts.

FIGURE 5-5: ULPI START-UP TIMING



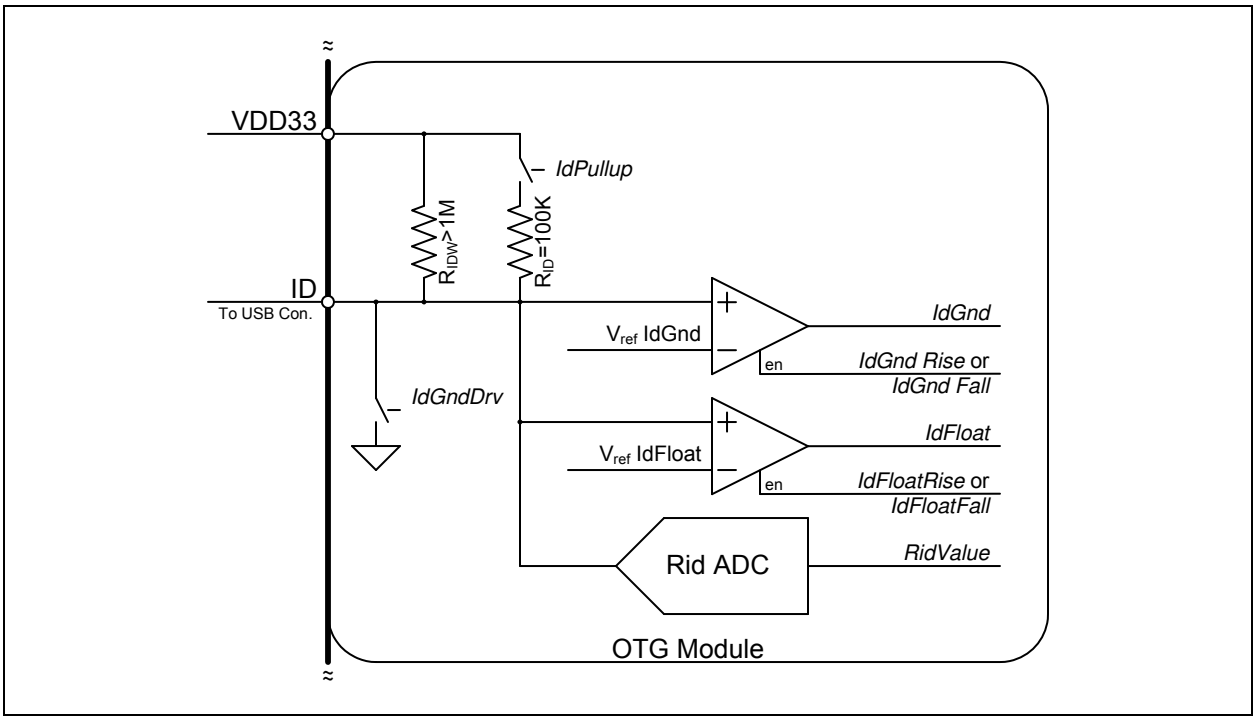
5.7 USB On-The-Go (OTG)

The USB3370 provides support for the USB OTG protocol. OTG allows the USB3370 to be dynamically configured as a host or peripheral depending on the type of cable inserted into the Micro-AB receptacle. When the Micro-A plug of a cable is inserted into the Micro-AB receptacle, the USB device becomes the A-device. When a Micro-B plug is inserted, the device becomes the B-device. The OTG A-device behaves similar to a Host while the B-device behaves similar to a peripheral. The differences are covered in the “On-The-Go Supplement to the USB 2.0 Specification”. In applications where only USB Host or USB Peripheral is required, the OTG Module is unused.

5.7.1 ID RESISTOR DETECTION

The ID pin of the USB connector is monitored by the **ID** pin of the USB3370 to detect the attachment of different types of USB devices and cables. For device only applications that do not use the ID signal the **ID** pin should be connected to **VDD33**. The block diagram of the ID detection circuitry is shown in Figure 5-6 and the related parameters are given in Table 4-8.

FIGURE 5-6: USB3370 ID RESISTOR DETECTION CIRCUITRY



5.7.1.1 USB OTG Operation

The USB3370 can detect **ID** grounded and **ID** floating to determine if an A or B cable has been inserted. The A plug will ground the **ID** pin while the B plug will float the **ID** pin. These are the only two valid states allowed in the OTG Protocol.

To monitor the status of the **ID** pin, the Link activates the *IdPullup* bit in the OTG Control register, waits 50mS and then reads the status of the *IdGnd* bit in the USB Interrupt Status register. If an A cable has been inserted the *IdGnd* bit will read 0. If a B cable is inserted, the **ID** pin is floating and the *IdGnd* bit will read 1.

The USB3370 provides an integrated weak pull-up resistor on the **ID** pin, R_{IDW}. This resistor is present to keep the **ID** pin in a known state when the *IdPullup* bit is disabled and the **ID** pin is floated. In addition to keeping the **ID** pin in a known state, it enables the USB3370 to generate an interrupt to inform the link when a cable with a resistor to ground has been attached to the **ID** pin. The weak pull-up is small enough that the largest valid RID resistor pulls the **ID** pin low and causes the IdGnd comparator to go low.

After the link has detected an **ID** pin state change, the RID converter can be used to determine the resistor value as described in Section 5.7.1.2.

5.7.1.2 Measuring ID Resistance to Ground

The Link can use the integrated resistance measurement capabilities of the USB3370 to determine the value of an ID resistance to ground. The following table details the valid values of resistance to ground that the USB3370 can detect.

FIGURE 5-7: VALID VALUES OF ID RESISTANCE TO GROUND

ID Resistance to Ground	Rid Value
Ground	000
75Ω +/-1%	001
102kΩ +/-1%	010
200kΩ+/-1%	011
Floating	101

Note: IdPullUp = 0

The ID resistance to ground can be read while the USB3370 is in Synchronous Mode. When a resistor to ground is attached to the **ID** pin, the state of the IdGnd comparator will change. After the Link has detected **ID** transition to ground, it can use the methods described in Section 6.8 to operate the Rid converter.

5.7.1.3 Using IdFloat Comparator (not recommended).

Note: The ULPI specification details a method to detect a 102kΩ resistance to ground using the IdFloat comparator. This method can only detect 0ohms, 102kΩ, and floating terminations of the **ID** pin. Due to this limitation it is recommended to use the RID Converter as described in Section 5.7.1.2.

The **ID** pin can be either grounded, floated, or connected to ground with a 102kΩ external resistor. To detect the 102K resistor, set the *idPullup* bit in the OTG Control register, causing the USB3370 to apply the 100K internal pull-up connected between the **ID** pin and VDD33. Set the *idFloatRise* and *idFloatFall* bits in the Carkit Interrupt Enable register to enable the IdFloat comparator to generate an RXCMD to the Link when the state of the IdFloat changes. As described in Figure 6-3, the alt_int bit of the RXCMD will be set. The values of IdGnd and IdFloat are shown for the three types cables that can attach to the USB Connector in Table 5-3.

TABLE 5-3: IDGND AND IDFLOAT VS. ID RESISTANCE TO GROUND

ID Resistance	IDGND	IDFLOAT
Float	1	1
102K	1	0
GND	0	0

Note: The ULPI register bits *IdPullUp*, *IdFloatRise,* and *IdFloatFall* should be enabled.

To save current when an A Plug is inserted, the internal 102kΩ pull-up resistor can be disabled by clearing the *IdPullUp* bit in the OTG Control register and the *IdFloatRise* and *IdFloatFall* bits in both the USB Interrupt Enable Rising and USB Interrupt Enable Falling registers. If the cable is removed the weak R_{IDW} will pull the **ID** pin high.

The *IdGnd* value can be read using the ULPI USB Interrupt Status register, bit 4. In host mode, it can be set to generate an interrupt when *IdGnd* changes by setting the appropriate bits in the USB Interrupt Enable Rising and USB Interrupt Enable Falling registers. The *IdFloat* value can be read by reading the ULPI Carkit Interrupt Status register bit 0.

Note: The IdGnd switch has been provided to ground the **ID** pin for future applications.