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USB3450

Hi-Speed USB Host or Device PHY With UTMI+ Interface

Highlights

- USB-IF “Hi-Speed” certified to the Universal Serial Bus Specification Rev. 2.0
- Interface compliant with the UTMI+ Specification, Rev. 1.0
- Functional as a host or device PHY
- Supports HS, FS, and LS data rates
- Supports FS pre-amble for FS hubs with a LS device attached (UTMI+ Level 3)
- Supports HS SOF and LS keep alive pulse
- Low Latency Hi-Speed Receiver (43 Hi-Speed clocks Max)
- Internal 1.8 volt regulators allow operation from a single 3.3 volt supply
- Internal short circuit protection of DP and DM lines to VBUS or ground
- Integrated 24MHz Crystal Oscillator supports either crystal operation or 24MHz external clock input
- Internal PLL for 480MHz Hi-Speed USB operation
- Supports Hi-Speed USB and legacy USB 1.1 devices
- 55mA Unconfigured Current (typical) - ideal for bus powered applications
- 83uA suspend current (typical) - ideal for battery powered applications
- Full Commercial operating temperature range from 0°C to +70°C
- 40 pin QFN RoHS compliant package (6 x 6 x 0.9mm height)

Functional Overview

The USB3450 is a highly integrated USB transceiver system. It contains a complete Hi-Speed PHY with the UTMI+ industry standard interface to support fast time to market for a USB controller. The USB3450 is composed of the functional blocks shown below.

USB3450 Block Diagram

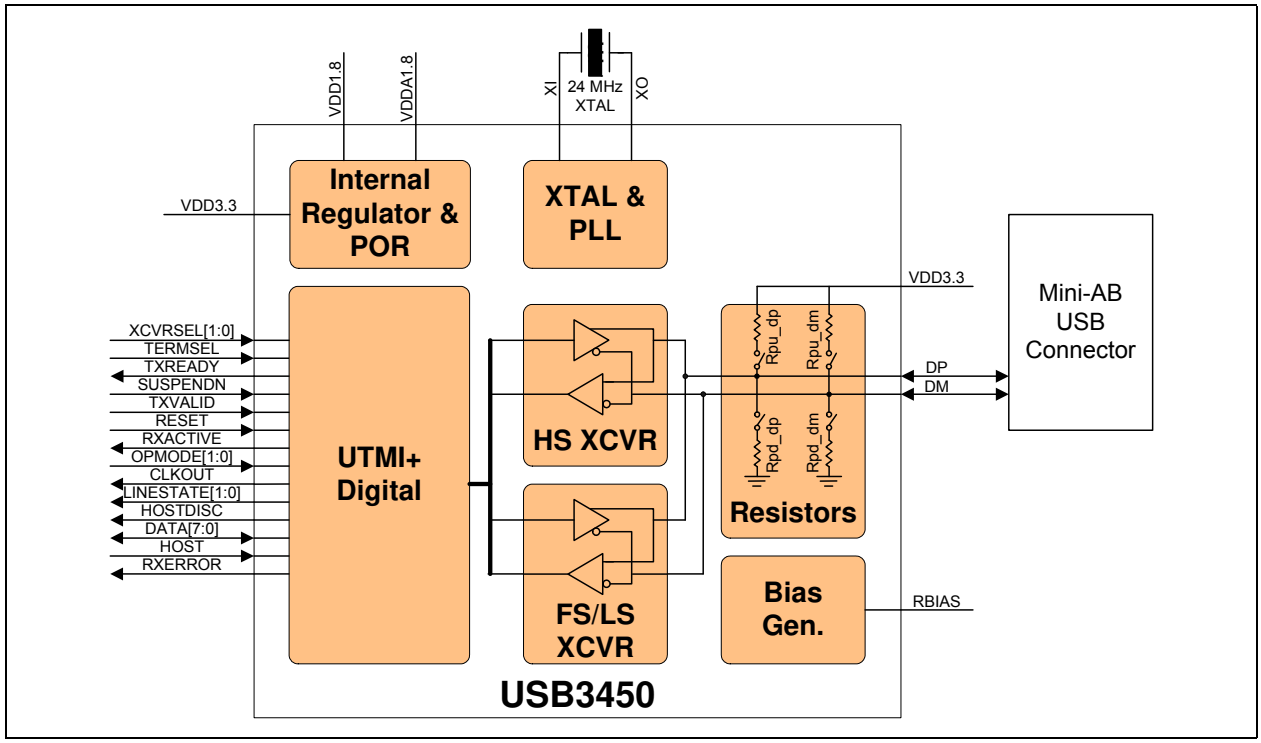

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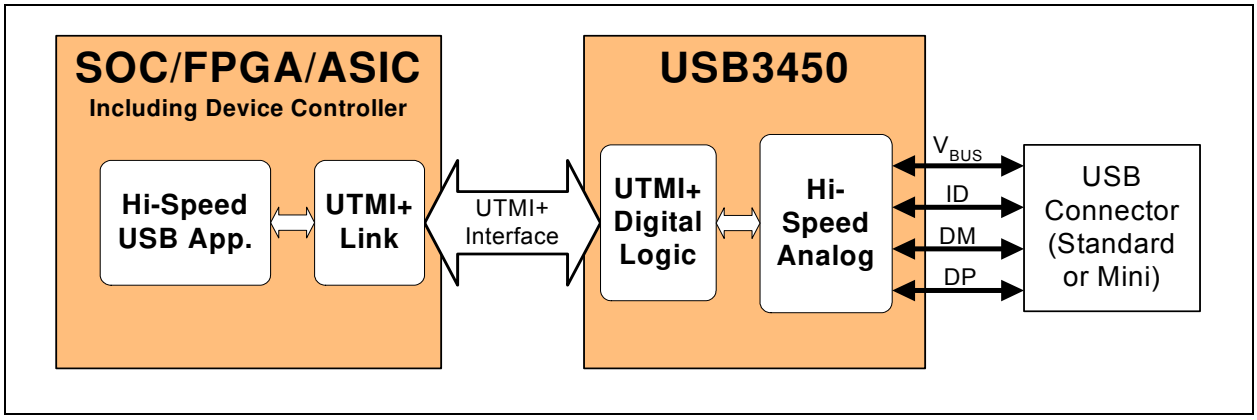
Table of Contents

1.0 GENERAL DESCRIPTION

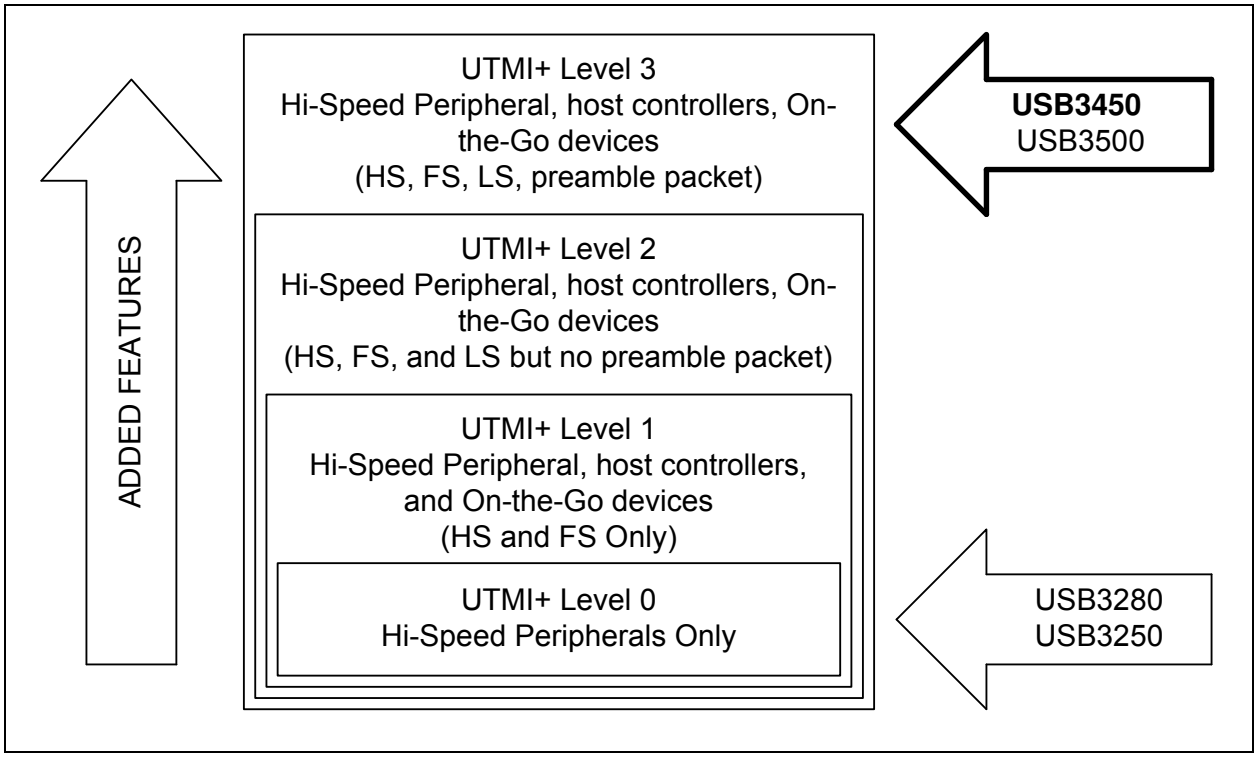
The USB3450 is a stand-alone Hi-Speed USB Physical Layer Transceiver (PHY). The USB3450 uses a UTMI+ interface to connect to an SOC or ASIC or FPGA. Microchip's advanced proprietary technology minimizes power dissipation, resulting in maximum battery life for portable applications. The USB3450 is a flexible solution for adding USB to new designs without integrating the analog PHY block.

FIGURE 1-1: BASIC UTMI+ USB DEVICE BLOCK DIAGRAM



The USB3450 provides a fully compliant Hi-Speed interface, and supports Hi-Speed (HS), Full-Speed (FS), and Low-Speed (LS) USB. The USB3450 supports all levels of the UTMI+ specification as shown in Figure 1-2.

FIGURE 1-2: UTMI+ LEVEL 3 SUPPORT



1.1 Applications

The USB3450 is targeted for any application where a high speed USB connection is desired.

The USB3450 is well suited for:

- Cell Phones
- MP3 Players
- Scanners
- Set Top Boxes
- Printers
- External Hard Drives
- Still and Video Cameras
- Portable Media Players
- Entertainment Devices

1.2 Reference Documents

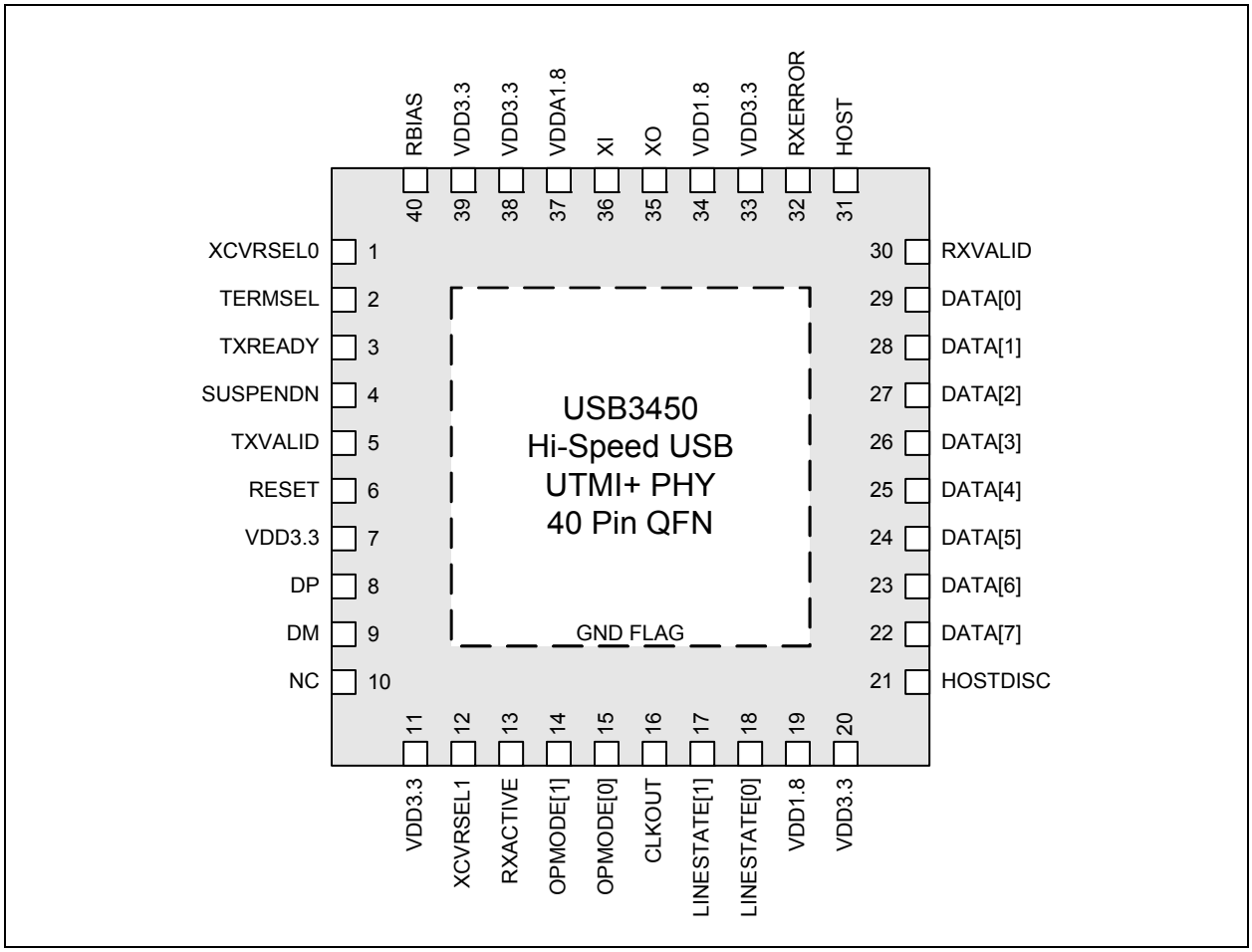
- Universal Serial Bus Specification, Revision 2.0, April 27, 2000
- Hi-Speed Transceiver Macrocell Interface (UTMI) Specification, Version 1.02, May 27, 2000
- UTMI+ Specification, Revision 1.0, February 2, 2004

2.0 PIN CONFIGURATION AND PIN DEFINITIONS

The USB3450 is offered in a 40 pin QFN package. The pin definitions and locations are documented below.

2.1 USB3450 Pin Locations

FIGURE 2-1: USB3450 PINOUT - TOP VIEW



The flag of the QFN package must be connected to ground.

2.2 Pin Definitions

TABLE 2-1: USB3450 PIN DEFINITIONS

Pin	Name	Direction, Type	Active Level	Description
1	XCVRSEL[0]	Input	N/A	Transceiver Select. These signals select between the FS and HS transceivers: Transceiver select. 00: HS 01: FS 10: LS 11: LS data, FS rise/fall times
2	TERMSEL	Input	N/A	Termination Select. This signal selects between the FS and HS terminations: 0: HS termination enabled 1: FS termination enabled
3	TXREADY	Output	High	Transmit Data Ready. If TXVALID is asserted, the Link must always have data available for clocking into the TX Holding Register on the rising edge of CLKOUT. TXREADY is an acknowledgment to the Link that the transceiver has clocked the data from the bus and is ready for the next transfer on the bus. If TXVALID is negated, TXREADY can be ignored by the Link.
4	SUSPENDN	Input	Low	Suspend. Places the transceiver in a mode that draws minimal power from supplies. In host mode, R_{PU} is removed during suspend. In device mode, R_{PD} is controlled by TERMSEL. In suspend mode the clocks are off. 0: PHY in suspend mode 1: PHY in normal operation
5	TXVALID	Input	High	Transmit Valid. Indicates that the DATA bus is valid for transmit. The assertion of TXVALID initiates the transmission of SYNC on the USB bus. The negation of TXVALID initiates EOP on the USB. Control inputs (OPMODE[1:0], TERMSEL,XCVERSEL) must not be changed on the de-assertion or assertion of TXVALID.
6	RESET	Input	High	Reset. Reset all state machines. After coming out of reset, must wait 5 rising edges of clock before asserting TXValid for transmit. Assertion of Reset: May be asynchronous to CLKOUT De-assertion of Reset: Must be synchronous to CLKOUT
7	VDD3.3	N/A	N/A	3.3V PHY Supply. Provides power for Hi-Speed Transceiver, UTMI+ Digital, Digital I/O, and Regulators.
8	DP	I/O, Analog	N/A	D+ pin of the USB cable.
9	DM	I/O, Analog	N/A	D- pin of the USB cable.
10	NC	N/A	N/A	No Connect.
11	VDD3.3	N/A	N/A	3.3V PHY Supply.
12	XCVRSEL[1]	Input	N/A	Transceiver Select. These signals select between the FS and HS transceivers: Transceiver select. 00: HS 01: FS 10: LS 11: LS data, FS rise/fall times
13	RXACTIVE	Output	High	Receive Active. Indicates that the receive state machine has detected Start of Packet and is active.

TABLE 2-1: USB3450 PIN DEFINITIONS (CONTINUED)

Pin	Name	Direction, Type	Active Level	Description
14	OPMODE[1]	Input	N/A	Operational Mode. These signals select between the various operational modes: [1] [0] Description 0 0 0: Normal Operation 0 1 1: Non-driving (all terminations removed) 1 0 2: Disable bit stuffing and NRZI encoding 1 1 3: Reserved
15	OPMODE[0]	Input	N/A	
16	CLKOUT	Output, CMOS	N/A	60MHz reference clock output. All UTMI+ signals are driven synchronous to this clock.
17	LINESTATE[1]	Output	N/A	Line State. These signals reflect the current state of the USB data bus in FS mode. Bit [0] reflects the state of DP and bit [1] reflects the state of DM. When the device is suspended or resuming from a suspended state, the signals are combinatorial. Otherwise, the signals are synchronized to CLKOUT. [1] [0] Description 0 0 0: SEO 0 1 1: J State 1 0 2: K State 1 1 3: SE1
18	LINESTATE[0]	Output	N/A	
19	VDD1.8	N/A	N/A	1.8V regulator output for digital circuitry on chip. Place a 0.1uF capacitor near this pin and connect the capacitor from this pin to ground. Connect pin 19 to pin 34.
20	VDD3.3	N/A	N/A	3.3V PHY Supply. Provides power for Hi-Speed Transceiver, UTMI+ Digital, Digital I/O, and Regulators.
21	HOSTDISC	Output	High	Host Disconnect. Indicates that a downstream device has been disconnected from this host PHY when operating in HS host mode. Automatically reset to 0b when Low Power Mode is entered.
22	DATA[7]	I/O, CMOS, Pull-low	N/A	8-bit bi-directional data bus. Data[7] is the MSB and Data[0] is the LSB.
23	DATA[6]	I/O, CMOS, Pull-low	N/A	
24	DATA[5]	I/O, CMOS, Pull-low	N/A	
25	DATA[4]	I/O, CMOS, Pull-low	N/A	
26	DATA[3]	I/O, CMOS, Pull-low	N/A	
27	DATA[2]	I/O, CMOS, Pull-low	N/A	
28	DATA[1]	I/O, CMOS, Pull-low	N/A	
29	DATA[0]	I/O, CMOS, Pull-low	N/A	

TABLE 2-1: USB3450 PIN DEFINITIONS (CONTINUED)

Pin	Name	Direction, Type	Active Level	Description
30	RXVALID	Output	High	Receive Data Valid. Indicates that the DATA bus has received valid data. The Receive Data Holding Register is full and ready to be unloaded. The Link is expected to register the DATA bus on the rising edge of CLKOUT.
31	HOST	Input	N/A	Host Pull-down Select. This signal enables the 15k Ohm pull-down resistor on the DM line. 0: Pull-down resistor not connected to DM 1: Pull-down resistor connected to DM
32	RXERROR	Output	High	Receive Error. This output is clocked with the same timing as the receive DATA lines and can occur at anytime during a transfer. 0: Indicates no error. 1: Indicates a receive error has been detected.
33	VDD3.3	N/A	N/A	3.3V PHY Supply. Provides power for Hi-Speed Transceiver, UTMI+ Digital, Digital I/O, and Regulators.
34	VDD1.8	N/A	N/A	1.8V regulator output for digital circuitry on chip. Place a 4.7uF low ESR capacitor near this pin and connect the capacitor from this pin to ground. Connect pin 34 to pin 19. See Section 5.6.1, "Internal Regulators".
35	XO	Output, Analog	N/A	Crystal pin. If using an external clock on XI this pin should be floated.
36	XI	Input, Analog	N/A	Crystal pin. A 24MHz crystal is supported. The crystal is placed across XI and XO. An external 24MHz clock source may be driven into XI in place of a crystal.
37	VDDA1.8	N/A	N/A	1.8V regulator output for analog circuitry on chip. Place a 0.1uF capacitor near this pin and connect the capacitor from this pin to ground. In parallel, place a 4.7uF low ESR capacitor near this pin and connect the capacitor from this pin to ground. See Section 5.6.1, "Internal Regulators".
38	VDD3.3	N/A	N/A	3.3V PHY Supply. Provides power for Hi-Speed Transceiver, UTMI+ Digital, Digital I/O, and Regulators.
39	VDD3.3	N/A	N/A	3.3V PHY Supply. Should be connected directly to pin 39.
40	RBIAS	Analog, CMOS	N/A	External 1% bias resistor. Requires a 12KΩ resistor to ground.
	GND FLAG	Ground	N/A	Ground. The flag must be connected to the ground plane.

3.0 LIMITING VALUES

TABLE 3-1: MAXIMUM RATINGS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
Maximum VBUS, ID, DP, and DM voltage to GND	V_{MAX_5V}		-0.5		+5.5	V
Maximum VDD1.8 and VDDA1.8 voltage to Ground	$V_{MAX\_1.8V}$		-0.5		2.5	V
Maximum 3.3V supply voltage to Ground	$V_{MAX\_3.3V}$		-0.5		4.0	V
Maximum I/O voltage to Ground	V_{MAX_IN}		-0.5		4.0	V
Operating Temperature	T_{MAX_OP}		0		70	C
Storage Temperature	T_{MAX_STG}		-55		150	C

Note: Stresses above those listed could cause damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

TABLE 3-2: RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
3.3V Supply Voltage	$V_{DD3.3}$		3.0	3.3	3.6	V
Input Voltage on Digital Pins	V_I		0.0		$V_{DD3.3}$	V
Input Voltage on Analog I/O Pins (DP, DM)	$V_{I(I/O)}$		0.0		$V_{DD3.3}$	V
Ambient Temperature	T_A		0		+70	^oC

TABLE 3-3: RECOMMENDED EXTERNAL CLOCK CONDITIONS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
System Clock Frequency		XI driven by the external clock; and no connection at XO		24 (±100ppm)		MHz
System Clock Duty Cycle		XI driven by the external clock; and no connection at XO	45	50	55	%

4.0 ELECTRICAL CHARACTERISTICS

TABLE 4-1: ELECTRICAL CHARACTERISTICS: SUPPLY PINS (Note 4-1)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
Unconfigured Current	$I_{AVG(UCFG)}$	Device Unconfigured		55		mA
FS Idle Current	$I_{AVG(FS)}$	FS idle not data transfer		55		mA
FS Transmit Current	$I_{AVG(FSTX)}$	FS current during data transmit		60.5		mA
FS Receive Current	$I_{AVG(FSRX)}$	FS current during data receive		57.5		mA
HS Idle Current	$I_{AVG(HS)}$	FS idle not data transfer		60.6		mA
HS Transmit Current	$I_{AVG(HSTX)}$	FS current during data transmit		62.4		mA
HS Receive Current	$I_{AVG(HSRX)}$	FS current during data receive		61.5		mA
Low Power Mode	$I_{DD(LPM)}$	VBUS 15kΩ pull-down and 1.5kΩ pull-up resistor currents not included.		83		uA

Note 4-1 $V_{DD3.3}$ = 3.0 to 3.6V; V_{SS} = 0V; T_A = 0C to +70C; unless otherwise specified.

TABLE 4-2: ELECTRICAL CHARACTERISTICS: CLKOUT START-UP

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
Suspend Recovery Time	T_{START}			2.25	3.5	ms

TABLE 4-3: DC ELECTRICAL CHARACTERISTICS: LOGIC PINS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
Low-Level Input Voltage	V_{IL}		V_{SS}		0.8	V
High-Level Input Voltage	V_{IH}		2.0		$V_{DD3.3}$	V
Low-Level Output Voltage	V_{OL}	I_{OL} = 8mA			0.4	V
High-Level Output Voltage	V_{OH}	I_{OH} = -8mA	$V_{DD3.3}$ - 0.4			V
Input Leakage Current	I_{LI}				±10	uA
Pin Capacitance	Cpin				4	pF

Note: $V_{DD3.3}$ = 3.0 to 3.6V; V_{SS} = 0V; T_A = 0C to +70C; unless otherwise specified.

TABLE 4-4: DC ELECTRICAL CHARACTERISTICS: ANALOG I/O PINS (DP/DM)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
FS FUNCTIONALITY						
Input levels						
Differential Receiver Input Sensitivity	V_{DIFS}	| V(DP) - V(DM) |	0.2			V
Differential Receiver Common-Mode Voltage	V_{CMFS}		0.8		2.5	V
Single-Ended Receiver Low Level Input Voltage	V_{ILSE}				0.8	V
Single-Ended Receiver High Level Input Voltage	V_{IHSE}		2.0			V
Single-Ended Receiver Hysteresis	V_{HYSSE}		0.050		0.150	V
Output Levels						
Low Level Output Voltage	V_{FSOL}	Pull-up resistor on DP; R_L = 1.5kΩ to $V_{DD3.3}$			0.3	V
High Level Output Voltage	V_{FSOH}	Pull-down resistor on DP, DM; R_L = 15kΩ to GND	2.8		3.6	V
Termination						
Driver Output Impedance for HS and FS	Z_{HSDRV}	Steady state drive	40.5	45	49.5	Ù
Input Impedance	Z_{INP}	TX, RPU disabled	1.0			MΩ
Pull-up Resistor Impedance	Z_{PU}	Bus Idle	0.900	1.24	1.575	kΩ
Pull-up Resistor Impedance	Z_{PURX}	Device Receiving	1.425	2.26	3.09	kΩ
Pull-dn Resistor Impedance	Z_{PD}		14.25	15.0	15.75	kΩ
HS FUNCTIONALITY						
Input levels						
HS Differential Input Sensitivity	V_{DIHS}	| V(DP) - V(DM) |	100			mV
HS Data Signaling Common Mode Voltage Range	V_{CMHS}		-50		500	mV
HS Squelch Detection Threshold (Differential)	V_{HSSQ}	Squelch Threshold			100	mV
		Un-squelch Threshold	150			mV
Output Levels						
Hi-Speed Low Level Output Voltage (DP/DM referenced to GND)	V_{HSOL}	45Ω load	-10		10	mV
Hi-Speed High Level Output Voltage (DP/DM referenced to GND)	V_{HSOH}	45Ω load	360		440	mV
Hi-Speed IDLE Level Output Voltage (DP/DM referenced to GND)	V_{OLHS}	45Ω load	-10		10	mV
Chirp-J Output Voltage (Differential)	V_{CHIRPJ}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	700		1100	mV
Chirp-K Output Voltage (Differential)	V_{CHIRPK}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	-900		-500	mV

TABLE 4-4: DC ELECTRICAL CHARACTERISTICS: ANALOG I/O PINS (DP/DM) (CONTINUED)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
Leakage Current						
OFF-State Leakage Current	I_{LZ}				±10	uA
Port Capacitance						
Transceiver Input Capacitance	C_{IN}	Pin to GND		5	10	pF

Note: $V_{DD3.3}$ = 3.0 to 3.6V; V_{SS} = 0V; T_A = 0C to +70C; unless otherwise specified.

TABLE 4-5: DYNAMIC CHARACTERISTICS: ANALOG I/O PINS (DP/DM)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
FS Output Driver Timing						
Rise Time	T_{FSR}	C_L = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
Fall Time	T_{FFF}	C_L = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
Output Signal Crossover Voltage	V_{CRS}	Excluding the first transition from IDLE state	1.3		2.0	V
Differential Rise/Fall Time Matching	FRFM	Excluding the first transition from IDLE state	90		111.1	%
HS Output Driver Timing						
Differential Rise Time	T_{HSR}		500			ps
Differential Fall Time	T_{HSF}		500			ps
Driver Waveform Requirements		Eye pattern of Template 1 in Hi-Speed specification				
Hi-Speed Mode Timing						
Receiver Waveform Requirements		Eye pattern of Template 4 in Hi-Speed specification				
Data Source Jitter and Receiver Jitter Tolerance		Eye pattern of Template 4 in Hi-Speed specification				

Note: $V_{DD3.3}$ = 3.0 to 3.6V; V_{SS} = 0V; T_A = 0C to +70C; unless otherwise specified.

TABLE 4-6: REGULATOR OUTPUT VOLTAGES

Parameter	Symbol	Condition	MIN	TYP	MAX	Units
$V_{DDA1.8}$	$V_{DDA1.8}$	Normal Operation (SUSPENDN = 1)	1.6	1.8	2.0	V
$V_{DDA1.8}$	$V_{DDA1.8}$	Low Power mode (SUSPENDN = 0)		0		V
$V_{DD1.8}$	$V_{DD1.8}$		1.6	1.8	2.0	V

Note: $V_{DD3.3}$ = 3.0 to 3.6V; V_{SS} = 0V; T_A = 0C to +70C; unless otherwise specified.

5.0 DETAILED FUNCTIONAL OVERVIEW

FIGURE 2-1: on page 5 shows the functional block diagram of the USB3450. Each of the functions is described in detail below.

5.1 8bit Bi-Directional Data Bus Operation

The USB3450 supports an 8-bit bi-directional parallel interface.

- CLKOUT runs at 60MHz
- The 8-bit data bus (DATA[7:0]) is used for transmit when TXVALID = 1
- The 8-bit data bus (DATA[7:0]) is used for receive when TXVALID = 0

Figure 5-1 shows the relationship between CLKOUT and the transmit data transfer signals in FS mode. TXREADY is only asserted for one CLKOUT per byte time to signal the Link that the data on the DATA lines has been read by the PHY. The Link may hold the data on the DATA lines for the duration of the byte time. Transitions of TXVALID must meet the defined setup and hold times relative to CLKOUT.

FIGURE 5-1: FS CLK RELATIONSHIP TO TRANSMIT DATA AND CONTROL SIGNALS

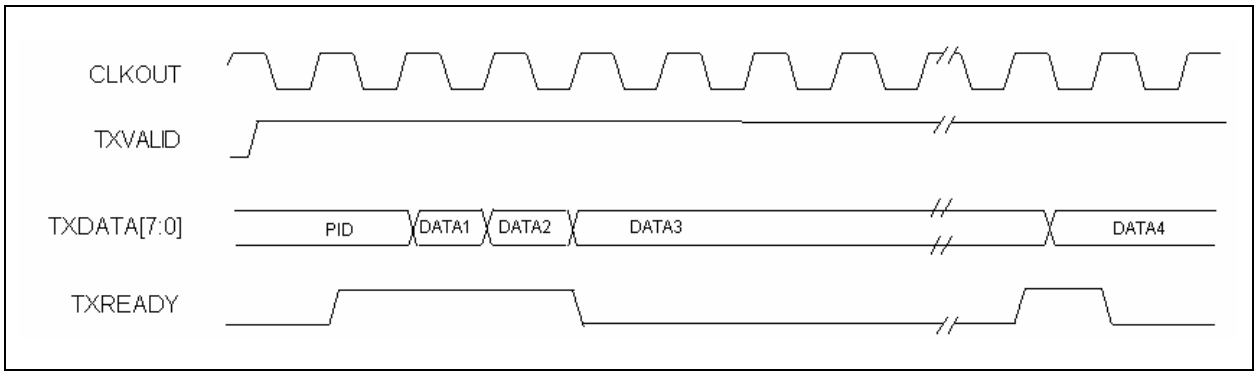
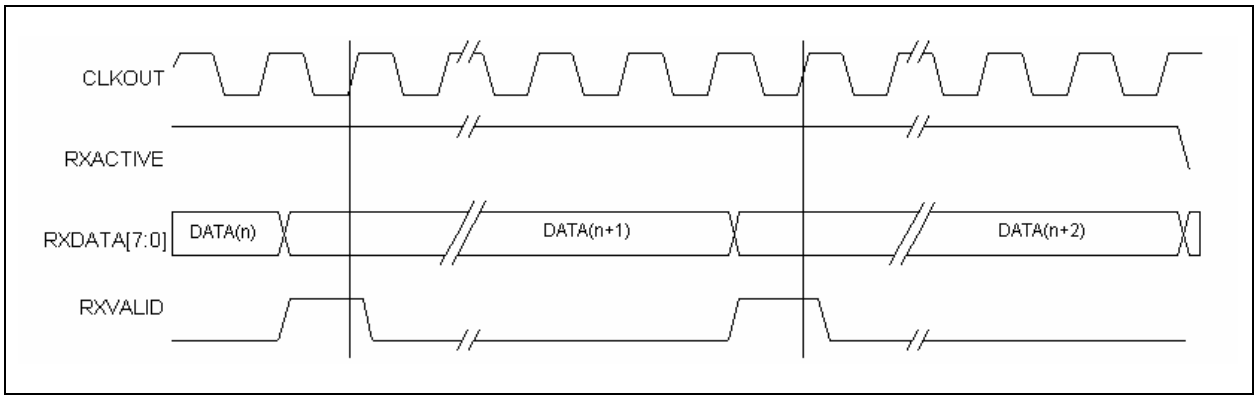


Figure 5-2 shows the relationship between CLKOUT and the receive data control signals in FS mode. RXACTIVE “frames” a packet, transitioning only at the beginning and end of a packet. However transitions of RXVALID may take place any time 8 bits of data are available. Figure 5-2 also shows how RXVALID is only asserted for one CLKOUT cycle per byte time even though the data may be presented for the full byte time. The XCVRSELECT signal determines whether the HS or FS timing relationship is applied to the data and control signals.

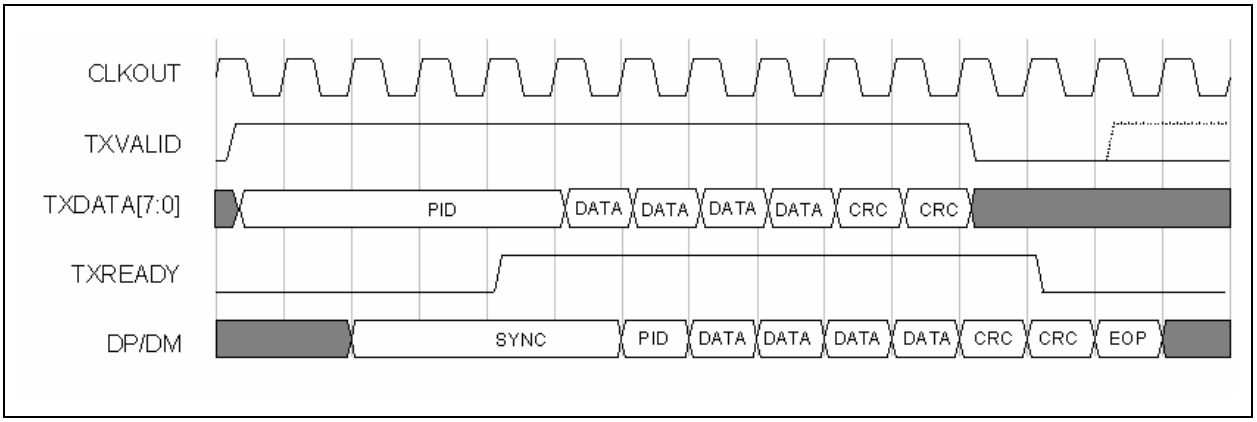
FIGURE 5-2: FS CLK RELATIONSHIP TO RECEIVE DATA AND CONTROL SIGNALS



5.2 TX Logic

This block receives parallel data bytes placed on the DATA bus and performs the necessary transmit operations. These operations include parallel to serial conversion, bit stuffing and NRZI encoding. Upon valid assertion of the proper TX control lines by the Link and TX State Machine, the TX LOGIC block will synchronously shift, at either the FS or HS rate, the data to the FS/HS TX block to be transmitted on the USB cable. Data transmit timing is shown in Figure 5-3.

FIGURE 5-3: TRANSMIT TIMING FOR A DATA PACKET



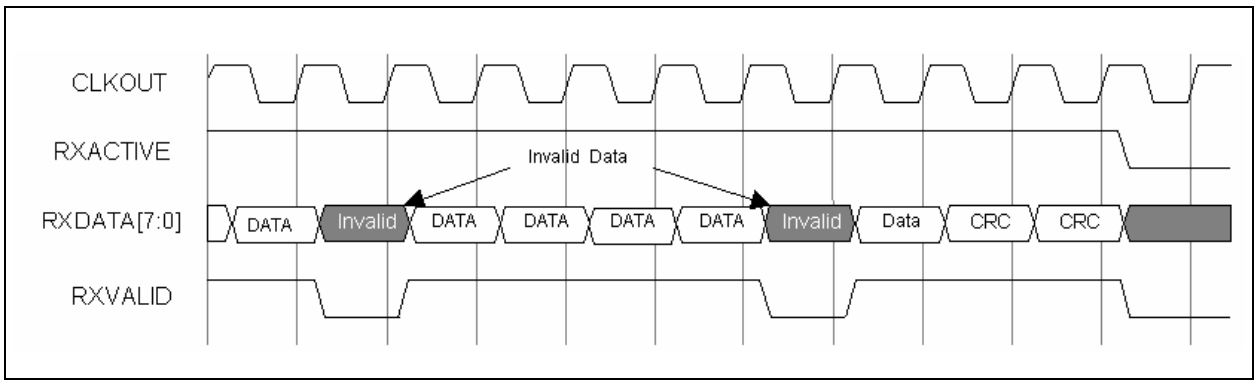
The behavior of the Transmit State Machine is described below.

- The Link asserts TXVALID to begin a transmission.
- After the Link asserts TXVALID it can assume that the transmission has started when it detects TXREADY has been asserted.
- The Link must assume that the USB3450 has consumed a data byte if TXREADY and TXVALID are asserted on the rising edge of CLKOUT.
- The Link must have valid packet information (PID) asserted on the DATA bus coincident with the assertion of TXVALID.
- TXREADY is sampled by the Link on the rising edge of CLKOUT.
- The Link negates TXVALID to complete a packet. Once negated, the transmit logic will never reassert TXREADY until after the EOP has been generated. (TXREADY will not re-assert until TXVALD asserts again.
- The USB3450 is ready to transmit another packet immediately, however the Link must conform to the minimum inter-packet delays identified in the Hi-Speed specification.
- Supports high speed disconnect detect through the HOSTDISC pin. In Host mode the USB3450 will sample the disconnect comparator at the 32nd bit of the 40 bit long EOP during SOF packets.
- Supports FS pre-amble for FS hubs with a LS device.
- Supports LS keep alive by receiving the SOF PID.
- Supports Host mode resume K which ends with two low speed times of SE0 followed by 1 FS “J”.

5.3 RX Logic

This block receives serial data from the clock recovery circuits and processes it to be transferred to the Link on the DATA bus. The processing involved includes NRZI decoding, bit unstuffing, and serial to parallel conversion. Upon valid assertion of the proper RX control lines, the RX Logic block will provide bytes to the DATA bus as shown in the figures below. The behavior of the receiver is described below.

FIGURE 5-4: RECEIVE TIMING FOR DATA WITH UNSTUFFED BITS



The assertion of RESET will cause the USB3450 to deasserts RXACTIVE and RXVALID. When the RESET signal is deasserted the Receive State Machine starts looking for a SYNC pattern on the USB. When a SYNC pattern is detected the receiver will assert RXACTIVE. The length of the received Hi-Speed SYNC pattern varies and can be up to 32 bits long or as short as 12 bits long when at the end of five hubs.

After valid serial data is received, the data is loaded into the RX Holding Register on the rising edge of CLKOUT and RXVALID is asserted. The Link must clock the data off the DATA bus on the next rising edge of CLKOUT. In normal mode (OPMODE = 00), then stuffed bits are stripped from the data stream. Each time 8 stuffed bits are accumulated the USB3450 will negate RXVALID for one clock cycle, thus skipping a byte time.

When the EOP is detected the USB3450 will negate RXACTIVE and RXVALID. After the EOP has been stripped the USB3450 will begin looking for the next packet.

The behavior of the USB3450 receiver is described below:

- RXACTIVE and RXREADY are sampled on the rising edge of CLKOUT.
- After a EOP is complete the receiver will begin looking for SYNC.
- The USB3450 asserts RXACTIVE when SYNC is detected.
- The USB3450 negates RXACTIVE when an EOP is detected and the elasticity buffer is empty.
- When RXACTIVE is asserted, RXVALID will be asserted if the RX Holding Register is full.
- RXVALID will be negated if the RX Holding Register was not loaded during the previous byte time. This will occur if 8 stuffed bits have been accumulated.
- The Link must be ready to consume a data byte if RXACTIVE and RXVALID are asserted (RX Data state).
- Figure 5-5 shows the timing relationship between the received data (DP/DM), RXVALID, RXACTIVE, RXERROR and DATA signals.

Note:

- Figure 5-5, Figure 5-6 and Figure 5-7 are timing examples of a HS/FS PHY when it is in HS mode. When a HS/FS PHY is in FS Mode there are approximately 40 CLKOUT cycles every byte time. The Receive State Machine assumes that the Link captures the data on the DATA bus if RXACTIVE and RXVALID are asserted. In FS mode, RXVALID will only be asserted for one CLKOUT per byte time.
- In Figure 5-5, Figure 5-6 and Figure 5-7 the SYNC pattern on DP/DM is shown as one byte long. The SYNC pattern received by a device can vary in length. These figures assume that all but the last 12 bits have been consumed by the hubs between the device and the host controller.

FIGURE 5-5: RECEIVE TIMING FOR A HANDSHAKE PACKET (NO CRC)

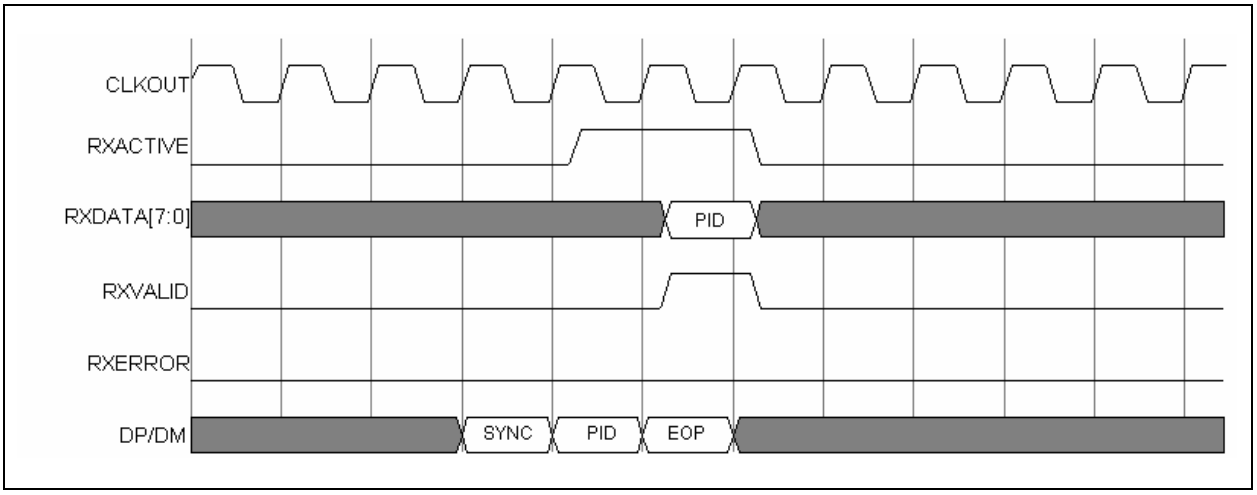


FIGURE 5-6: RECEIVE TIMING FOR SETUP PACKET

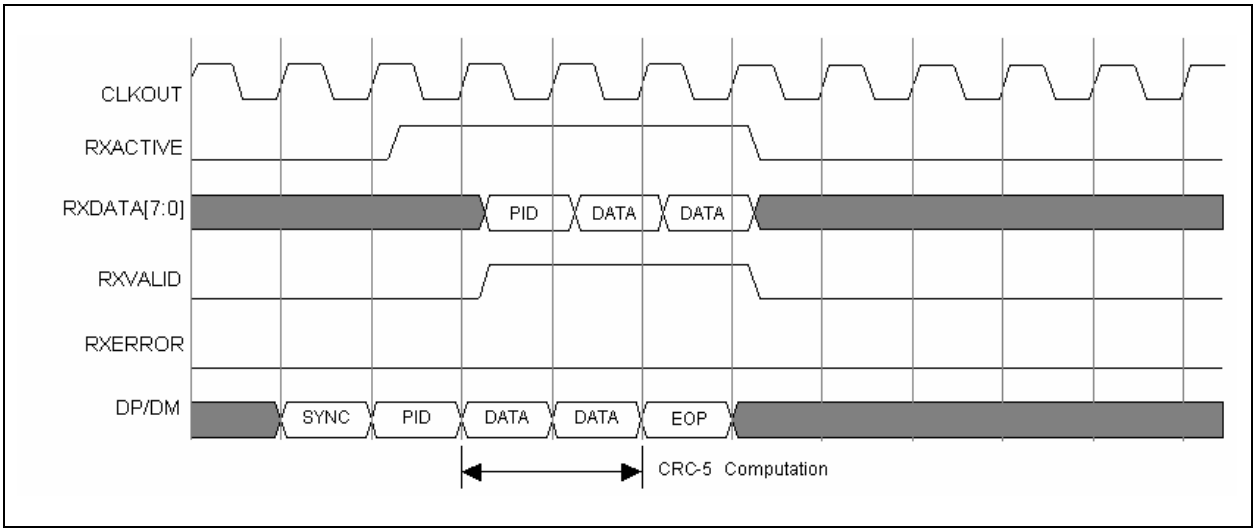
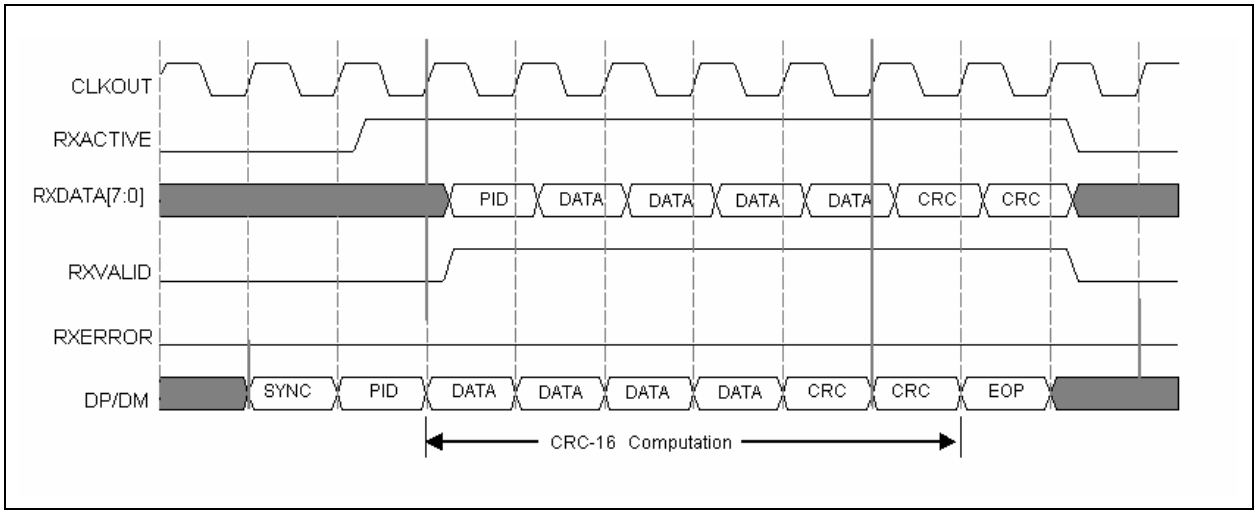


FIGURE 5-7: RECEIVE TIMING FOR DATA PACKET (WITH CRC-16)



The receivers connect directly to the USB cable. The block contains a separate differential receiver for HS and FS mode. Depending on the mode, the selected receiver provides the serial data stream through the mulitplexer to the RX Logic block. The FS mode section of the FS/HS RX block also consists of a single-ended receiver on each of the data lines to determine the correct FS LINESTATE. For HS mode support, the FS/HS RX block contains a squelch circuit to insure that noise is never interpreted as data.

5.4 Hi-Speed Transceiver

The Microchip Hi-Speed Transceiver consists of four blocks in the lower left corner of FIGURE 2-1: on page 5. These four blocks are labeled HS XCVR, FS/LS XCVR, Resistors, and Bias Gen.

5.4.1 HIGH SPEED AND FULL SPEED TRANSCEIVERS

The USB3450 transceiver meets all requirements in the Hi-Speed specification.

The receivers connect directly to the USB cable. This block contains a separate differential receiver for HS and FS mode. Depending on the mode, the selected receiver provides the serial data stream through the multiplexer to the RX Logic block. The FS mode section of the FS/HS RX block also consists of a single-ended receiver on each of the data lines to determine the correct FS linestate. For HS mode support, the FS/HS RX block contains a squelch circuit to insure that noise is never interpreted as data.

The transmitters connect directly to the USB cable. The block contains a separate differential FS and HS transmitter which receive encoded, bit stuffed, serialized data from the TX Logic block and transmit it on the USB cable.

5.4.2 TERMINATION RESISTORS

The USB3450 transceiver fully integrates all of the USB termination resistors. The USB3450 includes two 1.5kΩ pull-up resistors on DP and DM and a 15kΩ pull-down resistor on both DP and DM. In addition the 45Ω high speed termination resistors are also integrated. These integrated resistors require no tuning or trimming by the Link. The state of the resistors is determined by the operating mode of the PHY. The possible valid resistor combinations are shown in Figure 5-8. Operation is provided in the configurations given in Table 5-8, "DP/DM termination vs. Signaling Mode".

- RPU_DP_EN activates the 1.5kΩ DP pull-up resistor
- RPU_DM_EN activates the 1.5kΩ DM pull-up resistor
- RPD_DP_EN activates the 15kΩ DP pull-down resistor
- RPD_DM_EN activates the 15kΩ DM pull-down resistor
- HSTERM_EN activates the 45Ω DP and DM high speed termination resistors

FIGURE 5-8: DP/DM TERMINATION VS. SIGNALING MODE

Signaling Mode	UTMI+ Interface Settings				Resistor Settings				
	XCVRSEL[1:0]	TERMSEL	OPMODE[1:0]	HOST	RPU_DP_EN	RPU_DM_EN	RPD_DP_EN	RPD_DM_EN	HSTERM_EN
General Settings									
Tri-State Drivers	XXb	Xb	01b	Xb	0b	0b	0b	0b	0b
Power-up or Vbus < $V_{SESSEND}$	01b	0b	00b	1b	0b	0b	1b	1b	0b
Host Settings									
Host Chirp	00b	0b	10b	1b	0b	0b	1b	1b	1b
Host Hi-Speed	00b	0b	00b	1b	0b	0b	1b	1b	1b
Host Full Speed	X1b	1b	00b	1b	0b	0b	1b	1b	0b
Host HS/FS Suspend	01b	1b	00b	1b	0b	0b	1b	1b	0b
Host HS/FS Resume	01b	1b	10b	1b	0b	0b	1b	1b	0b
Host low Speed	10b	1b	00b	1b	0b	0b	1b	1b	0b
Host LS Suspend	10b	1b	00b	1b	0b	0b	1b	1b	0b
Host LS Resume	10b	1b	10b	1b	0b	0b	1b	1b	0b
Host Test J/Test_K	00b	0b	10b	1b	0b	0b	1b	1b	1b
Peripheral Settings									
Peripheral Chirp	00b	1b	10b	0b	1b	0b	0b	0b	0b
Peripheral HS	00b	0b	00b	0b	0b	0b	0b	0b	1b
Peripheral FS	01b	1b	00b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Suspend	01b	1b	00b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Resume	01b	1b	10b	0b	1b	0b	0b	0b	0b
Peripheral LS	10b	1b	00b	0b	0b	1b	0b	0b	0b
Peripheral LS Suspend	10b	1b	00b	0b	0b	1b	0b	0b	0b
Peripheral LS Resume	10b	1b	10b	0b	0b	1b	0b	0b	0b
Peripheral Test J/Test K	00b	0b	10b	0b	0b	0b	0b	0b	1b

5.4.3 BIAS GENERATOR

This block consists of an internal bandgap reference circuit used for generating the high speed driver currents and the biasing of the analog circuits. This block requires an external 12KΩ, 1% tolerance, external reference resistor connected from RBIAS to ground.

5.5 Crystal Oscillator and PLL

The USB3450 uses an internal crystal driver and PLL sub-system to provide a clean 480MHz reference clock that is used by the PHY during both transmit and receive. The USB3450 requires a clean 24MHz crystal or clock as a frequency reference. If the 24MHz reference is noisy or off frequency the PHY may not operate correctly.

The USB3450 can use either a crystal or an external clock oscillator for the 24MHz reference. The crystal is connected to the XI and XO pins as shown in the application diagram, Figure 6-9. If a clock oscillator is used the clock should be connected to the XI input and the XO pin left floating. When an external clock is used the XI pin is designed to be driven with a 0 to 3.3 volt signal. When using an external clock the user needs to take care to ensure the external clock source is clean enough to not degrade the high speed eye performance.

Once, the 480MHz PLL has locked to the correct frequency it will drive the CLKOUT pin with a 60MHz clock. The USB3450 will start the clock within the time specified in Table 4-2.

5.6 Internal Regulators and POR

The USB3450 includes an integrated set of built in power management functions. These power management features include a POR generation and allow the USB3450 to be powered from a single 3.3 volt power supply. This reduces the bill of materials and simplifies product design.

5.6.1 INTERNAL REGULATORS

The USB3450 has two internal regulators that create two 1.8V outputs (labeled VDD1.8 and VDDA1.8) from the 3.3volt power supply input (VDD3.3). Each regulator requires an external 4.7uF +/-20% low ESR bypass capacitor to ensure stability. X5R or X7R ceramic capacitors are recommended since they exhibit an ESR lower that 0.1ohm at frequencies greater than 10kHz.

The specific capacitor recommendations for each pin are detailed in Table 2-1, “USB3450 Pin Definitions,” on page 7, and shown in FIGURE 6-9: USB3450 Application Diagram (Top View) on page 32.

Note:	The USB3450 regulators are designed to generate a 1.8 volt supply for the USB3450 only. Using the regulators to provide current for other circuits is not recommended and Microchip does not ensure USB performance or regulator stability.

5.6.2 POWER ON RESET (POR)

The USB3450 provides an internal POR circuit that generates a reset pulse once the PHY supplies are stable. The UTMI+ Digital can be reset at any time with the RESET pin.

6.0 APPLICATION NOTES

The following sections consist of select functional explanations to aid in implementing the USB3450 into a system. For complete description and specifications consult the *Hi-Speed Transceiver Macrocell Interface Specification* and *Universal Serial Bus Specification Revision 2.0.*

6.1 Linestate

The voltage thresholds that the LINESTATE[1:0] signals use to reflect the state of DP and DM depend on the state of XCVRSELECT. LINESTATE[1:0] uses HS thresholds when the HS transceiver is enabled (XCVRSELECT = 0) and FS thresholds when the FS transceiver is enabled (XCVRSELECT = 1). There is not a concept of variable single-ended thresholds in the Hi-Speed specification for HS mode.

The HS receiver is used to detect Chirp J or K, where the output of the HS receiver is always qualified with the Squelch signal. If squelched, the output of the HS receiver is ignored. In the USB3450, as an alternative to using variable thresholds for the single-ended receivers, the following approach is used.

TABLE 6-1: LINESTATE STATES

		State of DP/DM Lines		
Linestate[1:0]		**Full Speed XCVRSELECT =1 TERMSELECT=1**	**High Speed XCVRSELECT =0 TERMSELECT=0**	**Chirp Mode XCVRSELECT =0 TERMSELECT=1**
LS[1]	**LS[0]**			
0	0	SE0	Squelch	Squelch
0	1	J	$\overline{\text{Squelch}}$	$\overline{\text{Squelch}}$ & HS Diff. Receiver Output
1	0	K	Invalid	$\overline{\text{Squelch}}$ & HS Diff. Receiver Output
1	1	SE1	Invalid	Invalid

In HS mode, 3ms of no USB activity (IDLE state) signals a reset. The Link monitors LINESTATE[1:0] for the IDLE state. To minimize transitions on LINESTATE[1:0] while in HS mode, the presence of $\overline{\text{Squelch}}$ is used to force LINESTATE[1:0] to a J state.

6.2 OPMODES

The OPMODE[1:0] pins allow control of the operating modes.

TABLE 6-2: OPERATIONAL MODES

Mode[1:0]	State#	State Name	Description
00	0	Normal Operation	Transceiver operates with normal USB data encoding and decoding
01	1	Non-Driving	Allows the transceiver logic to support a soft disconnect feature which tri-states both the HS and FS transmitters, and removes any termination from the USB making it appear to an upstream port that the device has been disconnected from the bus
10	2	Disable Bit Stuffing and NRZI encoding	Disables bitstuffing and NRZI encoding logic so that 1's loaded from the DATA bus become 'J's on the DP/DM and 0's become 'K's
11	3	Reserved	N/A

The OPMODE[1:0] signals are normally changed only when the transmitter and the receiver are quiescent, i.e. when entering a test mode or for a device initiated resume.

When using OPMODE[1:0] = 10 the SYNC and EOP patterns are not transmitted.

The only exception to this is when OPMODE[1:0] is set to state 2 while TXVALID has been asserted (the transceiver is transmitting a packet), in order to flag a transmission error. In this case, the USB3450 has already transmitted the SYNC pattern so upon negation of TXVALID the EOP must also be transmitted to properly terminate the packet. Changing the OPMODE[1:0] signals under all other conditions, while the transceiver is transmitting or receiving data will generate undefined results.

6.3 Test Mode Support

TABLE 6-3: HI-SPEED TEST MODES

Hi-Speed Test Modes	USB3450 Setup		
	Operational Mode	Link Transmitted Data	XCVRSELECT & TERMSELECT
SE0_NAK	State 0	No transmit	HS
J	State 2	All '1's	HS
K	State 2	All '0's	HS
Test_Packet	State 0	Test Packet data	HS

6.4 SE0 Handling

For FS operation, IDLE is a J state on the bus. SE0 is used as part of the EOP or to indicate reset. When asserted in an EOP, SE0 is never asserted for more than 2 bit times. The assertion of SE0 for more than 2.5us is interpreted as a reset by the device operating in FS mode.

For HS operation, IDLE is a SE0 state on the bus. SE0 is also used to reset a HS device. A HS device cannot use the 2.5us assertion of SE0 (as defined for FS operation) to indicate reset since the bus is often in this state between packets. If no bus activity (IDLE) is detected for more than 3ms, a HS device must determine whether the downstream facing port is signaling a suspend or a reset. The following section details how this determination is made. If a reset is signaled, the HS device will then initiate the HS Detection Handshake protocol.

6.5 Reset Detection

If a device in HS mode detects bus inactivity for more than 3ms (T1), it reverts to FS mode. This enables the FS pull-up on the DP line in an attempt to assert a continuous FS J state on the bus. The Link must then check LINESTATE for the SE0 condition. If SE0 is asserted at time T2, then the upstream port is forcing the reset state to the device (i.e., a Driven SE0). The device will then initiate the HS detection handshake protocol.

FIGURE 6-1: RESET TIMING BEHAVIOR (HS MODE)

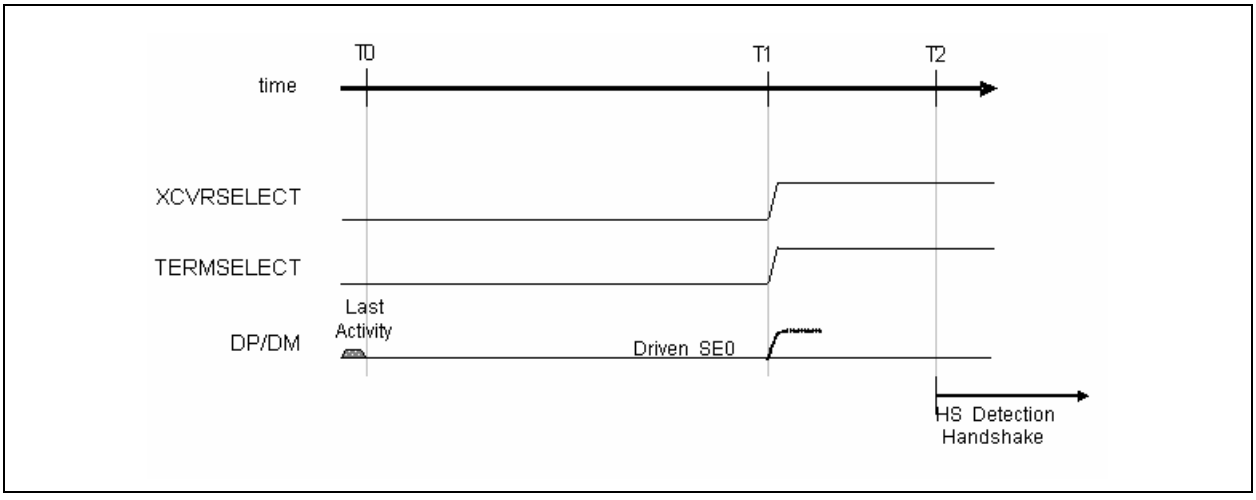


TABLE 6-4: RESET TIMING VALUES (HS MODE)

Timing Parameter	Description	Value
HS Reset T0	Bus activity ceases, signaling either a reset or a SUSPEND.	0 (reference)
T1	Earliest time at which the device may place itself in FS mode after bus activity stops.	HS Reset T0 + 3. 0ms < T1 < HS Reset T0 + 3.125ms
T2	Link samples LINESTATE. If LINESTATE = SE0, then the SE0 on the bus is due to a Reset state. The device now enters the HS Detection Handshake protocol.	T1 + 100µs < T2 < T1 + 875µs

6.6 Suspend Detection

If a HS device detects SE0 asserted on the bus for more than 3ms (T1), it reverts to FS mode. This enables the FS pull-up on the DP line in an attempt to assert a continuous FS J state on the bus. The Link must then check LINESTATE for the J condition. If J is asserted at time T2, then the upstream port is asserting a soft SE0 and the USB is in a J state indicating a suspend condition. By time T4 the device must be fully suspended.

FIGURE 6-2: SUSPEND TIMING BEHAVIOR (HS MODE)

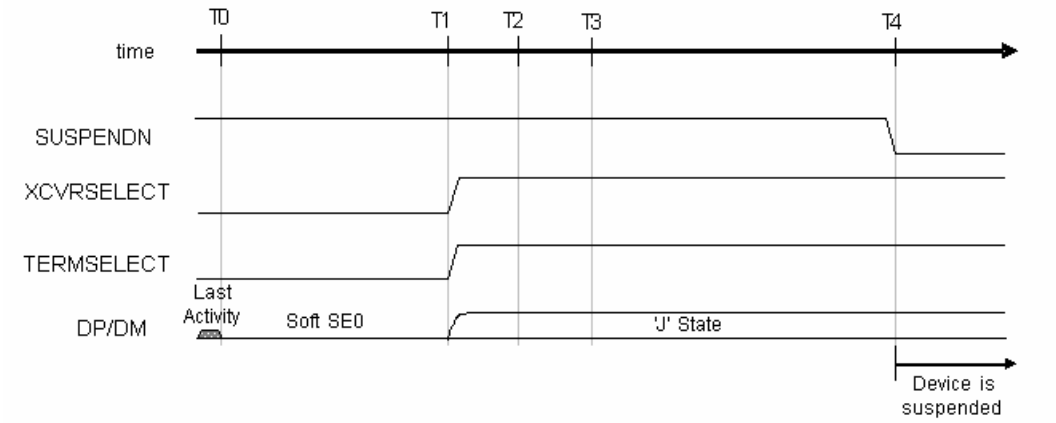


TABLE 6-5: SUSPEND TIMING VALUES (HS MODE)

Timing Parameter	Description	Value
HS Reset T0	End of last bus activity, signaling either a reset or a SUSPEND.	0 (reference)
T1	The time at which the device must place itself in FS mode after bus activity stops.	HS Reset T0 + 3. 0ms < T1 < HS Reset T0 + 3.125ms
T2	Link samples LINESTATE. If LINESTATE = 'J', then the initial SE0 on the bus (T0 - T1) had been due to a Suspend state and the Link remains in HS mode.	T1 + 100 µs < T2 < T1 + 875µs
T3	The earliest time where a device can issue Resume signaling.	HS Reset T0 + 5ms
T4	The latest time that a device must actually be suspended, drawing no more than the suspend current from the bus.	HS Reset T0 + 10ms

6.7 HS Detection Handshake

The High Speed Detection Handshake process is entered from one of three states: suspend, active FS or active HS. The downstream facing port asserting an SE0 state on the bus initiates the HS Detection Handshake. Depending on the initial state, an SE0 condition can be asserted from 0 to 4 ms before initiating the HS Detection Handshake. These states are described in the Hi-Speed specification.

There are three ways in which a device may enter the HS Handshake Detection process:

1. If the device is suspended and it detects an SE0 state on the bus it may immediately enter the HS handshake detection process.
2. If the device is in FS mode and an SE0 state is detected for more than 2.5µs. it may enter the HS handshake detection process.
3. If the device is in HS mode and an SE0 state is detected for more than 3.0ms. it may enter the HS handshake detection process. In HS mode, a device must first determine whether the SE0 state is signaling a suspend or a reset condition. To do this the device reverts to FS mode by placing XCVRSELECT and TERMSELECT into FS mode. The device must not wait more than 3.125ms before the reversion to FS mode. After reverting to FS mode, no less than 100µs and no more than 875µs later the Link must check the LINESTATE signals. If a J state is detected the device will enter a suspend state. If an SE0 state is detected, then the device will enter the HS Handshake detection process.

In each case, the assertion of the SE0 state on the bus initiates the reset. The minimum reset interval is 10ms. Depending on the previous mode that the bus was in, the delay between the initial assertion of the SE0 state and entering the HS Handshake detection can be from 0 to 4ms.

This transceiver design pushes as much of the responsibility for timing events on to the Link as possible, and the Link requires a stable CLKOUT signal to perform accurate timing. In case 2 and 3 above, CLKOUT has been running and is stable, however in case 1 the USB3450 is reset from a suspend state, and the internal oscillator and clocks of the transceiver are assumed to be powered down. A device has up to 6ms after the release of SUSPENDN to assert a minimum of a 1ms Chirp K.

6.8 HS Detection Handshake – FS Downstream Facing Port

Upon entering the HS Detection process (T0) XCVRSELECT and TERMSELECT are in FS mode. The DP pull-up is asserted and the HS terminations are disabled. The Link then sets OPMODE to *Disable Bit Stuffing and NRZI encoding*, XCVRSELECT to HS mode, and begins the transmission of all 0's data, which asserts a HS K (chirp) on the bus (T1). The device chirp must last at least 1.0ms, and must end no later than 7.0ms after HS Reset T0. At time T1 the device begins listening for a chirp sequence from the host port.

If the downstream facing port is not HS capable, then the HS K asserted by the device is ignored and the alternating sequence of HS Chirp K's and J's is not generated. If no chirps are detected (T4) by the device, it will enter FS mode by returning XCVRSELECT to FS mode.

FIGURE 6-3: HS DETECTION HANDSHAKE TIMING BEHAVIOR (FS MODE)

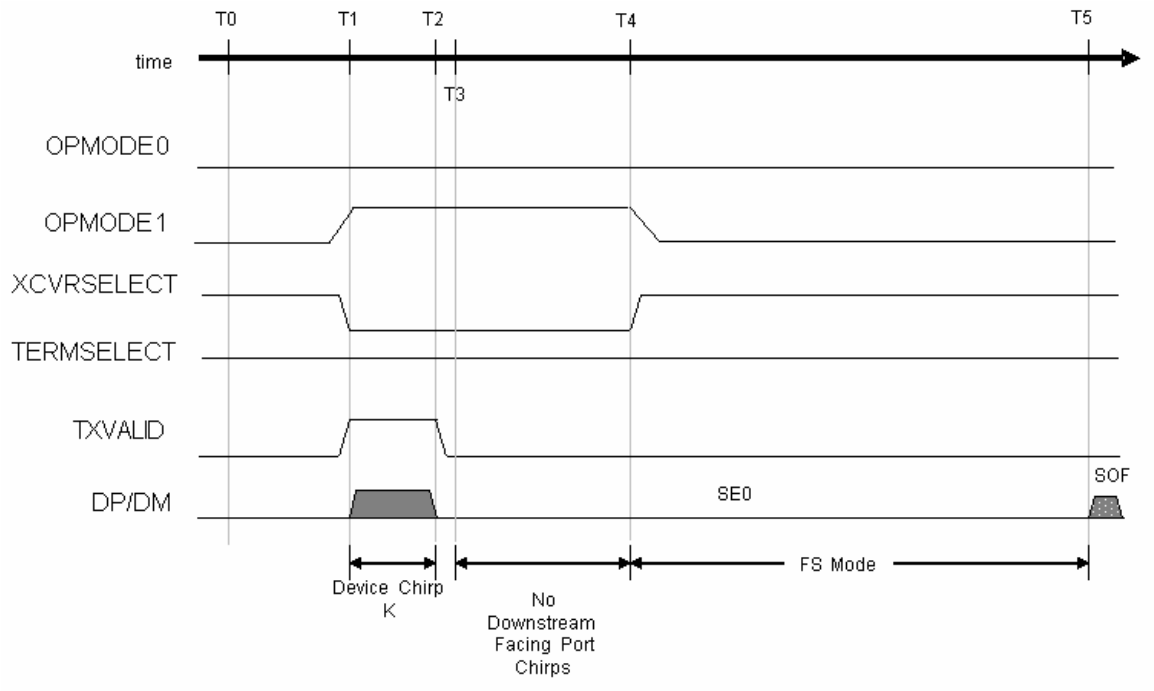


TABLE 6-6: HS DETECTION HANDSHAKE TIMING VALUES (FS MODE)

Timing Parameter	Description	Value
T0	HS Handshake begins. DP pull-up enabled, HS terminations disabled.	0 (reference)
T1	Device enables HS Transceiver and asserts Chirp K on the bus.	T0 < T1 < HS Reset T0 + 6.0ms
T2	Device removes Chirp K from the bus. 1ms minimum width.	T1 + 1.0 ms < T2 < HS Reset T0 + 7.0ms
T3	Earliest time when downstream facing port may assert Chirp KJ sequence on the bus.	T2 < T3 < T2+100µs
T4	Chirp not detected by the device. Device reverts to FS default state and waits for end of reset.	T2 + 1.0ms < T4 < T2 + 2.5ms
T5	Earliest time at which host port may end reset	HS Reset T0 + 10ms

Note:

- T0 may occur to 4ms after HS Reset T0.
- The Link must assert the Chirp K for 66000 CLKOUT cycles to ensure a 1ms minimum duration.