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USB3500

Hi-Speed USB Host, Device or OTG PHY With UTMI+ Interface

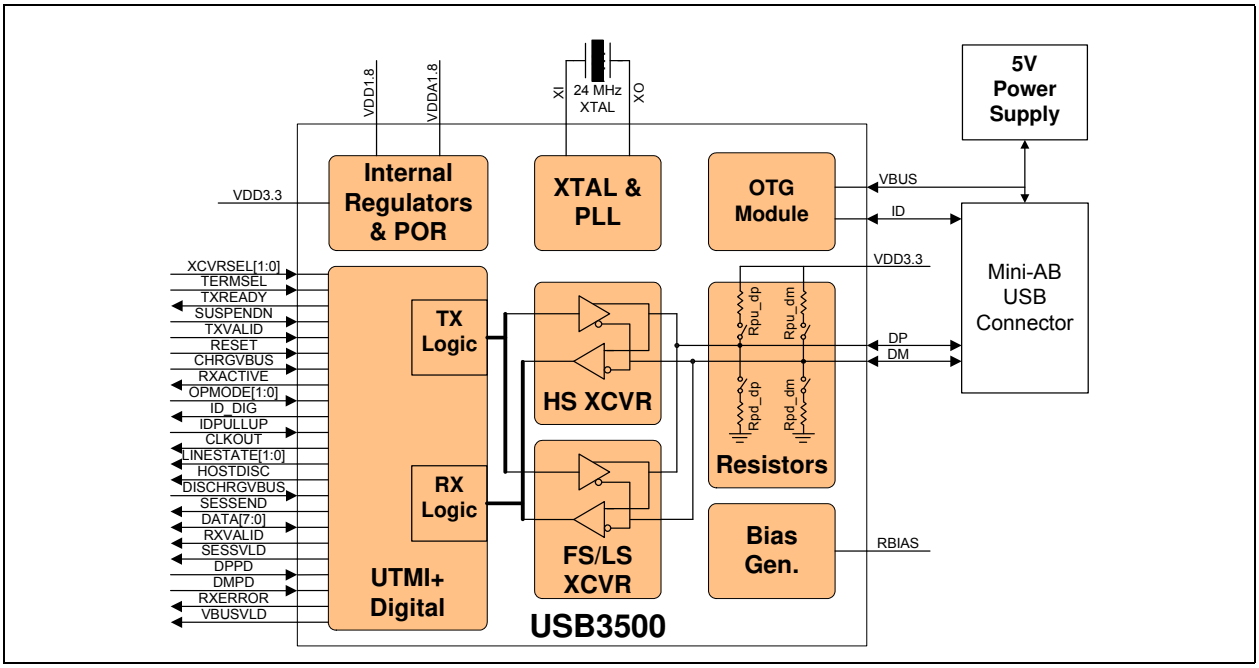
Highlights

- USB-IF “Hi-Speed” certified to the Universal Serial Bus Specification Rev 2.0
- Interface compliant with the UTMI+ Specification, Revision 1.0
- Includes full support for the optional On-The-Go (OTG) protocol detailed in the On-The-Go Supplement Revision 1.0a specification
- Functional as a host, device or OTG PHY
- Supports HS, FS, and LS data rates
- Supports FS pre-amble for FS hubs with a LS device attached (UTMI+ Level 3)
- Supports HS SOF and LS keep alive pulse.
- Supports Host Negotiation Protocol (HNP) and Session Request protocol (SRP)
- Internal comparators support OTG monitoring of VBUS levels
- Low Latency Hi-Speed Receiver (43 Hi-Speed clocks Max)
- Internal 1.8 volt regulators allow operation from a single 3.3 volt supply
- Internal short circuit protection of ID, DP and DM lines to VBUS or ground
- Integrated 24MHz Crystal Oscillator supports either crystal operation or 24MHz external clock input
- Internal PLL for 480MHz Hi-Speed USB operation
- Supports USB 2.0 and legacy USB 1.1 devices
- 55mA Unconfigured Current (typical) - ideal for bus powered applications
- 83uA suspend current (typical) - ideal for battery powered applications
- Full Commercial operating temperature range from 0C to +70C
- 56-Pin, QFN RoHS compliant package (8 x 8 x 0.90 mm height)

Functional Overview

The USB3500 is a highly integrated USB transceiver system. It contains a complete USB 2.0 PHY with the UTMI+ industry standard interface to support fast time to market for a USB controller. The USB3500 is composed of the functional blocks shown in the figure below.

USB3500 Block Diagram



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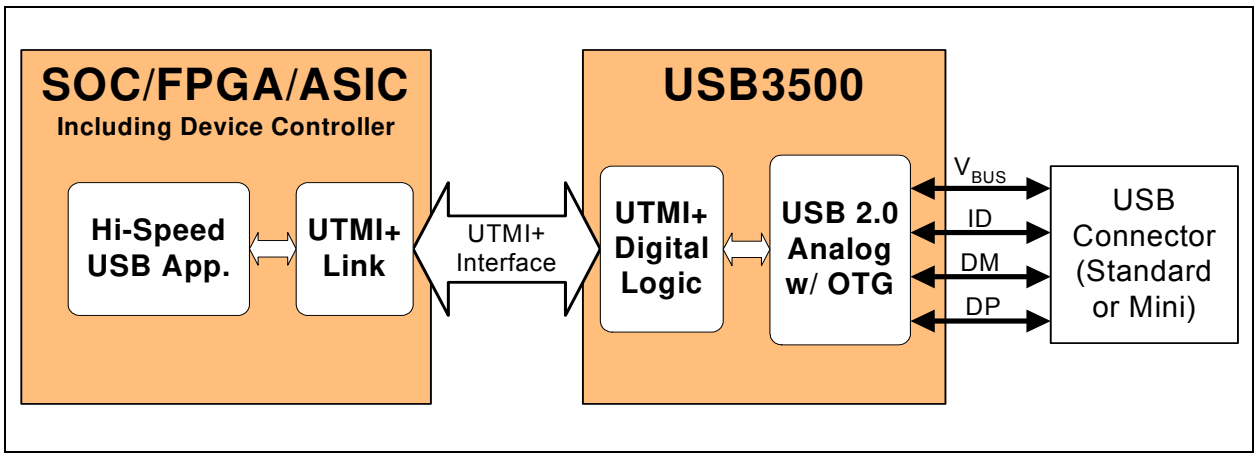
1.0 GENERAL DESCRIPTION

The USB3500 is a stand-alone Hi-Speed USB Physical Layer Transceiver (PHY). The USB3500 uses a UTMI+ interface to connect to an SOC or FPGA or custom ASIC. The USB3500 provides a flexible alternative to integrating the analog PHY block for new designs.

FIGURE 1-1: BASIC UTMI+ USB DEVICE BLOCK DIAGRAM



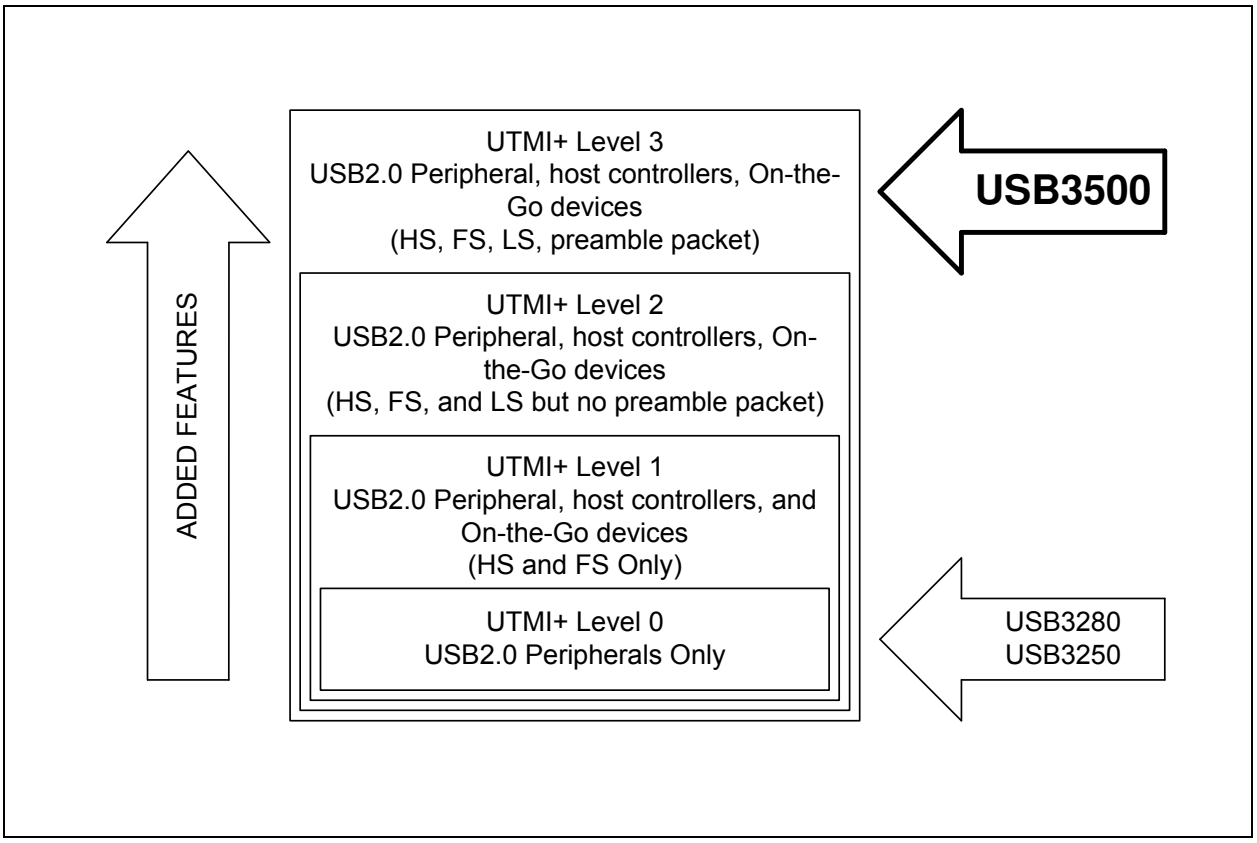
The USB3500 provides a fully compliant USB 2.0 interface, and supports High-Speed (HS), Full-Speed (FS), and Low-Speed (LS) USB. The USB3500 supports all levels of the UTMI+ specification as shown in Figure 1-2.

The USB3500 can also, as an option, fully support the On-the-Go (OTG) protocol defined in the On-The-Go Supplement to the USB 2.0 Specification. On-the-Go allows the Link to dynamically configure the USB3500 as host or peripheral configured dynamically by software. For example, a cell phone may connect to a computer as a peripheral to exchange address information or connect to a printer as a host to print pictures. Finally the OTG enabled device can connect to another OTG enabled device to exchange information. All this is supported using a single low profile Mini-AB USB connector.

Designs not needing OTG can ignore the OTG feature set.

The USB3500 uses Microchip's advanced proprietary technology to minimize power dissipation, resulting in maximized battery life in portable applications.

FIGURE 1-2: UTMI+ LEVEL 3 SUPPORT



1.1 Applications

The USB3500 is targeted for any application where a hi-speed USB connection is desired.

The USB3500 is well suited for:

- Cell Phones
- MP3 Players
- Scanners
- Printers
- External Hard Drives
- Still and Video Cameras
- Portable Media Players
- Entertainment Devices

1.2 Reference Documents

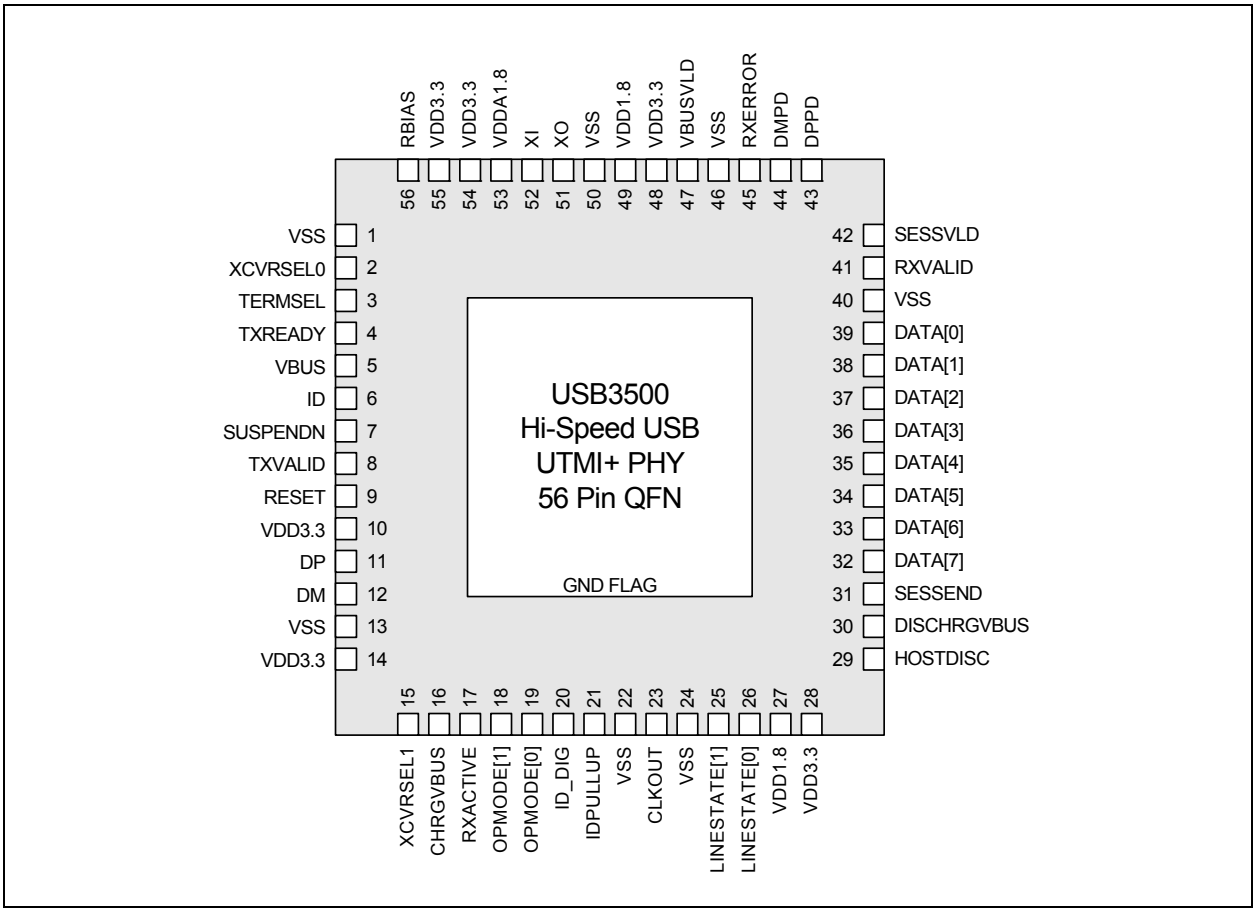
- Universal Serial Bus Specification, Revision 2.0, April 27, 2000
- USB 2.0 Transceiver Macrocell Interface (UTMI) Specification, Version 1.02, May 27, 2000
- On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a, June 24, 2003
- UTMI+ Specification, Revision 1.0, February 2, 2004

2.0 PIN CONFIGURATION AND PIN DEFINITIONS

The USB3500 is offered in a 56-pin QFN package. The pin definitions and locations are documented below.

2.1 USB3500 Pin Locations

FIGURE 2-1: USB3500 PINOUT - TOP VIEW



The flag of the QFN package must be connected to ground with a via array.

2.2 Pin Definitions

TABLE 2-1: USB3500 PIN DEFINITIONS

Pin	Name	Direction, Type	Active Level	Description
1	**VSS**	Ground	N/A	PHY ground.
2	**XCVRSEL[0]**	Input	N/A	Transceiver Select. These signals select between the FS and HS transceivers: Transceiver select. 00: HS 01: FS 10: LS 11: LS data, FS rise/fall times
3	**TERMSEL**	Input	N/A	Termination Select. This signal selects between the FS and HS terminations: 0: HS termination enabled 1: FS termination enabled

TABLE 2-1: USB3500 PIN DEFINITIONS (CONTINUED)

Pin	Name	Direction, Type	Active Level	Description
4	**TXREADY**	Output	High	Transmit Data Ready. If TXVALID is asserted, the Link must always have data available for clocking into the TX Holding Register on the rising edge of CLKOUT. TXREADY is an acknowledgment to the Link that the transceiver has clocked the data from the bus and is ready for the next transfer on the bus. If TXVALID is negated, TXREADY can be ignored by the Link.
5	**VBUS**	I/O, Analog	N/A	VBUS pin of the USB cable.
6	**ID**	Input, Analog	N/A	ID pin of the USB cable.
7	**SUSPENDN**	Input	Low	Suspend. Places the transceiver in a mode that draws minimal power from supplies. In host mode, R_{PU} is removed during suspend. In device mode, R_{PD} is controlled by TERMSEL. In suspend mode the clocks are off. 0: PHY in suspend mode 1: PHY in normal operation
8	**TXVALID**	Input	High	Transmit Valid. Indicates that the DATA bus is valid for transmit. The assertion of TXVALID initiates the transmission of SYNC on the USB bus. The negation of TXVALID initiates EOP on the USB. Control inputs (OPMODE[1:0], TERMSEL,XCVERSEL) must not be changed on the de-assertion or assertion of TXVALID.
9	**RESET**	Input	High	Reset. Reset all state machines. After coming out of reset, must wait 5 rising edges of clock before asserting TXValid for transmit. Assertion of Reset: May be asynchronous to CLKOUT De-assertion of Reset: Must be synchronous to CLKOUT
10	**VDD3.3**	N/A	N/A	3.3V PHY Supply. Provides power for USB 2.0 Transceiver, UTMI+ Digital, Digital I/O, and Regulators.
11	**DP**	I/O, Analog	N/A	D+ pin of the USB cable.
12	**DM**	I/O, Analog	N/A	D- pin of the USB cable.
13	**VSS**	Ground	N/A	PHY ground.
14	**VDD3.3**	N/A	N/A	3.3V PHY Supply.
15	**XCVRSEL[1]**	Input	N/A	Transceiver Select. These signals select between the FS and HS transceivers: Transceiver select. 00: HS 01: FS 10: LS 11: LS data, FS rise/fall times
16	**CHRGVBUS**	Input	High	Charge VBUS through a resistor to VDD3.3. 0: do not charge VBUS 1: charge VBUS
17	**RXACTIVE**	Output	High	Receive Active. Indicates that the receive state machine has detected Start of Packet and is active.
18	**OPMODE[1]**	Input	N/A	Operational Mode. These signals select between the various operational modes: [1] [0] Description 0 0 0: Normal Operation 0 1 1: Non-driving (all terminations removed) 1 0 2: Disable bit stuffing and NRZI encoding 1 1 3: Reserved
19	**OPMODE[0]**	Input	N/A	

TABLE 2-1: USB3500 PIN DEFINITIONS (CONTINUED)

Pin	Name	Direction, Type	Active Level	Description
20	**ID_DIG**	Output	High	ID Digital. Indicates the state of the ID pin. 0: connected plug is a mini-A 1: connected plug is a mini-B
21	**IDPULLUP**	Input	High	ID Pull-up. Enables sampling of the analog ID line. Disabling the ID line sampler will reduce PHY power consumption. 0: Disable sampling of ID line. 1: Enable sampling of ID line.
22	**VSS**	Ground	N/A	PHY ground.
23	**CLKOUT**	Output, CMOS	N/A	60MHz reference clock output. All UTMI+ signals are driven synchronous to this clock.
24	**VSS**	Ground	N/A	PHY ground.
25	**LINESTATE[1]**	Output	N/A	Line State. These signals reflect the current state of the USB data bus in FS mode. Bit [0] reflects the state of DP and bit [1] reflects the state of DM. When the device is suspended or resuming from a suspended state, the signals are combinatorial. Otherwise, the signals are synchronized to CLKOUT. [1] [0] Description 0 0 0: SEO 0 1 1: J State 1 0 2: K State 1 1 3: SE1
26	**LINESTATE[0]**	Output	N/A	
27	**VDD1.8**	N/A	N/A	1.8V regulator output for digital circuitry on chip. Place a 0.1uF capacitor near this pin and connect the capacitor from this pin to ground. Connect pin 27 to pin 49.
28	**VDD3.3**	N/A	N/A	3.3V PHY Supply. Provides power for USB 2.0 Transceiver, UTMI+ Digital, Digital I/O, and Regulators.
29	**HOSTDISC**	Output	High	Host Disconnect. In HS Host mode this indicates to that a downstream device has been disconnected. Automatically reset to 0b when Low Power Mode is entered.
30	**DISCHRGVBUS**	Input	High	Discharge VBUS through a resistor to ground. 0: do not discharge VBUS 1: discharge VBUS
31	**SESSEND**	Output	High	Session End. Indicates that the voltage on Vbus is below its B-Device Session End threshold. 0: VBUS > $V_{SessEnd}$ 1: VBUS < $V_{SessEnd}$

TABLE 2-1: USB3500 PIN DEFINITIONS (CONTINUED)

Pin	Name	Direction, Type	Active Level	Description
32	**DATA[7]**	I/O, CMOS, Pull-low	N/A	8-bit bi-directional data bus. Data[7] is the MSB and Data[0] is the LSB.
33	**DATA[6]**	I/O, CMOS, Pull-low	N/A	
34	**DATA[5]**	I/O, CMOS, Pull-low	N/A	
35	**DATA[4]**	I/O, CMOS, Pull-low	N/A	
36	**DATA[3]**	I/O, CMOS, Pull-low	N/A	
37	**DATA[2]**	I/O, CMOS, Pull-low	N/A	
38	**DATA[1]**	I/O, CMOS, Pull-low	N/A	
39	**DATA[0]**	I/O, CMOS, Pull-low	N/A	
40	**VSS**	Ground	N/A	PHY ground.
41	**RXVALID**	Output	High	Receive Data Valid. Indicates that the DATA bus has received valid data. The Receive Data Holding Register is full and ready to be unloaded. The Link is expected to register the DATA bus on the next rising edge of CLKOUT.
42	**SESSVLD**	Output	High	Session Valid. Indicates that the voltage on Vbus is above the indicated threshold. 0: VBUS < $V_{SessVld}$ 1: VBUS > $V_{SessVld}$
43	**DPPD**	Input	N/A	DP Pull-down Select. This signal enables the 15k Ohm pull-down resistor on the DP line. 0: Pull-down resistor not connected to DP 1: Pull-down resistor connected to DP
44	**DMPD**	Input	N/A	DM Pull-down Select. This signal enables the 15k Ohm pull-down resistor on the DM line. 0: Pull-down resistor not connected to DM 1: Pull-down resistor connected to DM
45	**RXERROR**	Output	High	Receive Error. This output is clocked with the same timing as the receive DATA lines and can occur at anytime during a transfer. 0: Indicates no error. 1: Indicates a receive error has been detected.
46	**VSS**	Ground	N/A	PHY ground.
47	**VBUSVLD**	Output	High	VBUS Valid. Indicates that the voltage on Vbus is above the indicated threshold. 0: VBUS < $V_{VbusVld}$ 1: VBUS > $V_{VbusVld}$
48	**VDD3.3**	N/A	N/A	3.3V PHY Supply. Provides power for USB 2.0 Transceiver, UTMI+ Digital, Digital I/O, and Regulators.

TABLE 2-1: USB3500 PIN DEFINITIONS (CONTINUED)

Pin	Name	Direction, Type	Active Level	Description
49	**VDD1.8**	N/A	N/A	1.8V regulator output for digital circuitry on chip. Place a 4.7uF low ESR capacitor near this pin and connect the capacitor from this pin to ground. Connect pin 49 to pin 27. See Section 5.6, "Internal Regulators and POR," on page 22.
50	**VSS**	Ground	N/A	PHY ground.
51	**XO**	Output, Analog	N/A	Crystal pin. If using an external clock on XI this pin should be floated.
52	**XI**	Input, Analog	N/A	Crystal pin. A 24MHz crystal is supported. The crystal is placed across XI and XO. An external 24MHz clock source may be driven into XI in place of a crystal.
53	**VDDA1.8**	N/A	N/A	1.8V regulator output for analog circuitry on chip. Place a 0.1uF capacitor near this pin and connect the capacitor from this pin to ground. In parallel, place a 4.7uF low ESR capacitor near this pin and connect the capacitor from this pin to ground. See Section 5.6, "Internal Regulators and POR".
54	**VDD3.3**	N/A	N/A	3.3V PHY Supply. Provides power for USB 2.0 Transceiver, UTMI+ Digital, Digital I/O, and Regulators.
55	**VDD3.3**	N/A	N/A	3.3V PHY Supply. Should be connected directly to pin 54.
56	**RBIAS**	Analog, CMOS	N/A	External 1% bias resistor. Requires a 12KΩ resistor to ground.
	GND FLAG	Ground	N/A	Ground. The flag must be connected to the ground plane.

3.0 LIMITING VALUES

TABLE 3-1: MAXIMUM RATINGS

Parameter	Symbol	Condition	MIN	TYP	MAX	Units
Maximum VBUS, ID, DP, and DM voltage to Ground	V_{MAX_5V}		-0.5		+5.5	V
Maximum VDD1.8 and VDDA1.8 voltage to Ground	$V_{MAX\_1.8V}$		-0.5		2.5	V
Maximum 3.3V supply voltage to Ground	$V_{MAX\_3.3V}$		-0.5		4.0	V
Maximum I/O voltage to Ground	V_{MAX_IN}		-0.5		4.0	V
Operating Temperature	T_{MAX_OP}		0		70	C
Storage Temperature	T_{MAX_STG}		-55		150	C

Note: Stresses above those listed could cause damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

TABLE 3-2: RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	MIN	TYP	MAX	Units
3.3V Supply Voltage	$V_{DD3.3}$		3.0	3.3	3.6	V
Input Voltage on Digital Pins	V_I		0.0		$V_{DD3.3}$	V
Input Voltage on Analog I/O Pins (DP, DM)	$V_{I(I/O)}$		0.0		$V_{DD3.3}$	V
Ambient Temperature	T_A		0		+70	^oC

TABLE 3-3: RECOMMENDED EXTERNAL CLOCK CONDITIONS

Parameter	Symbol	Condition	MIN	TYP	MAX	Units
System Clock Frequency		XI driven by the external clock; and no connection at XO		24 (±100ppm)		MHz
System Clock Duty Cycle		XI driven by the external clock; and no connection at XO	45	50	55	%

4.0 ELECTRICAL CHARACTERISTICS

TABLE 4-1: DC ELECTRICAL CHARACTERISTICS: SUPPLY PINS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
Unconfigured Current	$I_{AVG(UCFG)}$	Device Unconfigured		55		mA
FS Idle Current	$I_{AVG(FS)}$	FS idle not data transfer		55		mA
FS Transmit Current	$I_{AVG(FSTX)}$	FS current during data transmit		60.5		mA
FS Receive Current	$I_{AVG(FSRX)}$	FS current during data receive		57.5		mA
HS Idle Current	$I_{AVG(HS)}$	FS idle not data transfer		60.6		mA
HS Transmit Current	$I_{AVG(HSTX)}$	FS current during data transmit		62.4		mA
HS Receive Current	$I_{AVG(HSRX)}$	FS current during data receive		61.5		mA
Low Power Mode	$I_{DD(LPM)}$	VBUS 15kΩ pull-down and 1.5kΩ pull-up resistor currents not included.		83		uA

Note: $V_{DD3.3}$ = 3.0 to 3.6V; V_{SS} = 0V; T_A = 0C to +70C; unless otherwise specified.

TABLE 4-2: ELECTRICAL CHARACTERISTICS: CLKOUT START-UP

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
Suspend Recovery Time	T_{START}			2.25	3.5	ms

Note: $V_{DD3.3}$ = 3.0 to 3.6V; V_{SS} = 0V; T_A = 0C to +70C; unless otherwise specified.

TABLE 4-3: DC ELECTRICAL CHARACTERISTICS: LOGIC PINS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
Low-Level Input Voltage	V_{IL}		V_{SS}		0.8	V
High-Level Input Voltage	V_{IH}		2.0		$V_{DD3.3}$	V
Low-Level Output Voltage	V_{OL}	I_{OL} = 8mA			0.4	V
High-Level Output Voltage	V_{OH}	I_{OH} = -8mA	$V_{DD3.3}$ - 0.4			V
Input Leakage Current	I_{LI}				±10	uA
Pin Capacitance	Cpin				4	pF

Note: $V_{DD3.3}$ = 3.0 to 3.6V; V_{SS} = 0V; T_A = 0C to +70C; unless otherwise specified.

TABLE 4-4: DC ELECTRICAL CHARACTERISTICS: ANALOG I/O PINS (DP/DM)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
FS FUNCTIONALITY						
Input levels						
Differential Receiver Input Sensitivity	V_{DIFS}	| V(DP) - V(DM) |	0.2			V
Differential Receiver Common-Mode Voltage	V_{CMFS}		0.8		2.5	V

TABLE 4-4: DC ELECTRICAL CHARACTERISTICS: ANALOG I/O PINS (DP/DM) (CONTINUED)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
Single-Ended Receiver Low Level Input Voltage	V_{ILSE}				0.8	V
Single-Ended Receiver High Level Input Voltage	V_{IHSE}		2.0			V
Single-Ended Receiver Hysteresis	V_{HYSSE}		0.050		0.150	V
Output Levels						
Low Level Output Voltage	V_{FSOL}	Pull-up resistor on DP; R_L = 1.5kΩ to $V_{DD3.3}$			0.3	V
High Level Output Voltage	V_{FSOH}	Pull-down resistor on DP, DM; R_L = 15kΩ to GND	2.8		3.6	V
Termination						
Driver Output Impedance for HS and FS	Z_{HSDRV}	Steady state drive	40.5	45	49.5	Ω
Input Impedance	Z_{INP}	TX, RPU disabled	1.0			MΩ
Pull-up Resistor Impedance	Z_{PU}	Bus Idle	0.900	1.24	1.575	kΩ
Pull-up Resistor Impedance	Z_{PURX}	Device Receiving	1.425	2.26	3.09	kΩ
Pull-dn Resistor Impedance	Z_{PD}		14.25	15.0	15.75	kΩ
HS FUNCTIONALITY						
Input levels						
HS Differential Input Sensitivity	V_{DIHS}	| V(DP) - V(DM) |	100			mV
HS Data Signaling Common Mode Voltage Range	V_{CMHS}		-50		500	mV
HS Squelch Detection Threshold (Differential)	V_{HSSQ}	Squelch Threshold			100	mV
		Un-squelch Threshold	150			mV
Output Levels						
Hi-Speed Low Level Output Voltage (DP/DM referenced to GND)	V_{HSOL}	45Ω load	-10		10	mV
Hi-Speed High Level Output Voltage (DP/DM referenced to GND)	V_{HSOH}	45Ω load	360		440	mV
Hi-Speed IDLE Level Output Voltage (DP/DM referenced to GND)	V_{OLHS}	45Ω load	-10		10	mV
Chirp-J Output Voltage (Differential)	V_{CHIRPJ}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	700		1100	mV
Chirp-K Output Voltage (Differential)	V_{CHIRPK}	HS termination resistor disabled, pull-up resistor connected. 45Ω load.	-900		-500	mV
Leakage Current						
OFF-State Leakage Current	I_{LZ}				±10	uA
Port Capacitance						
Transceiver Input Capacitance	C_{IN}	Pin to GND		5	10	pF

Note: $V_{DD3.3}$ = 3.0 to 3.6V; V_{SS} = 0V; T_A = 0C to +70C; unless otherwise specified.

TABLE 4-5: DYNAMIC CHARACTERISTICS: ANALOG I/O PINS (DP/DM)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
FS Output Driver Timing						
Rise Time	T_{FSR}	C_L = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
Fall Time	T_{FFF}	C_L = 50pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
Output Signal Crossover Voltage	V_{CRS}	Excluding the first transition from IDLE state	1.3		2.0	V
Differential Rise/Fall Time Matching	FRFM	Excluding the first transition from IDLE state	90		111.1	%
HS Output Driver Timing						
Differential Rise Time	T_{HSR}		500			ps
Differential Fall Time	T_{HSF}		500			ps
Driver Waveform Requirements		Eye pattern of Template 1 in USB 2.0 specification				
Hi-Speed Mode Timing						
Receiver Waveform Requirements		Eye pattern of Template 4 in USB 2.0 specification				
Data Source Jitter and Receiver Jitter Tolerance		Eye pattern of Template 4 in USB 2.0 specification				

Note: $V_{DD3.3}$ = 3.0 to 3.6V; V_{SS} = 0V; T_A = 0C to +70C; unless otherwise specified.

TABLE 4-6: DYNAMIC CHARACTERISTICS: DIGITAL UTMI PINS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
UTMI Timing						
DATA[7:0]	T_{PD}	Output Delay. Measured from PHY output to the rising edge of CLKOUT	2		5	ns
RXVALID						
RXACTIVE						
RXERROR						
LINESTATE[1:0]						
TXREADY						
DATA[7:0]	T_{SU}	Setup Time. Measured from PHY input to the rising edge of CLKOUT.	5		1	ns
TXVALID						
OPMODE[1:0]						
XCVRSELECT[1:0]						
TERMSELECT						
DATA[7:0]	T_H	Hold time. Measured from the rising edge of CLKOUT to the PHY input signal edge.	0			ns
TXVALID						
OPMODE[1:0]						
XCVRSELECT[1:0]						
TERMSELECT						

Note: $V_{DD3.3}$ = 3.0 to 3.6V; V_{SS} = 0V; T_A = 0C to +70C; unless otherwise specified.

TABLE 4-7: OTG ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
SessEnd trip point	$V_{SessEnd}$		0.2	0.5	0.8	V
SessVld trip point	$V_{SessVld}$		0.8	1.4	2.0	V
VBUSVld trip point	$V_{VbusVld}$		4.4	4.58	4.75	V
Vbus Pull-Up	R_{VbusPu}	Vbus to VDD3.3 (CHRGVBUS = 1)	281	340		Ω
Vbus Pull-down	R_{VbusPd}	Vbus to GND (DISCHRGVBUS = 1)	656	850		Ω
Vbus Impedance	R_{Vbus}	Vbus to GND	40	75	100	kΩ
ID pull-up resistance	$R_{IdPullUp}$	(IDOULLUP = 1)	80	100	120	kΩ
ID pull-up resistance	R_{Id}	(IDPULLUP = 0)	1			MΩ

Note: $V_{DD3.3}$ = 3.0 to 3.6V; V_{SS} = 0V; T_A = 0C to +70C; unless otherwise specified.

TABLE 4-8: REGULATOR OUTPUT VOLTAGES

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
$V_{DDA1.8}$	$V_{DDA1.8}$	Normal Operation (SUSPENDN = 1)	1.6	1.8	2.0	V
$V_{DDA1.8}$	$V_{DDA1.8}$	Low Power mode (SUSPENDN = 0)		0		V
$V_{DD1.8}$	$V_{DD1.8}$		1.6	1.8	2.0	V

Note: $V_{DD3.3}$ = 3.0 to 3.6V; V_{SS} = 0V; T_A = 0C to +70C; unless otherwise specified.

5.0 DETAILED FUNCTIONAL DESCRIPTION

FIGURE 2-1: on page 5 shows the functional block diagram of the USB3500. Each of the functions is described in detail below.

5.1 8bit Bi-Directional Data Bus Operation

The USB3500 supports an 8-bit bi-directional parallel interface.

- CLKOUT runs at 60MHz
- The 8-bit data bus (DATA[7:0]) is used for transmit when TXVALID = 1
- The 8-bit data bus (DATA[7:0]) is used for receive when TXVALID = 0

Figure 5-1 shows the relationship between CLKOUT and the transmit data transfer signals in FS mode. TXREADY is only asserted for one CLKOUT per byte time to signal the Link that the data on the DATA lines has been read by the PHY. The Link may hold the data on the DATA lines for the duration of the byte time. Transitions of TXVALID must meet the defined setup and hold times relative to CLKOUT.

FIGURE 5-1: FS CLK RELATIONSHIP TO TRANSMIT DATA AND CONTROL SIGNALS

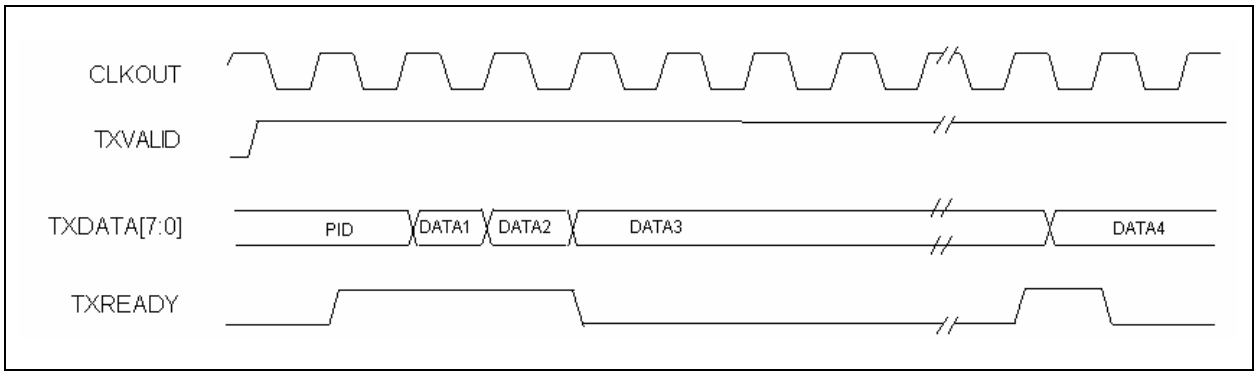
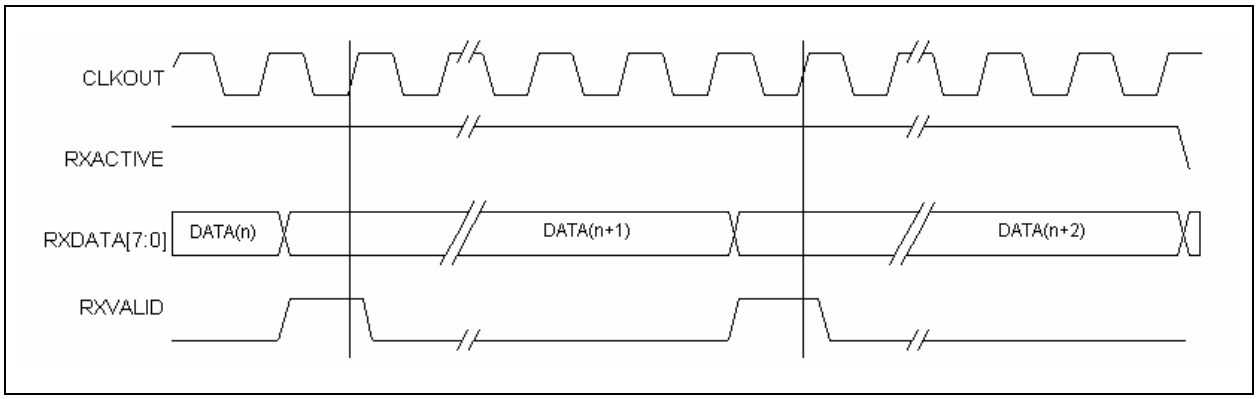


Figure 5-2 shows the relationship between CLKOUT and the receive data control signals in FS mode. RXACTIVE “frames” a packet, transitioning only at the beginning and end of a packet. However transitions of RXVALID may take place any time 8 bits of data are available. Figure 5-2 also shows how RXVALID is only asserted for one CLKOUT cycle per byte time even though the data may be presented for the full byte time. The XCVRSELECT signal determines whether the HS or FS timing relationship is applied to the data and control signals.

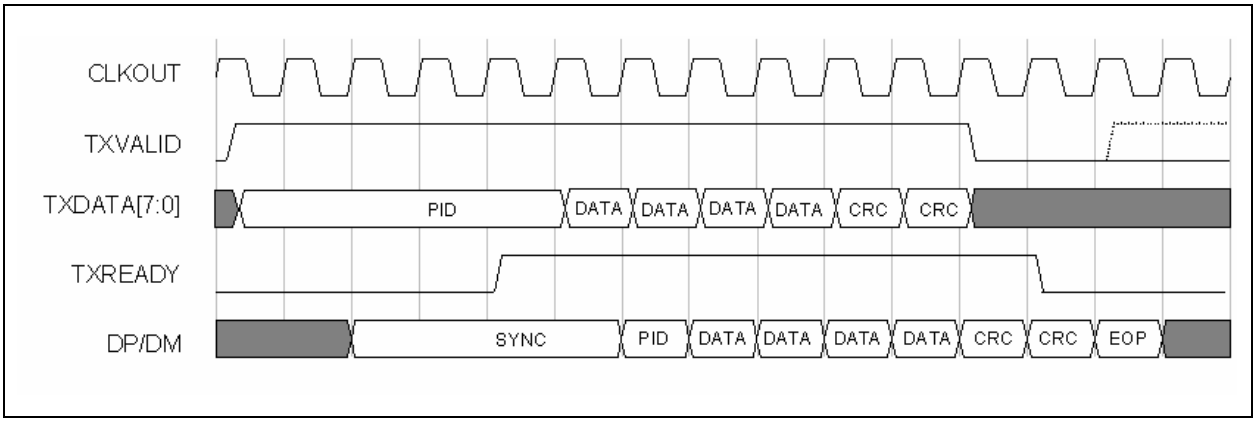
FIGURE 5-2: FS CLK RELATIONSHIP TO RECEIVE DATA AND CONTROL SIGNALS



5.2 TX Logic

This block receives parallel data bytes placed on the DATA bus and performs the necessary transmit operations. These operations include parallel to serial conversion, bit stuffing and NRZI encoding. Upon valid assertion of the proper TX control lines by the Link and TX State Machine, the TX LOGIC block will synchronously shift, at either the FS or HS rate, the data to the FS/HS TX block to be transmitted on the USB cable. Data transmit timing is shown in Figure 5-3.

FIGURE 5-3: TRANSMIT TIMING FOR A DATA PACKET



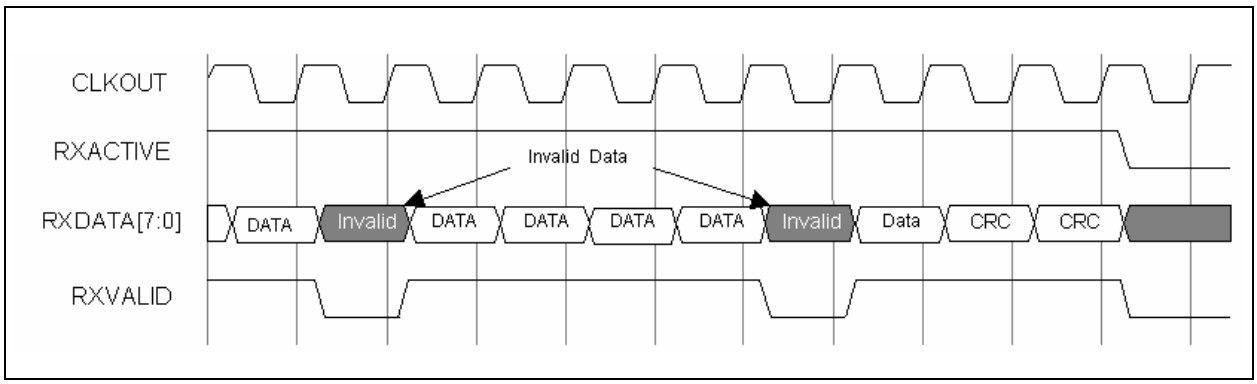
The behavior of the Transmit State Machine is described below.

- The Link asserts TXVALID to begin a transmission.
- After the Link asserts TXVALID it can assume that the transmission has started when it detects TXREADY has been asserted.
- The Link must assume that the USB3500 has consumed a data byte if TXREADY and TXVALID are asserted on the rising edge of CLKOUT.
- The Link must have valid packet information (PID) asserted on the DATA bus coincident with the assertion of TXVALID.
- TXREADY is sampled by the Link on the rising edge of CLKOUT.
- The Link negates TXVALID to complete a packet. Once negated, the transmit logic will never reassert TXREADY until after the EOP has been generated. (TXREADY will not re-assert until TXVALD asserts again.)
- The USB3500 is ready to transmit another packet immediately. However, the Link must conform to the minimum inter-packet delays identified in the USB 2.0 specification.
- Supports high speed disconnect detect through the HOSTDISC pin. In Host mode the USB3500 will sample the disconnect comparator at the 32nd bit of the 40 bit long EOP during SOF packets.
- Supports FS pre-amble for FS hubs with a LS device.
- Supports LS keep alive by receiving the SOF PID.
- Supports Host mode resume K which ends with two low speed times of SE0 followed by 1 FS “J”.

5.3 RX Logic

This block receives serial data from the clock recovery circuits and processes it to be transferred to the Link on the DATA bus. The processing involved includes NRZI decoding, bit unstuffing, and serial to parallel conversion. Upon valid assertion of the proper RX control lines, the RX Logic block will provide bytes to the DATA bus as shown in the figures below. The behavior of the receiver is described below.

FIGURE 5-4: RECEIVE TIMING FOR DATA WITH UNSTUFFED BITS



The assertion of RESET will cause the USB3500 to deasserts RXACTIVE and RXVALID. When the RESET signal is deasserted the Receive State Machine starts looking for a SYNC pattern on the USB. When a SYNC pattern is detected, the receiver will assert RXACTIVE. The length of the received Hi-Speed SYNC pattern varies and can be up to 32 bits long or as short as 12 bits long when at the end of five hubs.

After valid serial data is received, the data is loaded into the RX Holding Register on the rising edge of CLKOUT, and RXVALID is asserted. The Link must read the DATA bus on the next rising edge of CLKOUT. In normal mode (OPMODE = 00), then stuffed bits are stripped from the data stream. Each time 8 stuffed bits are accumulated the USB3500 will negate RXVALID for one clock cycle, thus skipping a byte time.

When the EOP is detected the USB3500 will negate RXACTIVE and RXVALID. After the EOP has been stripped, the USB3500 will begin looking for the next packet.

The behavior of the USB3500 receiver is described below:

- RXACTIVE and RXREADY are sampled on the rising edge of CLKOUT.
- After a EOP is complete the receiver will begin looking for SYNC.
- The USB3500 asserts RXACTIVE when SYNC is detected.
- The USB3500 negates RXACTIVE when an EOP is detected and the elasticity buffer is empty.
- When RXACTIVE is asserted, RXVALID will be asserted if the RX Holding Register is full.
- RXVALID will be negated if the RX Holding Register was not loaded during the previous byte time. This will occur if 8 stuffed bits have been accumulated.
- The Link must be ready to consume a data byte if RXACTIVE and RXVALID are asserted (RX Data state).
- Figure 5-5 shows the timing relationship between the received data (DP/DM), RXVALID, RXACTIVE, RXERROR and DATA signals.

Note:

- Figure 5-5, Figure 5-6 and Figure 5-7 are timing examples of a HS/FS PHY when it is in HS mode. When a HS/FS PHY is in FS Mode there are approximately 40 CLKOUT cycles every byte time. The Receive State Machine assumes that the Link captures the data on the DATA bus if RXACTIVE and RXVALID are asserted. In FS mode, RXVALID will only be asserted for one CLKOUT per byte time.
- In Figure 5-5, Figure 5-6 and Figure 5-7 the SYNC pattern on DP/DM is shown as one byte long. The SYNC pattern received by a device can vary in length. These figures assume that all but the last 12 bits have been consumed by the hubs between the device and the host controller.

FIGURE 5-5: RECEIVE TIMING FOR A HANDSHAKE PACKET (NO CRC)

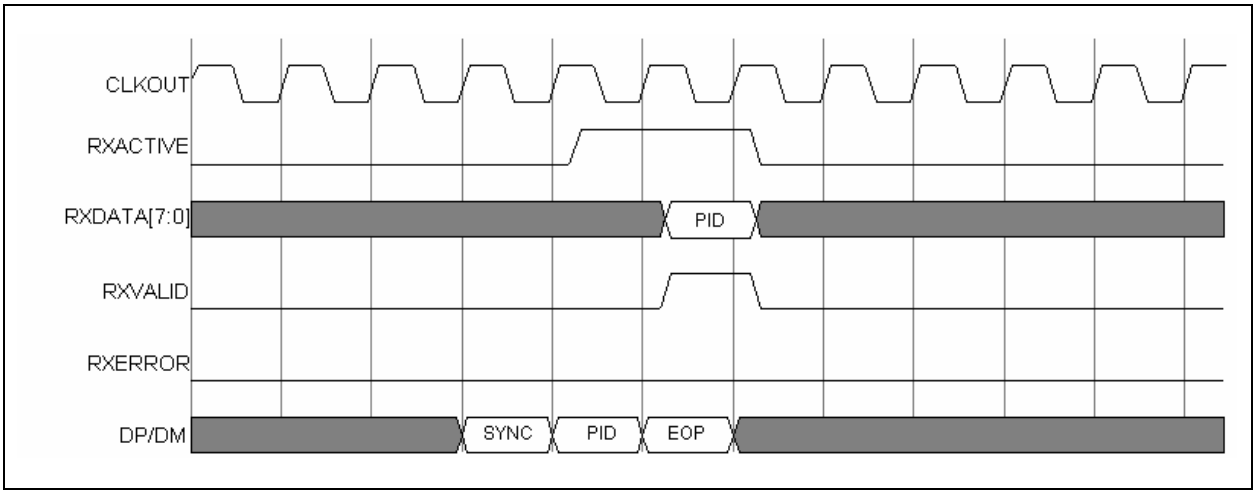


FIGURE 5-6: RECEIVE TIMING FOR SETUP PACKET

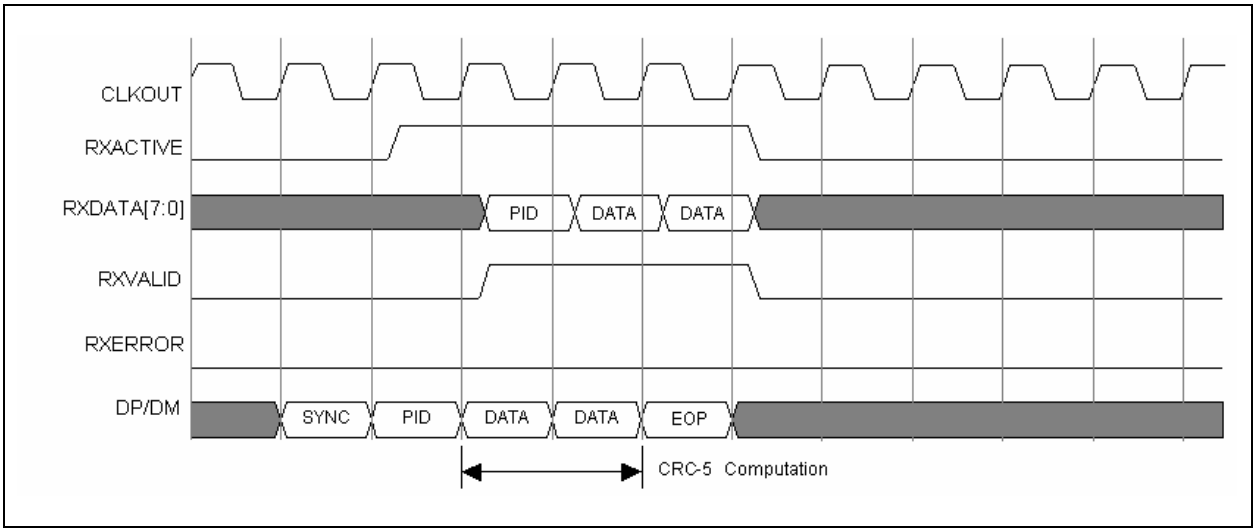
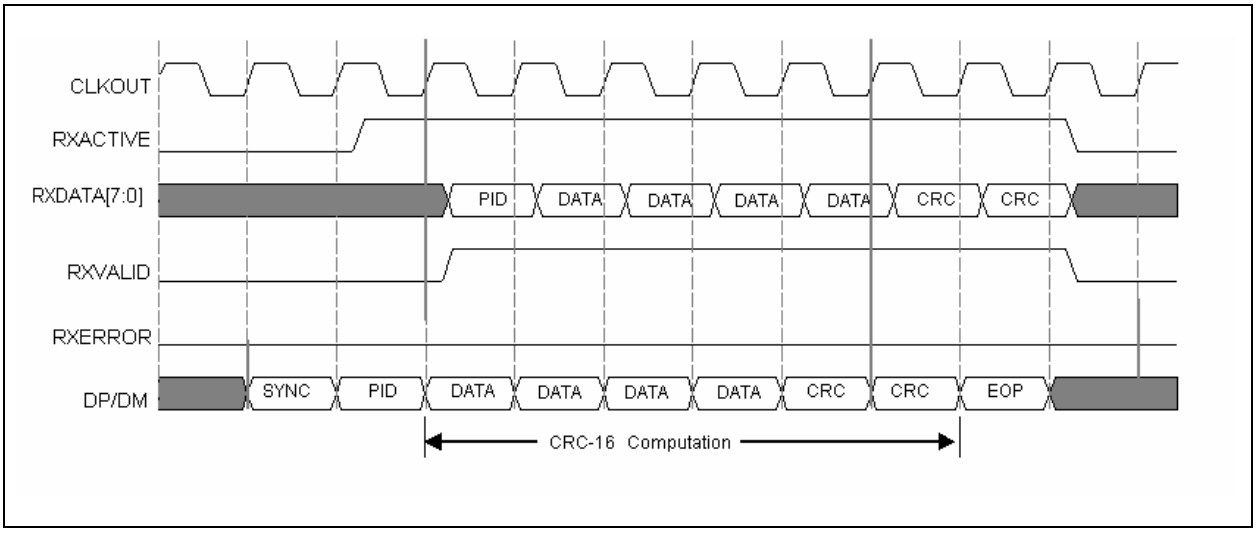


FIGURE 5-7: RECEIVE TIMING FOR DATA PACKET (WITH CRC-16)



5.4 USB 2.0 Transceiver

The Microchip Hi-Speed USB 2.0 Transceiver consists of four blocks in the lower left corner of FIGURE 2-1: on page 5. These four blocks are labeled HS XCVR, FS/LS XCVR, Resistors, and Bias Gen.

5.4.1 HIGH SPEED AND FULL SPEED TRANSCEIVERS

The USB3500 transceiver meets all requirements in the USB 2.0 specification.

The receivers connect directly to the USB cable. This block contains a separate differential receiver for HS and FS mode. Depending on the mode, the selected receiver provides the serial data stream through the multiplexer to the RX Logic block. The FS mode section of the FS/HS RX block also consists of a single-ended receiver on each of the data lines to determine the correct FS linestate. For HS mode support, the FS/HS RX block contains a squelch circuit to insure that noise is never interpreted as data.

The transmitters connect directly to the USB cable. The block contains a separate differential FS and HS transmitter which receive encoded, bit stuffed, serialized data from the TX Logic block and transmit it on the USB cable.

5.4.2 TERMINATION RESISTORS

The USB3500 transceiver fully integrates all of the USB termination resistors. The USB3500 includes two 1.5kΩ pull-up resistors on DP and DM and a 15kΩ pull-down resistor on both DP and DM. In addition the 45Ω high speed termination resistors are also integrated. These integrated resistors require no tuning or trimming by the Link. The state of the resistors is determined by the operating mode of the PHY. The possible valid resistor combinations are shown in Table 5-1. The RESISTOR SETTINGS signals shown in the table are internal to the USB3500.

- RPU_DP_EN activates the 1.5kΩ DP pull-up resistor
- RPU_DM_EN activates the 1.5kΩ DM pull-up resistor
- RPD_DP_EN activates the 15kΩ DP pull-down resistor
- RPD_DM_EN activates the 15kΩ DM pull-down resistor
- HSTERM_EN activates the 45Ω DP and DM high speed termination resistors

TABLE 5-1: DP/DM TERMINATION VS. SIGNALING MODE

Signaling Mode	UTMI+ Interface Settings					Resistor Settings				
	XCVRSEL[1:0]	TERMSEL	OPMODE[1:0]	DPPD	DMPD	RPU_DP_EN	RPU_DM_EN	RPD_DP_EN	RPD_DM_EN	HSTERM_EN
General Settings										
Tri-State Drivers	XXb	Xb	01b	Xb	Xb	0b	0b	0b	0b	0b
Power-up or Vbus < $V_{SESSEND}$	01b	0b	00b	1b	1b	0b	0b	1b	1b	0b
Host Settings										
Host Chirp	00b	0b	10b	1b	1b	0b	0b	1b	1b	1b
Host Hi-Speed	00b	0b	00b	1b	1b	0b	0b	1b	1b	1b
Host Full Speed	X1b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host HS/FS Suspend	01b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host HS/FS Resume	01b	1b	10b	1b	1b	0b	0b	1b	1b	0b
Host low Speed	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host LS Suspend	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host LS Resume	10b	1b	10b	1b	1b	0b	0b	1b	1b	0b
Host Test J/Test_K	00b	0b	10b	1b	1b	0b	0b	1b	1b	1b
Peripheral Settings										
Peripheral Chirp	00b	1b	10b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS	00b	0b	00b	0b	0b	0b	0b	0b	0b	1b
Peripheral FS	01b	1b	00b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Suspend	01b	1b	00b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Resume	01b	1b	10b	0b	0b	1b	0b	0b	0b	0b
Peripheral LS	10b	1b	00b	0b	0b	0b	1b	0b	0b	0b
Peripheral LS Suspend	10b	1b	00b	0b	0b	0b	1b	0b	0b	0b
Peripheral LS Resume	10b	1b	10b	0b	0b	0b	1b	0b	0b	0b
Peripheral Test J/Test K	00b	0b	10b	0b	0b	0b	0b	0b	0b	1b
OTG device, Peripheral Chirp	00b	1b	10b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS	00b	0b	00b	0b	1b	0b	0b	0b	1b	1b
OTG device, Peripheral FS	01b	1b	00b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS/FS Suspend	01b	1b	00b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS/FS Resume	01b	1b	10b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral Test J/Test K	00b	0b	10b	0b	1b	0b	0b	0b	1b	1b

5.4.3 BIAS GENERATOR

This block consists of an internal bandgap reference circuit used for generating the high speed driver currents and the biasing of the analog circuits. This block requires an external 12KΩ, 1% tolerance, external reference resistor connected from RBIAS to ground.

5.5 Crystal Oscillator and PLL

The USB3500 uses an internal crystal driver and PLL sub-system to provide a clean 480MHz reference clock that is used by the PHY during both transmit and receive. The USB3500 requires a clean 24MHz crystal or clock as a frequency reference. If the 24MHz reference is noisy or off frequency the PHY may not operate correctly.

The USB3500 can use either a crystal or an external clock oscillator for the 24MHz reference. The crystal is connected to the XI and XO pins as shown in the application diagram, Figure 6-10. If a clock oscillator is used, the clock should be connected to the XI input and the XO pin left floating. When using an external clock, the clock source must be clean so it does not degrade performance, and should be driven with a 0 to 3.3 volt signal.

After the 480MHz PLL has locked to the correct frequency, it will drive the CLKOUT pin with a 60MHz clock. The USB3500 is ensured to start the clock within the time specified in Table 4-2.

5.6 Internal Regulators and POR

The USB3500 includes integrated power management functions to reduce the bill of materials and simplify product design.

5.6.1 INTERNAL REGULATORS

The USB3500 has two internal regulators that create two 1.8V outputs (labeled VDD1.8 and VDDA1.8) from the 3.3 volt power supply input (VDD3.3). Each regulator requires an external 4.7uF +/-20% low ESR bypass capacitor to ensure stability. X5R or X7R ceramic capacitors are recommended since they exhibit an ESR lower that 0.1ohm at frequencies greater than 10kHz.

The specific capacitor recommendations for each pin are detailed in Table 2.1, "USB3500 Pin Locations", and shown in Figure 6-10, "USB3500 Application Diagram (Top View)".

Note:	The USB3500 regulators are designed to generate a 1.8volt supply for the USB3500 only. Using the regulators to provide current for other circuits is not recommended and Microchip does not ensure USB performance or regulator stability in this case.

5.6.2 POWER ON RESET (POR)

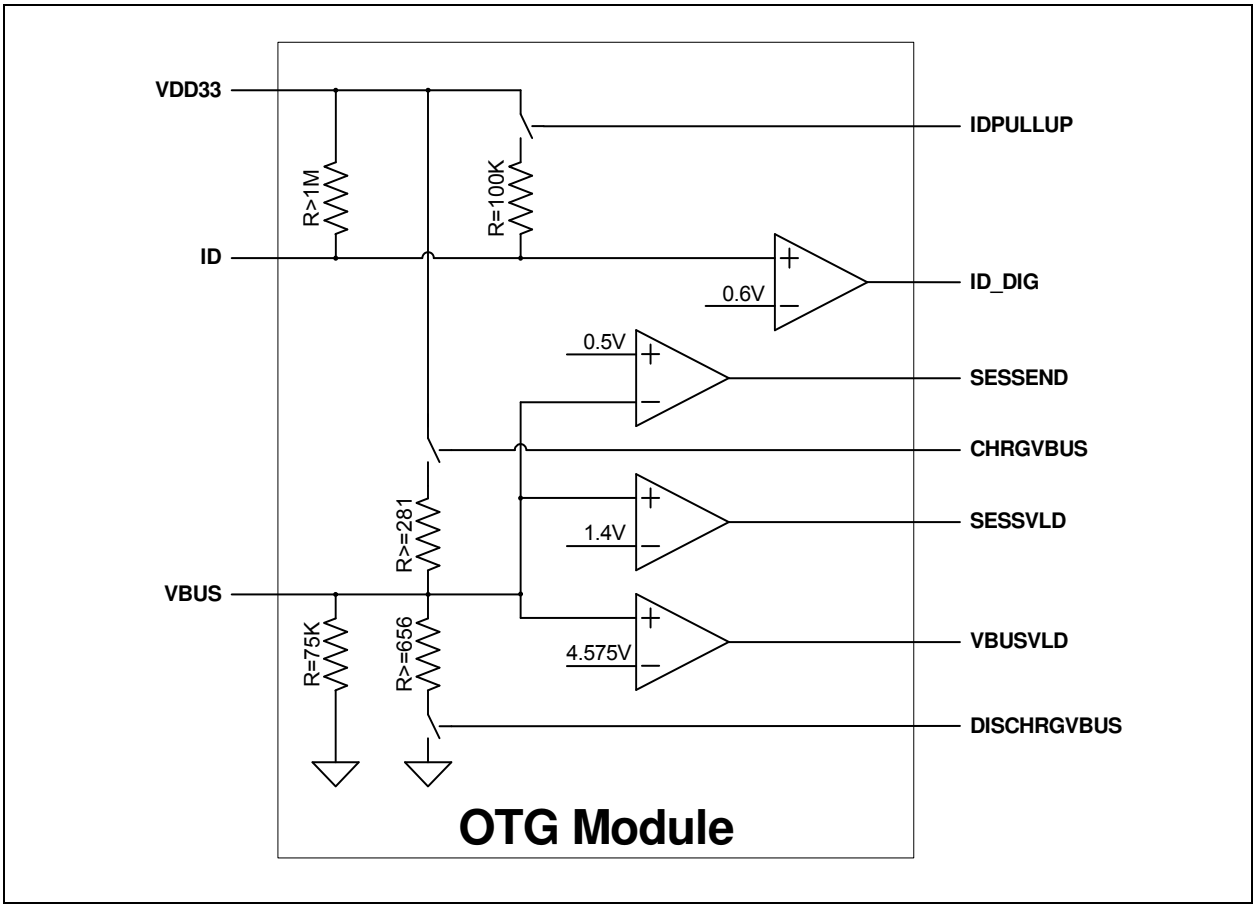
The USB3500 provides an internal POR circuit that generates a reset pulse once the PHY supplies are stable. The UTMI+ Digital can be reset at any time with the RESET pin.

5.7 USB On-The-Go (OTG) Module

The USB3500 provides support for USB OTG. This mode allows the USB3500 to be dynamically configured as a host or a device depending on the type of cable inserted into the Mini-AB connector. When the Mini-A plug of a cable is inserted into the Mini-AB connector the USB device becomes the A-device. When a Mini-B plug is inserted the device becomes the B-device. The OTG A-device behaves similar to a Host while the B-device behaves similar to a peripheral. The differences are covered in the OTG supplement.

The OTG Module meets all the requirements in the “On-The-Go Supplement to the USB 2.0 Specification”. In applications where only Host or Device is required, the OTG Module is unused.

FIGURE 5-8: USB3500 ON-THE-GO MODULE



The OTG Module can be broken into 4 main blocks; ID Detection, VBUS Control, Driving External VBUS, and External VBUS Detection. Each of these blocks is covered in the sections below.

5.7.1 ID DETECTION

The USB3500 provides an ID pin to determine the type of USB cable connected. When the Mini-A Plug of a USB cable is inserted into the Mini-AB connector, the ID pin is shorted to ground. When the Mini-B Plug is inserted into the Mini-AB connector, the ID pin is allowed to float.

TABLE 5-2: IDGND VS. USB CABLE TYPE

USB Plug	OTG Role	ID Voltage	IDGND
A	HOST	0	0
B	PERIPHERAL	3.3	1

The USB3500 provides an integrated pull-up resistor to pull the ID pin to VDD3.3 when a Mini-B plug is inserted and the cable is floating. When a Mini-A plug is connected, the pull-up resistor will be overpowered and the ID pin will be brought to ground. To save current when a Mini-A Plug is inserted, the ID pull-up resistor can be disabled by clearing the IDPULLUP pin. To prevent the ID pin from floating to a random value, a weak pull-up resistor is provided at all times. The circuits related to the ID comparator are shown in Figure 5-8 and their related parameters are shown in Table 4-7.

5.7.2 VBUS CONTROL

The USB3500 includes all of the Vbus comparators required for OTG. The VbusVld, SessVld, and SessEnd comparators are fully integrated into the USB3500. These comparators are used to ensure the Vbus voltage is the correct value for proper USB operation.

The VbusVld comparator is used by the Link, when configured as an A device, to ensure that the Vbus voltage on the cable is valid. The SessVld comparator is used by the Link when configured as either an A or B device to indicate a session is requested or valid. Finally the SessEnd comparator is used by the B-device to indicate a USB session has ended.

Also included in the VBUS Control block are the resistors used for VBUS pulsing in SRP. The resistors used for VBUS pulsing include a pull-down to ground and a pull-up to VDD3.3.

5.7.2.1 SessEnd Comparator

The SessEnd comparator is designed to trip when Vbus is less than 0.5 volts. When Vbus goes below 0.5 volts, the session is considered to be ended and SessEnd will transition from 0 to 1. The SessEnd comparator is disabled when the Suspendn = 0. When disabled, the SessEnd output is 0. The SessEnd comparator trip points are detailed in Table 4-7.

5.7.2.2 SessVld Comparator

The SessVld comparator is used when the PHY is configured as either an A or B device. When configured as an A device, the SessVld is used to detect Session Request protocol (SRP). When configured as a B device, SessVld is used to detect the presence of Vbus. The SessVld comparator is not disabled with Suspendn and its output will always reflect the state of VBUS. The SessVld comparator trip point is detailed in Table 4-7.

Note:	The OTG Supplement specifies a voltage range for A-Device Session Valid and B-Device Session Valid comparator. The USB3500 PHY combines the two comparators into one and uses the narrower threshold range.

5.7.2.3 VbusVld Comparator

The final Vbus comparator is the VbusVld comparator. This comparator is only used when configured as an A-device. In the OTG protocol the A-device is responsible to ensure that the VBUS voltage is within a certain range. The VbusVld comparator is disabled when Suspendn = 0. When disabled the VbusVld will read 0. The VbusVld comparator trip points are detailed in Table 4-7.

When the A-device is able to provide 8-100mA, it must ensure Vbus doesn't go below 4.4 volts. If the A-device can provide 100-500mA on VBUS, it must ensure that Vbus does not go below 4.75 volts.

The internal Vbus comparator is designed to ensure that Vbus remains above 4.4 volts. If the design is required to supply over 100mA an external Vbus comparator or overcurrent fault detection should be used.

5.7.2.4 Vbus Pull-up and Pull-down Resistors

In addition to the internal Vbus comparators, the USB3500 also includes the integrated VBUS pull-up and pull-down resistors used for VBUS Pulsing. To discharge the VBUS voltage, so that a Session Request can begin, the USB3500 provides a pull-down resistor from VBUS to Ground. This resistor is controlled by the DISCHRGVBUS pin. The pull-up resistor is connected between VBUS and VDD3.3. This resistor is used to pull Vbus above 2.1 volts to indicate to the A-Device that a USB session has been requested. The state of the pull-up resistor is controlled by the CHRGVBUS pin. The Pull-Up and Pull-Down resistor values are detailed in Table 4-7.

5.7.2.5 Vbus Input Impedance

The OTG Supplement requires an A-Device that supports Session request protocol to have an input impedance less than 100kohm and greater the 40kohm to ground. In addition, if configured as a B-Device, the PHY cannot draw more then 150uA from Vbus. The USB3500 provides a 75kΩ nominal resistance to ground which meets the above requirements.

6.0 APPLICATION NOTES

The following sections consist of select functional explanations to aid in implementing the USB3500 into a system. For complete description and specifications consult the *USB 2.0 Transceiver Macrocell Interface Specification* and *Universal Serial Bus Specification Revision 2.0.*

6.1 Linestate

The voltage thresholds that the LINESTATE[1:0] signals use to reflect the state of DP and DM depend on the state of XCVRSELECT. LINESTATE[1:0] uses HS thresholds when the HS transceiver is enabled (XCVRSELECT = 0) and FS thresholds when the FS transceiver is enabled (XCVRSELECT = 1). There is not a concept of variable single-ended thresholds in the USB 2.0 specification for HS mode.

The HS receiver is used to detect Chirp J or K, where the output of the HS receiver is always qualified with the Squelch signal. If squelched, the output of the HS receiver is ignored. In the USB3500, as an alternative to using variable thresholds for the single-ended receivers, the following approach is used. In HS device mode, 3ms of no USB activity (IDLE state) signals a reset. The Link monitors LINESTATE[1:0] for the IDLE state. To minimize transitions on LINESTATE[1:0] while in HS mode, the presence of !Squelch is used to force LINESTATE[1:0] to a J state.

TABLE 6-1: DEVICE LINESTATE STATES (DPPD & DMPD = 0)

		State of DP/DM Lines		
Linestate[1:0]		**Full Speed XCVRSELECT[1:0]=01 TERMSELECT=1**	**High Speed XCVRSELECT[1:0]=00 TERMSELECT=0**	**Chirp Mode XCVRSELECT[1:0]=00 TERMSELECT=1**
LS[1]	**LS[0]**			
0	0	SE0	Squelch	Squelch
0	1	FS-J	!Squelch	!Squelch & HS Differential Receiver Output
1	0	FS-K	Invalid	!Squelch & !HS Differential Receiver Output
1	1	SE1	Invalid	Invalid

TABLE 6-2: HOST LINESTATE STATES (DPPD & DMPD = 1)

		State of DPDM Lines			
Linestate[1:0]		**Low Speed XCVRSEL[1:0]=10 TERMSELECT=1**	**Full Speed XCVRSEL[1:0]=01 TERMSELECT=1**	**High Speed XCVRSEL[1:0]=00 TERMSELECT=0 OPMODE=00/01**	**Chirp Mode XCVRSEL[1:0]=00 TERMSELECT=0 OPMODE=10**
LS[1]	**LS[0]**				
0	0	SE0	SE0	Squelch	Squelch
0	1	LS-K	FS-J	!Squelch	!Squelch & HS Differential Receiver Output
1	0	LS-J	FS-K	Invalid	!Squelch & !HS Differential Receiver Output
1	1	SE1	SE1	Invalid	Invalid