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USB3803

USB 2.0 High-Speed Hub Controller Optimized for Portable Applications

Features

- Integrated USB 2.0 Compatible 3-Port Hub
- Advanced power saving features
  - 1 µA Typical Standby Current
  - Port goes into power saving state when no devices are connected downstream
  - Port is shutdown when port is disabled
  - Digital core shut down in Bypass ***(***USB3803***C only)*** and Standby Mode
- Provides USB Battery Charger Detection for:
  - USB-IF Battery Charging 1.1 compliant Dedicated Charging Ports (DCP)
  - USB-IF Battery Charging 1.1 compliant Charging Downstream Port (CDP)
  - Standard Downstream Port (SDP); ie. USB host or downstream hub port
  - Downstream Hub Ports Support USB-IF Battery Charging 1.1 as Charging Downstream Port (CDP)
- Supports either Single-TT or Multi-TT configurations for Full-Speed and Low-Speed connections (when connected to a High-Speed host)
- Bypass Switch for low power single port operation
  - Battery charging detection using a PMIC
  - Stereo and mono/mic audio
  - USB1.1 Data
- Enhanced configuration options available through serial I2C Slave Port
  - VID/PID/DID
  - String Descriptors
  - Configuration options for Hub.
- Internal Default configuration option when serial I2C host not available
- MultiTRAK™
  - Dedicated Transaction Translator per port
- PortMap
  - Configurable port mapping and disable sequencing
- PortSwap
  - Configurable differential intra-pair signal swapping
- PHYBoost™
  - Programmable USB transceiver drive strength for recovering signal integrity
- VariSense™
  - Programmable USB receiver sensitivity
- flexPWR® Technology
  - Low current design ideal for battery powered applications
  - Internal supply switching provides low power modes
- External 12, 19.2, 26, or 38.4MHz clock input
- Internal 3.3V & 1.2V Voltage Regulators for single supply operation
  - External VBAT and 1.8V dual supply input option
- Internal Short Circuit protection of USB differential signal pins
- ±5kV HBM ESD Protection
- 25-pin WLCS (1.95mm x 1.95mm Wafer Level Chip Scale) Package - 0.4mm ball pitch

Target Applications

The USB3803 is targeted for applications where more than one USB port is required. As mobile devices add more features and the systems become more complex it is necessary to have more than one USB port to take communicate with the internal and peripheral devices.

- Mobile Phones
- Ultra Mobile PCs
- Tablet Computers
- Digital Still Cameras
- Digital Video Camcorders
- Gaming Consoles
- PDAs
- Portable Media Players
- GPS Personal Navigation Devices
- Media Players/Viewers

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1.0 GENERAL DESCRIPTION

The USB3803 is a family of low-power, USB 2.0 hub controllers with three downstream ports. “USB3803” is a generic term referring to the entire family, which includes the following devices:

- USB3803C
- USB3803Ci
- USB3803B
- USB3803Bi

The USB3803 is available in two functional revisions (USB3803B and USB3803C) and two temperature ranges (commercial and industrial). USB3803C is recommended for new designs. The difference between functional revisions is the inclusion of an integrated USB bypass switch in the USB3803C device. This device specific feature, which does not pertain to the USB3803B, is called out independently throughout the document. Table 1-1 provides a summary of the feature differences between family members.

TABLE 1-1: USB3803 FAMILY DIFFERENCES

Part Number	USB Bypass Switch	0°C to +70°C	-40°C to +85°C
USB3803C	**X**	**X**	
USB3803Ci	**X**		**X**
USB3803B		**X**	
USB3803Bi			**X**

The USB3803 can attach to an upstream port as a full-speed hub or as a full-/hi-speed hub and supports low-speed, full-speed, and hi-speed (if operating as a hi-speed hub) downstream devices on all of the enabled downstream ports. The USB3803 has been specifically optimized for mobile embedded applications. The pin-count has been reduced by optimizing the USB3803 for mobile battery-powered embedded systems where power consumption, small package size, minimal BOM, and battery charger detection capabilities are critical design requirements. Standby mode and Bypass mode ***(***USB3803***C only)*** power has been minimized. Instead of a dedicated crystal, reference clock inputs are aligned to mobile applications. Flexible integrated power regulators ease integration into battery powered devices. Automatic battery charger detection is available on the upstream port. All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors on D+ and D– pins and all required pull-down and pull-up resistors on D+ and D– pins.

The integrated USB switch ***(***USB3803***C only)*** allows the USB3803C to bypass the USB Hub and directly connect the upstream and Port 3 downstream USB port for operational modes that do not require Hi-Speed media transfers. The bypass switch enables multiple connectivity options to the USB port while preserving the high speed signal quality in USB Hub Mode.

The USB3803 integrated battery charger detection circuitry supports USB-IF 1.1 charger detection methods. These circuits are used to detect the attachment and type of a USB Charger and provide an interrupt output to the portable device indicating that charger information is available to be read from USB3803 status registers via the serial interface.

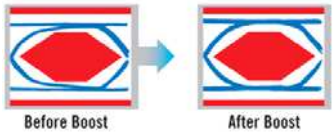
The USB3803 includes programmable features such as:

MultiTRAK™ Technology which utilizes a dedicated Transaction Translator (TT) per port to maintain consistent full-speed data throughput regardless of the number of active downstream connections. MultiTRAK™ outperforms conventional USB 2.0 hubs with a single TT in USB full-speed data transfers.

PortMap which provides flexible port mapping and disable sequences. The downstream ports of a USB3803 hub can be reordered or disabled in any sequence to support multiple platform designs with minimum effort. For any port that is disabled, the USB3803 hub controllers automatically reorder the remaining ports to match the USB host controller’s port numbering scheme.

PortSwap which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.

PHYBoost which provides programmable levels of Hi-Speed USB signal drive strength in the upstream and downstream port transceivers. PHYBoost attempts to restore USB signal integrity in a compromised system environment. The graphic on the right shows an example of Hi-Speed USB eye diagrams before and after PHY-Boost signal integrity restoration.



VariSense which controls the USB receiver sensitivity enabling programmable levels of USB signal receive sensitivity. This capability allows operation in a sub-optimal system environment, such as when a captive USB cable is used.

1.1 Customer Selectable Features

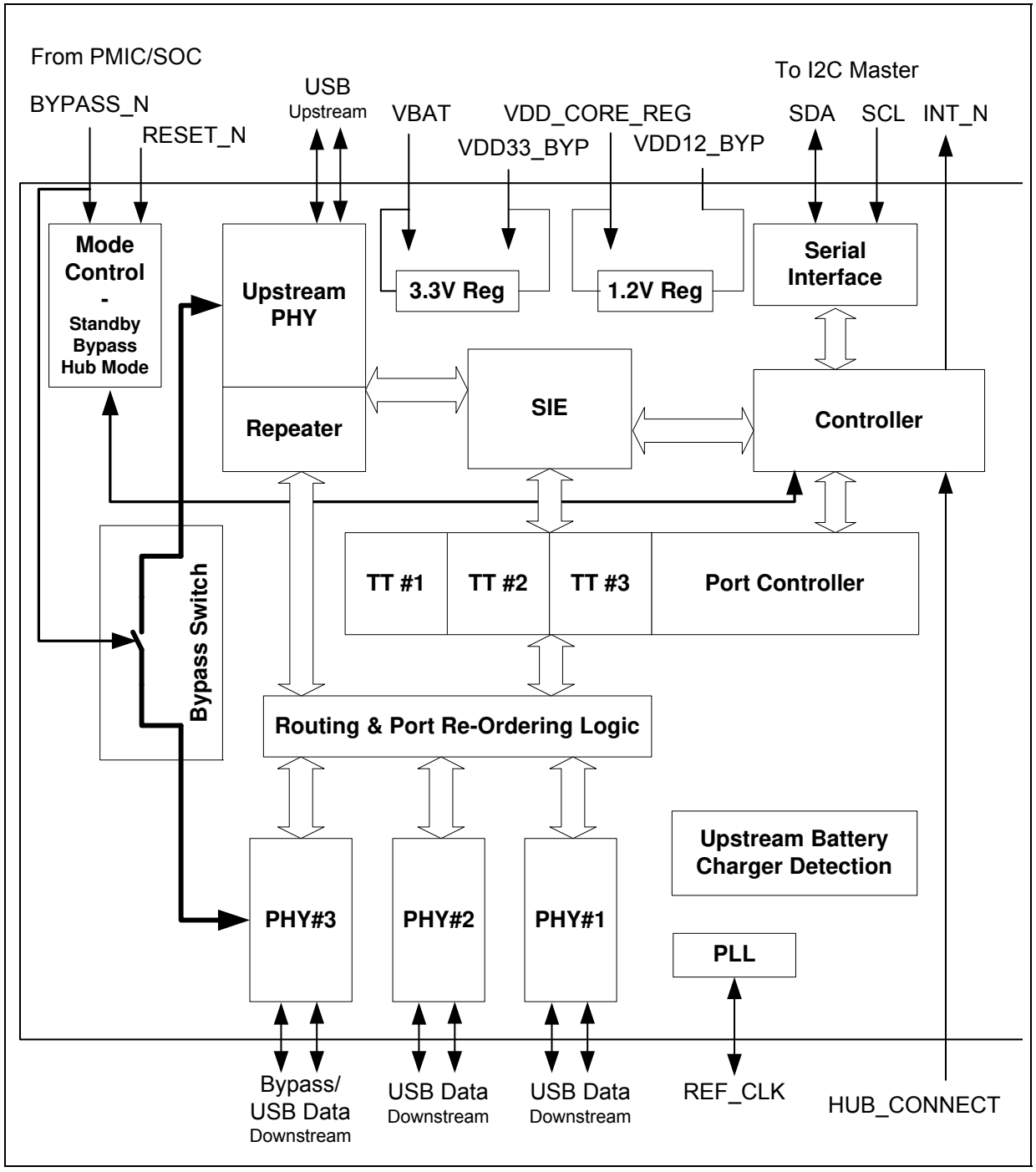
A default configuration is available in the USB3803 following a reset. This configuration may be sufficient for most applications. The USB3803 hub may also be configured by an external microcontroller. When using the microcontroller interface, the hub appears as an I^2C slave device.

The USB3803 hub supports customer selectable features including:

- Optional customer configuration via I^2C.
- Supports compound devices on a port-by-port basis.
- Customizable vendor ID, product ID, and device ID.
- Configurable downstream port power-on time reported to the host.
- Supports indication of the maximum current that the hub consumes from the USB upstream port.
- Supports Indication of the maximum current required for the hub controller.
- Configurable as a Self-Powered and Bus-Powered Hub
- Supports custom string descriptors (up to 30 characters):
  - Product string
  - Manufacturer string
  - Serial number string
- When available, I^2C configurable options for default configuration may include:
  - Downstream ports as non-removable ports
  - Downstream ports as disabled ports
  - USB signal drive strength
  - USB receiver sensitivity
  - USB differential pair pin location

1.1.1 BLOCK DIAGRAM

FIGURE 1-1: USB3803 BLOCK DIAGRAM



2.0 ACRONYMS AND DEFINITIONS

2.1 Acronyms

EP: Endpoint

FS: Full-Speed

HS: Hi-Speed

I^2C®: Inter-Integrated Circuit[1]

LS: Low-Speed

2.2 Reference Documents

1. USB Engineering Change Notice dated December 29th, 2004, *UNICODE UTF-16LE For String Descriptors*.
2. *Universal Serial Bus Specification*, Revision 2.0, Dated April 27th, 2000.
3. *Battery Charging Specification*, Revision 1.1, Release Candidate 10, Dated Sept. 22, 2008
4. *High-Speed Inter-Chip USB Electrical Specification*, Version 1.0, Dated Sept. 23, 2007

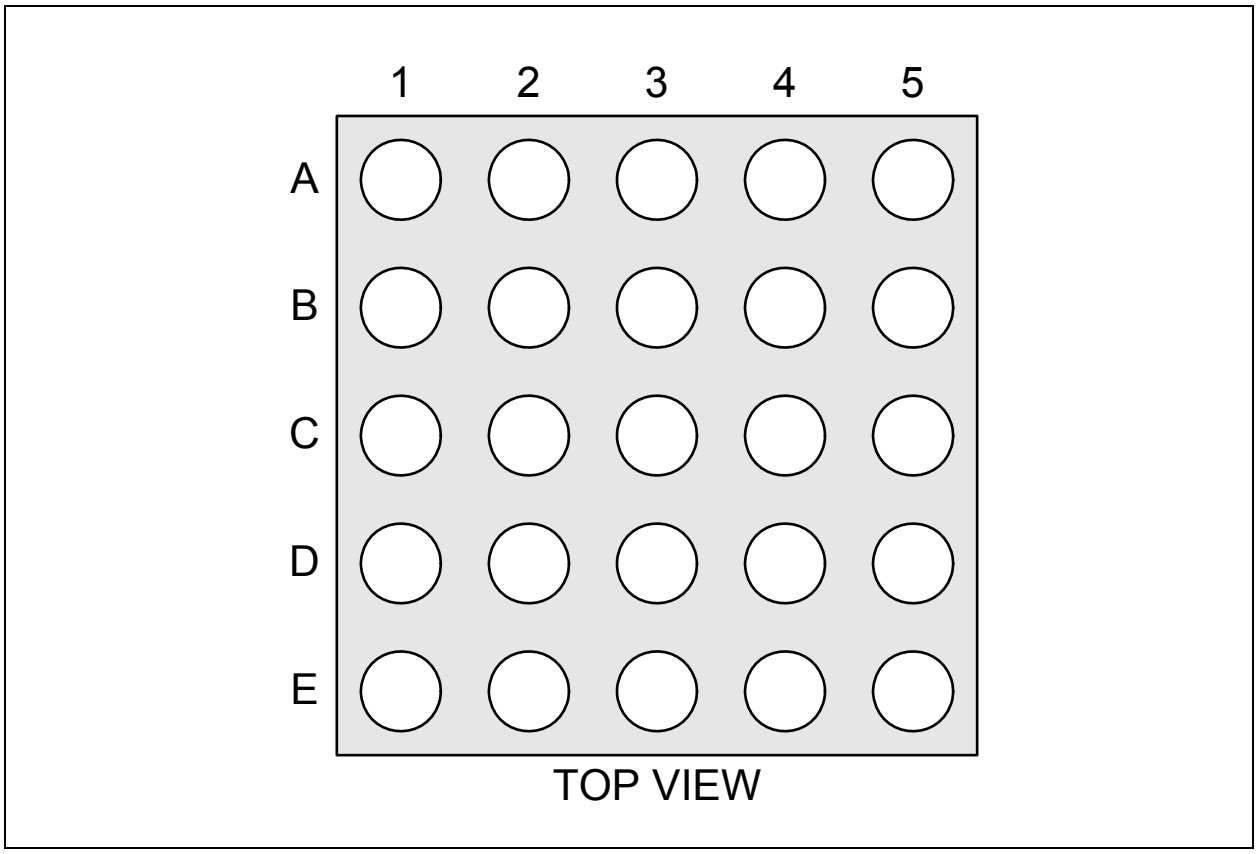
1.I^2C is a registered trademark of Philips Corporation.

3.0 USB3803 PIN DEFINITIONS

3.1 Pin Configuration

The illustration below shows the package diagram.

FIGURE 3-1: USB3803 25-BALL PACKAGE



3.2 Signal Definitions

WLCSP Pin	Name	Description
E2	USBUP_DP	Upstream D+ data pin of the USB Interface
E1	USBUP_DM	Upstream D- data pin of the USB Interface
A5	BYPASS_N	Control signal to select between HUB MODE and BYPASS MODE **Note:** Bypass mode is only available in the USB3803C.
C4	I2C_ASEL0	I^2C Address Select Bit 0
B4	I2C_ASEL1	I^2C Address Select Bit 1
A1	USBDN1_DP	USB downstream Port 1 D+ data pin
B1	USBDN1_DM	USB downstream Port 1 D- data pin
C2	USBDN2_DP	USB downstream Port 2 D+ data pin
D2	USBDN2_DM	USB downstream Port 2 D- data pin
C1	USBDN3_DP	USB downstream Port 3 D+ data pin
D1	USBDN3_DM	USB downstream Port 3 D- data pin
E5	SCL	I^2C clock input
D5	SDA	I^2C bi-directional data pin
E3	RESET_N	Active low reset signal
B5	HUB_CONNECT	Hub Connect
C5	INT_N	Active low interrupt signal
D4	REF_SEL1	Reference Clock Select 1 input
E4	REF_SEL0	Reference Clock Select 0 input
B3	REFCLK	Reference Clock input
A4	RBIAS	Bias Resistor pin
D3	VDD12_BYP	1.2 V Regulator
A2	VDD33_BYP	3.3 V Regulator
B2	VBAT	Voltage input from the battery supply
A3	VDD_CORE_REG	Power supply input to 1.2V regulator for digital logic core
C3	VSS	Ground

3.3 Pin Descriptions

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The terms assertion and negation are used. This is done to avoid confusion when working with a mixture of “active low” and “active high” signal. The term “assert”, or “assertion” indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term “negate”, or “negation” indicates that a signal is inactive.

3.3.1 PIN DEFINITION

TABLE 3-1: PIN DESCRIPTIONS

Name	Symbol	Type	Description
Upstream USB 2.0 / Bypass Interface			
USB Bus Data	USBUP_DP USBUP_DM	A-I/O	These pins connect to the upstream USB bus data signals (Host port, or upstream hub)
Bypass Select for Analog Switch	BYPASS_N	I	Control signal to select between Hub Mode and Bypass Mode. When asserted low, the device transitions to Bypass Mode, connects the Bypass Port to the upstream USB Port, places Port 1 and Port 2 in high impedance state, and places the core logic in a reduced power state. When negated high, the device transitions to HUB MODE and enables operation as a USB hub. **Note:** Bypass mode is only available in the USB3803C. For the USB3803B, this pin must always be driven high.
Downstream USB 2.0 / Bypass Interface			
High-Speed USB Data & Port Disable Strap Option	USBDN_DP[2:1] & USBDN_DM[2:1]	A-I/O	These pins connect to the downstream USB peripheral devices attached to the hub’s ports
			Downstream Port Disable Strap option: This pin will be sampled at RESET_N negation to determine if the port is disabled. Both USB data pins for the corresponding port must be tied to VDD33_BYP to disable the associated downstream port.

TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Type	Description
HS USB Data & Bypass Port	USBDN_DP[3] & USBDN_DM[3]	A-I/O	When BYPASS_N is negated high, these pins connect to the downstream USB peripheral devices attached to the hub's ports.
			There is no downstream Port Disable Strap option on these ports. When BYPASS_N is asserted low, USBDN_DP[3] and USBDN_DM[3] respectively are connected through the analog switch to the upstream port USBUP_DP and USBUP_DM. PortSwap setting has no effect in Bypass Mode. **Note:** Bypass mode is only available in the USB3803C. For the USB3803B, BYPASS_N must always be driven high.
Serial Port Interface			
Serial Data	SDA	I/OD	I^2C Serial Data
Serial Clock	SCL	I	Serial Clock (SCL)
Interrupt	INT_N	OD	Interrupt The function of this pin is determined by the setting in the CFGP.INTSUSP configuration register. When CFGP.INTSUSP = 0 (General Interrupt) A transition from high to low identifies when one of the interrupt enabled status registers has been updated. SOC must update the Serial Port Interrupt Status Register to reset the interrupt pin high. When CFGP.INTSUSP = 1 (Suspend Interrupt) Indicates USB state of the hub. 'Asserted' low = Unconfigured or configured and in USB Suspend 'Negated' high = Hub is configured, and is active (i.e., not in suspend) The Suspend Interrupt can be used by the system to determine whether the full current based on the USB descriptor can be drawn on VBUS or whether a reduced current should be drawn in accordance with the USB specification for unconfigured or suspend mode. If unused, this pin must be tied to **VDD33_BYP**.

TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Type	Description
Serial Address Select	I2C_ASEL[1:0]	I	Address Select – the USB3803 has the ability to be programmed with four different I^2C slave addresses as part of the configuration in order to provide flexibility. When sharing the serial bus in the system with another part that conflicts with one of the address settings, these pins may be used to change the selection to a non-conflicting I^2C address. The customer should tie these pins to ground or VDD33_BYP. This input is latched during HUB.Init stage. I2C_ASEL[1] selects between the I2C addresses defined in registers I2CADD0 and I2CADD1. I2C_ASEL[0] determines the LSB of the I2C address.
Misc			
Reference Clock Input	REFCLK	I	Reference clock input.
Reference Clock Select	REF_SEL[1:0]	I	The reference select input must be set to correspond to the frequency applied to the REFCLK input. The customer should tie these pins to ground or VDD33_BYP. This input is latched during HUB.Init stage. Selects input reference clock frequency per Table 3-3.
RESET Input	RESET_N	I	This active low signal is used by the system to reset the chip and hold the chip in low power STANDBY MODE.
USB Transceiver Bias	RBIAS	A-I/O	A 12.0kΩ (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings.
Hub Connect	HUB_CONNECT	I	Hub will transition to the Hub Communication Stage when this pin is asserted high. It can be used in three different ways: Tied to Ground - Hub will not transition to the Hub Communication Stage until connect_n bit of the SP_ILOCK register is negated. Tied to **VDD33_BYP** - Hub will automatically transition to the Hub Communication Stage regardless of the setting of the connect_n bit and without pausing for the SOC to reference status registers. Transition from low to high - Hub will transition to the Hub Communication Stage after this pin transitions from low to high. HUB_CONNECT should never be driven high when USB3803 is in Standby Mode.
Power			
1.2V VDD Power	VDD12_BYP	Power	1.2 V Regulator. A 1.0 µF (<1 Ω ESR) capacitor to ground is required for regulator stability. The capacitor should be placed as close as possible to the USB3803.

TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Type	Description
3.3V VDD Power	VDD33_BYP	Power	3.3V Regulator. A 4.7µF (<1 Ω ESR) capacitor to ground is required for regulator stability. The capacitor should be placed as close as possible to the USB3803.
Core Power Supply Input	VDD_CORE_REG	Power	Power supply to 1.2V regulator. This power pin should be connected to VDD33_BYP for single supply applications. Refer to Section 9.0, Integrated Power Regulators for power supply configuration options.
Battery Power Supply Input	VBAT	Power	Battery power supply. Refer to Section 9.0 for power supply configuration options.
VSS	VSS	Ground	Ground

3.3.2 I/O TYPE DESCRIPTIONS

TABLE 3-2: USB3803 I/O TYPE DESCRIPTIONS

I/O Type	Description
I	Digital Input
OD	Digital Output. Open Drain.
I/O	Digital Input or Output.
A-I/O	Analog Input or Output.
Power	DC input or Output.
Ground	Ground.

3.3.3 REFERENCE CLOCK

The REFCLK input is can be driven with a square wave from 0 V to VDD33_BYP. The USB3803 only uses the positive edge of the clock. The duty cycle is not critical.

The USB3803 is tolerant to jitter on the reference clock. The REFCLK jitter should be limited to a peak to peak jitter of less than 1 nS over a 10 µS time interval. If this level of jitter is exceeded the USB3803 high speed eye diagram may be degraded.

To select the REFCLK input frequency, the REF_SEL pins must be set according to Table 3-3.

TABLE 3-3: USB3803 REFERENCE CLOCK FREQUENCIES

REF_SEL[1:0]	Frequency (MHz)
‘00’	38.4
‘01’	26.0
‘10’	19.2
‘11’	12.0

3.3.4 INTERRUPT

The general interrupt pin (INT_N) is intended to communicate a condition change within the hub. The conditions which may cause an interrupt are captured within a register mapped to the serial port (Register E8h: Serial Port Interrupt Status - INT_STATUS.) The conditions which cause the interrupt to assert can be controlled through use of an interrupt mask register (Register E9h: Serial Port Interrupt Mask - INT_MASK.)

The general interrupt and all interrupt conditions are functionally latched and event driven. Once the interrupt or any of the conditions have asserted, the status bit will remain asserted until the SOC negates the bit using the serial port. The bits will then remain negated until a new event condition occurs. The latching nature of the register causes the status to remain even if the condition that caused the interrupt ceases to be active. The event driven nature of the register causes the interrupt to only occur when a new event occurs- when a condition is removed and then is applied again. (e.g. if the battery charger detection routine has completed and the SOC negates the interrupt status, it will not cause an interrupt just because the charger detection is still completed- a new charger detection routine has to run before its associated interrupt will assert again.)

The function of the interrupt and the associated status and masking registers are illustrated in Figure 3-2, "INT_N Operation". Registers & Register bits shown in the figure are defined in Table 5-2, “Serial Interface Registers,” on page 21 and Section 5.3, "Serial Interface Register Definitions," on page 23.

FIGURE 3-2: INT_N OPERATION

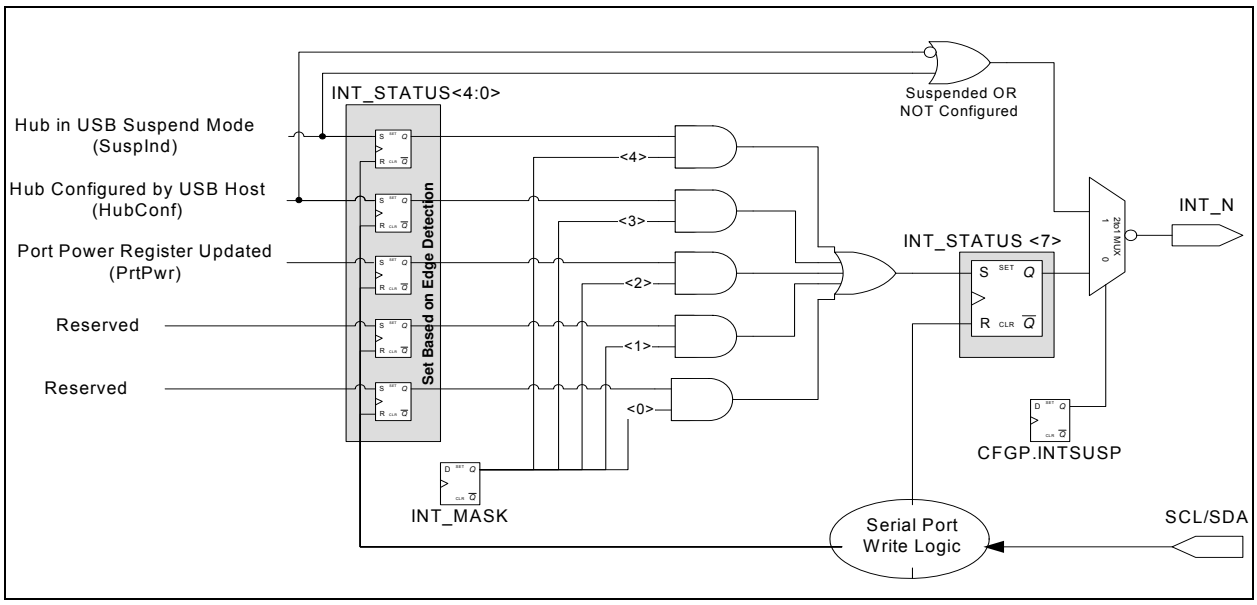


Figure 3-2 also shows an alternate configuration option (CFGP.INTSUSP) for a suspend interrupt. This option allows the user to change the behavior of the INT_N pin to become a direct level indication of configuration and suspend status.

When selected, the INT_N indicates that the entire hub has entered the USB suspend state and that VBUS current consumption should be reduced in accordance with the USB specification. Selective suspend set by the host on downstream hub ports have no effect on this signal because there is no requirement to reduce current consumption from the upstream VBUS. It can be used by the system to monitor INT_N to dynamically adjust how much current the PMIC draws from VBUS to charge the battery in the system during a USB session. Because it is a level indication, it will assert or negate to reflect the current status of suspend without any interaction through the serial port.

When negated high this means no level suspend interrupt and device has been configured by the USB Host. The full configured current can be drawn from the USB VBUS pin on the USB connector for charging - up to 500mA depending on descriptor setting. When asserted low, this indicates a suspend interrupt or device not yet configured by USB Host. The current draw can be limited by the system according to the USB specification. The USB specification limits current to 100mA before configuration, and up to 12.5mA in USB suspend mode.

Note:	Because INT_N is driven low when active, care must be taken when selecting the external pullup resistor value for this open drain output. A sufficiently large resistor must be selected to insure suspend current requirements can be satisfied for the system.

4.0 MODES OF OPERATION

The USB3803 has modes of operation - Standby Mode, Bypass Mode ***(***USB3803***C only)*** and Hub Mode which balance power consumption with functionality. The operating mode of the USB3803 is selected by setting values on primary inputs according to the table below.

TABLE 4-1: CONTROLLING MODES OF OPERATION

RESET_N input	BYPASS_N Input (Note 1)	Resulting Mode	Summary
0	0	Standby	Lowest Power Mode – no function other than monitoring RESET_N and BYPASS_N inputs to move to higher states. Switch Resistance is R_{STDBY}. All regulators are powered off.
1	0	Bypass (Note 1)	Low Power Mode - Bypass Switch connects bypass port (downstream port 3) to upstream port with low switch resistance R_{ON}.
1	1	Hub	Full Feature Mode - Operates as a configurable USB hub with battery charger detection. Switch is disabled and assumes high switch resistance R_{OFF}. Power consumption based on how many ports are active, at what speeds they are running and amount of data transferred (refer to Table 10-3 and Table 10-4).

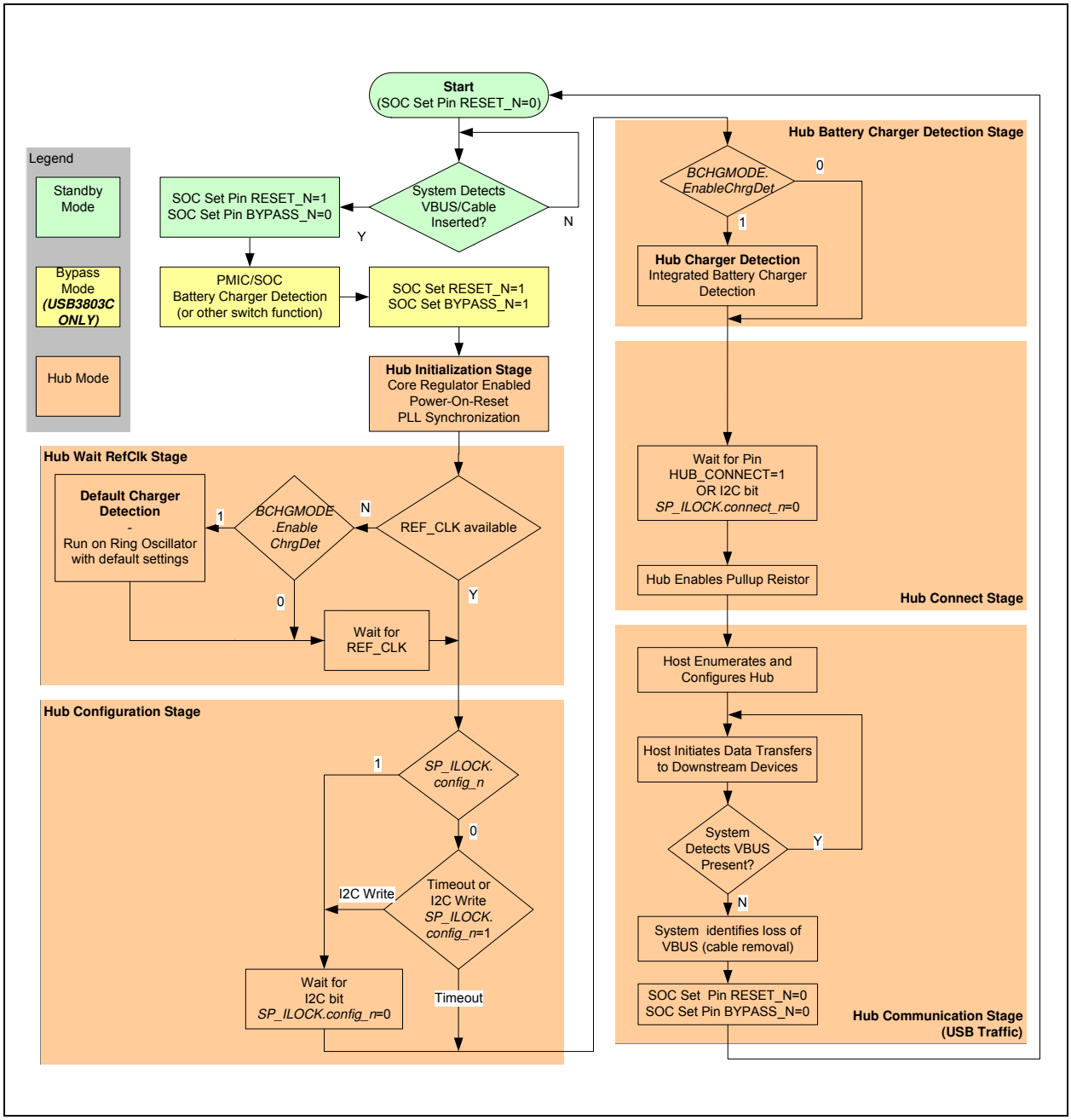
Note 1: Bypass mode is only available in the USB3803C. The BYPASS_N pin must always be driven high in the USB3803B. Refer to Section 1.0, "General Description," on page 4 for a list of differences between each version of the USB3803.

4.1 Operational Mode Flowchart

The flowchart in Figure 4-1 shows the modes of operation. It also shows how the USB3803 traverses through the Hub mode stages (shown in bold.) The flow of control is dictated by control register bits shown in Italics as well as other events such as availability of reference clock. Refer to Section 5.3, "Serial Interface Register Definitions," on page 23 for the detailed definition of the control register bits. In this specification register bits are referenced using the syntax <Register>.<RegisterBit>. A summary of all registers can be found in Table 5-2, “Serial Interface Registers,” on page 21.

The remaining sections in this chapter provide more detail on each stage and mode of operation.

FIGURE 4-1: MODES OF OPERATION FLOWCHART



4.2 Standby Mode

Standby Mode provides a very low power state for maximum power efficiency when no signaling is required. This is the lowest power state. In Standby Mode all internal regulators are powered off, the bypass switch resistance is unconstrained, the PLL is not running, and core logic is powered down in order to reduce power. Because core logic is powered off, no configuration settings are retained in this mode and must be re-initialized after RESET_N is negated high.

4.2.1 EXTERNAL HARDWARE RESET_N

A valid hardware reset is defined as an assertion of RESET_N low for a minimum of 100us after all power supplies are within operating range. While reset is asserted, the Hub (and its associated external circuitry) enters STANDBY MODE and consumes extremely lowcurrent as defined in Table 10-3 and Table 10-4.

Assertion of RESET_N (external pin) causes the following:

- All downstream ports are disabled.
- The switch assumes resistance R_{STDBY}.
- All transactions immediately terminate; no states are saved.
- All internal registers return to the default state.
- The PLL is halted.

After RESET_N is negated high in the Hub.Init stage, the Hub reads customer-specific data from the ROM.

4.3 Bypass Mode *(USB3803C Only)*

Bypass Mode combines low power operation with the function of an integrated bypass switch. This mode allows a bypass port (Downstream Port 3) to be electrically connected to the upstream port through use of a pass gate as illustrated in Figure 1-1. Compliant full speed USB signals may be successfully passed through the switch.

There are several applications for this mode. The bypass port can be used to provide connectivity to a PMIC to implement battery charger detection. In this configuration any special signaling is replicated on the line as if the hub were not in series. Another application is for a downstream device on Port 3 to assume a full speed host role for an application such as USB OTG or embedded usb host. It can also be used to provide audio signaling (must be offset to avoid negative signal swing.)

To insure that Bypass mode entered, RESET_N must be asserted and then de-asserted prior to asserting BYPASS_N (refer to Table 4-1). In Bypass Mode the 1.2V regulator is powered off, PLL is not running and core logic is powered down in order to reduce power. Because core logic is powered off, no configuration settings are retained in this mode and must be re-initialized when BYPASS_N is negated to a high value.

4.3.1 VOLTAGE RANGE

The switch shall operate in a voltage range as specified by V_{switch} in Table 10-9, “Analog Switch Characteristics,” on page 83. Negative voltage swing is not supported.

4.3.2 SWITCH BANDWIDTH

The switch shall support compliant operation with an external full speed USB Port and with external battery charger detection. Under certain conditions with short cables it may be possible to pass high speed USB signals. However, due to physical design constraints, the switch is not necessarily intended to pass a fully compliant high speed USB eye.

4.4 Hub Mode

Hub Mode provides functions of configuration, upstream battery charger detection, and high speed USB hub operation including connection and communication. Upon entering Hub Mode and initializing internal logic, the device passes through several sequential stages based on a fixed time interval. In Hub Mode the bypass switch is disabled.

Note:	In order to adhere to the USB 2.0 Specification the system must not consume more than 100mA from the upstream VBUS until the Hub is configured by the host.

4.4.1 HUB INITIALIZATION STAGE (HUB.INIT)

The first stage is the initialization stage and occurs when Hub mode is entered based on the conditions in Table 4-1. In this stage the 1.2V regulator is enabled and stabilizes, internal logic is reset, and the PLL locks if a valid REFCLK is supplied. Configuration registers are initialized to their default state and I2C_ASEL[1:0] and REF_SEL[1:0] input values are latched. The USB3803 will complete initialization and automatically enter the next stage after $T_{hubinit}$. Because the digital logic within the device is not yet stable, no communication with the device using the serial port is possible. Configuration registers are initialzed to their default state.

4.4.2 HUB WAIT REFCLK STAGE (HUB.WAITREF)

In this stage the reference clock is checked for activity. If the reference clock is active the part will continue to the Hub configuration stage. If the reference clock is not active but the default ROM has enabled battery charger detection, the detection sequence will begin while operating on an internal ring oscillator.

If the PLL locks while battery charger detection is still in progress, the sequence will be aborted until the battery charger detection stage is complete. If aborted, no results are captured. If battery charger detection completes, the results of the battery charger detection may be communicated through the INT_N pin.

During this stage the serial port is not functional.

If the reference clock is provided before entering hub mode, the USB3803 will transition to the Hub Configuration stage without pausing in the Hub Wait RefClk stage. Otherwise, the USB3803 will transition to the Hub configuration stage once a valid reference clock is supplied and the PLL has locked.

4.4.3 HUB CONFIGURATION STAGE (HUB.CONFIG)

The next stage is the configuration stage. In this stage, the SOC has an opportunity to control the configuration of the USB3803 and modify any of the default configuration settings specified in the integrated ROM such as USB device descriptors, or port electrical settings such as PHY BOOST, and control features such as battery charging detection. The SOC implements the changes using the serial slave port interface to write configuration & control registers.

See Section 5.3.30, "Register E7h: Serial Port Interlock Control - SP_ILOCK," on page 32 for definition of SP_ILOCK register and how it controls progress through hub stages. If the SP_ILOCK.config_n bit has its default asserted low and the bit is not written by the serial port, then the USB3803 completes configuration and automatically enters the Battery Charger Detection Stage after $T_{hubconfig}$ without any I2C intervention.

If the SP_ILOCK.config_n bit has its default negated high or the SOC negates the bit high using the serial port during $T_{hubconfig}$, the USB3803 will remain in the Hub Configuration Stage indefinitely. This will allow the SOC to update other configuration and control registers without any remaining time-out restrictions. Once the SP_ILOCK.config_n bit is asserted low by the SOC the device will transition to the next stage.

4.4.4 HUB BATTERY CHARGER DETECTION STAGE (HUB.CHGDET)

After configuration, the device enters Battery Charger Detection Stage. If the battery charger detection feature was disabled during the Hub Configuration Stage, the USB3803 will immediately transition to the Hub Connect Stage. If the battery charger detection feature remains enabled, the battery charger detection sequence is started automatically and the USB3803 will transition to the Hub Connect Stage after $T_{hubchgdet}$.

4.4.5 HUB CONNECT STAGE (HUB.CONNECT)

Next, the USB3803 enters the Hub Connect Stage. See Section 5.3.37, "Register EEh: Configure Portable Hub - CFGP," on page 36 and Section 5.3.30, "Register E7h: Serial Port Interlock Control - SP_ILOCK," on page 32 for definition of control registers which affect how the device transitions through the hub stages.

By using the appropriate controls, the USB3803 can be set to immediately transition, or instead to remain in the Hub Connect Stage indefinitely until one of the SOC handshake events occur. When set to wait on the handshake, the SOC may read or update any of the serial port registers. Once the SOC is finished accessing any registers and is ready for USB communication to start, it can perform one of the selected handshakes which will cause the USB3803 to assert its pull-up on the USBUP_DP pin and connect within $T_{hubconnect}$ and transition to the Hub Communication Stage.

4.4.6 HUB COMMUNICATION STAGE (HUB.COM)

Once it exits the Hub Connect Stage, the USB3803 enters Hub Communication Stage. In this stage full USB operation is supported under control of the USB Host on the upstream port. The USB3803 will remain in the Hub Communication Stage until the operating mode is changed by the system asserting RESET_N or BYPASS_N low.

While in the Hub Communication Stage, communication over the serial port is no longer supported and the resulting behavior of the serial port if accessed is undefined. In order to re-enable the serial port interface, the device must exit Hub Communication Stage. Exiting this stage is only possible by entering Standby or Bypass mode.

4.4.7 HUB MODE TIMING DIAGRAM

The following timing diagram shows the progression through the stages of Hub Mode and the associated timing parameters.

The following table lists the timing parameters associated with the stages of the Hub Mode.

TABLE 4-2: TIMING PARAMETERS FOR HUB STAGES

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Hub Initialization Time	$T_{HUBINIT}$		3	4	mS	
Hub Connect Time	$T_{HUBCONNECT}$	0	1	10	uS	

5.0 CONFIGURATION OPTIONS

5.1 Hub Configuration Options

The Hub supports a number of features (some are mutually exclusive), and must be configured in order to correctly function when attached to a USB host controller. There are two principal ways to configure the hub: by writing to configuration registers using the serial slave port, or by internal default settings. Any configuration registers which are not written by the serial slave retain their default settings.

5.1.1 MULTI/SINGLE TT

The USB 2.0 Hub is fully specification compliant to the Universal Serial Bus Specification Revision 2.0 April 27,2000 (12/7/2000 and 5/28/2002 Errata). Please reference Chapter 11 (Hub Specification) for general details regarding Hub operation and functionality.

For performance reasons, the Hub provides 1 Transaction Translator (TT) per port (defined as Multi-TT configuration), and each TT has 1512 bytes of periodic buffer space and 272 Bytes of non- periodic buffer space (divided into 4 non-periodic buffers per TT), for a total of 1784 bytes of buffer space for each Transaction Translator.

When configured as a Single-TT Hub (required by USB 2.0 Specification), the Single Transaction Translator will have 1512 bytes of periodic buffer space and 272 bytes of non-periodic buffer space (divided into 4 non-periodic buffers per TT), for a total of 1784 bytes of buffer space for the entire Transaction Translator. **Each Transaction Translator's buffer is divided as shown in** Table 5-1, "Transaction Translator Buffer Chart"**.**

TABLE 5-1: TRANSACTION TRANSLATOR BUFFER CHART

Periodic Start-Split Descriptors	256 Bytes
Periodic Start-Split Data	752 Bytes
Periodic Complete-Split Descriptors	128 Bytes
Periodic Complete-Split Data	376 Bytes
Non-Periodic Descriptors	16 Bytes
Non-Periodic Data	256 Bytes
Total for each Transaction Translator	1784 Bytes

5.1.2 VBUS DETECT

According to Section 7.2.1 of the USB 2.0 Specification, a downstream port can never provide power to its D+ or D- pull-up resistors unless the upstream port's VBUS is in the asserted (powered) state. Depending on input tie-offs and values in the configuration registers, the USB3803 may automatically enable the D+ pull-up resistor once it enters the Hub.Connect stage of Hub Mode (after RESET_N and BYPASS_N ***(***USB3803***C Only)*** are both negated high.) To fully adhere to the USB specification, the system should not cause the part to enter Hub.Com Hub Mode until VBUS has been detected on the upstream port and a connection is desired.

5.2 Default Serial Interface Register Memory Map

The Serial Interface Registers are used to customize the USB3803 for specific applications. Reserved registers or reserved bits within a defined register should not be written to non-default values or undefined behavior may result.

TABLE 5-2: SERIAL INTERFACE REGISTERS

Reg Addr	R/W	Register Name	Abbrevation	Section
00h	R/W	VID LSB	VIDL	5.3.1, page 23
01h	R/W	VID MSB	VIDM	5.3.2, page 23
02h	R/W	PID LSB	PIDL	5.3.3, page 23
03h	R/W	PID MSB	PIDM	5.3.4, page 23
04h	R/W	DID LSB	DIDL	5.3.5, page 23
05h	R/W	DID MSB	DIDM	5.3.6, page 23
06h	R/W	Config Data Byte 1	CFG1	5.3.7, page 24
07h	R/W	Config Data Byte 2	CFG2	5.3.8, page 25
08h	R/W	Config Data Byte 3	CFG3	5.3.9, page 25
09h	R/W	Non-Removable Devices	NRD	5.3.10, page 26
0Ah	R/W	Port Disable (Self)	PDS	5.3.11, page 26
0Bh	R/W	Port Disable (Bus)	PDB	5.3.12, page 27
0Ch	R/W	Max Power (Self)	MAXPS	5.3.13, page 27
0Dh	R/W	Max Power (Bus)	MAXPB	5.3.14, page 27
0Eh	R/W	Hub Controller Max Current (Self)	HCMCS	5.3.15, page 28
0Fh	R/W	Hub Controller Max Current (Bus)	HCMCB	5.3.16, page 28
10h	R/W	Power-on Time	PWRT	5.3.17, page 28
11h	R/W	LANG_ID_H	LANGIDH	5.3.18, page 28
12h	R/W	LANG_ID_L	LANGIDL	5.3.19, page 29
13h	R/W	MFR_STR_LEN	MFRSL	5.3.20, page 29
14h	R/W	PRD_STR_LEN	PRDSL	5.3.21, page 29
15h	R/W	SER_STR_LEN	SERSL	5.3.22, page 29
16h-53h	R/W	MFR_STR	MANSTR	5.3.23, page 29
54h-91h	R/W	PROD_STR	PRDSTR	5.3.24, page 29
92h-CFh	R/W	SER_STR	SERSTR	5.3.25, page 30
D0h	R/W	Downstream Battery Charging	BC_EN	5.3.26, page 30
D1-E1h	R/W	Reserved	N/A	

TABLE 5-2: SERIAL INTERFACE REGISTERS (CONTINUED)

Reg Addr	R/W	Register Name	Abbrevation	Section
E2h	R/W	Upstream Battery Charger Detection	BATT_CHG	5.3.27, page 31
E3-E4h	R/W	Reserved	N/A	
E5h	R	Port Power Status	PRTPWR	5.3.28, page 32
E6h	R/W	Over Current Sense Control	OCS	5.3.29, page 32
E7h	R/W	Serial Port Interlock Control	SP_ILOCK	5.3.30, page 32
E8h	R/W	Serial Port Interrupt Status	INT_STATUS	5.3.31, page 33
E9h	R/W	Serial Port Interrupt Mask	INT_MASK	5.3.32, page 34
EAh	R	I2C Address 0	I2CADD0	5.3.33, page 34
EBh	R	I2C Address 1	I2CADD1	5.3.34, page 35
ECh	R/W	Battery Charger Mode	BCHGMODE	5.3.35, page 35
EDh	R/W	Charger Detect Mask	CHGDETMASK	5.3.36, page 35
EEh	R/W	Configure Portable Hub	CFGP	5.3.37, page 36
EFh-F3h	R	Reserved	N/A	
F4h	R/W	Varisense_Up3	VSNSUP3	5.3.38, page 36
F5h	R/W	Varisense_21	VSNS21	5.3.39, page 37
F6h	R/W	Boost_Up3	BSTUP3	5.3.40, page 37
F7h	R/W	Reserved	N/A	
F8h	R/W	Boost_21	BST21	5.3.41, page 38
F9h	R/W	Reserved	N/A	
FAh	R/W	Port Swap	PRTSP	5.3.42, page 38
FBh	R/W	Port Remap 12	PRTR12	5.3.43, page 39
FCh	R/W	Port Remap 34	PRTR34	5.3.44, page 40
FDh	R/W	Reserved	N/A	
FEh	R/W	Reserved	N/A	
FFh	R/W	I2C Status/Command	STCD	5.3.45, page 41

5.3 Serial Interface Register Definitions

5.3.1 REGISTER 00H: VENDOR ID (LSB) - VIDL

Default = 0x24h - Corresponds to MCHP Vendor ID.

Bit Number	Bit Name	Description
7:0	VID_LSB	Least Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Interface Forum). This field is set by the customer using the serial interface options.

5.3.2 REGISTER 01H: VENDOR ID (MSB) - VIDM

Default = 0x04h - Corresponds to MCHP Vendor ID.

Bit Number	Bit Name	Description
7:0	VID_MSB	Most Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB-Interface Forum). This field is set by the customer using serial interface options.

5.3.3 REGISTER 02H: PRODUCT ID (LSB) - PIDL

Default = 0x03h - Corresponds to MCHP USB part number for 3-port device.

Bit Number	Bit Name	Description
7:0	PID_LSB	Least Significant Byte of the Product ID. This is a 16-bit value that the Vendor can assign that uniquely identifies this particular product (assigned by customer). This field is set by the customer using the serial interface options.

5.3.4 REGISTER 03H: PRODUCT ID (MSB) - PIDM

Bit Number	Bit Name	Description
7:0	PID_MSB	Most Significant Byte of the Product ID. This is a 16-bit value that the Vendor can assign that uniquely identifies this particular product (assigned by customer). This field is set by the customer using the serial interface options.

5.3.5 REGISTER 04H: DEVICE ID (LSB) - DIDL

Bit Number	Bit Name	Description
7:0	DID_LSB	Least Significant Byte of the Device ID. This is a 16-bit device release number in BCD format (assigned by customer). This field is set by the customer using the serial interface options.

5.3.6 REGISTER 05H: DEVICE ID (MSB) - DIDM

Bit Number	Bit Name	Description
7:0	DID_MSB	Most Significant Byte of the Device ID. This is a 16-bit device release number in BCD format (assigned by customer). This field is set by the customer using the serial interface options.

5.3.7 REGISTER 06H: CONFIG_BYTE_1 - CFG1

Bit Number	Bit Name	Description
7	SELF-_BUS_PWR	Self or Bus Power: Selects between Self- and Bus-Powered operation. The Hub is either Self-Powered (draws less than 2mA of upstream bus power) or Bus-Powered (limited to a 100mA maximum of upstream power prior to being configured by the host controller). When configured as a Bus-Powered device, the Microchip Hub consumes less than 100mA of current prior to being configured. After configuration, the Bus-Powered Microchip Hub (along with all associated hub circuitry, any embedded devices if part of a compound device, and 100mA per externally available down-stream port) must consume no more than 500mA of upstream VBUS current. The current consumption is system dependent, and the customer must ensure that the USB 2.0 specifications are not violated. When configured as a Self-Powered device, <1mA of upstream VBUS current is consumed and all ports are available, with each port being capable of sourcing 500mA of current. This field is set by the customer using the serial interface options. 0 = Bus-Powered operation. 1 = Self-Powered operation.
6	Reserved	Reserved
5	HS_DISABLE	High Speed Disable: Disables the capability to attach as either a High/Full-speed device, and forces attachment as Full-speed only i.e. (no High-Speed support). 0 = High-/Full-Speed. 1 = Full-Speed-Only (High-Speed disabled!)
4	MTT_ENABLE	Multi-TT enable: Enables one transaction translator per port operation. Selects between a mode where only one transaction translator is available for all ports (Single-TT), or each port gets a dedicated transaction translator (Multi-TT) {Note: The host may force Single-TT mode only}. 0 = single TT for all ports. 1 = one TT per port (multiple TT's supported)
3	EOP_DISABLE	EOP Disable: Disables EOP generation of EOF1 when in Full-Speed mode. During FS operation only, this permits the Hub to send EOP if no downstream traffic is detected at EOF1. See Section 11.3.1 of the USB 2.0 Specification for additional details. Note: generation of an EOP at the EOF1 point may prevent a Host controller (operating in FS mode) from placing the USB bus in suspend. 0 = An EOP is generated at the EOF1 point if no traffic is detected. 1 = EOP generation at EOF1 is disabled (note: this is normal USB operation). **Note:** This is a rarely used feature in the PC environment, existing drivers may not have been thoroughly debugged with this feature enabled. It is included because it is a permitted feature in Chapter 11 of the USB specification.

Bit Number	Bit Name	Description
2:1	CURRENT_SNS	Over Current Sense: Selects current sensing on a port-by-port basis, all ports ganged, or none (only for bus-powered hubs) The ability to support current sensing on a port or ganged basis is hardware implementation dependent. 00 = Ganged sensing (all ports together). 01 = Individual port-by-port. 1x = Over current sensing not supported. (must only be used with Bus- Powered configurations!)
0	PORT_PWR	Port Power Switching: Enables power switching on all ports simultaneously (ganged), or port power is individually switched on and off on a port- by-port basis (individual). The ability to support power enabling on a port or ganged basis is hardware implementation dependent. 0 = Ganged switching (all ports together) 1 = Individual port-by-port switching.

5.3.8 REGISTER 07H: CONFIGURATION DATA BYTE 2 - CFG2

Bit Number	Bit Name	Description
7:4	Reserved	Reserved
3	COMPOUND	Compound Device: Allows the customer to indicate that the Hub is part of a compound (see the USB Specification for definition) device. The applicable port(s) must also be defined as having a “Non-Removable Device”. 0 = No. 1 = Yes, Hub is part of a compound device.
2:0	Reserved	Reserved

5.3.9 REGISTER 08H: CONFIGURATION DATA BYTE 3 - CFG3

Bit Number	Bit Name	Description
7:4	Reserved	Reserved
3	PRTMAP_EN	Port Re-Mapping enable: Selects the method used by the hub to assign port numbers and disable ports ‘0’ = Standard Mode. The following registers are used to define which ports are enabled, and the ports are mapped as Port “n” on the hub is reported as Port ‘n’ to the host, unless one of the ports is disabled, then the higher numbered ports are remapped in order to report contiguous port numbers to the host. Section 5.3.11 Register 0A Section 5.3.12 Register 0B ‘1’ = Port Re-Map mode. The mode enables remapping via the registers defined below. Section 5.3.43 Register FB Section 5.3.44 Register FC