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USB4604

USB 2.0 HSIC Hi-Speed 4-Port Hub Controller

PRODUCT FEATURES

Datasheet

Highlights

- Hub Controller IC with 4 downstream ports
- High-Speed Inter-Chip (HSIC) support
  - Upstream port selectable between HSIC or USB 2.0
- USB-IF Battery Charger revision 1.2 support on up & downstream ports (DCP, CDP, SDP)
- Battery charging support for Apple® devices
- **FlexConnect**: Downstream port 1 able to swap with upstream port, allowing master capable devices to control other devices on the hub
- USB to I²C™/SPI bridge endpoint support
- USB Link Power Management (LPM) support
- SUSPEND pin for remote wakeup indication to host
- Start Of Frame (SOF) synchronized clock output pin
- Vendor Specific Messaging (VSM) support
- Enhanced OEM configuration options available through OTP or SMBus Slave Port
- Flexible power rail support
  - VBUS or VBAT only operation
  - 3.3V only operation
  - VBAT + 1.8V operation
  - 3.3V + 1.8V operation
- 48-pin (7x7mm) SQFN, RoHS compliant package

Target Applications

- LCD monitors and TVs
- Multi-function USB peripherals
- PC mother boards
- Set-top boxes, DVD players, DVR/PVR
- Printers and scanners
- PC media drive bay
- Portable hub boxes
- Mobile PC docking
- Embedded systems

Additional Features

- **MultiTRAK**™
  - Dedicated Transaction Translator per port
- **PortMap**
  - Configurable port mapping and disable sequencing
- **PortSwap**
  - Configurable differential intra-pair signal swapping
- **PHYBoost**™
  - Programmable USB transceiver drive strength for recovering signal integrity
- **VariSense**™
  - Programmable USB receiver sensitivity
- Low power operation
- Full Power Management with individual or ganged power control of each downstream port
- Built-in Self-Powered or Bus-Powered internal default settings provide flexibility in the quantity of USB expansion ports utilized without redesign
- Supports “Quad Page” configuration OTP flash
  - Four consecutive 200 byte configuration pages
- Fully integrated USB termination and Pull-up/Pull-down resistors
- On-chip Power On Reset (POR)
- Internal 3.3V and 1.2V voltage regulators
- On Board 24MHz Crystal Driver, Resonator, or External 24MHz clock input
- USB host/device speed indicator. Per-port 3-color LED drivers indicate the speed of USB host and device connection - hi-speed (480 Mbps), full-speed (12 Mbps), low-speed (1.5 Mbps)
- Environmental
  - Commercial temperature range support (0ºC to 70ºC)
  - Industrial temperature range support (-40ºC to 85ºC)

Order Number(s):

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
USB4604-1080HN (Hub Controller Enabled)	0°C to +70°C	48-pin SQFN
USB4604-1070HN (Hub Controller Disabled)		
USB4604-1080HN-TR (Hub Controller Enabled)	0°C to +70°C	48-pin SQFN (Tape & Reel)
USB4604-1070HN-TR (Hub Controller Disabled)		
USB4604i-1080HN (Hub Controller Enabled)	-40°C to +85°C	48-pin SQFN
USB4604i-1070HN (Hub Controller Disabled)		
USB4604i-1080HN-TR (Hub Controller Enabled)	-40°C to +85°C	48-pin SQFN (Tape & Reel)
USB4604i-1070HN-TR (Hub Controller Disabled)		

This product meets the halogen maximum concentration values per IEC61249-2-21

The table above represents valid part numbers at the time of printing and may not represent parts that are currently available. For the latest list of valid ordering numbers for this product, please contact the nearest sales office.

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Chapter 1 General Description

The USB4604 is a low-power, OEM configurable, MTT (Multi-Transaction Translator) USB 2.0 hub controller with 4 downstream ports and advanced features for embedded USB applications. The USB4604 is fully compliant with the USB 2.0 Specification, USB 2.0 Link Power Management Addendum, High-Speed Inter-Chip (HSIC) USB Electrical Specification Revision 1.0, and will attach to an upstream port as a Full-Speed hub or as a Full-/Hi-Speed hub. The 4-port hub supports Low-Speed, Full-Speed, and Hi-Speed (if operating as a Hi-Speed hub) downstream devices on all of the enabled downstream (non-HSIC) ports. HSIC ports support only Hi-Speed operation.

The USB4604 has been specifically optimized for embedded systems where high performance, and minimal BOM costs are critical design requirements. Standby mode power has been minimized and reference clock inputs can be aligned to the customer's specific application. Flexible power rail options ease integration into energy efficient designs by allowing the USB4604 to be powered in a single-source (VBUS, VBAT, 3.3V) or a dual-source (VBAT + 1.8, 3.3V + 1.8) configuration. Additionally, all required resistors on the USB ports are integrated into the hub, including all series termination and pull-up/pull-down resistors on the D+ and D– pins.

The USB4604 supports both upstream battery charger detection and downstream battery charging. The USB4604 integrated battery charger detection circuitry supports the USB-IF Battery Charging (BC1.2) detection method and most Apple devices. These circuits are used to detect the attachment and type of a USB charger and provide an interrupt output to indicate charger information is available to be read from the device's status registers via the serial interface. The USB4604 provides the battery charging handshake and supports the following USB-IF BC1.2 charging profiles:

- DCP: Dedicated Charging Port (Power brick with no data)
- CDP: Charging Downstream Port (1.5A with data)
- SDP: Standard Downstream Port (0.5A with data)
- Custom profiles loaded via SMBus or OTP

The USB4604 provides an additional USB endpoint dedicated for use as a USB to I^2C/SPI interface, allowing external circuits or devices to be monitored, controlled, or configured via the USB interface. Additionally, the USB4604 includes many powerful and unique features such as:

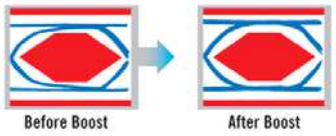
FlexConnect, which provides flexible connectivity options. The USB4604's downstream port 1 can be swapped with the upstream port, allowing master capable devices to control other devices on the hub.

MultiTRAK™ Technology, which utilizes a dedicated Transaction Translator (TT) per port to maintain consistent full-speed data throughput regardless of the number of active downstream connections. MultiTRAK™ outperforms conventional USB 2.0 hubs with a single TT in USB full-speed data transfers.

PortMap, which provides flexible port mapping and disable sequences. The downstream ports of a USB4604 hub can be reordered or disabled in any sequence to support multiple platform designs with minimum effort. For any port that is disabled, the USB4604 hub controllers automatically reorder the remaining ports to match the USB host controller's port numbering scheme.

PortSwap, which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.

PHYBoost, which provides programmable levels of Hi-Speed USB signal drive strength in the downstream port transceivers. PHYBoost attempts to restore USB signal integrity in a compromised system environment. The graphic on the right shows an example of Hi-Speed USB eye diagrams before and after PHYBoost signal integrity restoration.



VariSense, which controls the USB receiver sensitivity enabling programmable levels of USB signal receive sensitivity. This capability allows operation in a sub-optimal system environment, such as when a captive USB cable is used.

The USB4604 is available in commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature range versions.

As shown in the ordering code matrix, two USB4604 firmware revisions are available: “-1080” and “-1070”. The -1080 version enables the internal Hub Controller, while the -1070 version disables it. There are no additional differences between these two versions.

The Hub Controller adds advanced functionality to the USB4604 by enabling the host to send commands directly to it via the upstream USB connection. Commands to the Hub Controller must be sent to the virtual 5th port in the hub. The following functions can be controlled via commands through the Hub Controller:

- USB to SMBus Bridging: The host can send commands through USB to any device connected to the hub through the SMBus.
- USB to UART Bridging: The host can send commands through SUB to any device connected to the hub through the UART.
- GPIO Control: The GPIOs on the hub can be dynamically configured and controlled by the host.
- OTP Programming: Permanent customer configurations can be loaded to the One Time Programmable memory.

1.1 Block Diagram

Figure 1.1 details the internal block diagram of the USB4604.

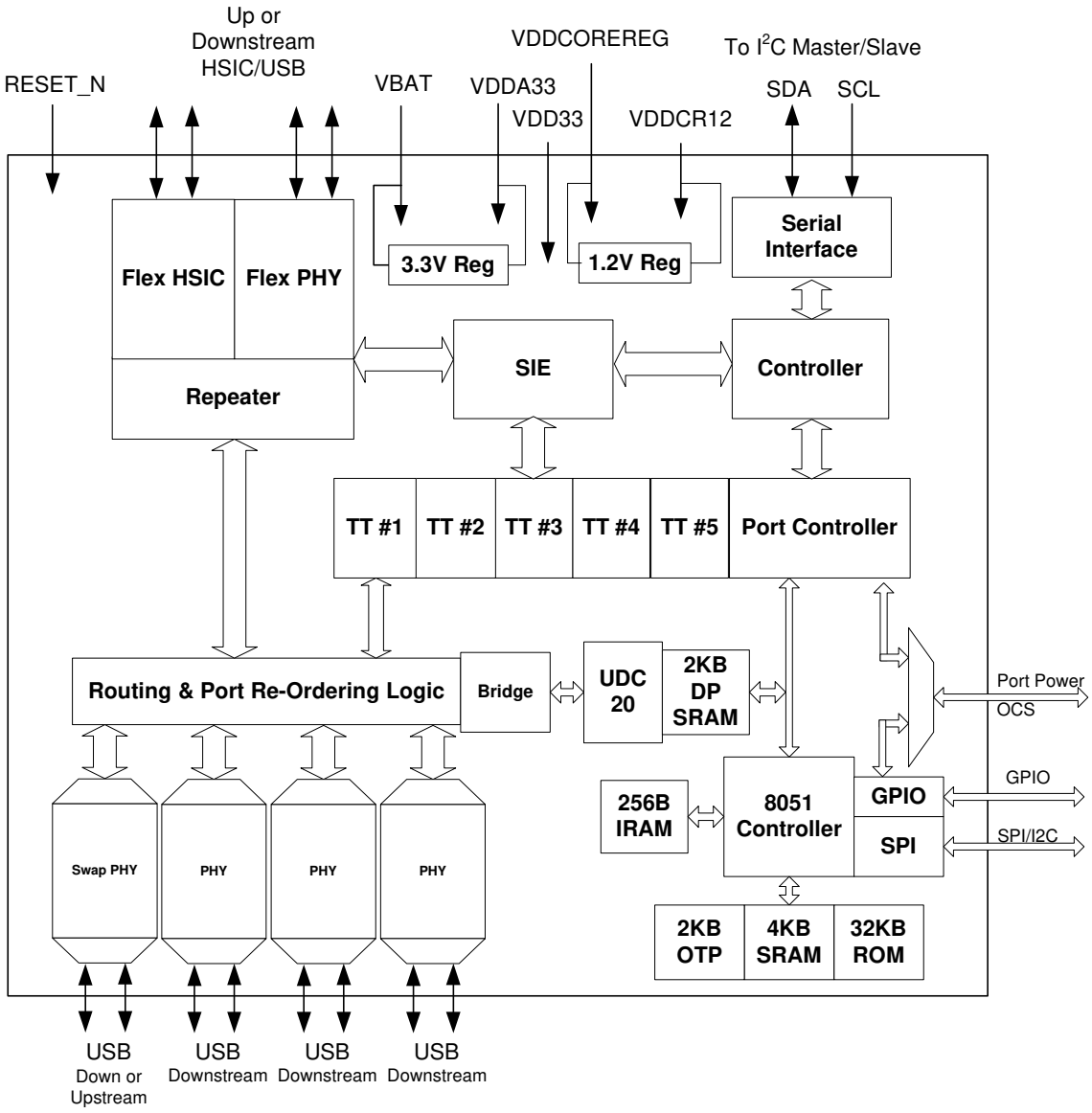


Figure 1.1 System Block Diagram

Chapter 2 Acronyms and Definitions

2.1 Acronyms

EOP: End of Packet

EP: Endpoint

FS: Full-Speed

GPIO: General Purpose I/O (that is input/output to/from the device)

HS: Hi-Speed

HSOS: High Speed Over Sampling

HSIC: High-Speed Inter-Chip

I^2C®: Inter-Integrated Circuit

LS: Low-Speed

OTP: One Time Programmable

PCB: Printed Circuit Board

PCS: Physical Coding Sublayer

PHY: Physical Layer

SMBus: System Management Bus

UUID: Universally Unique IDentification

2.2 Reference Documents

1. *UNICODE UTF-16LE For String Descriptors* USB Engineering Change Notice, December 29th, 2004, http://www.usb.org
2. *Universal Serial Bus Specification*, Revision 2.0, April 27th, 2000, http://www.usb.org
3. *Battery Charging Specification*, Revision 1.2, Dec. 07, 2010, http://www.usb.org
4. *High-Speed Inter-Chip USB Electrical Specification*, Version 1.0, Sept. 23, 2007, http://www.usb.org
5. *I^2C-Bus Specification*, Version 1.1, http://www.nxp.com
6. *System Management Bus Specification*, Version 1.0, http://smbus.org/specs

Chapter 3 Pin Descriptions

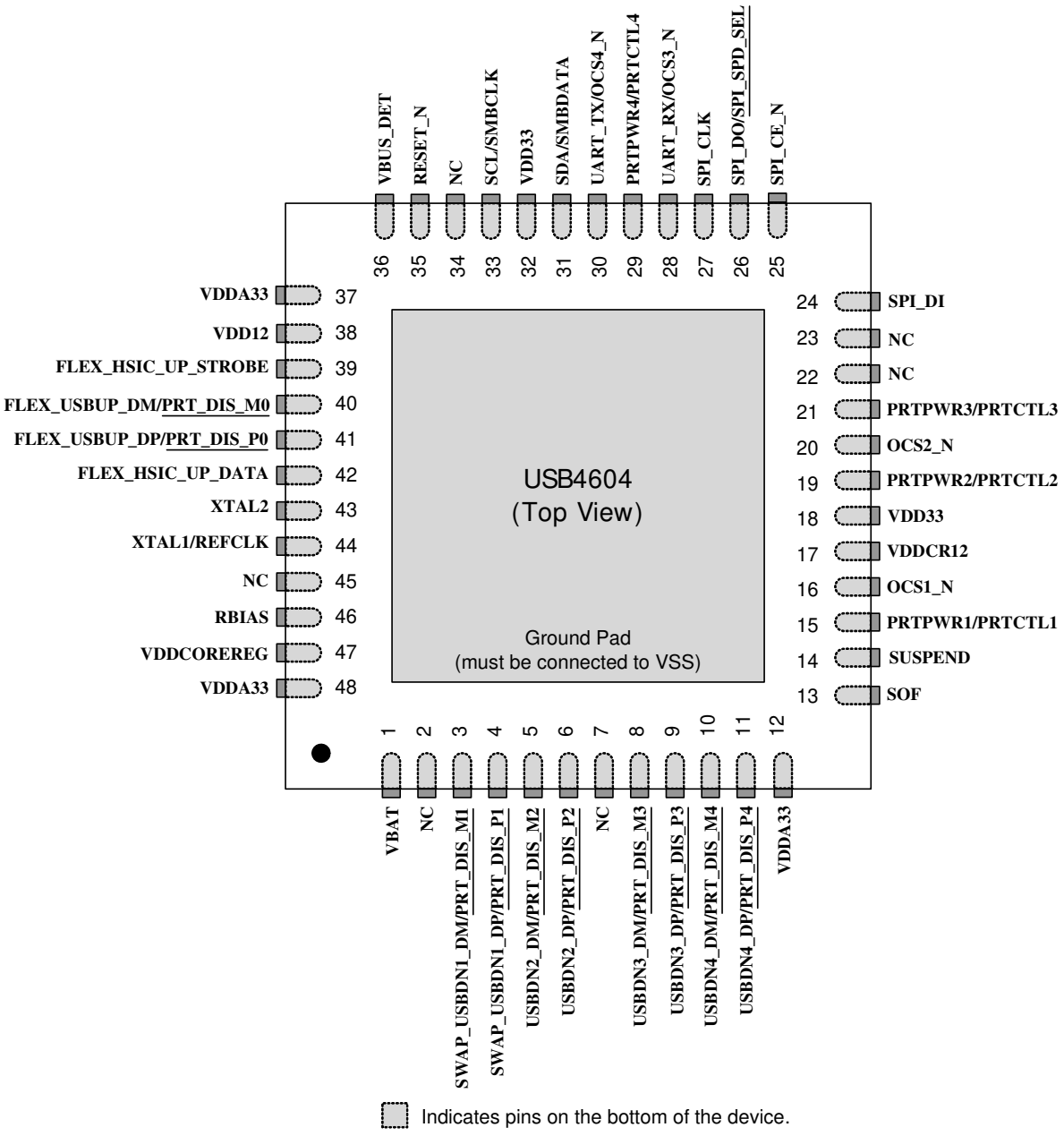


Figure 3.1 48-SQFN Pin Assignments

3.1 Pin Descriptions

This section provides a detailed description of each pin. The signals are arranged in functional groups according to their associated interface.

The "_N" symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, RESET_N indicates that the reset signal is active low. When "_N" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of "active low" and "active high" signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

Note: The buffer type for each signal is indicated in the BUFFER TYPE column of Table 3.1. A description of the buffer types is provided in Section 3.3.

Note: Compatibility with the UCS100x family of USB port power controllers requires the UCS100x be connected on Port 1 of the USB4604. Additionally, both PRTPWR1 and OCS1_N must be pulled high at Power-On Reset (POR).

Table 3.1 Pin Descriptions

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
USB/HSIC INTERFACES				
1	Upstream USB D+ (Flex Port 0)	FLEX_USBUP_DP	AIO	Upstream USB Port 0 D+ data signal. See Note 3.2. **Note:** The upstream Port 0 signals can be optionally swapped with the downstream Port 1 signals.
	Port 0 D+ Disable Configuration Strap	PRT_DIS_P0	IS	This strap is used in conjunction with PRT_DIS_M0 to disable USB Port 0. 0 = Port 0 D+ Enabled 1 = Port 0 D+ Disabled **Note:** Both PRT_DIS_P0 and PRT_DIS_M0 must be tied to VDD33 at reset to place Port 0 into HSIC mode. See Note 3.3 for more information on configuration straps.

Table 3.1 Pin Descriptions (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
	Upstream USB D- (Flex Port 0)	FLEX_USBUP_DM	AIO	Upstream USB Port 0 D- data signal. See Note 3.2. **Note:** The upstream Port 0 signals can be optionally swapped with the downstream Port 1 signals.
1	Port 0 D- Disable Configuration Strap	PRT_DIS_M0	IS	This strap is used in conjunction with PRT_DIS_P0 to disable USB Port 0. 0 = Port 0 D- Enabled 1 = Port 0 D- Disabled **Note:** Both PRT_DIS_P0 and PRT_DIS_M0 must be tied to VDD33 at reset to place Port 0 into HSIC mode. See Note 3.3 for more information on configuration straps.
1	Upstream HSIC Data (Flex Port 0)	FLEX_HSIC_UP_DATA	HSIC	Upstream HSIC Port 0 DATA signal. See Note 3.2. **Note:** The upstream Port 0 signals can be optionally swapped with the downstream Port 1 signals.
1	Upstream HSIC Strobe (Flex Port 0)	FLEX_HSIC_UP_STROBE	HSIC	Upstream HSIC Port 0 STROBE signal. See Note 3.2. **Note:** The upstream Port 0 signals can be optionally swapped with the downstream Port 1 signals.
	Downstream USB D+ (Swap Port 1)	SWAP_USBDN1_DP	AIO	Downstream USB Port 1 D+ data signal. **Note:** The downstream Port 1 signals can be optionally swapped with the upstream Port 0 signals.
1	Port 1 D+ Disable Configuration Strap	PRT_DIS_P1	IS	This strap is used in conjunction with PRT_DIS_M1 to disable USB Port 1. 0 = Port 1 D+ Enabled 1 = Port 1 D+ Disabled **Note:** Both PRT_DIS_P1 and PRT_DIS_M1 must be tied to VDD33 at reset to disable the associated port. See Note 3.3 for more information on configuration straps.

Table 3.1 Pin Descriptions (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
	Downstream USB D- (Swap Port 1)	SWAP_USBDN1_DM	AIO	Downstream USB Port 1 D- data signal. **Note:** The downstream Port 1 signals can be optionally swapped with the upstream Port 0 signals.
1	Port 1 D- Disable Configuration Strap	PRT_DIS_M1	IS	This strap is used in conjunction with PRT_DIS_P1 to disable USB Port 1. 0 = Port 1 D- Enabled 1 = Port 1 D- Disabled **Note:** Both PRT_DIS_P1 and PRT_DIS_M1 must be tied to VDD33 at reset to disable the associated port. See Note 3.3 for more information on configuration straps.
	Downstream USB D+ (Port 2)	USBDN2_DP	AIO	Downstream USB Port 2 D+ data signal.
1	Port 2 D+ Disable Configuration Strap	PRT_DIS_P2	IS	This strap is used in conjunction with PRT_DIS_M2 to disable USB Port 2. 0 = Port 2 D+ Enabled 1 = Port 2 D+ Disabled **Note:** Both PRT_DIS_P2 and PRT_DIS_M2 must be tied to VDD33 at reset to disable the associated port. See Note 3.3 for more information on configuration straps.
	Downstream USB D- (Port 2)	USBDN2_DM	AIO	Downstream USB Port 2 D- data signal.
1	Port 2 D- Disable Configuration Strap	PRT_DIS_M2	IS	This strap is used in conjunction with PRT_DIS_P2 to disable USB Port 2. 0 = Port 2 D- Enabled 1 = Port 2 D- Disabled **Note:** Both PRT_DIS_P2 and PRT_DIS_M2 must be tied to VDD33 at reset to disable the associated port. See Note 3.3 for more information on configuration straps.

Table 3.1 Pin Descriptions (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Downstream USB D+ (Port 3)	USBDN3_DP	AIO	Downstream USB Port 3 D+ data signal.
	Port 3 D+ Disable Configuration Strap	PRT_DIS_P3	IS	This strap is used in conjunction with PRT_DIS_M3 to disable USB Port 3. 0 = Port 3 D+ Enabled 1 = Port 3 D+ Disabled **Note:** Both PRT_DIS_P3 and PRT_DIS_M3 must be tied to VDD33 at reset to disable the associated port. See Note 3.3 for more information on configuration straps.
1	Downstream USB D- (Port 3)	USBDN3_DM	AIO	Downstream USB Port 3 D- data signal.
	Port 3 D- Disable Configuration Strap	PRT_DIS_M3	IS	This strap is used in conjunction with PRT_DIS_P3 to disable USB Port 3. 0 = Port 3 D- Enabled 1 = Port 3 D- Disabled **Note:** Both PRT_DIS_P3 and PRT_DIS_M3 must be tied to VDD33 at reset to disable the associated port. See Note 3.3 for more information on configuration straps.
1	Downstream USB D+ (Port 4)	USBDN4_DP	AIO	Downstream USB Port 4 D+ data signal.
	Port 4 D+ Disable Configuration Strap	PRT_DIS_P4	IS	This strap is used in conjunction with PRT_DIS_M4 to disable USB Port 4. 0 = Port 4 D+ Enabled 1 = Port 4 D+ Disabled **Note:** Both PRT_DIS_P4 and PRT_DIS_M4 must be tied to VDD33 at reset to disable the associated port. See Note 3.3 for more information on configuration straps.

Table 3.1 Pin Descriptions (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Downstream USB D- (Port 4)	USBDN4_DM	AIO	Downstream USB Port 4 D- data signal.
	Port 4 D- Disable Configuration Strap	PRT_DIS_M4	IS	This strap is used in conjunction with PRT_DIS_P4 to disable USB Port 4. 0 = Port 4 D- Enabled 1 = Port 4 D- Disabled **Note:** Both PRT_DIS_P4 and PRT_DIS_M4 must be tied to VDD33 at reset to disable the associated port. See Note 3.3 for more information on configuration straps.
I²C/SMBUS INTERFACE				
1	I²C Serial Clock Input	SCL	I_SMB	I²C serial clock input
	SMBus Clock	SMBCLK	I_SMB	SMBus serial clock input
1	I²C Serial Data	SDA	IS/OD8	I²C bidirectional serial data
	SMBus Serial Data	SMBDATA	IS/OD8	SMBus bidirectional serial data
SPI MASTER INTERFACE				
1	SPI Chip Enable Output	SPI_CE_N	O12	Active-low SPI chip enable output. **Note:** If the SPI is enabled, this pin will be driven high in powerdown states.
1	SPI Clock Output	SPI_CLK	O12	SPI clock output
1	SPI Data Output	SPI_DO	O12	SPI data output
	SPI Speed Select Configuration Strap	SPI_SPD_SEL	IS (PD)	This strap is used to select the speed of the SPI. 0 = 30MHz (default) 1 = 60MHz **Note:** If the latched value on reset is 1, this pin is tri-stated when the chip is in the suspend state. If the latched value on reset is 0, this pin is driven low during a suspend state. See Note 3.3 for more information on configuration straps.
1	SPI Data Input	SPI_DI	IS (PD)	SPI data input

Table 3.1 Pin Descriptions (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
MISC.				
1	Port 1 Over-Current Sense Input	OCS1_N	IS (PU)	This active-low signal is input from an external current monitor to indicate an over-current condition on USB Port 1.
1	Port 2 Over-Current Sense Input	OCS2_N	IS (PU)	This active-low signal is input from an external current monitor to indicate an over-current condition on USB Port 2.
1	UART Receive Input	UART_RX	IS	Internal UART receive input **Note:** This is a 3.3V signal. For RS232 operation, an external 12V translator is required.
	Port 3 Over-Current Sense Input	OCS3_N	IS (PU)	This active-low signal is input from an external current monitor to indicate an over-current condition on USB Port 3.
1	UART Transmit Output	UART_TX	O8	Internal UART transmit output **Note:** This is a 3.3V signal. For RS232 operation, an external 12V driver is required.
	Port 4 Over-Current Sense Input	OCS4_N	IS (PU)	This active-low signal is input from an external current monitor to indicate an over-current condition on USB Port 4.
1	System Reset Input	RESET_N	I_RST	This active-low signal allows external hardware to reset the device. **Note:** The active-low pulse must be at least 5us wide. Refer to Section 8.4.2, "External Chip Reset (RESET_N)," on page 46 for additional information.
1	Crystal Input	XTAL1	ICLK	External 24 MHz crystal input
	Reference Clock Input	REFCLK	ICLK	Reference clock input. The device may be alternatively driven by a single-ended clock oscillator. When this method is used, XTAL2 should be left unconnected.
1	Crystal Output	XTAL2	OCLK	External 24 MHz crystal output
1	External USB Transceiver Bias Resistor	RBIAS	AI	A 12.0kΩ (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings.

Table 3.1 Pin Descriptions (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Suspend Output	SUSPEND	PU	This signal is used to indicate that the entire hub has entered the USB suspend state and that VBUS current consumption should be reduced in accordance with the USB specification. Refer to Section 8.6, "Suspend (SUSPEND)," on page 47 for additional information. **Note:** SUSPEND must be enabled via the Protouch configuration tool.
1	SOF Synchronized 8KHz Clock Output	SOF	O8	This signal outputs an 8KHz clock synchronized with the USB Host SOF. **Note:** SOF output is controlled via the SOF_ENABLE bit in the UTIL_CONFIG1 register
1	Detect Upstream VBUS Power	VBUS_DET	IS	Detects state of upstream bus power. When designing a detachable hub, this pin must be connected to the VBUS power pin of the upstream USB port through a resistor divider (50kΩ by 100kΩ) to provide 3.3V. For self-powered applications with a permanently attached host, this pin must be connected to either 3.3V or 5.0V through a resistor divider to provide 3.3V. In embedded applications, VBUS_DET may be controlled (toggled) when the host desires to renegotiate a connection without requiring a full reset of the device.
1	Port 1 Power Output	PRTPWR1	O8	Enables power to a downstream USB device attached to Port 1. 0 = Power disabled on downstream Port 1 1 = Power enabled on downstream Port 1
	Port 1 Control	PRTCTL1	OD8/IS (PU)	When configured as PRTCTL1, this pin functions as both the Port 1 power enable output (PRTPWR1) and the Port 1 over-current sense input (OCS1_N). Refer to the PRTPWR1 and OCS1_N descriptions for additional information.
1	Port 2 Power Output	PRTPWR2	O8	Enables power to a downstream USB device attached to Port 2. 0 = Power disabled on downstream Port 2 1 = Power enabled on downstream Port 2
	Port 2 Control	PRTCTL2	OD8/IS (PU)	When configured as PRTCTL2, this pin functions as both the Port 2 power enable output (PRTPWR2) and the Port 2 over-current sense input (OCS2_N). Refer to the PRTPWR2 and OCS2_N descriptions for additional information.

Table 3.1 Pin Descriptions (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Port 3 Power Output	PRTPWR3	O8	Enables power to a downstream USB device attached to Port 3. 0 = Power disabled on downstream Port 3 1 = Power enabled on downstream Port 3
	Port 3 Control	PRTCTL3	OD8/IS (PU)	When configured as PRTCTL3, this pin functions as both the Port 3 power enable output (PRTPWR3) and the Port 3 over-current sense input (OCS3_N). Refer to the PRTPWR3 and OCS3_N descriptions for additional information.
1	Port 4 Power Output	PRTPWR4	O8	Enables power to a downstream USB device attached to Port 4. 0 = Power disabled on downstream Port 4 1 = Power enabled on downstream Port 4
	Port 4 Control	PRTCTL4	OD8/IS (PU)	When configured as PRTCTL4, this pin functions as both the Port 4 power enable output (PRTPWR4) and the Port 4 over-current sense input (OCS4_N). Refer to the PRTPWR4 and OCS4_N descriptions for additional information.
6	No Connect	NC	-	These pins must be left floating for normal device operation.
POWER				
1	Battery Power Supply Input	VBAT	P	Battery power supply input. When VBAT is connected directly to a +3.3V supply from the system, the internal +3.3V regulator runs in dropout and regulator power consumption is eliminated. A 4.7 µF (<1 Ω ESR) capacitor to ground is required for regulator stability. The capacitor should be placed as close as possible to the device. Refer to Chapter 4, "Power Connections," on page 23 for power connection information.
3	+3.3V Analog Power Supply	VDDA33	P	+3.3V analog power supply. A 1.0 µF (<1 Ω ESR) capacitor to ground is required for regulator stability. The capacitor should be placed as close as possible to the device. Refer to Chapter 4, "Power Connections," on page 23 for power connection information.
2	+3.3V Power Supply	VDD33	P	+3.3V power supply. These pins must be connected to VDDA33. Refer to Chapter 4, "Power Connections," on page 23 for power connection information.

Table 3.1 Pin Descriptions (continued)

NUM PINS	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	+1.8-3.3V Core Power Supply Input	VDDCOREREG	P	+1.8-3.3V core power supply input to internal +1.2V regulator. This pin may be connected to VDD33 for single supply applications when VBAT equals +3.3V. Running in a dual supply configuration with VDDCOREREG at a lower voltage, such as +1.8V, may reduce overall system power consumption. In dual supply configurations, a 4.7 µF (<1 Ω ESR) capacitor to ground is required for regulator stability. The capacitor should be placed as close as possible to the device. Refer to Chapter 4, "Power Connections," on page 23 for power connection information.
1	+1.2V Core Power Supply	VDDCR12	P	+1.2V core power supply. In single supply applications or dual supply applications where 1.2V is not used, a 1.0 µF (<1 Ω ESR) capacitor to ground is required for regulator stability. The capacitor should be placed as close as possible to the device. Refer to Chapter 4, "Power Connections," on page 23 for power connection information.
1	+1.2V HSIC Power Supply Input	VDD12	P	+1.2V HSIC power supply input. Refer to Chapter 4, "Power Connections," on page 23 for power connection information.
Exposed Pad on package bottom (Figure 3.1)	Ground	VSS	P	Common ground. This exposed pad must be connected to the ground plane with a via array.

Note 3.2 When the device is configured to enable the HSIC upstream port, the USB Product ID (PID) will be 4604. When the device is configured to enable the USB upstream port, the USB PID will be 4504.

Note 3.3 Configuration strap values are latched on Power-On Reset (POR) and the rising edge of RESET_N (external chip reset). Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to Section 6.3, "Device Configuration Straps," on page 32 for additional information.

3.2 Pin Assignments

Table 3.2 48-SQFN Package Pin Assignments

PIN NUM	PIN NAME	PIN NUM	PIN NAME
1	VBAT	25	SPI_CE_N
2	NC	26	SPI_DO/SPI_SPD_SEL
3	USBDN1_DM/PRT_DIS_M1	27	SPI_CLK
4	USBDN1_DP/PRT_DIS_P1	28	UART_RX/OCS3_N
5	USBDN2_DM/PRT_DIS_M2	29	PRTPWR4/PRTCTL4
6	USBDN2_DP/PRT_DIS_P2	30	UART_TX/OCS4_N
7	NC	31	SDA/SMBDATA
8	USBDN3_DM/PRT_DIS_M3	32	VDD33
9	USBDN3_DP/PRT_DIS_P3	33	SCL/SMBCLK
10	USBDN4_DM/PRT_DIS_M4	34	NC
11	USBDN4_DP/PRT_DIS_P4	35	RESET_N
12	VDDA33	36	VBUS_DET
13	SOF	37	VDDA33
14	SUSPEND	38	VDD12
15	PRTPWR1/PRTCTL1/	39	FLEX_HSIC_UP_STROBE
16	OCS1_N	40	FLEX_USBUP_DM/PRT_DIS_M0
17	VDDCR12	41	FLEX_USBUP_DP/PRT_DIS_P0
18	VDD33	42	FLEX_HSIC_UP_DATA
19	PRTPWR2/PRTCTL2/	43	XTAL2
20	OCS2_N	44	XTAL1/REFCLK
21	PRTPWR3/PRTCTL3	45	NC
22	NC	46	RBIAS
23	NC	47	VDDCOREREG
24	SPI_DI	48	VDDA33

3.3 Buffer Type Descriptions

Table 3.3 Buffer Types

BUFFER TYPE	DESCRIPTION
IS	Schmitt-triggered input
I_RST	Reset Input
I_SMB	I^2C/SMBus Clock Input
O8	Output with 8 mA sink and 8 mA source
OD8	Open-drain output with 8 mA sink
O12	Output with 12 mA sink and 12 mA source
OD12	Open-drain output with 12 mA sink
HSIC	*High-Speed Inter-Chip (HSIC) USB Specification, Version 1.0* compliant input/output
PU	50 µA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50 µA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
AIO	Analog bi-directional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power pin

Chapter 4 Power Connections

4.1 Integrated Power Regulators

The integrated 3.3V and 1.2V power regulators provide flexibility to the system in providing power the device. Several different configurations are allowed in order to align the power structure to supplies available in the system.

The regulators are controlled by RESET_N. When RESET_N is brought high, the 3.3V regulator will turn on. When RESET_N is brought low the 3.3V regulator will turn off.

4.1.1 3.3V Regulator

The device has an integrated regulator to convert from VBAT to 3.3V.

4.1.2 1.2V Regulator

The device has an integrated regulator to convert from a variable voltage input on VDDCOREREG to 1.2V. The 1.2V regulator is tolerant to the presence of low voltage (~0V) on the VDDCOREREG pin in order to support system power solutions where a supply is not always present in low power states.

The 1.2V regulator supports an input voltage range consistent with a 1.8V input in order to reduce power consumption in systems which provide multiple power supply levels. In addition, the 1.2V regulator supports an input voltage up to 3.3V for systems which provide only a single power supply. The device will support operation where the 3.3V regulator output can drive the 1.2V regulator input such that VBAT is the only required supply.

4.2 Power Configurations

The device supports operation with no back current when power is connected in each of the following configurations. Power connection diagrams for these configurations are included in Section 4.3, "Power Connection Diagrams," on page 25.

4.2.1 Single Supply Configurations

4.2.1.1 VBAT Only

VBAT must be tied to the VBAT system supply. VDD33, VDDA33, and VDDCOREREG must be tied together on the board. In this configuration the 3.3V and 1.2V regulators will be active. For HSIC operation, VDD12 must be tied to VDDCR12.

4.2.1.2 3.3V Only

VBAT must be tied to the 3.3V system supply. VDD33, VDDA33, and VDDCOREREG must be tied together on the board. In this configuration the 3.3V regulator will operate in dropout mode and the 1.2V regulator will be active. For HSIC operation, VDD12 must be tied to VDDCR12.

4.2.2 Dual Supply Configurations

4.2.2.1 VBAT + 1.8V

VBAT must be tied to the VBAT system supply. VDDCOREREG must be tied to the 1.8V system supply. In this configuration, the 3.3V regulator and the 1.2V regulator will be active. For HSIC operation, VDD12 must be tied to VDDCR12.

4.2.2.2 3.3V + 1.8V

VBAT must be tied to the 3.3V system supply. VDDCOREREG must be tied to the 1.8V system supply. In this configuration the 3.3V regulator will operate in dropout mode and the 1.2V regulator will be active. For HSIC operation, VDD12 must be tied to VDDCR12.

4.3 Power Connection Diagrams

Figure 4.1 illustrates the power connections for the USB4604 with various power supply configurations.

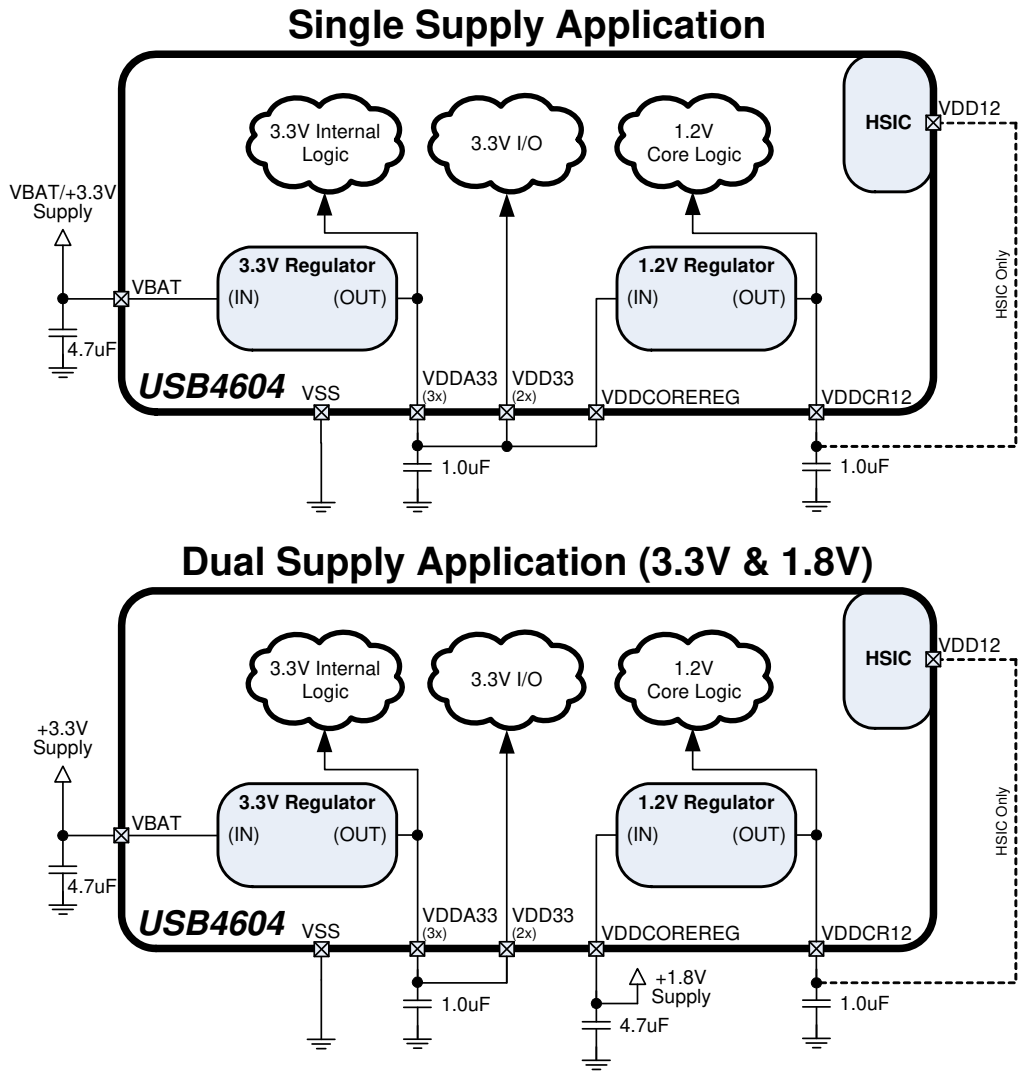


Figure 4.1 Power Connections

Note: To achieve the lowest power possible, tie the VDD12 pin to VDD12CR.