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USB4640/USB4640i

High-Speed Inter-Chip (HSIC) USB 2.0 Hub and Flash Media Controller

PRODUCT FEATURES

Datasheet

General Description

The SMSC USB4640/USB4640i is a Hi-Speed HSIC USB hub and card reader combo solution with an upstream port that is compliant to HSIC 1.0 (supplement to the *USB 2.0 Specification*). The two downstream ports are compliant with the *USB 2.0 Specification*.

High-Speed Inter-Chip (HSIC) is a digital interconnect bus that enables the use of USB technology as a low-power chip-to-chip interconnect at speeds up to 480 Mb/s. The HSIC interface is an industry standard 2-pin digital interface which uses standard USB software. The USB4640/USB4640i provides an ultra fast interface between an HSIC enabled host and several popular flash media formats. The controller allows read/write capability to flash media from the following families:

- Secure Digital™ (SD)
- MultiMediaCard™ (MMC)
- Memory Stick® (MS)
- xD-Picture Card™ (xD)[1]

The USB4640/USB4640i combo solution leverages SMSC's innovative technology that delivers industry-leading data throughput in mixed-speed USB environments. Average sustained transfer rates exceeding 35 MB/s are possible[2].

Highlights

- Upstream HSIC port and 2 exposed Hi-Speed USB 2.0 downstream ports for external peripheral expansion
- Dedicated flash media reader internally attached to a 3rd downstream port of the hub as a USB compound device
  - single or multiplexed flash media reader interface
- **PortMap**
  - Flexible port mapping and disable sequencing
- **PortSwap**
  - Programmable USB differential-pair pin locations ease PCB design by aligning USB signal lines directly to connectors
- **PHYBoost**
  - Programmable USB signal drive strength for recovering signal integrity using 4-level driving strength resolution

Features

- Compliance with the following flash media card specifications SD 2.0; MMC 4.2; MS 1.43; MS-Pro 1.02; MS-Pro-HG 1.01; MS-Duo 1.10; and xD 1.2
- Low-power digital HSIC interface offers a replacement for onboard host and device connection for analog USB bus cable
- HSIC interface enables printers, mobile PCs, ultra-mobile PCs, and cell phone products to reduce the total power budget
- HSIC interface provides use of USB connectivity and compatibility with existing USB drivers and software
- External 1.2 V reference allows upstream/downstream HSIC links to use the same voltage reference
- Supports a single external 3.3 V supply source; internal regulators provide 1.8 V internal core voltage for additional bill of materials and power savings
- The hub transaction translator (TT) supports Full-Speed and Low-Speed peripheral operation
- 9 KB RAM | 64 KB on-chip ROM
- Enhanced EMI rejection and ESD protection performance
- Hub and flash media reader/writer configuration from a single source:
  - Configures internal code using an external I^2C EEPROM
  - Supports external code using an SPI Flash EEPROM
  - Customizable vendor ID, product ID, and language ID if using an external EEPROM
- Up to 9 configurable GPIOs for special functions
- The USB4640 supports the commercial temperature range of 0°C to +70°C
- The USB4640i supports the industrial temperature range of -40°C to +85°C
- 48-pin QFN (7 x 7 mm) lead-free, RoHS compliant package

Applications

- 3G/4G handsets, smartphones, cell phones, and other mobile devices
- Desktop and mobile PCs
- Printers
- GPS navigation systems
- Media players/viewers
- Consumer A/V
- Set-top boxes
- Industrial products

1. Obtain user license from the xD-Picture Card License Office.
2. Host and media dependent.

Order Number(s):

USB4640/USB4640i-HZH-xx for 48-pin, QFN lead-free RoHS compliant package

USB4640/USB4640i-HZH-TR-xx for 48-pin, QFN lead-free RoHS compliant tape and reel package

"XX" in the order number indicates the internal ROM firmware revision level. Please contact SMSC for more information.

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.

Conventions

Within this manual, the following abbreviations and symbols are used to improve readability.

Example	Description
BIT	Name of a single bit within a field
FIELD.BIT	Name of a single bit (BIT) in FIELD
x…y	Range from x to y, inclusive
BITS[m:n]	Groups of bits from m to n, inclusive
PIN	Pin Name
zzzzb	Binary number (value zzzz)
0xzzz	Hexadecimal number (value zzz)
zzh	Hexadecimal number (value zz)
rsvd	Reserved memory location. Must write 0, read value indeterminate
N/A	Not applicable
`code`	Instruction code, or API function or parameter
Multi Word Name	Used for multiple words that are considered a single unit, such as: *Resource Allocate* message, or *Connection Label*, or *Decrement Stack Pointer* instruction.
Section Name	Section or Document name.
$\overline{\text{VAL}}$	Over-bar indicates active low pin or register bit
x	Don't care
<Parameter>	<> indicate a Parameter is optional or is only used under some conditions
{,Parameter}	Braces indicate Parameter(s) that repeat one or more times.
[Parameter]	Brackets indicate a nested Parameter. This Parameter is not real and actually decodes into one or more real parameters.

Table of Contents

List of Tables

List of Figures

Chapter 1 Overview

The USB4640/USB4640i is a Hi-Speed HSIC USB hub and card reader combo solution with an upstream port compliant to the *High-Speed Inter-Chip USB Electrical Specification Revision 1.0* [2]. The two downstream ports are USB 2.0 compliant, and the dedicated flash media reader/writer is internally attached to a 3rd downstream port as a USB compound device.

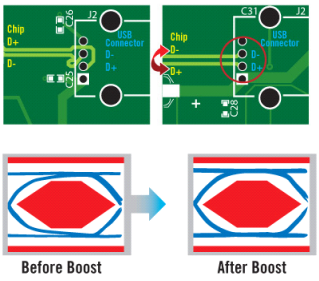
High-Speed Inter-Chip (HSIC) is a digital interconnect bus that enables the use of USB technology as a low-power chip-to-chip interconnect at speeds up to 480 Mb/s (see the *High-Speed Inter-Chip USB Electrical Specification Revision 1.0*). This combo solution supports several multi-format flash media cards. This multi-format flash media controller and USB hub combo features two exposed downstream USB ports available for external peripheral expansion.

The USB4640/USB4640i can attach to an upstream port as a Full- or Full/Hi-Speed hub. The hub supports Low-Speed, Full-Speed, and Hi-Speed downstream devices (if operating as a Hi-Speed hub) on all of the enabled downstream ports.

All required resistors on the USB ports are integrated into the hub, including all series termination resistors on D+ and D– pins and all required pull-down and pull-up resistors. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

The USB4640/USB4640i includes programmable features, such as:

- **PortMap**: provides flexible port mapping and disable sequences. The downstream ports of a USB4640/USB4640i hub can be reordered or disabled in any sequence to support multiple platform designs with minimum effort. For any port that is disabled, the USB4640/USB4640i hub controllers automatically reorder the remaining ports to match the USB host controller's port numbering scheme.
- **PortSwap**: adds per-port programmability to USB differential-pair pin locations. PortSwap also allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.
- **PHYBoost**: enables 4 programmable levels of USB signal drive strength in downstream port transceivers. PHYBoost will also attempt to restore USB signal integrity.



Note: PHYBoost is only available on the two USB downstream ports.

1.1 Hardware Features

- Single chip HSIC hub and flash media controller combo
- USB2660/USB2660i supports the commercial temperature range of 0°C to +70°C
- USB4640/USB4640i supports the industrial temperature range of -40°C to +85°C
- Transaction translator (TT) in the hub supports operation of FS and LS peripherals
- Full power management with individual or ganged power control of each downstream port
- Optional support for external firmware access via SPI interface
- Onboard 24 MHz crystal driver circuit
- Optional external 24 MHz clock input (must be a 1.8 V signal)
- Code execution via SPI ROM which must meet the following criteria:
  —30 MHz or 60 MHz operation support
  —Single bit or dual bit mode support
  —Mode 0 or mode 3 SPI support

- Compliance with the following flash media card specifications:
  - —Secure Digital 2.0 and MultiMediaCard 4.2
    - –SD 2.0, SD-HS, SD-HC
    - –TransFlash™ and reduced form factor media
    - –1/4/8 bit MMC 4.2
  - —Memory Stick 1.43
  - —Memory Stick Pro Format 1.02
  - —Memory Stick Pro-HG Duo Format 1.01
    - –Memory Stick, MS Duo, MS-HS, MS Pro-HG, MS Pro
  - —Memory Stick Duo 1.10
    - –xD-Picture Card 1.2
- Up to 9 GPIOs: configuration and polarity for special function use
  - —The number of actual GPIOs depends on the implementation configuration used
  - —One GPIO available with up to 200 mA drive and protected fold-back short circuit current
- 8051 8-bit microprocessor
  - —60 MHz - single cycle execution
  - —64 KB ROM | 9 KB RAM
- Integrated regulator for 1.8 V core operation

1.2 Software Features

- Hub and flash media reader/writer configuration from a single source: External I^2C ROM or external SPI ROM, where the following features are then available:
  - —Customizable vendor ID, product ID, and device ID
  - —12-hex digits maximum for the serial number string
  - —28-character manufacturer ID and product strings for the flash media reader/writer

1.3 OEM Selectable Hub Features

The USB4640/USB4640i provides a default configuration that may be sufficient for most applications. following a reset. The USB4640/USB4640i can instead be configured by an external I^2C EEPROM or SPI ROM.

- Compound Device support on a port-by-port basis
  - —a port is permanently hardwired to a downstream USB peripheral device
- Select over-current sensing and port power control on an individual or ganged (all ports together) basis to match the OEM's choice of circuit board component selection
- Port power control and over-current detection/delay features
- Configure the delay time for filtering the over-current sense inputs
- Configure the delay time for turning on downstream port power
- Bus- or self-powered selection
- Hub port disable or non-removable configurations
- Flexible port mapping and disable sequencing supports multiple platform designs
- Programmable USB differential-pair pin location eases PCB layout by aligning USB signal lines directly to connectors
- Programmable USB signal drive strength recovers USB signal integrity using 4 levels of signal drive strength
- Indicate the maximum current that the 2-port hub consumes
- Indicate the maximum current required for the hub controller

Chapter 2 Block Diagram

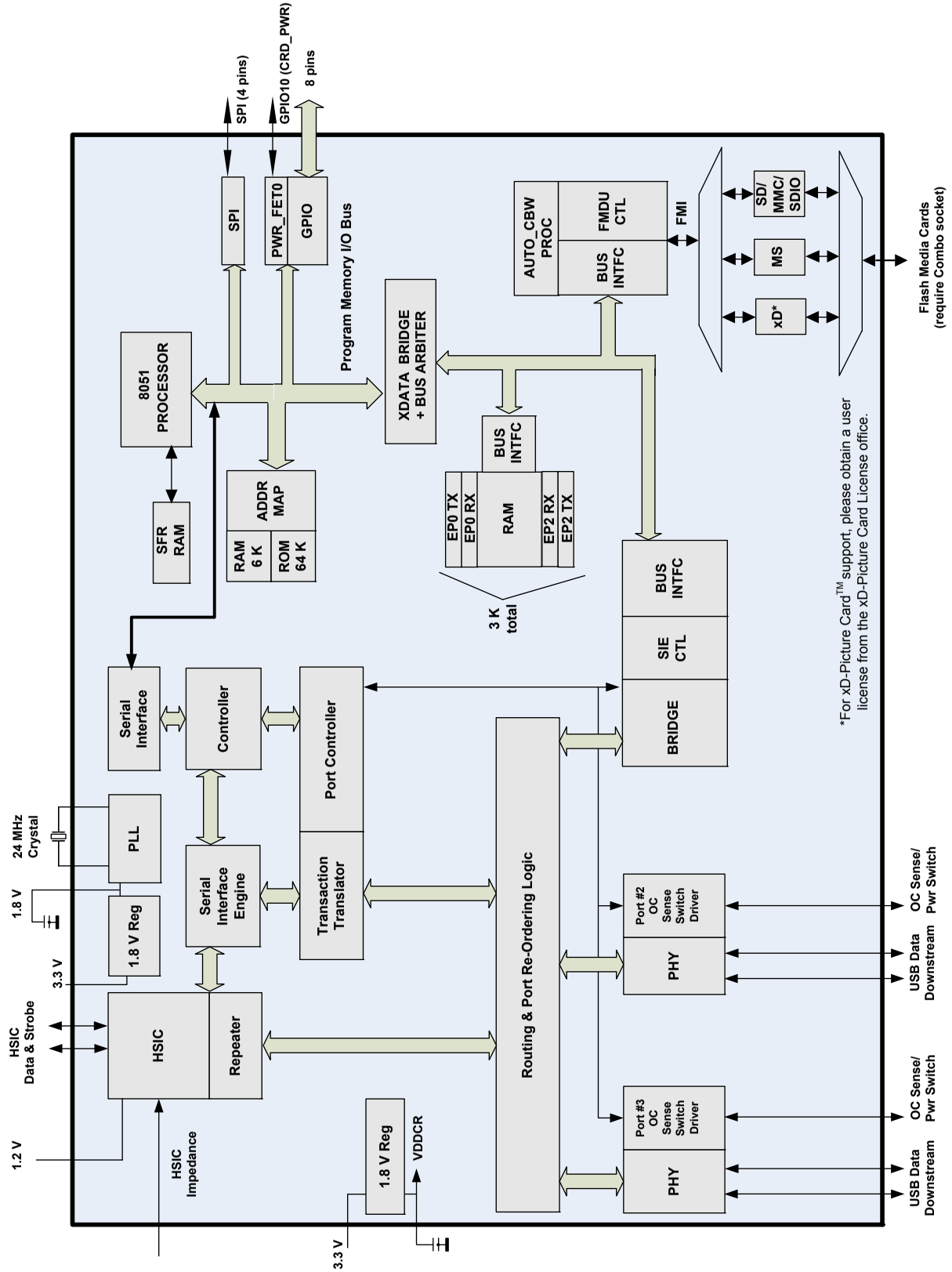


Figure 2.1 USB4640/USB4640i Block Diagram

Chapter 3 Pinning Information

This chapter outlines the pinning configuration, followed by a corresponding pin list grouped by function. The detailed pin descriptions are listed then outlined in Section 3.3, on page 13.

3.1 Pin Configurations

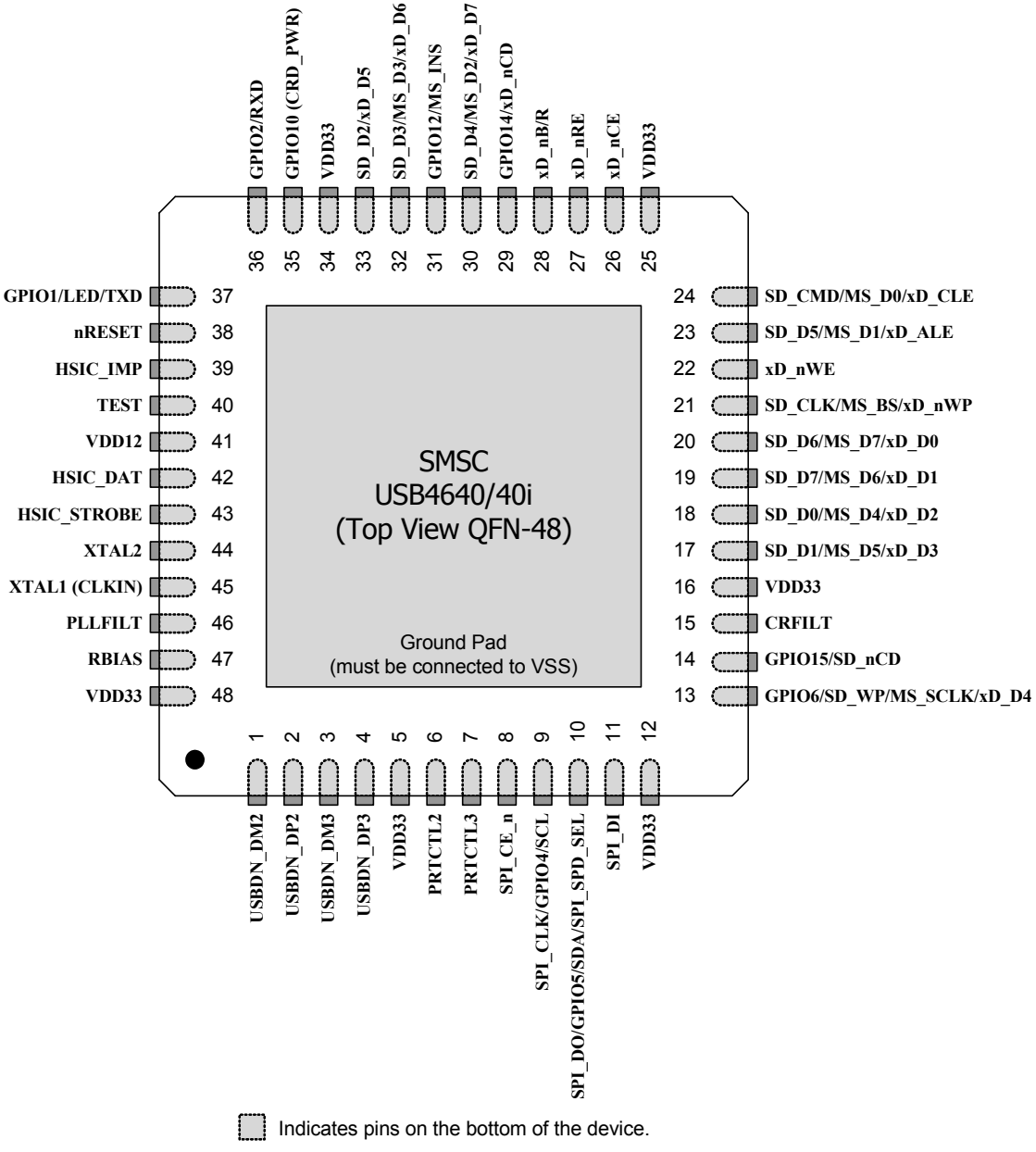


Figure 3.1 USB4640/USB4640i 48-Pin QFN

3.2 48-Pin List

Table 3.1 USB4640/USB4640i 48-Pin List

UPSTREAM HSIC INTERFACE (3 PINS)			
HSIC_IMP	HSIC_DAT	HSIC_STROBE	
DOWNSTREAM USB INTERFACE (3 PINS)			
XTAL1 (CLKIN)	XTAL2	RBIAS	
DOWNSTREAM 2-PORT USB INTERFACE (6 PINS)			
USBDN_DP2	USBDN_DM2	PRTCTL2	PRTCTL3
USBDN_DP3	USBDN_DM3		
SECURE DIGITAL/MEMORY STICK/xD INTERFACE (18 PINS)			
SD_D7/ MS_D6/ xD_D1	SD_D6/ MS_D7/ xD_D0	SD_D5/ MS_D1/ xD_ALE	SD_D4/ MS_D2/ xD_D7
SD_D3/ MS_D3/ xD_D6	SD_D2/ xD_D5	SD_D1/ MS_D5/ xD_D3	SD_D0/ MS_D4/ xD_D2
SD_CLK/ MS_BS/ xD_nWP	SD_CMD/ MS_D0/ xD_CLE	GPIO15/ SD_nCD	GPIO12/ MS_INS
GPIO6/ SD_WP/ MS_SCLK/ xD_D4	GPIO14/ xD_nCD	xD_nWE	xD_nB/R
xD_nRE	xD_nCE		
SPI INTERFACE (4 PINS)			
SPI_CE_N	SPI_CLK/ GPIO4/ SCL	SPI_DO/ GPIO5/ SDA/ SPI_SPD_SEL	SPI_DI
MISC (5 PINS)			
nRESET	TEST	GPIO1/ LED/ TXD	GPIO2/ RXD
GPIO10 (CRD_PWR)			
POWER (9 PINS)			
(6) VDD33	VDD12	CRFILT	PLLFILT
TOTAL 48			

3.3 Pin Descriptions

This section provides a detailed description of each pin. The pins are arranged in functional groups according to their associated interface. The pin descriptions below are applied when using the internal default firmware and can be referenced in Chapter 4: *Configuration Options* on page 25. See Appendix A: *(Acronyms)* on page 61 for details.

An *n* in the signal name indicates that the active (asserted) state occurs when the signal is at a low voltage level. When the *n* is not present, the signal is asserted when it is at a high voltage level. The terms assertion and negation are used exclusively in order to avoid confusion when working with a mixture of active low and active high signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

Table 3.2 USB4640/USB4640i Pin Descriptions

SYMBOL	48-PIN QFN	BUFFER TYPE	DESCRIPTION
UPSTREAM HSIC INTERFACE			
HSIC_IMP	39	I	HSIC Impedance Control Selects the driver impedance of **HSIC_DAT** and **HSIC_STROBE** 1 : Approximately 50 Ω impedance 0 : Approximately 40 Ω impedance
HSIC_DAT	42	I/O	HSIC Data Bi-directional double data rate (DDR) data signal that is synchronous to the **HSIC_STROBE** signal as defined in the *High-Speed Inter-Chip USB Specification, Version 1.0*.
HSIC_STROBE	43	I/O	HSIC Strobe Bi-directional data strobe signal defined in the *High-Speed Inter-Chip USB Specification, Version 1.0*.
DOWNSTREAM USB INTERFACE			
USBDN_DM[3:2] USBDN_DP[3:2]	3 1 4 2	I/O-U	USB Bus Data Connect to the downstream USB bus data signals and can be swapped using the PortSwap feature (See Section 4.4.4.20: *F1h: Port Swap* on page 43).
PRTCTL[3:2]	7 6	I/OD6PU	USB Power Enable, when used as an: ▪ output: enables power to downstream USB peripheral devices and have weak internal pull-up resistors. (See Section 3.5: *Port Power Control* on page 20 for diagram and usage instructions.) ▪ input: monitor the over-current condition (when the power is enabled). When an over-current condition is detected, the pins turn the power off.
RBIAS	47	I-R	USB Transceiver Bias Sets the transceiver's internal bias currents using a 12.0 kΩ, ±1.0% resistor attached from VSS.
XTAL1 (CLKIN)	45	ICLKx	24 MHz Crystal Input or External Clock Input Can be connected to one terminal of the crystal or connected to an external 24 MHz clock when a crystal is not used.

Table 3.2 USB4640/USB4640i Pin Descriptions (continued)

SYMBOL	48-PIN QFN	BUFFER TYPE	DESCRIPTION
XTAL2	44	OCLKx	24 MHz Crystal Output The other terminal of the crystal, or it is left open when an external clock source is used to drive **XTAL1(CLKIN)**.
SECURE DIGITAL INTERFACE			
SD_D[7:0]	19 20 23 30 32 33 17 18	I/O8PU	Secure Digital Data 7-0 Bi-directional data signals **SD_D0** - **SD_D7** with weak pull-up resistors.
SD_CLK	21	O8	Secure Digital Clock The output clock signal to the SD/MMC device.
SD_CMD	24	I/O8PU	Secure Digital Command Bi-directional signal that connects to the CMD signal of the SD/MMC device. The bi-directional signal has a weak internal pull-up resistor.
GPIO15/	14	I/O6	General Purpose IO 15 Can be used either as an input; edge sensitive interrupt input; or output. Custom firmware is required to activate this function.
SD_nCD		I/O8PU	Secure Digital Card Detect GPIO Designated by the default firmware as the Secure Digital card detection pin and has an internal pull-up.
GPIO6/	13	I/O6	General Purpose IO 6 Can be used either as input; edge sensitive interrupt input; or output. Custom firmware is required to activate this function.
SD_WP		I/O8	Secure Digital Write Protected GPIO Designated by the default firmware as the Secure Digital card interface mechanical write protect detect pin.
MEMORY STICK INTERFACE			
MS_BS	21	O8	Memory Stick Bus State Connected to the bus state pin of the MS device. It is used to control the Bus States 0, 1, 2, and 3 (BS0, BS1, and BS3) of the MS device.
GPIO12/	31	I/O8	General Purpose IO 12 Can be used either as input; edge sensitive interrupt input; or output. Custom firmware is required to activate this function.
MS_INS		IPU	Memory Stick Card Insertion GPIO Designated by the default software as the Memory Stick card detection pin and has a weak internal pull-up resistor.
MS_SCLK	13	O8	Memory Stick System Clock Output clock signal to the MS device.

Table 3.2 USB4640/USB4640i Pin Descriptions (continued)

SYMBOL	48-PIN QFN	BUFFER TYPE	DESCRIPTION
MS_D[7:0]	20 19 17 18 32 30 23 24	I/O8PD	Memory Stick System Data In/Out Bi-directional data signals for the MS device. In serial mode, the most significant bit (MSB) of each byte is transmitted first by either the memory stick controller MSC or the MS device on **MS_D0**. **MS_D0**, **MS_D2**, and **MS_D3** have weak pull-down resistors. **MS_D1** has a pull-down resistor when in parallel mode. Otherwise, it is disabled. In 4- or 8-bit parallel modes, all **MS_D7** - **MS_D0** signals have weak pull-down resistors.
xD-PICTURE CARD INTERFACE			
xD_D[7:0]	30 32 33 13 17 18 19 20	I/O8PD	xD-Picture Card Data 7-0 Bi-directional data signals **xD_D7** - **xD_D0** and have weak internal pull-down resistors.
xD_ALE	23	O8PD	xD-Picture Card Address Strobe Active high Address Latch Enable (ALE) signal for the xD-Picture Card device. This pin has a weak pull-down resistor that is permanently enabled.
xD_nB/R	28	IPU	xD-Picture Card Busy or Data Ready Connected to the **BSY/RDY** pin of the xD-Picture Card device. When using the internal FET, this pin has a weak internal pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (the internal FET is disabled), then the internal pull-up is not available (an external pull-up is required).
xD_nCE	26	O8PU	xD-Picture Card Chip Enable Active low chip enable signal for the xD-Picture Card device. When using the internal FET, this pin has weak internal pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (internal FET is disabled), then the internal pull-up is not available (an external pull-up is required).
xD_CLE	24	O8PD	xD-Picture Card Command Strobe An active high Command Latch Enable signal for the xD-Picture Card device. This pin has a weak pull-down resistor that is permanently enabled.
GPIO14/	29	I/O6	General Purpose IO 14 Can be used either as input; edge sensitive interrupt input; or output. Custom firmware is required to activate this function.
xD_nCD		I/O8	xD-Picture Card Detection GPIO Designated by the default firmware as the xD-Picture Card detection pin and has an internal pull-up.

Table 3.2 USB4640/USB4640i Pin Descriptions (continued)

SYMBOL	48-PIN QFN	BUFFER TYPE	DESCRIPTION
xD_nRE	27	O8PU	xD-Picture Card Read Enable Active low read strobe signal for the xD-Picture Card device. When using the internal FET, this pin has a weak internal pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (internal FET is disabled), then the internal pull-up is not available (an external pull-up is required).
xD_nWE	22	O8PU	xD-Picture Card Write Enable Active low write strobe signal for the xD-Picture Card device. When using the internal FET, this pin has a weak internal pull-up resistor that is tied to the output of the internal power FET. If an external FET is used (internal FET is disabled), then the internal pull-up is not available (an external pull-up is required).
xD_nWP	21	O8PD	xD-Picture Card Write Protect Active low write-protect signal for the xD-Picture Card device. This pin has a weak pull-down resistor that is permanently enabled.
SPI INTERFACE			
SPI_CE_n	8	O12	SPI Chip Enable Active low chip enable output. If the SPI interface is enabled, this pin must be driven high in power down states.
SPI_CLK/	9	I/O12	SPI Clock Out Clock signal out to the serial ROM. See Section 3.6: *ROM BOOT Sequence* on page 21 for diagram and usage instructions. During reset, this pin must be driven low.
GPIO4/		I/O6	General Purpose IO 4 Can be used either as input; edge sensitive interrupt input; or output. Custom firmware is required to activate this function.
SCL			Serial Clock The I^2C EEPROM clock pin when the device is connected to the optional I^2C EEPROM.

Table 3.2 USB4640/USB4640i Pin Descriptions (continued)

SYMBOL	48-PIN QFN	BUFFER TYPE	DESCRIPTION
SPI_DO/	10	I/O12	SPI Serial Data Out The output for the SPI port. See Section 3.6: *ROM BOOT Sequence* for diagram and usage instructions.
GPIO5/		I/O6	This pin may be used either as an input; edge sensitive interrupt input; or output. Custom firmware is required to activate this function.
SDA/			Serial Data Line The I^2C EEPROM data pin when the device is connected to the optional I^2C EEPROM.
SPI_SPD_SEL		I/O12	SPI Speed Select Selects the speed of the SPI interface. During **nRESET** assertion, this pin will be tri-stated with the weak pull-down resistor enabled. When **nRESET** is negated, the value on the pin will be internally latched, and the pin will revert to **SPI_DO** functionality, where the internal pull-down will be disabled. 0 : 30 MHz (no external resistor should be applied) 1 : 60 MHz (a 10 kΩ external pull-up resistor must be applied) If the latched value is 1, then the pin is tri-stated when the chip is in the suspend state. If the latched value is 0, then the pin is driven low during a suspend state.
SPI_DI	11	I/O12PD	SPI Serial Data In The SPI data in to the controller from the ROM. This pin has a weak internal pull-down applied at all times to prevent floating.
MISC			
GPIO1/	37	I/O6	General Purpose I/O 1 Can be used either as an input; edge sensitive interrupt input; or output. Custom firmware is required to activate this function.
LED/			Can be used as an LED output.
TXD			This signal can be configured as the TXD output of the internal UART. Custom firmware is required to activate this function.
GPIO2/	36	I/O6	General Purpose I/O 2 Can be used either as an input; edge sensitive interrupt input; or output. Custom firmware is required to activate this function.
RXD			This signal can be configured as input to the RXD of the internal UART. Custom firmware is required to activate this function.
GPIO10 (CRD_PWR)	35	I/O200	Card Power Drive: 3.3 V (100 mA or 200 mA) This must be the only FET used to power devices. Failure to do this will violate voltage specifications on device pins. If this pin is not being used as a card power pin, this pin may be used either as an input; edge sensitive interrupt input; or output (GPIO). Please see Section 4.4.2.3: *A4h-A5h: Smart Media Device Power Configuration* on page 34 for more information.

Table 3.2 USB4640/USB4640i Pin Descriptions (continued)

SYMBOL	48-PIN QFN	BUFFER TYPE	DESCRIPTION
nRESET	38	IS	Reset Input The system uses this active low signal to reset the chip. The active low pulse should be at least 1 µs wide.
TEST	40	I	Test Input Tie to ground for normal operation.
DIGITAL / POWER / GROUND			
CRFILT	15		VDD Core Regulator Filter Capacitor Requires a 1.0 µF (or greater) ± 20% (ESR <0.1Ω) capacitor to VSS.
PLLFILT	46		Phase-Locked Loop Regulator Filter Capacitor Requires a 1.0 µF (or greater) ± 20% (ESR < 0.1 Ω) capacitor to VSS.
VDD12	41		1.2 V Power For HSIC pads and buffers
VDD33	5 12 16 25 34 48		3.3 V Power and Regulator Input See Chapter 6: *DC Parameters* on page 51 for more information. Pins 16 and 48 each require an external bypass capacitor of 4.7 µF minimum.
VSS	ePad		Ground Pad/ePad The package slug is the only VSS for the device and must be tied to ground with multiple vias.

3.4 Buffer Type Descriptions

Table 3.3 USB4640/USB4640i Buffer Type Descriptions

BUFFER	DESCRIPTION
I	Input.
I/O	Input/output
IPU	Input with weak internal pull-up
IS	Input with Schmitt trigger
I/O6	Input/output buffer with 6 mA sink and 6 mA source
I/OD6PU	Input/open drain output buffer with a 6 mA sink
O8	Output buffer with an 8 mA sink and an 8 mA source
O8PD	Output buffer with an 8 mA sink and an 8 mA source with a weak internal pull-down resistor
O8PU	Output buffer with an 8 mA sink and an 8 mA source with a weak internal pull-up resistor
I/O8	Input/output buffer with an 8 mA sink and an 8 mA source

Table 3.3 USB4640/USB4640i Buffer Type Descriptions (continued)

BUFFER	DESCRIPTION
I/O8PD	Input/output buffer with an 8 mA sink and an 8 mA source with a weak internal pull-down resistor
I/O8PU	Input/output buffer with an 8 mA sink and an 8 mA source with a weak internal pull-up resistor
O12	Output buffer with a 12 mA sink and a 12 mA source
I/O12	Input/output buffer with 12 mA sink and 12 mA source
I/O12PD	Input/output buffer with 12 mA sink and 12 mA source with a weak internal pull-down resistor
I/O200	Input/output buffer 12 mA with FET disabled, 100/200 mA source only when the FET is enabled
ICLKx	XTAL clock input
OCLKx	XTAL clock output
I/O-U	Analog input/output as defined in the *USB 2.0 Specification*
I-R	RBIAS

3.5 Port Power Control

3.5.1 Port Power Control Using a USB Power Switch

The USB4640/USB4640i has a single port power control and over-current sense signal for each downstream port. When disabling port power, the driver will actively drive a 0. To avoid unnecessary power dissipation, the internal pull-up resistor will be disabled at that time. When port power is enabled, the output driver is disabled, and the pull-up resistor is enabled creating an open drain output.

If there is an over-current situation, the USB Power Switch will assert the open drain OCS signal. The Schmitt trigger input will detect this event as a low. The open drain output does not interfere. The internal over-current sense filter handles the transient conditions, such as low voltage, while the device is powering up.

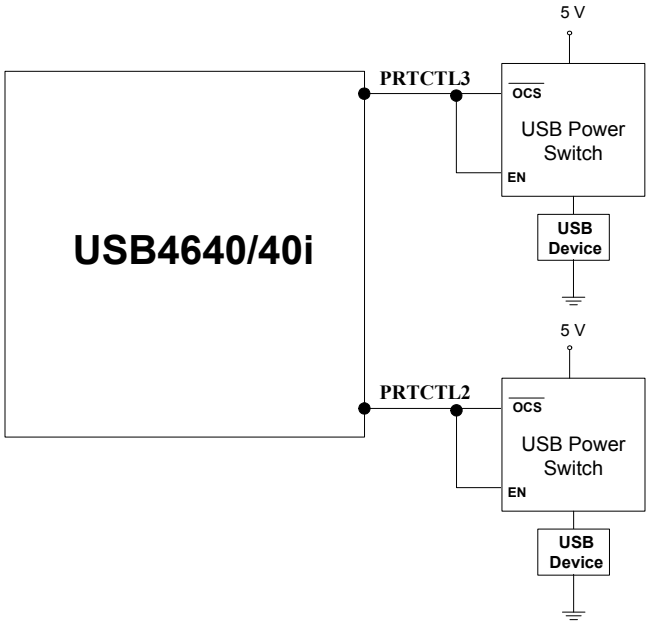


Figure 3.2 Port Power Control with USB Power Switch

3.5.2 Port Power Control Using a Poly Fuse

When using the USB4640/USB4640i with a poly fuse, an external diode must be used (see Figure 3.3). When disabling port power, the USB4640/USB4640i will drive a 0. This procedure will have no effect since the external diode will isolate the pin from the load. When port power is enabled, the USB4640/USB4640i output driver is disabled, and the pull-up resistor is enabled which creates an open drain output. This open drain output condition means that the pull-up resistor is providing 3.3 volts to the anode of the diode. If there is an over-current situation, the poly fuse will open. This will cause the cathode of the diode to go to zero volts. The anode of the diode will be at 0.7 volts, and the

Schmitt trigger input will register this as a low resulting in an over-current detection. The open drain output does not interfere.

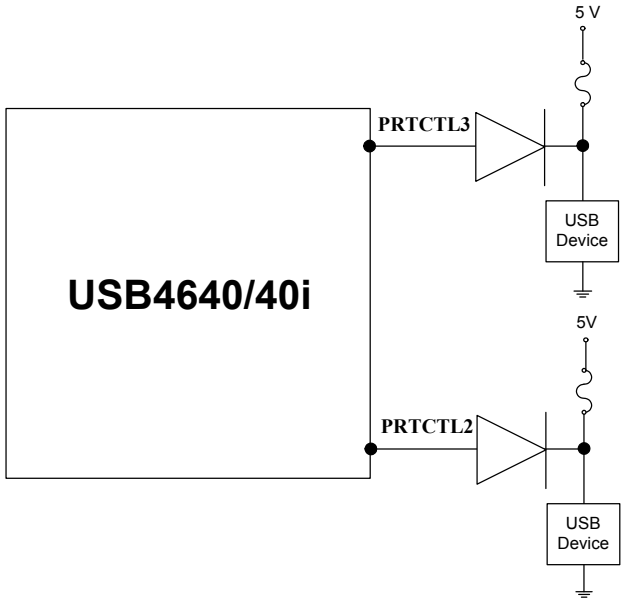


Figure 3.3 Port Power Control with a Single Poly Fuse and Multiple Loads

When using a single poly fuse to power all devices, note that for the ganged situation, all power control pins must be tied together.

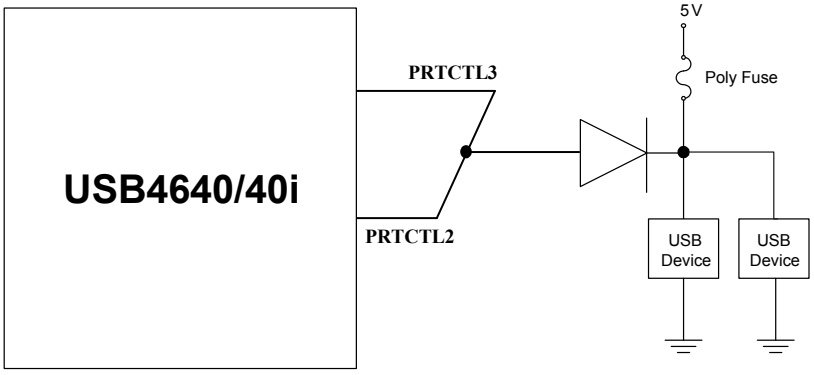


Figure 3.4 Port Power with Ganged Control with Poly Fuse

3.6 ROM BOOT Sequence

After power-on reset, the internal firmware checks for an external SPI flash device that contains a valid signature of *2DFU* (device firmware upgrade) beginning at address 0xFFFA. If a valid signature is found, then the external ROM is enabled and code execution begins at address 0x0000 in the external SPI device. Otherwise, code execution continues from the internal ROM.

If there is no SPI ROM detected, the internal firmware then checks for the presence of an I^2C ROM. The firmware looks for the signature *ATA2* at the offset of FCh-FFh and *ecf1* at the offset of 17Ch-17Fh in the I^2C ROM. The firmware reads in the I^2C ROM to configure the hardware and software internally. Please refer to Section 4.3.2: *EEPROM Data Descriptor* on page 26 for the details of the configuration options.

The SPI ROM required for the USB4640/USB4640i is a recommended minimum of 1 Mb and support either 30 MHz or 60 MHz. The frequency used is set using the **SPI_SPD_SEL**. For 30 MHz operation, this pin must be pulled to ground through a 100 kΩ resistor. For 60 MHz operation, this pin must pulled up through a 100 kΩ resistor.

The **SPI_SPD_SEL** pin is used to choose the speed of the SPI interface. During **nRESET** assertion, this pin will be tri-stated with the weak pull-down resistor enabled. When nRESET is negated, the value on the pin will be internally latched, and the pin will revert to **SPI_DO** functionality. The internal pull-down will be disabled.

The firmware can determine the speed of operation on the SPI port by checking the **SPI_CTL.SPI_SPEED** bit (0x2400 - RESET = 0x02). Both 1- and 2-bit SPI operation is supported. For optimum throughput, a 2-bit SPI ROM is recommended. Both mode 0 and mode 3 SPI ROMS are also supported.

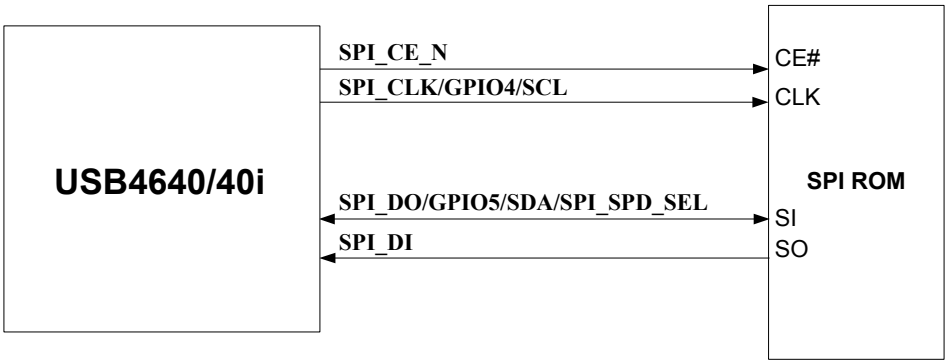


Figure 3.5 SPI ROM Connection

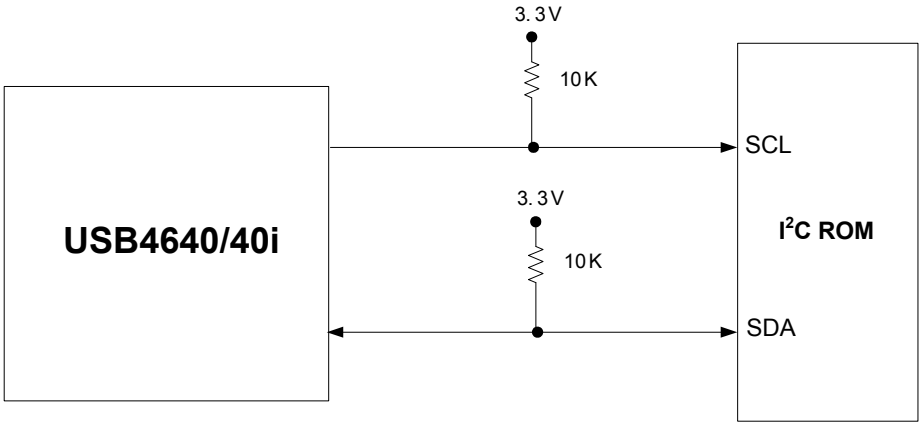


Figure 3.6 I2C Connection

3.7 Pin Reset States

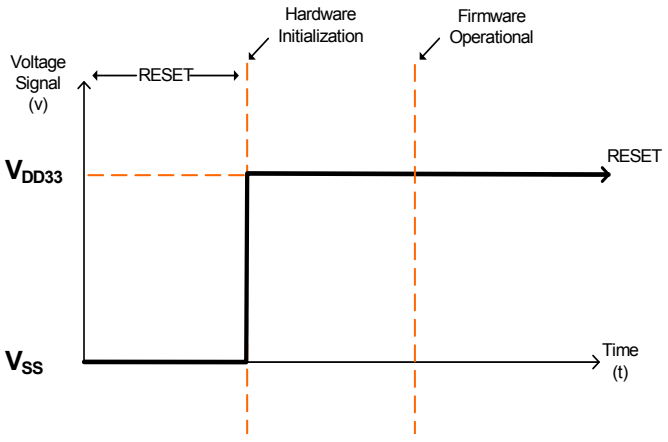


Figure 3.7 Pin Reset States

Table 3.4 Legend for Pin Reset States Table

SYMBOL	DESCRIPTION
0	Output driven low
1	Output driven high
IP	Input enabled
PU	Hardware enables pull-up
PD	Hardware enables pull-down
none	Hardware disables pad
--	Hardware disables function
Z	Hardware disables pad. Both output driver and input buffers are disabled.

Table 3.5 USB4640/USB4640i Reset States Table

		RESET STATE		
PIN	**PIN NAME**	**FUNCTION**	**INPUT/ OUTPUT**	**PU/ PD**
1	USBDN_DM2	USBDN_DM2	IP	PD
2	USBDN_DP2	USBDN_DP2	IP	PD
3	USBDN_DM3	USBDN_DM3	IP	PD
4	USBDN_DP3	USBDN_DP3	IP	PD
6	PRTCTL2	PRTCTL	0	--
7	PRTCTL3	PRTCTL	0	--
8	SPI_CE_n	SPI_CE_n	1	--
9	SPI_CLK/GPIO4/SCL	GPIO	0	--
10	SPI_DO/GPIO5/SDA/SPI_SPD_SEL	GPIO	0	--
11	SPI_DI	SPI_DI	IP	PD
13	GPIO6/SD_WP/MS_SCLK/xD_D4	GPIO	0	--
14	GPIO15/SD_nCD	GPIO	IP	PU
17	SD_D1/MS_D5/xD_D3	none	Z	--
18	SD_D0/MS_D4/xD_D2	none	Z	--
19	SD_D7/MS_D6/xD_D1	none	Z	--

Table 3.5 USB4640/USB4640i Reset States Table (continued)

		RESET STATE		
PIN	**PIN NAME**	**FUNCTION**	**INPUT/ OUTPUT**	**PU/ PD**
20	SD_D6/MS_D7/xD_D0	none	Z	--
21	SD_CLK/MS_BS/xD_nWP	none	Z	--
22	xD_nWE	xD_nWE	Z	--
23	SD_D5/MS_D1/xD_ALE	none	Z	--
24	SD_CMD/MS_D0/xD_CLE	none	Z	--
26	xD_nCE	xD_nCE	Z	--
27	xD_nRE	xD_nRE	Z	--
28	xD_nB/R	xD_nB/R	Z	--
29	GPIO14/xD_nCD	GPIO	IP	PU
30	SD_D4/MS_D2/xD_D7	none	Z	--
31	GPIO12/MS_INS	GPIO	IP	PU
32	SD_D3/MS_D3/xD_D6	none	Z	--
33	SD_D2/xD_D5	none	Z	--
35	GPIO10 (CRD_PWR)	GPIO	Z	--
36	GPIO2/RXD	GPIO	0	--
37	GPIO1/LED/TXD	GPIO	0	--
38	nRESET	nRESET	IP	--
39	HSIC_IMP	HSIC_IMP	Z	--
40	TEST	TEST	IP	PD
42	HSIC_DAT	HSIC_DAT	IP	--
43	HSIC_STROBE	HSIC_STROBE	IP	--

Chapter 4 Configuration Options

4.1 Hub

SMSC's USB 2.0 hub is fully compliant to the *Universal Serial Bus Specification* [1].

The hub provides 1 transaction translator (TT) that is shared by both downstream ports defined as a single-TT configuration. The TT contains 4 non-periodic buffers. The hub supports a large number of features (some are mutually exclusive), and must be configured in order to correctly function when attached to a USB host controller. There are two principal ways to configure the hub:

- Internal default settings
- External EEPROM or SPI Flash device

Note: See Chapter 11 (Hub Specification) of the USB specification for general details regarding hub operation and functionality.

4.2 Card Reader

The SMSC USB4640/USB4640i is fully compliant with the following flash media card reader specifications:

- Secure Digital 2.0/MultiMediaCard 4.2
  —SD 2.0, HS-SD, HC-SD
  —TransFlash™ and reduced form factor media
  —1/4/8 bit MMC 4.2
- Memory Stick 1.43
- Memory Stick Pro Format 1.02
- Memory Stick Pro-HG Duo Format 1.01
  —Memory Stick, MS Duo, HS-MS, MS Pro-HG, MS Pro
- Memory Stick Duo 1.10
- xD-Picture Card 1.2

4.3 System Configurations

4.3.1 EEPROM/SPI Interface

The USB4640/USB4640i can be configured via a 2-wire I^2C EEPROM (512x8) or an external SPI flash device containing the USB4640/USB4640i firmware. If an external configuration device does not exist the internal default values will be used. If one of the external devices is used for configuration, the USB4640/USB4640i values can be updated through the USB interface. The hub will then attach to the upstream USB host.

The USBDM tool set is available in the USB264x Hub Card reader combo software release package. To download the software package from SMSC's website, visit:

- https://www2.smsc.com/mkt/CW_SFT_PUB.nsf/Agreements/OBJ+Hub+Card+Reader

Review the license and select the *I agree* checkbox, followed by the *Confirm* button. Download the *USB264x Hub Card reader combo Release Package* zip file with the USBDM tool set will then be available for download.