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USB5533B

3-Port SS/HS USB Hub Controller

General Description

The USB5533B hub is a 3-port SuperSpeed/Hi-Speed, low-power, configurable hub controller family fully compliant with the *USB 3.0 Specification*. The USB5533B supports 5 Gbps SuperSpeed (SS), 480 Mbps Hi-Speed (HS), 12 Mbps Full-Speed (FS) and 1.5 Mbps Low-Speed (LS) USB signaling for complete coverage of all defined USB operating speeds.

The USB5533B supports USB 2.0 speeds through its USB 2.0 hub controller. The new SuperSpeed hub controller operates in parallel with the USB 2.0 controller, so the 5 Gbps SuperSpeed data transfers are not affected by the slower USB 2.0 traffic.

The USB5533B supports battery charging on a per port basis. On battery charging enabled ports, the devices provide automatic USB data line handshaking. The handshaking supports USB 1.2 Charging Downstream Port (CDP), Dedicated Charging Port (DCP) and non-USB 1.2 devices.

The USB5533B is configured for operation through internal default settings, where custom configurations are supported through an on-chip OTP ROM, an external SPI ROM, or SMBus.

Product Features

- USB 3.0 compliant 5 Gbps, 480 Mbps, 12 Mbps and 1.5 Mbps operation, USB pins are 5 V tolerant
  - Integrated termination and pull-up/pull-down resistors
- Three downstream USB 3.0 ports
- Supports battery charging of most popular battery powered devices
  - USB-IF Battery Charging rev. 1.2 support (DCP & CDP)
  - Apple Portable product charger emulation
  - Blackberry charger emulation
  - Chinese YD/T 1591-2006 charger emulation
  - Chinese YD/T 1591-2009 charger emulation
  - Supports additional portable devices
- Emulates portable/handheld native wall chargers
  - Charging profiles emulate a handheld device's wall charger to enable fast charging (minutes vs. hours)
- Enables charging from a mobile platform that is off
- Support tablets' high current requirements
- Optimized for low-power operation and low thermal dissipation
- Vendor Specific Messaging (VSM) support for firmware upload over USB
- Configuration via OTP ROM, SPI ROM, or SMBus
- On-chip 8051 µC manages VBUS, and other hub signals
- 8 KB RAM, 32 KB ROM
- One Time programmable (OTP) ROM: 8 kbit
  - Includes on-chip charge pump
- Single 25 MHz XTAL or clock input for all on-chip PLL and clocking requirements
- Supports JTAG boundary scan
- PHYBoost (USB 2.0)
  - Selectable drive strength for improved signal integrity
- VariSense (USB 2.0)
  - controls the receiver sensitivity enabling four programmable levels of USB signal receive sensitivity
- IETF RFC 4122 compliant 128-bit UUID

Software Features

- Compatible with Microsoft Windows 7, Vista, XP, Mac OSX10.4+, and Linux Hub Drivers

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Table of Contents

1.0 INTRODUCTION

1.1 Conventions

Within this manual, the following abbreviations and symbols are used to improve readability.

Example	Description
BIT	Name of a single bit within a field
FIELD.BIT	Name of a single bit (BIT) in FIELD
x…y	Range from x to y, inclusive
BITS[m:n]	Groups of bits from m to n, inclusive
PIN	Pin Name
zzzzb	Binary number (value zzzz)
0xzzz	Hexadecimal number (value zzz)
zzh	Hexadecimal number (value zz)
rsvd	Reserved memory location. Must write 0, read value indeterminate
`code`	Instruction code, or API function or parameter
Multi Word Name	Used for multiple words that are considered a single unit, such as: *Resource Allocate* message, or *Connection Label*, or *Decrement Stack Pointer* instruction.
Section Name	Section or Document name.
x	Don't care
<Parameter>	<> indicate a Parameter is optional or is only used under some conditions
{,Parameter}	Braces indicate Parameter(s) that repeat one or more times.
[Parameter]	Brackets indicate a nested Parameter. This Parameter is not real and actually decodes into one or more real parameters.

1.2 Overview

The USB5533B hub is a 3-port, low-power, configurable Hub Controller fully compliant with the *USB 3.0 Specification 2.* The USB5533B supports 5 Gbps SuperSpeed (SS), 480 Mbps Hi-Speed (HS), 12 Mbps Full-Speed (FS) and 1.5 Mbps Low-Speed (LS) USB signaling for complete coverage of all defined USB operating speeds.

All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors and all required pull-down and pull-up resistors on D+ and D- pins. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

The USB5533B hub includes programmable features such as:

- **MultiTRAK™ Technology** (USB 2.0): implements a dedicated Transaction Translator (TT) for each port. Dedicated TTs help maintain consistent full-speed data throughput regardless of the number of active downstream connections.
- **PortSwap** (USB 2.0): allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.
- **PHYBoost** (USB 2.0): enables 4 programmable levels of USB signal drive strength in downstream port transceivers. PHYBoost will also attempt to restore USB signal integrity.

As shown on the Product Identification System page, two USB5533B firmware versions are available: "-5000" and "-6080". These options differ in the following ways:

- The Dynamic Charging Port feature and related DYNCPDIS_N pin function are only available on the -6080 device. Refer to Section 5.1.3, "Dynamic Charging Port (6080 Only)" for additional details.
- The TRST/DYNCPDIS_N/UCS_SMBALERT_N pin buffer type is "IPU" in the -6080 device and "I" in the -5000 device. Refer to Pin Information on page 7 for additional details.
- The Global Suspend power consumption has been significantly lowered in the -6080 device. Refer to Section 6.3, "Power Consumption" for additional details.

1.3 Configurable Features

The USB5533B hub controller provides a default configuration that is sufficient for most applications. When initialized in the default configuration, the following features may be configured:

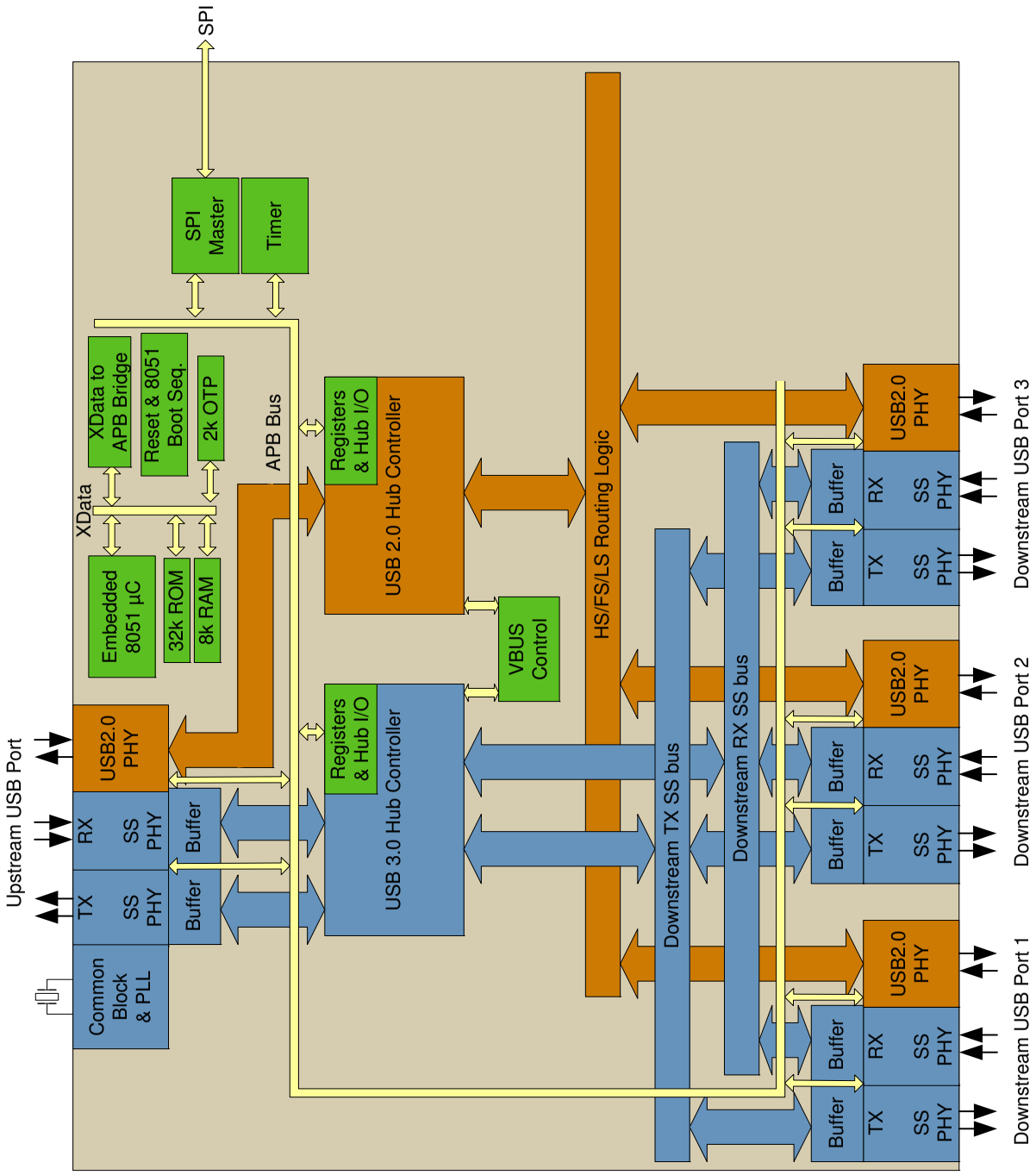
- Downstream non-removable ports, where the hub will automatically report as a compound device
- Downstream disabled ports
- Downstream port power control and over-current detection on a ganged or individual basis
- USB signal drive strength
- USB differential pair pin location

The USB5533B hub controllers can alternatively be configured by OTP or as an SMBus slave device. When configured by an OTP or over SMBus, the following configurable features are provided:

- Support for compound devices on a port-by-port basis
- Selectable over-current sensing and port power control on an individual or ganged basis to match the circuit board component selection
- Customizable vendor ID, product ID, and device ID
- Configurable delay time for filtering the over-current sense inputs
- Indication of the maximum current that the hub consumes from the USB upstream port
- Indication of the maximum current required for the hub controller
- Custom string descriptors (up to 30 characters): Product, manufacturer, and serial number

2.0 BLOCK DIAGRAM

FIGURE 2-1: USB5533B BLOCK DIAGRAM

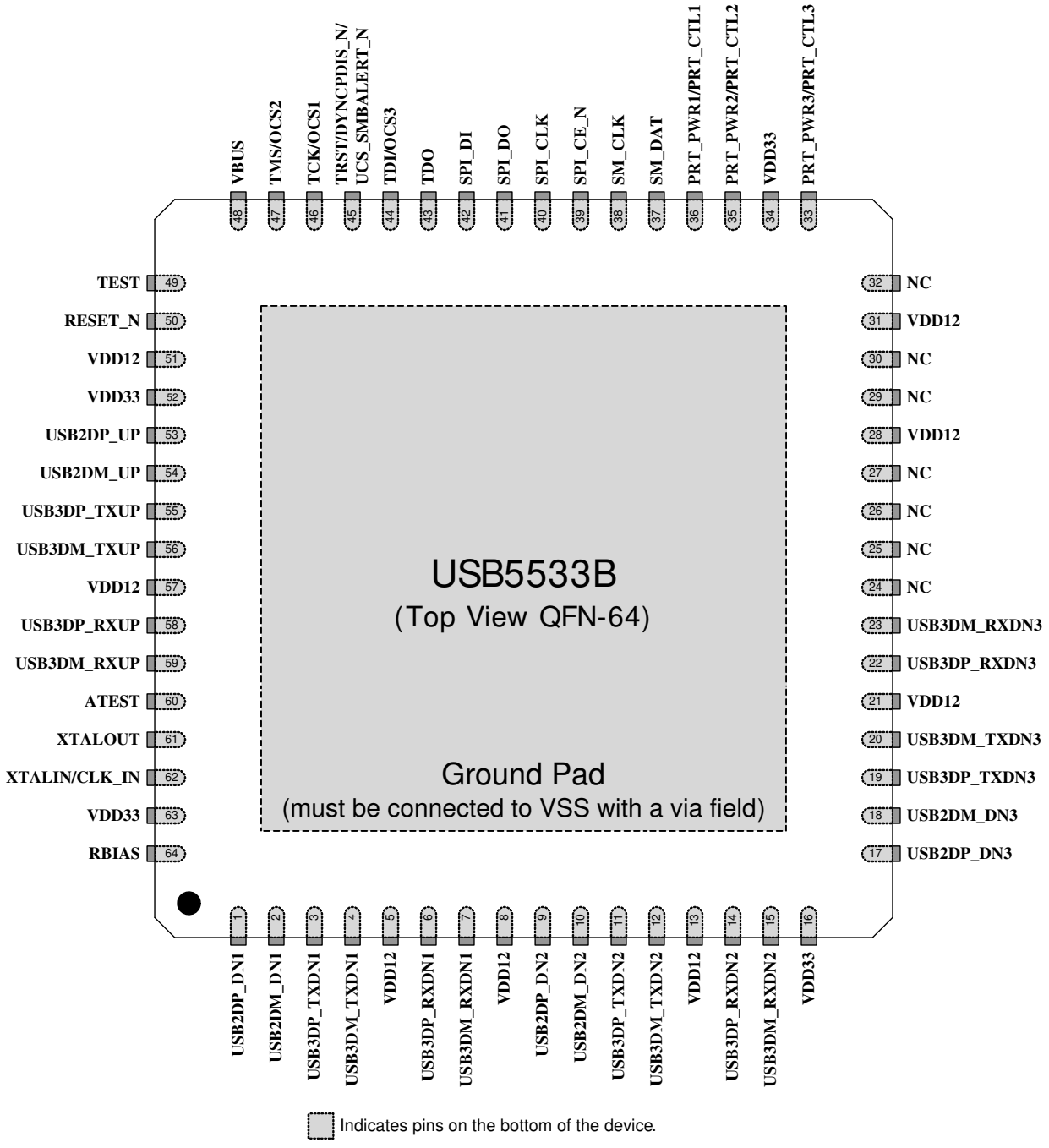


3.0 PIN INFORMATION

This chapter outlines the pinning configurations for each chip. The detailed pin descriptions are listed by function in Section 3.2, "Pin Descriptions (Grouped by Function)," on page 8.

3.1 Pin Configurations

FIGURE 3-1: USB5533B 64-PIN QFN



3.2 Pin Descriptions (Grouped by Function)

An *N* at the end of a signal name indicates that the active (asserted) state occurs when the signal is at a low voltage level. When the *N* is not present, the signal is asserted when it is at a high voltage level. The terms assertion and negation are used exclusively in order to avoid confusion when working with a mixture of active low and active high signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

TABLE 3-1: USB5533B PIN DESCRIPTIONS

Symbol	Buffer Type	Description
USB 3.0 INTERFACE		
USB3DP_TXUP	IO-U	USB 3 Upstream Upstream SuperSpeed transmit data plus
USB3DM_TXUP	IO-U	USB 3 Upstream Upstream SuperSpeed transmit data minus
USB3DP_RXUP	IO-U	USB 3 Upstream Upstream SuperSpeed receive data plus
USB3DM_RXUP	IO-U	USB 3 Upstream Upstream SuperSpeed receive data minus
USB3DP_TXDN[3:1]	IO-U	USB 3 Downstream Downstream SuperSpeed transmit data plus for ports 1 through 3.
USB3DM_TXDN[3:1]	IO-U	USB 3 Downstream Downstream SuperSpeed transmit data minus for ports 1 through 3.
USB3DP_RXDN[3:1]	IO-U	USB 3 Downstream Downstream SuperSpeed receive data plus for ports 1 through 3.
USB3DM_RXDN[3:1]	IO-U	USB 3 Downstream Downstream SuperSpeed receive data minus for ports 1 through 3.
USB 2.0 INTERFACE		
USB2DP_UP	IO-U	USB Bus Data These pins connect to the upstream USB bus data signals.
USB2DM_UP	IO-U	USB Bus Data These pins connect to the upstream USB bus data signals.
USB2DP_DN[3:1]	IO-U	USB Downstream Downstream Hi-Speed data plus for ports 1 through 3.
USB2DM_DN[3:1]	IO-U	USB Downstream Downstream Hi-Speed data minus for ports 1 through 3.

TABLE 3-1: USB5533B PIN DESCRIPTIONS (CONTINUED)

Symbol	Buffer Type	Description
USB PORT CONTROL		
PRT_PWR[3:1]/ PRT_CTL[3:1]	O12	USB Power Enable Enables power to USB peripheral devices downstream. **Note:** This pin also provides configuration strap functions. See Note 3-1.
VBUS	I	Upstream VBUS Power Detect This pin can be used to detect the state of the upstream bus power. The device monitors this pin to determine when to assert the internal D+ pull-up resistor (signaling a connect event). When designing a detachable hub, this pin should be connected to VBUS on the upstream port via a 2:1 voltage divider. Two 100 kΩ resistors are suggested. For self-powered applications with a permanently attached host, this pin must be connected to a dedicated host control output, or connected to the 3.3 V domain that powers the host (typically **VDD33**).
SPI INTERFACE (4 PINS)		
SPI_CE_N	O12	SPI Enable
SPI_CLK	O12	SPI Clock
SPI_DO	O12	SPI Serial Data Out The output for the SPI port. **Note:** This pin also provides configuration strap functions. See .
SPI_DI	I	SPI Serial Data In The SPI data in to the controller from the ROM. This pin has a weak internal pull-down applied at all times to prevent floating.
JTAG/OCS INTERFACE		
TRST	IPU (Note 3-4)	JTAG Asynchronous Reset **Note:** If using the SMBus interface, a pull-up on this signal will enable Legacy Mode, while leaving it unconnected or pulled-down will enable Advanced Mode. **Note:** Only available in test mode.
DYNCPDIS_N		Dynamic Charging Port Disable This active-low signal is used to globally disable Battery Charging support on all USB downstream ports configured as Charging Ports. **Note:** This signal available in -6080 versions only
UCS_SMBALERT_N		UCS1002 SMBus Alert When charging port is enabled and SMBus devices are used, this signal acts as an active-low SMBus alert.

TABLE 3-1: USB5533B PIN DESCRIPTIONS (CONTINUED)

Symbol	Buffer Type	Description
TCK	I	JTAG Clock This input is used for JTAG boundary scan and has a weak pull-down. It can be left floating or grounded when not used. If the JTAG is connected, then this signal will be detected high, and the software disables the pull up after reset. **Note:** Only available in test mode.
OCS1		Over-Current Sense 1 Input from external current monitor indicating an over-current condition. **Note:** This pin also provides configuration strap functions. See Note 3-3.
TMS	I	JTAG TMS Used for JTAG boundary scan. **Note:** Only available in test mode.
OCS2		Over-Current Sense 2 Input from external current monitor indicating an over-current condition. **Note:** This pin also provides configuration strap functions. See Note 3-3.
TDI	I	JTAG TDI Used for JTAG boundary scan. **Note:** Only available in test mode.
OCS3		Over-Current Sense 3 Input from external current monitor indicating an over-current condition. **Note:** This pin also provides configuration strap functions. See Note 3-3.
TDO	O12	JTAG TDO Used for JTAG boundary scan. **Note:** Only available in test mode.
MISC		
RESET_N	IS	Reset Input The system uses this active low signal to reset the chip. The active low pulse should be at least 1 µs wide.
XTALIN	ICLKx	Crystal Input: 25 MHz crystal. This pin connects to either one terminal of the crystal or to an external 25 MHz clock when a crystal is not used.
CLK_IN		External Clock Input This pin connects to either one terminal of the crystal or to an external 25 MHz clock when a crystal is not used.
XTALOUT	OCLKx	Crystal Output The clock output, providing a crystal 25 MHz. When an external clock source is used to drive **XTALIN/CLK_IN**, this pin becomes a no connect.
TEST	IPD	Test Pin Treat as a no connect pin or connect to ground. No trace or signal should be routed or attached to this pin.

TABLE 3-1: USB5533B PIN DESCRIPTIONS (CONTINUED)

Symbol	Buffer Type	Description
RBIAS	I-R	USB Transceiver Bias A12.0 kΩ (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings.
ATEST	A	Analog Test Pin This signal is used for testing the chip and must always be connected to ground.
SM_CLK	I/O12	SMBus Clock
SM_DAT	I/O12	SMBus Data Pin
(7) **NC**	-	No connect pins
DIGITAL AND POWER		
(4) **VDD33**		3.3 V Power
(8) **VDD12**		1.25 V Power
VSS		Ground Pad This exposed pad is the device's only connection to VSS and the primary thermal conduction path. Connect to an appropriate via field.

Note 3-1 The PRT_PWR[3:1] pins can optionally provide additional configuration strap functions to enable/disable the associated port and configure its battery charging capabilities. Configuration strap values are latched on device reset. Table 3-2 details the functions associated with the various strap settings.

Strapping features are enabled by default and can be optionally disabled via the Pro-Touch software programming tool. For additional information on the Pro-Touch programming tool, contact your local sales representative.

Strapping functions are not supported for designs that support OCS but not power switching.

TABLE 3-2: PRT_PWR[3:1] CONFIGURATION STRAP STATES

PRT_PWR[3:1] Strap Setting	Port State	Battery Charging
No Pull-Up or Pull-Down	Enabled	Disabled
Pull-Down: <10 kΩ to VSS	Disabled	N/A
Pull-Up: <10 kΩ and >1 kΩ to VDD33	Enabled	Enabled

Note 3-2 The SPI_DO pin provides an additional SPI_SPD_SEL configuration strap function. SPI_SPD_SEL selects between the 30MHz SPI Mode when pulled-down to ground (default) and the 60MHz SPI Mode when pulled-up to VDD33. The SPI_SPD_SEL strap value is latched on Power-On Reset (POR) or RESET_N deassertion.

Note 3-3 The OCS[3:1] pins can optionally provide additional configuration strap functions. To set the associated port into the non-removable state, the OCS pin must be configured with a pull-down (<10 kΩ to VSS). Otherwise, the port will be configured in the removable state. Configuration strap values are latched on device reset.

Strapping features are enabled by default and can be optionally disabled via the Pro-Touch software programming tool. For additional information on the Pro-Touch programming tool, contact your local sales representative.

Strapping functions are not supported for designs that support OCS but not power switching.

Note 3-4 This pin has an internal pull-up only in the -6080 version. The internal pull-up is only active after the SMBus mode (Legacy/Advanced) configuration strap has been sampled at POR or reset. The -5000 version is an “I” type buffer.

3.3 Buffer Type Descriptions

TABLE 3-3: BUFFER TYPE DESCRIPTIONS

Buffer Type	Description
I	Input
I/O	Input/output
IPD	Input with internal weak pull-down resistor
IPU	Input with internal weak pull-up resistor
IS	Input with Schmitt trigger
O12	Output 12 mA
I/O12	Input/output buffer with 12 mA sink and 12 mA source
I/OSD12	Open drain with Schmitt trigger and 12 mA sink.
ICLKx	XTAL clock input
OCLKx	XTAL clock output
I-R	RBIAS
I/O-U	Analog input/output defined in USB specification

4.0 STANDARD INTERFACE CONNECTIONS

4.1 SPI Interface

The hub will interface to external memory depending on configuration of the USB5533B pins associated with each interface type. The USB5533B will first check to see whether an external SPI Flash is present. If not, the USB5533B will operate from internal ROM. If SPI Flash is present, the chip will operate from the external ROM.

The USB5533B is capable of code execution from an external SPI ROM. On power up, the firmware looks for an external SPI flash device that contains a valid signature of `2DFU` (device firmware upgrade) beginning at address 0xFFFA. If a valid signature is found, then the external ROM is enabled and the code execution begins at address 0x0000 in the external SPI device. If a valid signature is not found, then execution continues from internal ROM. The following sections describe the interface options to the external SPI ROM.

4.1.1 OPERATION OF THE HI-SPEED READ SEQUENCE

The SPI controller will automatically handle code reads going out to the SPI ROM Address. When the controller detects a read, the controller drops the **SPI_CE**, and puts out a 0x0B, followed by the 24-bit address. The SPI controller then puts out a DUMMY byte. The next eight clocks clock in the first byte. When the first byte is clocked in a ready signal is sent back to the processor, and the processor gets one byte.

After the processor gets the first byte, its address will change. If the address is one more than the last address, the SPI controller will clock out one more byte. If the address in anything other than one more than the last address, the SPI controller will terminate the transaction by taking **SPI_CE** high. As long as the addresses are sequential, the SPI Controller will keep clocking in data.

FIGURE 4-1: SPI HI-SPEED READ OPERATION

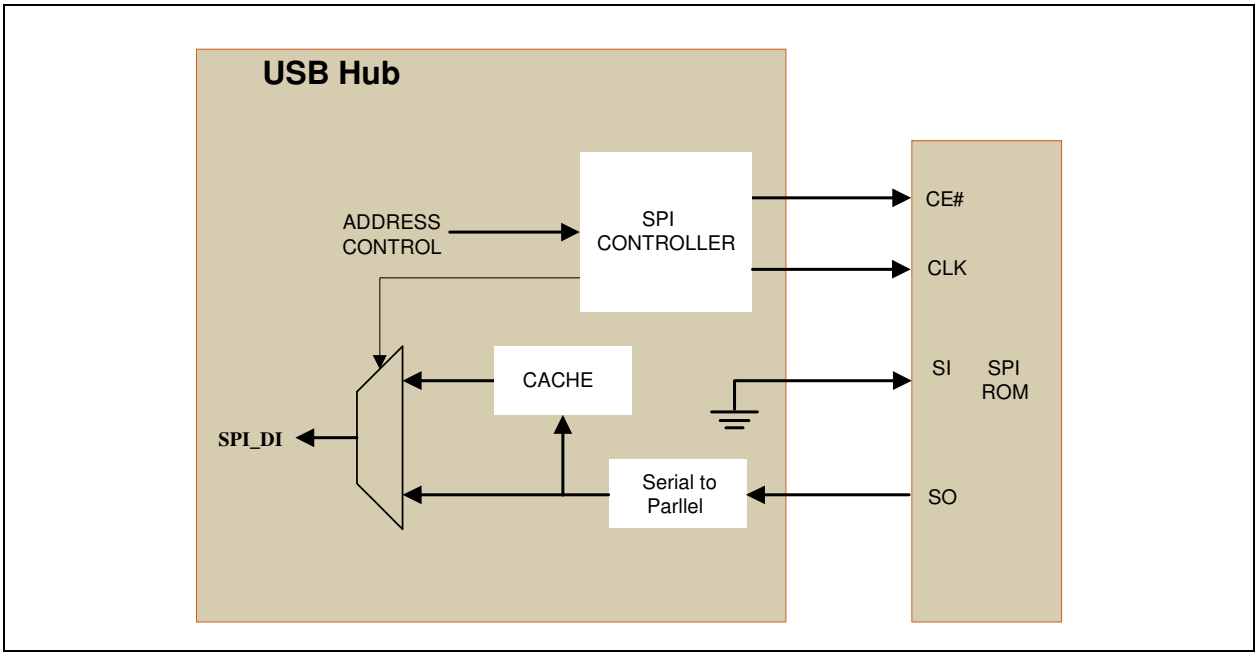
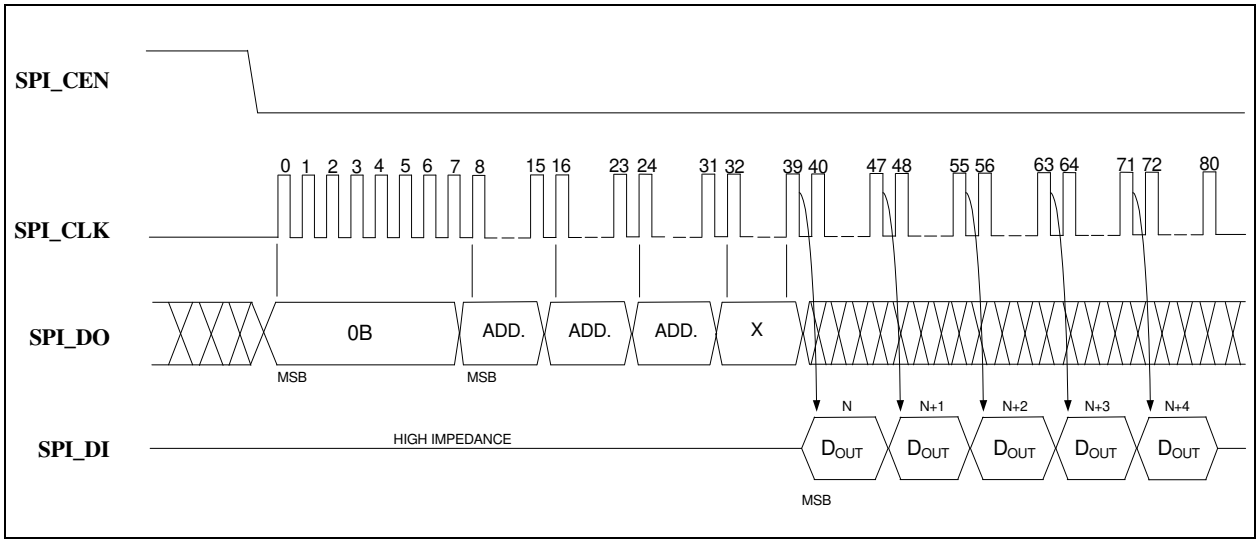


FIGURE 4-2: SPI HI-SPEED READ SEQUENCE



4.1.2 OPERATION OF THE DUAL HI-SPEED READ SEQUENCE

The SPI controller also supports dual data mode (at 30 MHz SPI speed only). When configured in dual mode, the SPI controller will automatically handle reads going out to the SPI ROM. When the controller detects a read, the controller drops the **SPI_CE_N**, and puts out a 0x3B, followed by the 24-bit address. The SPI controller then puts out a DUMMY byte. The next four clocks clock in the first byte. The data appears two bits at a time on data out and data in. When the first byte is clocked in a ready signal is sent back to the processor, and the processor gets one byte.

After the processor gets the first byte, the address will change. If the address is one more than the last address, the SPI controller will clock out one more byte. If the address in anything other than one more than the last address, the SPI controller will terminate the transaction by taking **SPI_CE_N** high. As long as the addresses are sequential, the SPI Controller will keep clocking in data.

FIGURE 4-3: SPI DUAL HI-SPEED READ OPERATION

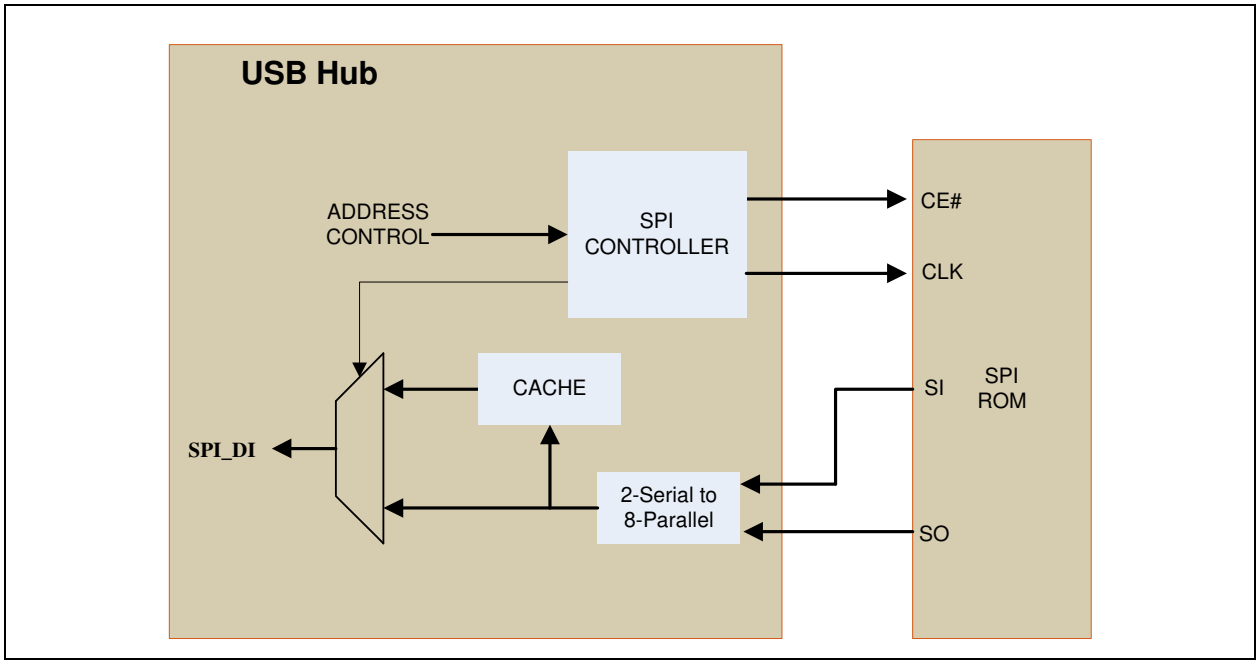
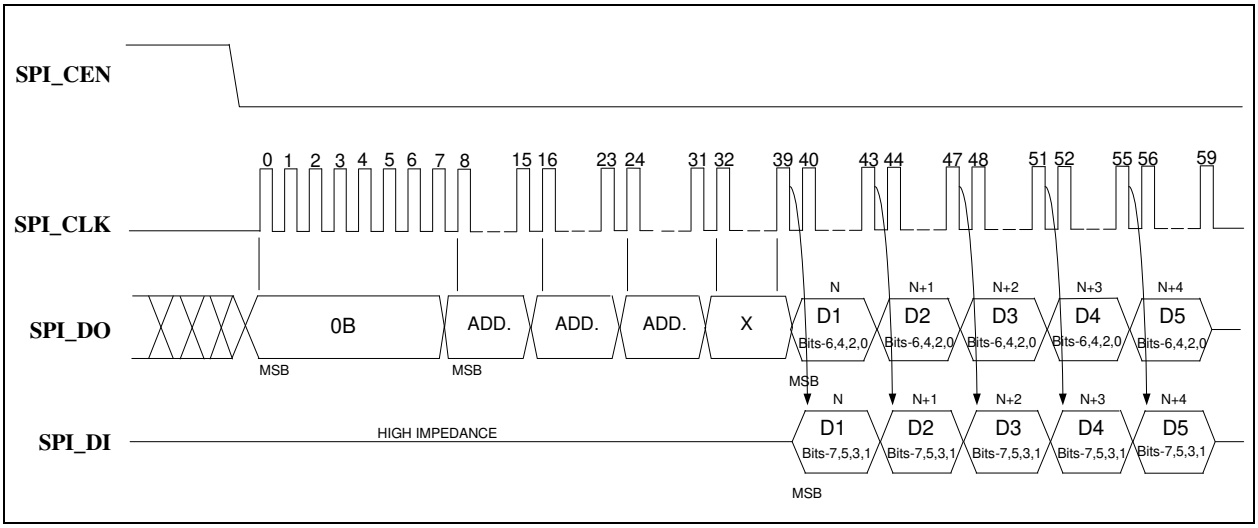


FIGURE 4-4: SPI DUAL HI-SPEED READ SEQUENCE



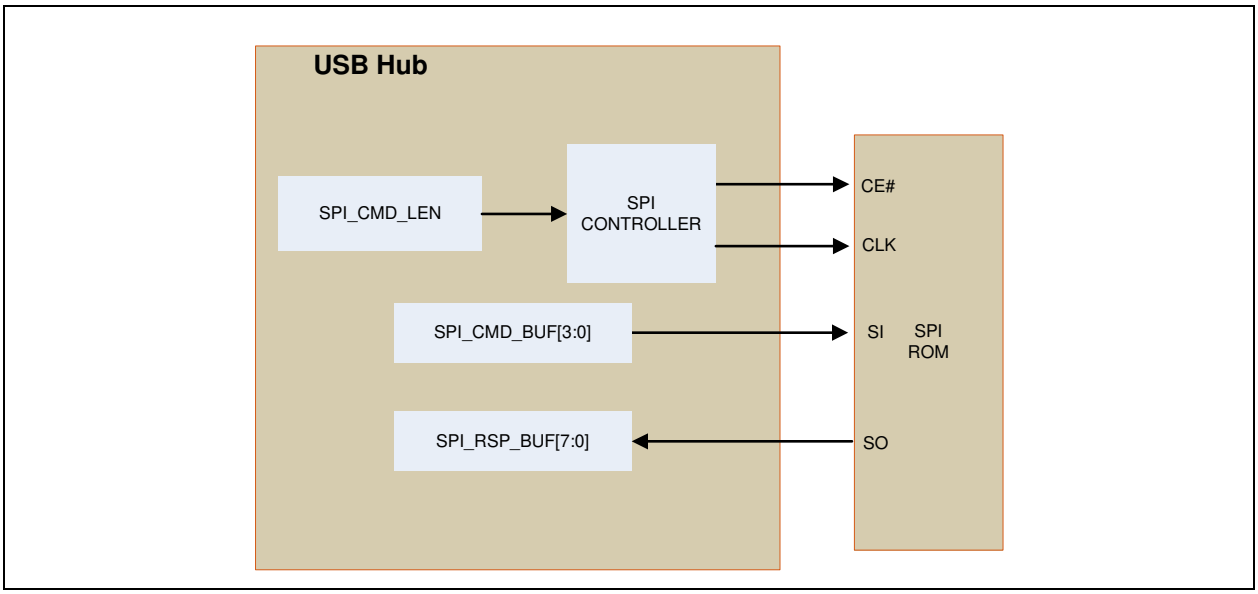
4.1.3 32-BYTE CACHE

There is a 32-byte pipeline cache, and associated with the cache is a base address pointer and a length pointer. Once the SPI controller detects a jump, the base address pointer is initialized to that address. As each new sequential data byte is fetched, the data is written into the cache, and the length is incremented. If the sequential run exceeds 32 bytes, the base address pointer is incremented to indicate the last 32 bytes fetched. If the USB5533B does a jump, and the jump is in the cache address range, the fetch is done in 1 clock from the internal cache instead of an external access.

4.1.4 INTERFACE OPERATION TO SPI PORT WHEN NOT DOING FAST READS

There is an 8-byte command buffer: SPI_CMD_BUF[7:0]; an 8-byte response buffer: SPI_RESP_BUF[7:0]; and a length register that counts out the number of bytes: SPI_CMD_LEN. Additionally, there is a self-clearing **GO** bit in the SPI_CTL Register. Once the **GO** bit is set, the device drops **SPI_CE_N**, and starts clocking. It will put out SPI_CMD_LEN X 8 number of clocks. After the first byte, the COMMAND, has been sent out, and the **SPI_DI** is stored in the SPI_RESP buffer. If the SPI_CMD_LEN is longer than the SPI_CMD_BUF, don't cares are sent out on the **SPI_DO** line. This mode is used for program execution out of internal RAM or ROM.

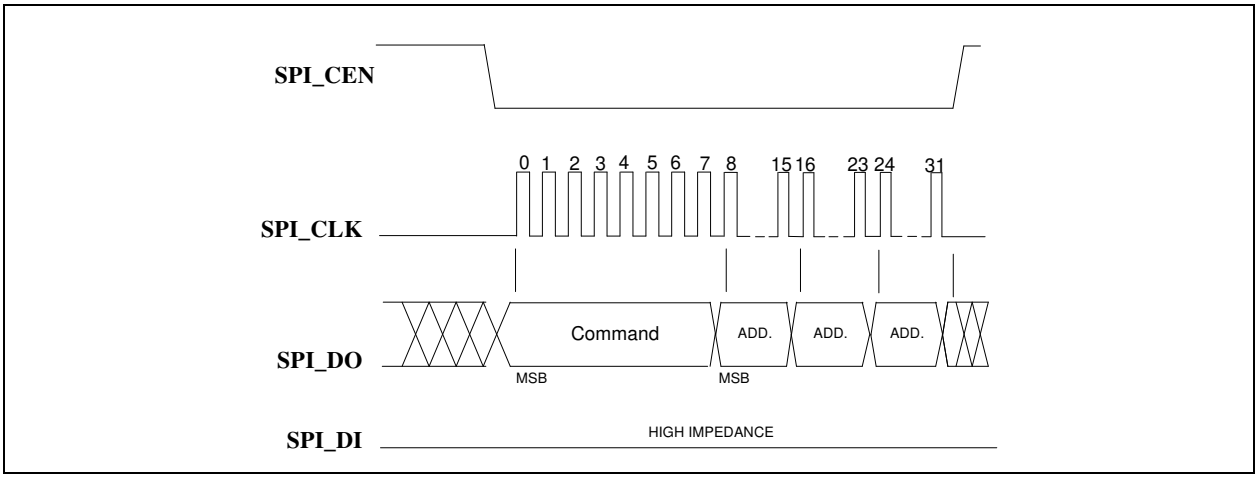
FIGURE 4-5: SPI INTERNALLY-CONTROLLED OPERATION



4.1.4.1 ERASE EXAMPLE

To perform a SCTR_ERASE, 32BLK_ERASE, or 64BLK_ERASE, the device writes 0x20, 0x52, or 0xD8, respectively to the first byte of the command buffer, followed by a 3-byte address. The length of the transfer is set to 4 bytes. To do this, the device first drops **SPI_CE_N**, then counts out 8 clocks. It then puts out the 8 bits of command, followed by 24 bits of address of the location to be erased on the **SPI_DO** pin. When the transfer is complete, the **SPI_CE_N** goes high, while the **SPI_DI** line is ignored in this example.

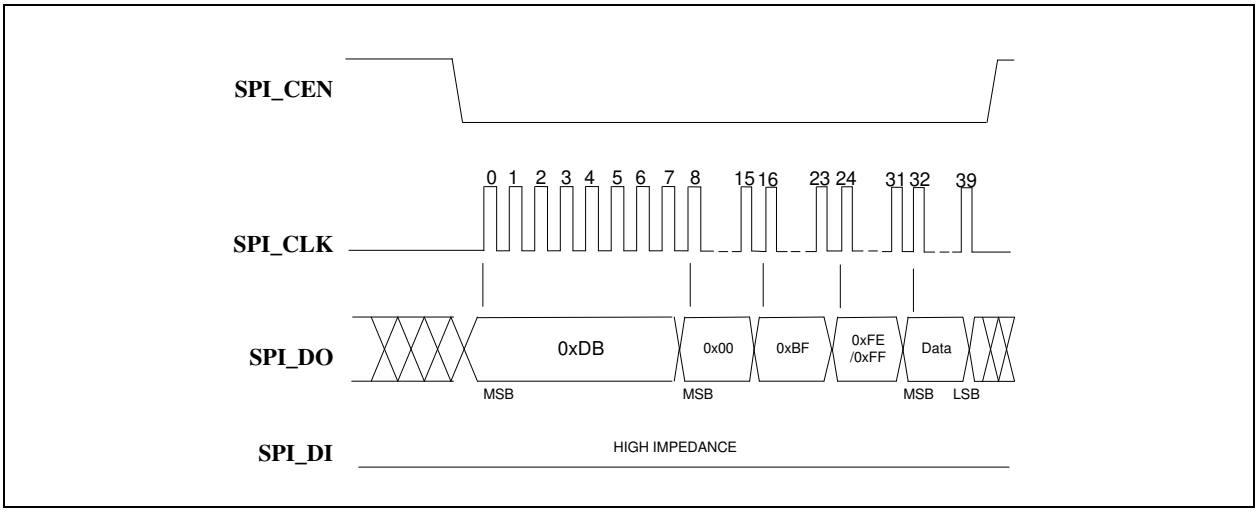
FIGURE 4-6: SPI ERASE SEQUENCE



4.1.4.2 BYTE PROGRAM EXAMPLE

To perform a Byte Program, the device writes 0x02 to the first byte of the command buffer, followed by a 3-byte address of the location that will be written to, and one data byte. The length of the transfer is set to 5 bytes. The device first drops **SPI_CE_N**, 8 bits of command are clocked out, followed by 24 bits of address, and one byte of data on the **SPI_DO** pin. The **SPI_DI** line is not used in this example.

FIGURE 4-7: SPI BYTE PROGRAM



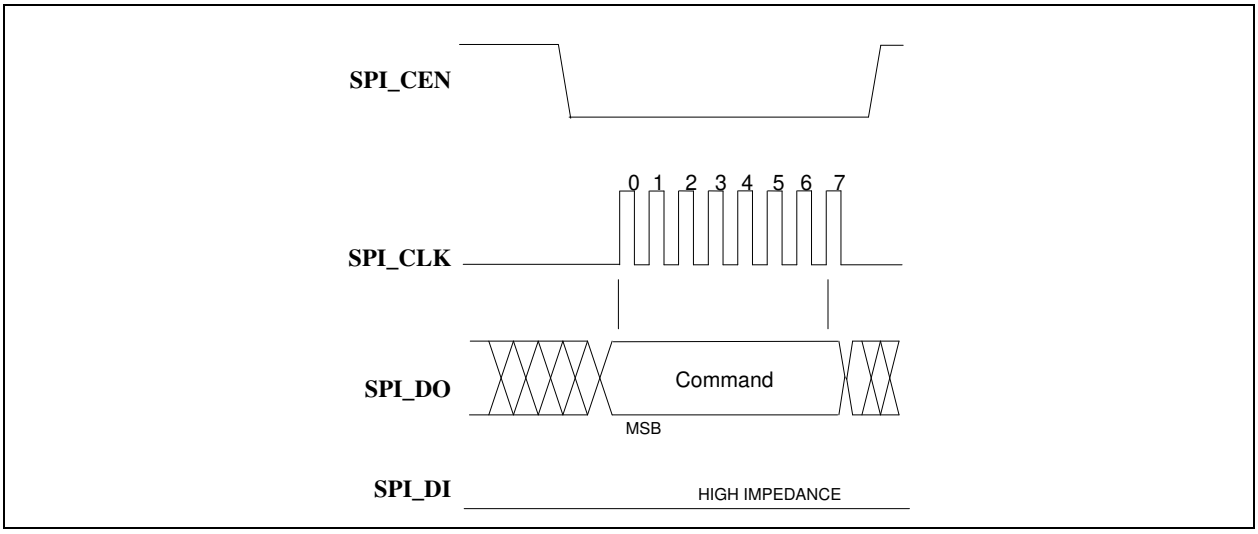
4.1.4.3 COMMAND ONLY PROGRAM EXAMPLE

To perform a single byte command such as the following:

- - WRDI
- - WREN
- - EWSR
- - CHIP_ERASE
- - EBSY
- - DBSY

The device writes the opcode into the first byte of the SPI_CMD_BUF and the SPI_CMD_LEN is set to one. The device first drops **SPI_CE**, then 8 bits of the command are clocked out on the **SPI_DO** pin. The **SPI_DI** is not used in this example.

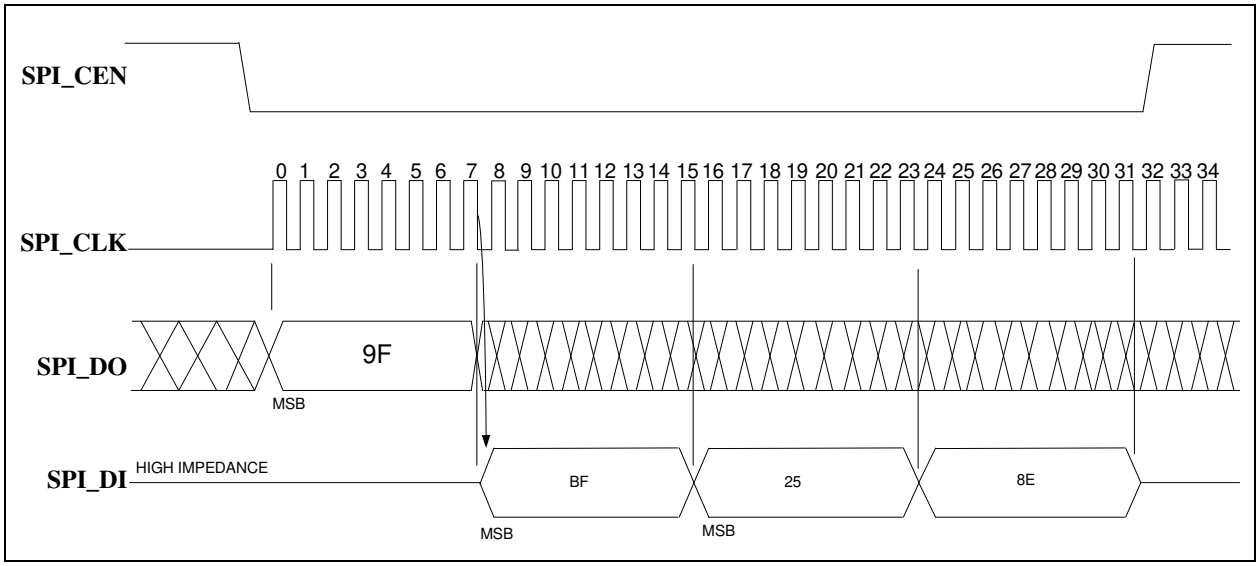
FIGURE 4-8: SPI COMMAND ONLY SEQUENCE



4.1.4.4 JEDEC-ID READ EXAMPLE

To perform a JEDEC-ID command, the device writes 0x9F into the first byte of the SPI_CMD_BUF and the length of the transfer is 4 bytes. The device first drops **SPI_CE_N**, then 8 bits of the command are clocked out, followed by the 24 bits of dummy bytes (due to the length being set to 4) on the **SPI_DO** pin. When the transfer is complete, the **SPI_CE_N** goes high. After the first byte, the data on **SPI_DI** is clocked into the SPI_RSP_BUF. At the end of the command, there are three valid bytes in the SPI_RSP_BUF. In this example, 0xBF, 0x25, 0x8E.

FIGURE 4-9: SPI JEDEC-ID SEQUENCE



4.2 SMBus Slave Interface

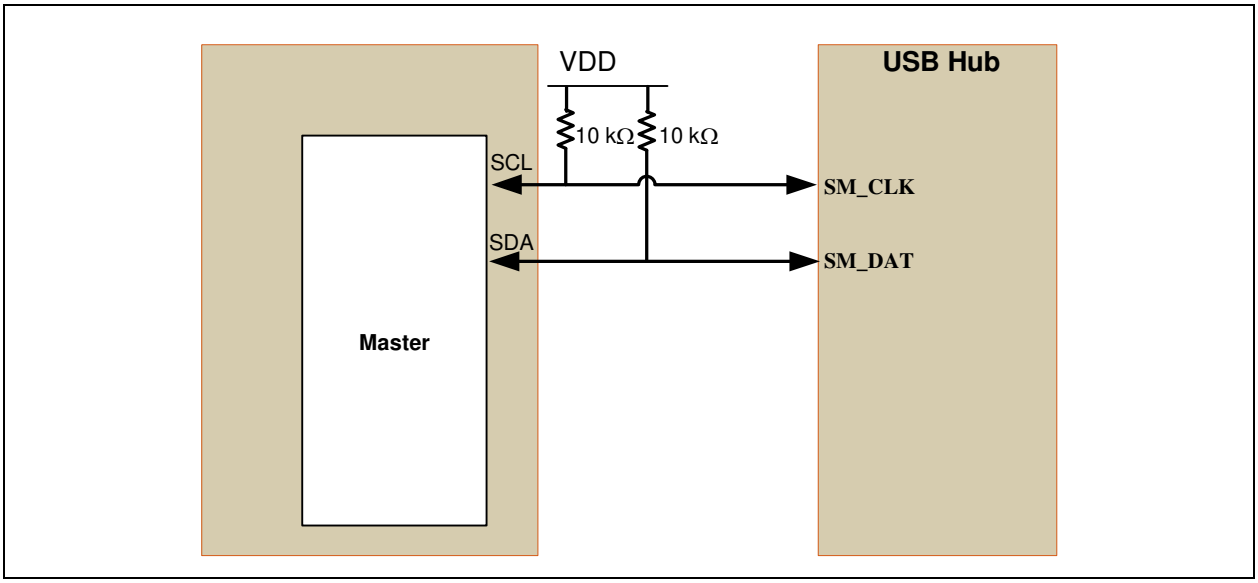
Next, the USB5533B will look to receive configuration and commands from an optional SMBus master (if present). When SMBus is enabled, the SMBus can operate in either legacy (USB 2.0 only) or advanced mode (access to both USB 2.0 and 3.0 registers). Next, the USB5533B will look for (optional) configuration present in the internal OTP memory. Any register settings that are modified via the SMBus interface will overwrite the internal OTP settings.

The SMBus slave interface is enabled when pull-up resistors are detected on both **SM_DAT** and **SM_CLK** for the first millisecond after reset. For operation in SMBus Legacy Mode, an additional pull-up resistor is required on **TRST**. If the SMBus interface is enabled, then the USB5533B will wait indefinitely for the SMBus host to configure the device. Once SMBus configuration is complete, device initialization will proceed. To disable the SMBus, a pull-down resistor of 10 KΩ must be applied to either **SM_DAT**, **SM_CLK**, or both **SM_DAT** and **SM_CLK** if desired. If SMBus is disabled, the device proceeds directly to device initialization using the internal OTP ROM.

4.2.1 PULL-UP RESISTOR FOR SMBUS

External pull-up resistors (10 kΩ recommended) are required on the **SM_DAT** and **SM_CLK** pins when implementing either SMBus mode.

FIGURE 4-10: SMBUS SLAVE CONNECTION



4.2.1.1 Invalid Protocol Response Behavior

Note that any attempt to update registers with an invalid protocol will not be updated. The only valid protocols are write block and read block (described Section 5.5, "SMBus Slave Interface," on page 29), where the hub only responds to the 7-bit hardware selected slave addresses (0101100b or 0101101b). Additionally, the only valid registers for the hub are outlined in the *USB5533B Configuration Release Notes* documentation.

4.2.2 SLAVE DEVICE TIMEOUT

Devices in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds 25 ms ($T_{TIMEOUT, MIN}$). The master must detect this condition and generate a stop condition within or after the transfer of the interrupted data byte. Slave devices must reset their communication and be able to receive a new START condition no later than 35 ms ($T_{TIMEOUT, MAX}$).

Note:	Some simple devices do not contain a clock low drive circuit; this simple kind of device typically resets its communications port after a start or stop condition. The slave device timeout must be implemented.

4.2.3 STRETCHING THE SCLK SIGNAL

The hub supports stretching of the **SCLK** by other devices on the SMBus. The hub will stretch the clock as needed.

4.2.4 BUS RESET SEQUENCE

The SMBus slave interface resets and returns to the idle state upon a START condition followed immediately by a STOP condition.

4.2.5 SMBUS ALERT RESPONSE ADDRESS

The SMBALERT# signal is not supported by the USB5533B.

4.3 Reset

There are two different resets that the device experiences. One is a hardware reset (either from the internal POR reset circuit or via the **RESET_N** pin) and the second is a USB Bus Reset.

4.3.1 INTERNAL POR

All reset timing parameters are guaranteed by design.

4.3.2 EXTERNAL HARDWARE RESET

A valid hardware reset is defined as assertion of **RESET_N** for a minimum of 1 µs after all power supplies are within operating range.

Assertion of **RESET_N** (external pin) causes the following:

1. The PHY is disabled, and the differential pairs will be in a high-impedance state.
2. All transactions immediately terminate; no states are saved.
3. All internal registers return to the default state.
4. The external crystal oscillator is halted.
5. The PLL is halted.

4.4 Standard Port Power Configuration

The device natively operates with standard port power controllers or poly-fuse devices for the downstream port powers when battery charging is not enabled on a port. It is not recommended to have the downstream ports of a single device mix poly-fuse and standard power controller support, as the configuration of the hub cannot correctly report which ports are poly-fuse and which are port power controllers to the host.

Any port without battery charging can also be used in individual port power controls or ganged power controls. The port power control output only supports either Ganged or Individual modes on a global basis for all downstream ports.

The overcurrent setting also supports individual or global settings, but also adds the ability to configure specific ports to be part of an overcurrent gang with others setup for individual connections. This hybrid configuration should only be used when utilizing poly-fuse power devices.

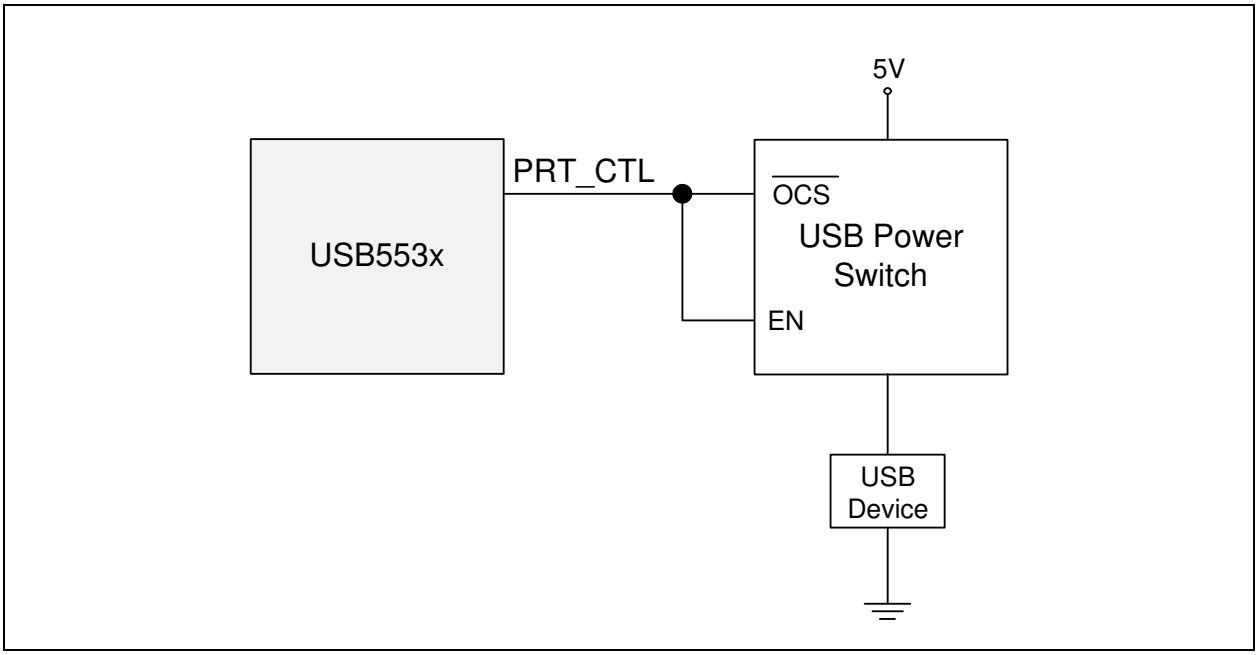
4.4.1 PORT POWER CONTROLLER

The most common method for downstream port power controls is to utilize current-limited power switches for USB applications. The devices allow the downstream port powers to be enabled through a control signal and report over-current conditions through a flag output.

Two connection methods are possible for these controllers, Combined mode and Independent mode.

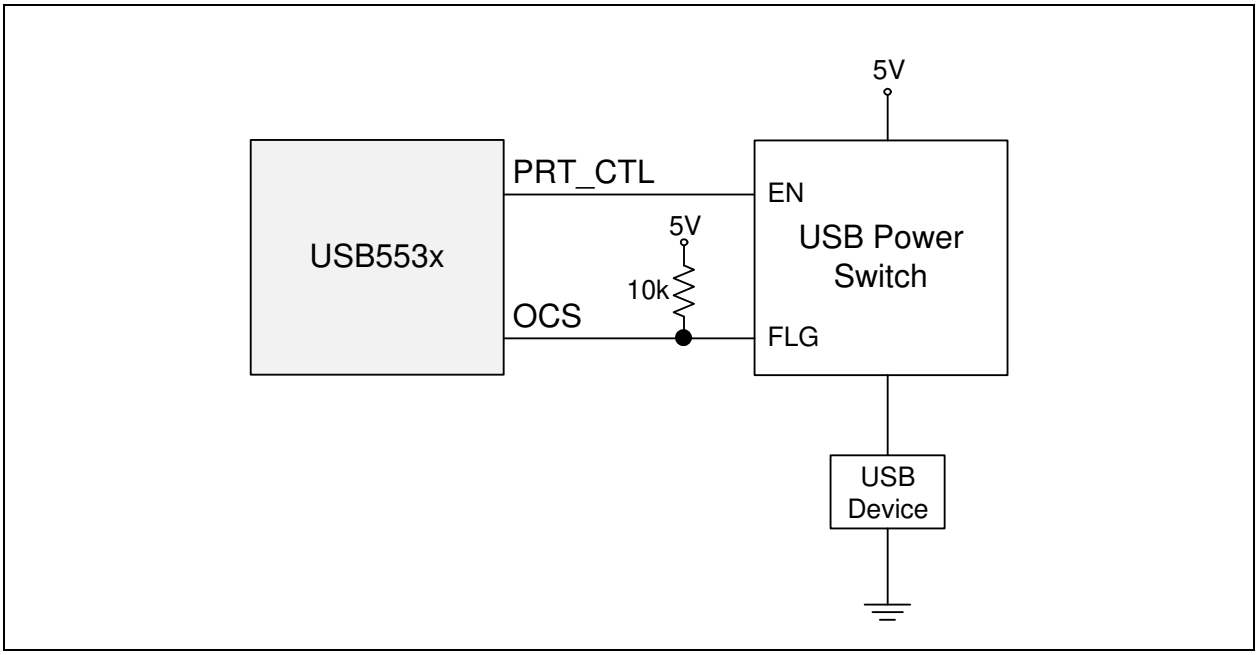
In Combined mode, the FLG and EN signals are tied together with an external 10K ohm pull-up and driven to a single PRT_CTL signal on the device, as shown in Figure 4-11.

FIGURE 4-11: COMBINED MODE IMPLEMENTATION



In Individual mode, the PRT_CTL signal is driven directly to the EN input of the power switch and the OCS input is connected to the FLG output of the power switch with a 10K pull-up connected, as shown in Figure 4-12.

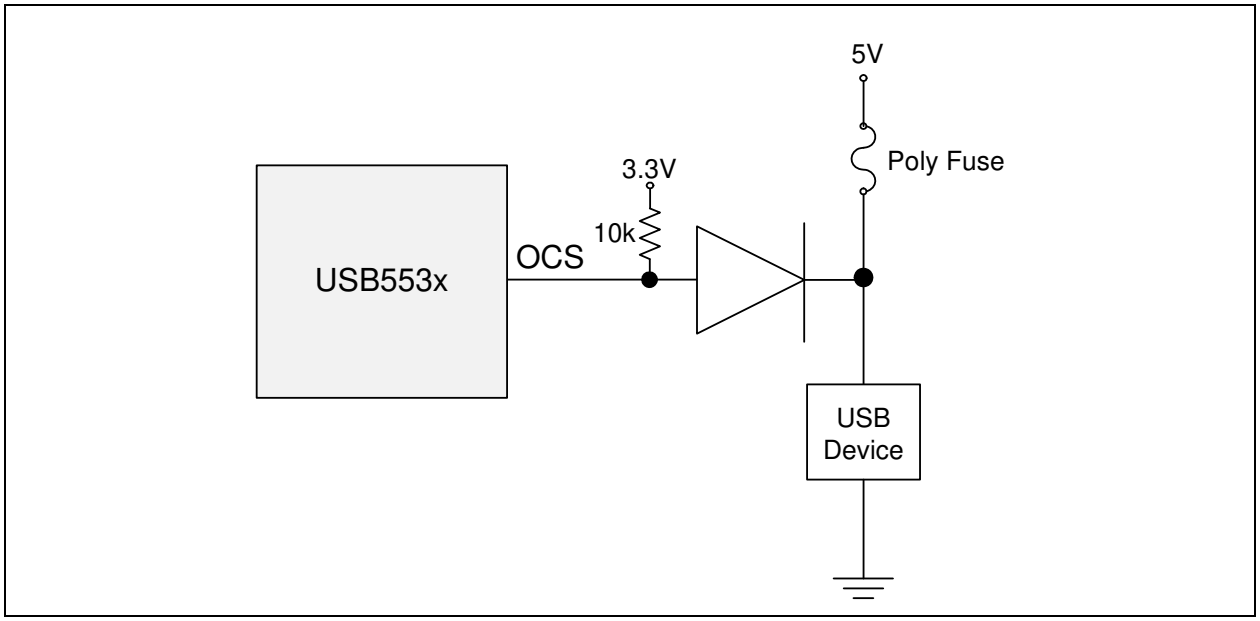
FIGURE 4-12: INDIVIDUAL MODE IMPLEMENTATION



4.4.2 POLY-FUSE

An alternate method of downstream power control is to utilize poly-fuse devices. In this configuration, the poly-fuse devices are used to report overcurrent conditions to the USB5533B through the OCS input, as shown in Figure 4-13.

FIGURE 4-13: POLY-FUSE IMPLEMENTATION



4.5 Charging Port Configurations

The device can also be configured to operate as a charging port for one or more downstream ports. Ganged port power control and/or overcurrent is not supported if any of the downstream ports are configured as charging ports. If a port is configured to support a charging port mode, either a standard port power controller or a UCS1002 may be implemented.

For more information on charging port support, refer to Section 5.1, "Charging Port Configuration," on page 24.

4.5.1 PORT POWER CONTROLLER

The only special limitation of using the device as a charging port is that the port power controller must be capable of the higher current to support the charging port modes. Refer to Section 4.4.1, "Port Power Controller," on page 20 for more information on this implementation.

4.5.2 UCS1002

Using a UCS1002 device as a downstream port power controller is only supported on ports that are enabled as charging ports.

If the UCS1002 is implemented, the USB5533B communicates with all of the implemented UCS1002 ports over SMBus using one of the PRT_CTLx/OCSx signals as the SMCLK/SMDAT. Additionally, DYNCPDIS_N becomes the UCS_SMBALERT_N signal. Multiple UCS1002 devices may be connected to the SMBus in parallel.

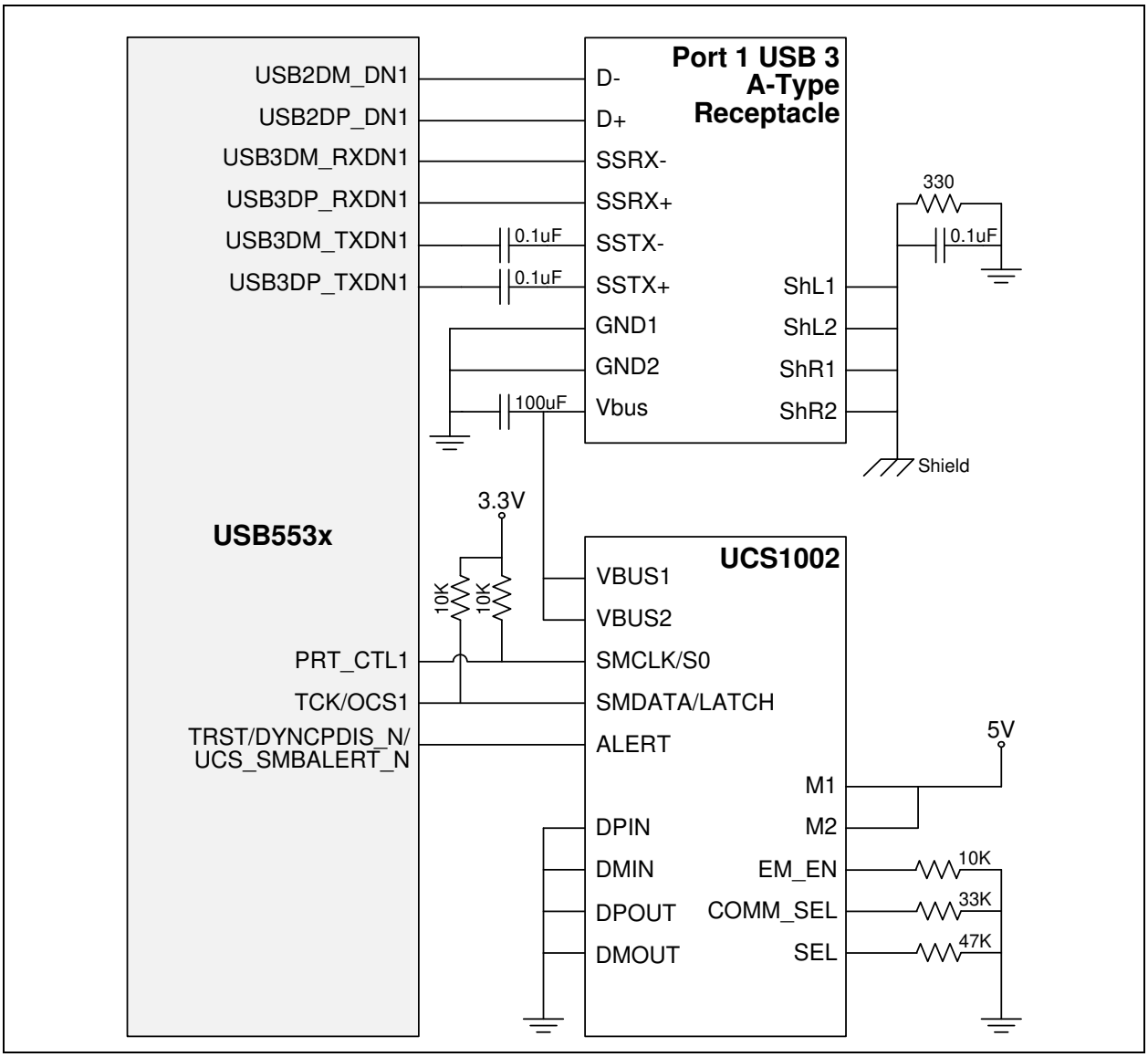
After reset, for any enabled charging ports, the USB5533B performs SMBus commands on the configured PRT_CTLx/OCSx signals and checks UCS1002 devices at specific addresses (see Table 4-1) to confirm which ports are utilizing UCS1002 devices as the downstream power controllers.

TABLE 4-1: UCS1002 ADDRESS MAPPING

Port	Address
1	0x30
2	0x31
3	0x32

In this configuration, the UCS1002 is utilized as an SMBus enabled port power switch and all charging port handshaking on the D+/D- signals are controlled directly from the USB5533B. An example implementation can be seen in Figure 4-14.

FIGURE 4-14: UCS1002 CHARGING IMPLEMENTATION



5.0 FUNCTIONAL OPERATION

This chapter details the functional operation of various device features.

5.1 Charging Port Configuration

The USB5533B supports downstream charging ports on any available port. The hub contains internal hardware and algorithms to natively support various voltage levels on the D+/D- signals along with the BC 1.2 Handshaking protocol, allowing charging devices to detect the downstream port as a charging port.

A port can be configured for either RapidCharge support or Samsung Legacy Charging mode support. This section details the various charging port modes. The following terminology will be helpful in the understanding of these features:

- SDP - Standard Downstream Port - A port that is not operating as a charging port and has active USB communications.
- CDP - Charging Downstream Port - A port that is operating as a charging port and has active USB communications.
- DCP - Dedicated Charging Port - A port that is operating as a charging port but has no USB communications.
- S0 - Normal system power state in full run.
- S3 - Typically a Sleep state, where the system can be woken from USB HID devices
- S4 - Typically a Hibernate sleep state, where the system state is stored to a hard drive and does not support wake from USB HID devices.
- S5 - Typically an OFF state for a system.

5.1.1 RAPID CHARGE

This mode enables concurrent operation of Apple, BC 1.2 and DP/DM Shorted Emulation charging. The only applicable options are to choose Apple 1A or Apple 2A charging mode on a per port basis. Refer to Section 5.2.1.1, "Apple Charging Mode," on page 26.

Note:	Apple and DP/DM Shorted Emulation charging modes are only operational in DCP mode.

5.1.2 SAMSUNG LEGACY CHARGING

This mode drives a specified voltage on the DP/DM lines to allow legacy Samsung devices to detect the port as Charging capable. This is only operational in DCP modes.

5.1.3 DYNAMIC CHARGING PORT (6080 ONLY)

Dynamic Charging Port support utilizes the device's DYNCPDIS_N pin to disable Battery Charging support globally when low and, when high, allow any ports configured as Charging Ports (either through a configuration file or straps) to resume their Battery Charging operation in the configured Charging mode.

This feature is currently supported only when using standard USB port power controllers. Please contact your Microchip FAE if required to use this feature with other port power controller configurations.

Figure 5-1, Figure 5-2, and Figure 5-3 detail the operation of Dynamic Charging Port in the S0, S3, and S4/S5 power modes, respectively. For any of the flow diagram transitions, there is a Y/Z nomenclature.

Y = Dynamic BC enable signal

Z = Device attached and sensed by device

Note:	The Dynamic Charging Port feature and related DYNCPDIS_N pin function is available in the "-6080" version of the device only.

FIGURE 5-1: S0 STATE TRANSITIONS

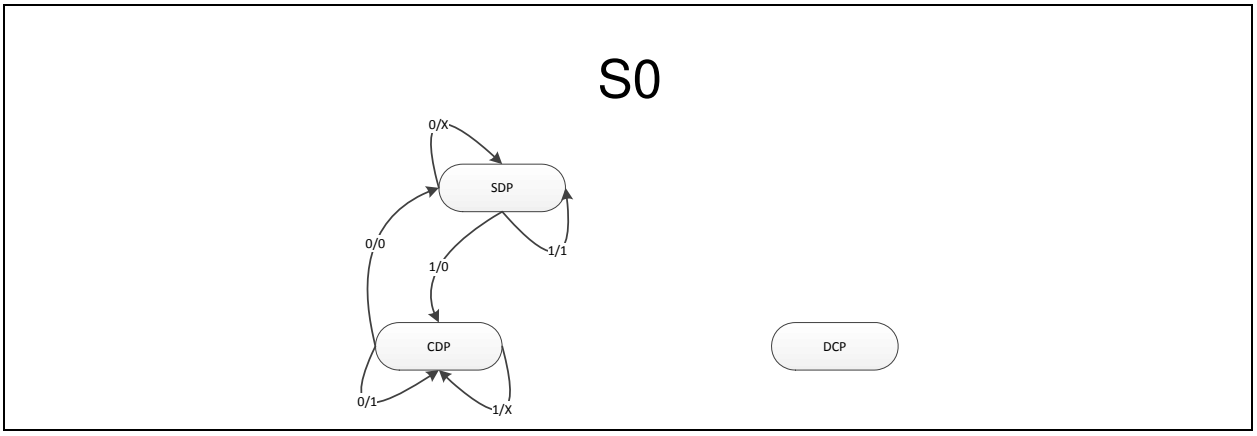


FIGURE 5-2: S3 STATE TRANSITIONS

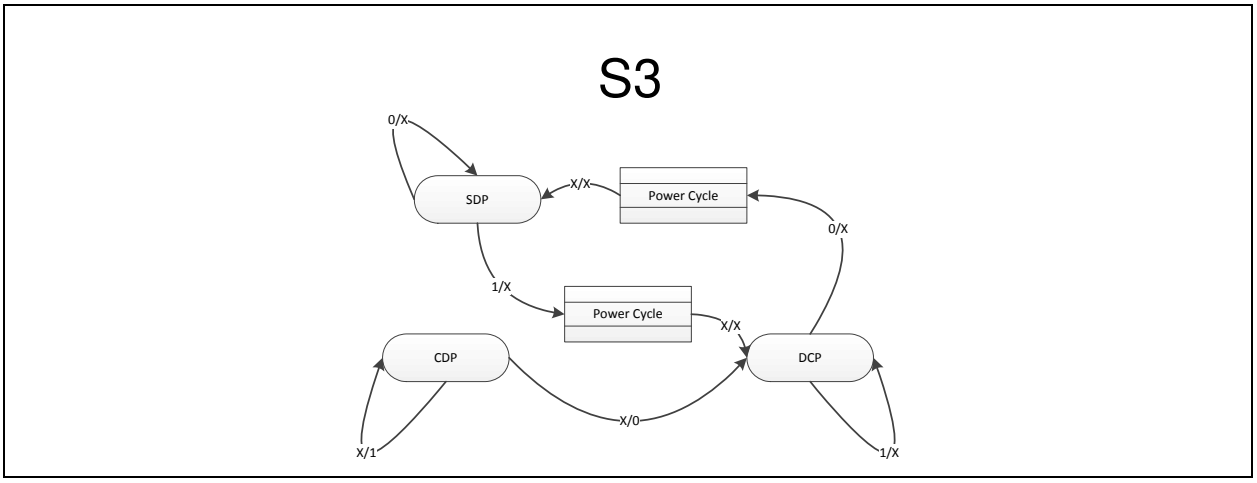


FIGURE 5-3: S4/S5 STATE TRANSITIONS