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USB5734

4-Port SS/HS USB Controller Hub

Highlights

- USB Hub Feature Controller IC with 4 USB 3.1 Gen 1 / USB 2.0 downstream ports
- USB-IF Battery Charger revision 1.2 support on up & downstream ports (DCP, CDP, SDP)
- **FlexConnect**: Downstream port able to swap with upstream port, allowing master capable devices to control other devices on the hub
- USB to I^2C/UART/SPI/GPIO bridge endpoint support
- USB Link Power Management (LPM) support
- Enhanced OEM configuration options available through either OTP or SPI ROM
- Available in 64-pin (9 x 9 mm) VQFN lead-free, RoHS compliant package
- Commercial and industrial grade temperature support
- Configuration Straps: Predefined configuration of system level functions including GPIOs

Target Applications

- Standalone USB Hubs
- Laptop Docks
- PC Motherboards
- PC Monitor Docks
- Multi-function USB 3.1 Gen 1 Peripherals

Key Benefits

- USB 3.1 Gen 1 compliant 5 Gbps, 480 Mbps, 12 Mbps and 1.5 Mbps operation
  - 5 V tolerant USB 2.0 pins
  - 1.32 V tolerant USB 3.1 Gen 1 pins
  - Integrated termination & pull-up/pull-down resistors
- Supports per port battery charging of most popular battery powered devices
  - USB-IF Battery Charging rev. 1.2 support (DCP, CDP, SDP)
  - Apple® portable product charger emulation
  - Chinese YD/T 1591-2006 charger emulation
  - Chinese YD/T 1591-2009 charger emulation
  - European Union universal mobile charger support
  - Support for Microchip USC100x family of battery charging controllers
  - Supports additional portable devices
- Smart port controller operation
  - Firmware handling of companion port controllers
- On-chip microcontroller
  - Manages I/Os, VBUS, and other signals
- 8 KB RAM, 64 KB ROM
- 8 KB One Time Programmable (OTP) ROM
  - Includes on-chip charge pump
- Configuration programming via OTP ROM, SPI ROM, or SMBus
- **PortSwap**
  - Configurable differential intro-pair signal swapping
- **PHYBoost™**
  - Programmable USB transceiver drive strength for recovering signal integrity
- **VariSense™**
  - Programmable USB receiver sensitivity
- Compatible with Microsoft Windows 8, 7, XP, Apple OS X 10.4+, and Linux hub drivers
- Optimized for low-power operation and low thermal dissipation
- Package
  - 64-pin VQFN (9 x 9 mm)
- Environmental
  - 3 kV HBM JESD22-A114F ESD protection
  - Commercial temperature range (0°C to +70°C)
  - Industrial temperature range (-40°C to +85°C)

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1.0 PREFACE

1.1 General Terms

TABLE 1-1: GENERAL TERMS

Term	Description
ADC	Analog-to-Digital Converter
Byte	8 bits
CDC	Communication Device Class
CSR	Control and Status Registers
DWORD	32 bits
EOP	End of Packet
EP	Endpoint
FIFO	First In First Out buffer
FS	Full-Speed
FSM	Finite State Machine
GPIO	General Purpose I/O
HS	Hi-Speed
HSOS	High Speed Over Sampling
Hub Feature Controller	The Hub Feature Controller, sometimes called a Hub Controller for short is the internal processor used to enable the unique features of the USB Controller Hub. This is not to be confused with the USB Hub Controller that is used to communicate the hub status back to the Host during a USB session.
I^2C	Inter-Integrated Circuit
LS	Low-Speed
lsb	Least Significant Bit
LSB	Least Significant Byte
msb	Most Significant Bit
MSB	Most Significant Byte
N/A	Not Applicable
NC	No Connect
OTP	One Time Programmable
PCB	Printed Circuit Board
PCS	Physical Coding Sublayer
PHY	Physical Layer
PLL	Phase Lock Loop
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
SDK	Software Development Kit
SMBus	System Management Bus
UUID	Universally Unique IDentifier
WORD	16 bits

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1.2 Reference Documents

1. *UNICODE UTF-16LE For String Descriptors* USB Engineering Change Notice, December 29th, 2004, http://www.usb.org
2. *Universal Serial Bus Revision 3.1 Specification*, http://www.usb.org
3. *Battery Charging Specification*, Revision 1.2, Dec. 07, 2010, http://www.usb.org
4. *I^2C-Bus Specification*, Version 1.1, http://www.nxp.com
5. *System Management Bus Specification*, Version 1.0, http://smbus.org/specs

2.0 INTRODUCTION

2.1 General Description

The Microchip USB5734 hub is low-power, OEM configurable, USB 3.1 Gen 1 hub feature controller with 4 downstream ports and advanced features for embedded USB applications. The USB5734 is fully compliant with the *Universal Serial Bus Revision 3.1 Specification* and *USB 2.0 Link Power Management Addendum*. The USB5734 supports 5 Gbps SuperSpeed (SS), 480 Mbps Hi-Speed (HS), 12 Mbps Full-Speed (FS), and 1.5 Mbps Low-Speed (LS) USB downstream devices on all enabled downstream ports.

The USB5734 supports the legacy USB speeds (HS/FS/LS) through a dedicated USB 2.0 hub feature controller that is the culmination of five generations of Microchip hub feature controller design and experience with proven reliability, interoperability, and device compatibility. The SuperSpeed hub feature controller operates in parallel with the USB 2.0 controller, decoupling the 5 Gbps SS data transfers from bottlenecks due to the slower USB 2.0 traffic.

The USB5734 enables OEMs to configure their system using “Configuration Straps.” These straps simplify the configuration process assigning default values to USB3.1 Gen 1 ports and GPIOs OEMs can disable ports, enable battery charging and define GPIO functions as default assignments on power up removing the need for OTP or external SPI ROM.

The USB5734 supports downstream battery charging. The USB5734 integrated battery charger detection circuitry supports the USB-IF Battery Charging (BC1.2) detection method and most Apple devices. The USB5734 provides the battery charging handshake and supports the following USB-IF BC1.2 charging profiles:

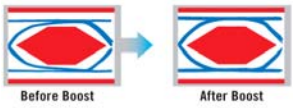
- DCP: Dedicated Charging Port (Power brick with no data)
- CDP: Charging Downstream Port (1.5A with data)
- SDP: Standard Downstream Port (0.5A with data)
- Custom profiles loaded via SMBus or OTP

The USB5734 provides an additional USB endpoint dedicated for use as a USB to I^2C/UART/SPI/GPIO interface, allowing external circuits or devices to be monitored, controlled, or configured via the USB interface. Additionally, the USB5734 includes many powerful and unique features such as:

FlexConnect, which provides flexible connectivity options. One of the USB5734’s downstream ports can be reconfigured to become the upstream port, allowing master capable devices to control other devices on the hub.

PortSwap, which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.

PHYBoost, which provides programmable levels of Hi-Speed USB signal drive strength in the downstream port transceivers. PHYBoost attempts to restore USB signal integrity in a compromised system environment. The graphic on the right shows an example of Hi-Speed USB eye diagrams before and after PHYBoost signal integrity restoration. in a compromised system environment



VariSense, which controls the USB receiver sensitivity enabling programmable levels of USB signal receive sensitivity. This capability allows operation in a sub-optimal system environment, such as when a captive USB cable is used.

The USB5734 can be configured for operation through internal default settings. Custom OEM configurations are supported through external SPI ROM or OTP ROM. All port control signal pins are under firmware control in order to allow for maximum operational flexibility, and are available as GPIOs for customer specific use.

The USB5734 is available in commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature ranges. An internal block diagram of the USB5734 is shown in Figure 2-1.

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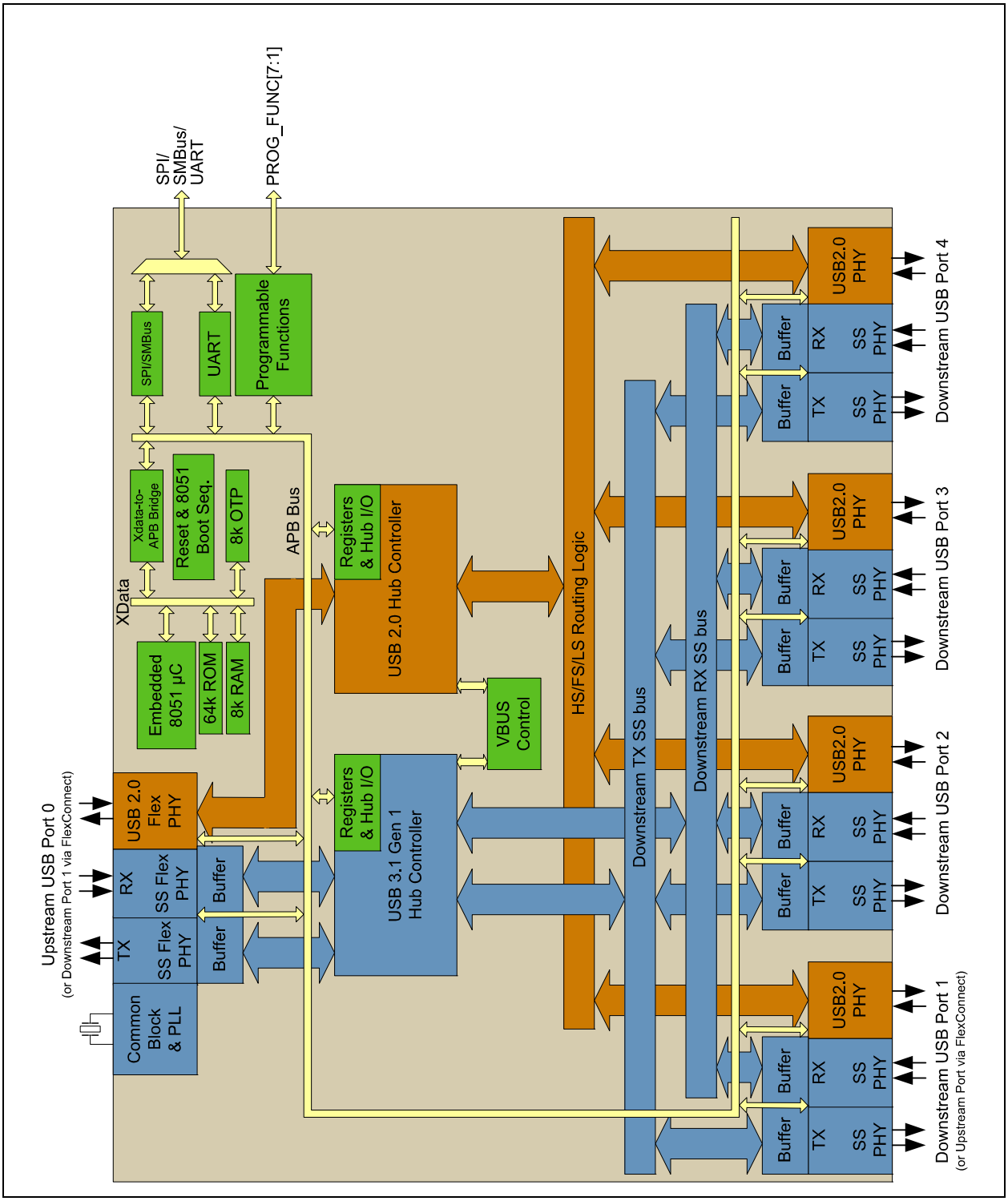
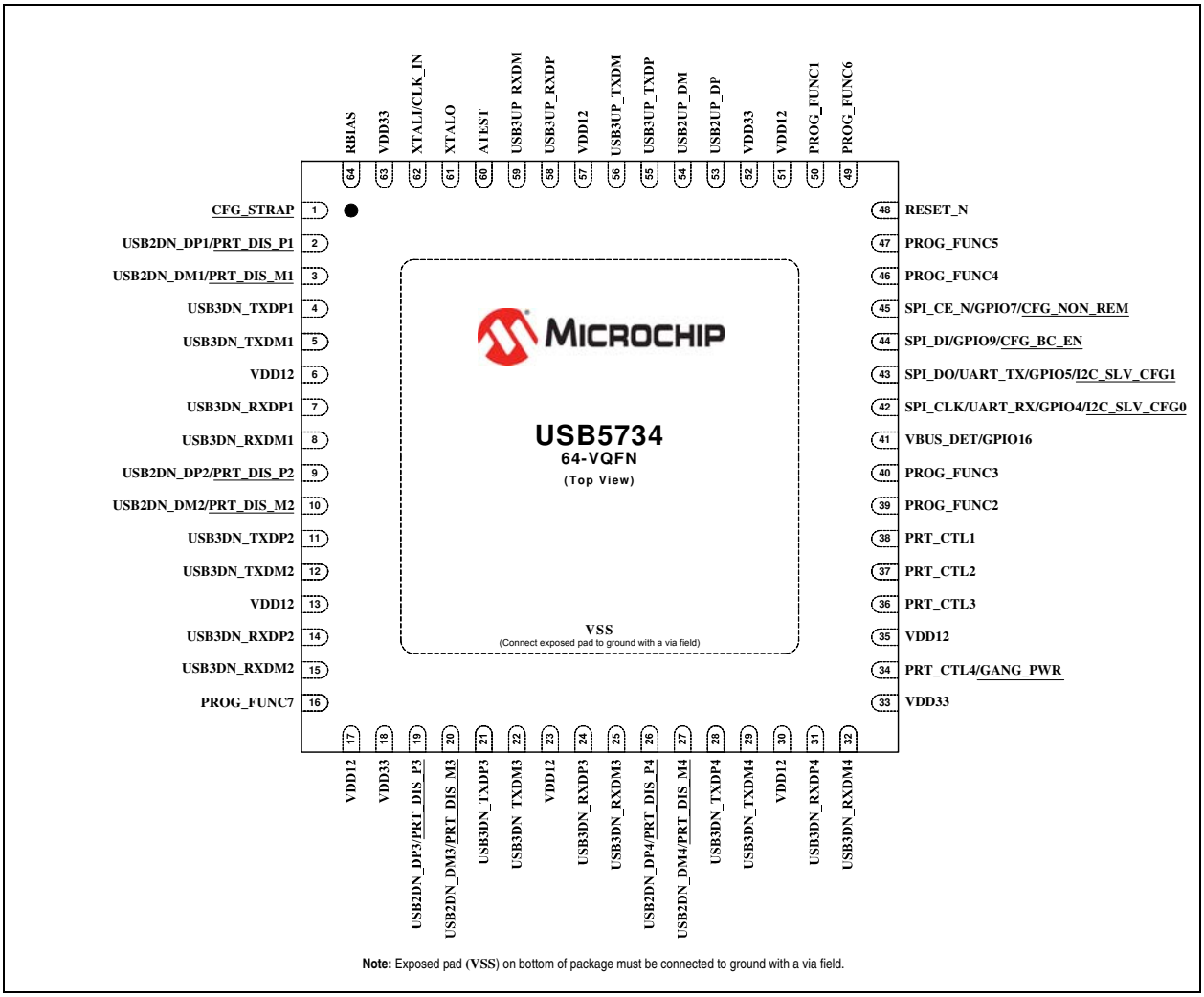
FIGURE 2-1: INTERNAL BLOCK DIAGRAM



3.0 PIN DESCRIPTION AND CONFIGURATION

3.1 Pin Assignments

FIGURE 3-1: 64-VQFN PIN ASSIGNMENTS



Note 1: Configuration straps are identified by an underlined symbol name. Signals that function as configurations traps must be augmented with an external resistor when connected to a load. Refer to Section 3.4, "Configuration Straps and Programmable Functions" for additional information.

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Table 3-1 details the package pin assignments in table format.

TABLE 3-1: 64-VQFN PIN ASSIGNMENTS

Pin Number	Pin Name	Pin Number	Pin Name
1	CFG_STRAP	33	VDD33
2	USB2DN_DP1/PRT_DIS_P1	34	PRT_CTL4/GANG_PWR
3	USB2DN_DM1/PRT_DIS_M1	35	VDD12
4	USB3DN_TXDP1	36	PRT_CTL3
5	USB3DN_TXDM1	37	PRT_CTL2
6	VDD12	38	PRT_CTL1
7	USB3DN_RXDP1	39	PROG_FUNC2
8	USB3DN_RXDM1	40	PROG_FUNC3
9	USB2DN_DP2/PRT_DIS_P2	41	VBUS_DET/GPIO16
10	USB2DN_DM2/PRT_DIS_M2	42	SPI_CLK/UART_RX/GPIO4/I2C_SLV_CFG0
11	USB3DN_TXDP2	43	SPI_DO/UART_TX/GPIO5/I2C_SLV_CFG1
12	USB3DN_TXDM2	44	SPI_DI/GPIO9/CFG_BC_EN
13	VDD12	45	SPI_CE_N/GPIO7/CFG_NON_REM
14	USB3DN_RXDP2	46	PROG_FUNC4
15	USB3DN_RXDM2	47	PROG_FUNC5
16	PROG_FUNC7	48	RESET_N
17	VDD12	49	PROG_FUNC6
18	VDD33	50	PROG_FUNC1
19	USB2DN_DP3/PRT_DIS_P3	51	VDD12
20	USB2DN_DM3/PRT_DIS_M3	52	VDD33
21	USB3DN_TXDP3	53	USB2UP_DP
22	USB3DN_TXDM3	54	USB2UP_DM
23	VDD12	55	USB3UP_TXDP
24	USB3DN_RXDP3	56	USB3UP_TXDM
25	USB3DN_RXDM3	57	VDD12
26	USB2DN_DP4/PRT_DIS_P4	58	USB3UP_RXDP
27	USB2DN_DM4/PRT_DIS_M4	59	USB3UP_RXDM
28	USB3DN_TXDP4	60	ATEST
29	USB3DN_TXDM4	61	XTALO
30	VDD12	62	XTALI/CLK_IN
31	USB3DN_RXDP4	63	VDD33
32	USB3DN_RXDM4	64	RBIAS

3.2 Pin Descriptions

This section contains descriptions of the various USB5734 pins. This pin descriptions have been broken into functional groups as follows:

- USB 3.1 Gen 1 Pin Descriptions
- USB 2.0 Pin Descriptions
- USB Port Control Pin Descriptions
- SPI/UART Pin Descriptions
- Programmable Function Pin Descriptions
- Miscellaneous Pin Descriptions
- Power and Ground Pin Descriptions

The "**_N**" symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, **RESET_N** indicates that the reset signal is active low. When "**_N**" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of "active low" and "Active high" signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

Note: The buffer type for each signal is indicated in the "Buffer Type" column of the pin description tables. A description of the buffer types is provided in Section 3.3, "Buffer Types," on page 15.
For additional information on configuration straps and configurable pins, refer to Section 3.4, "Configuration Straps and Programmable Functions".

TABLE 3-2: USB 3.1 GEN 1 PIN DESCRIPTIONS

Num Pins	Symbol	Buffer Type	Description
1	**USB3UP_TXDP**	IO-U	USB 3.1 Gen 1 upstream SuperSpeed transmit data plus.
1	**USB3UP_TXDM**	IO-U	USB 3.1 Gen 1 upstream SuperSpeed transmit data minus.
1	**USB3UP_RXDP**	IO-U	USB 3.1 Gen 1 upstream SuperSpeed receive data plus.
1	**USB3UP_RXDM**	IO-U	USB 3.1 Gen 1 upstream SuperSpeed receive data minus.
4	**USBDN_TXDP[4:1]**	IO-U	USB 3.1 Gen 1 downstream ports 4-1 SuperSpeed transmit data plus.
4	**USBDN_TXDM[4:1]**	IO-U	USB 3.1 Gen 1 downstream ports 4-1 SuperSpeed transmit data minus.
4	**USBDN_RXDP[4:1]**	IO-U	USB 3.1 Gen 1 downstream ports 4-1 SuperSpeed receive data plus.
4	**USBDN_RXDM[4:1]**	IO-U	USB 3.1 Gen 1 downstream ports 4-1 SuperSpeed receive data minus.

TABLE 3-3: USB 2.0 PIN DESCRIPTIONS

Num Pins	Symbol	Buffer Type	Description
1	**USB2UP_DP**	IO-U	USB 2.0 upstream data plus (D+).
1	**USB2UP_DM**	IO-U	USB 2.0 upstream data minus (D-).

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TABLE 3-3: USB 2.0 PIN DESCRIPTIONS (CONTINUED)

Num Pins	Symbol	Buffer Type	Description
4	**USB2DN_DP[4:1]**	IO-U	USB 2.0 downstream ports 4-1 data plus (D+).
	PRT_DIS_P[4:1]	I	Port 4-1 D+ Disable Configuration Strap. These configuration straps are used in conjunction with the corresponding **PRT_DIS_M[4:1]** straps to disable the related port (4-1). Refer to Section 3.4.2, "Port Disable Configuration (PRT_DIS_P[4:1] / PRT_DIS_M[4:1])" for more information. See Note 2.
4	**USB2DN_DM[4:1]**	IO-U	USB 2.0 downstream ports 4-1 data minus (D-).
	PRT_DIS_M[4:1]	I	Port 4-1 D- Disable Configuration Strap. These configuration straps are used in conjunction with the corresponding **PRT_DIS_P[4:1]** straps to disable the related port (4-1). Refer to Section 3.4.2, "Port Disable Configuration (PRT_DIS_P[4:1] / PRT_DIS_M[4:1])" for more information. See Note 2.
1	**VBUS_DET**	IS	This signal detects the state of the upstream bus power. When designing a detachable hub, this pin must be connected to the VBUS power pin of the upstream USB port through a resistor divider (50 kΩ by 100 kΩ) to provide 3.3 V. For self-powered applications with a permanently attached host, this pin must be connected to either 3.3 V or 5.0 V through a resistor divider to provide 3.3 V. In embedded applications, **VBUS_DET** may be controlled (toggled) when the host desires to renegotiate a connection without requiring a full reset of the device.
	GPIO16	I/O6	General purpose input/output 16.

Note 2: Configuration strap values are latched on Power-On Reset (POR) and the rising edge of **RESET_N** (external chip reset). Configuration straps are identified by an underlined symbol name. Signals that function as configurations traps must be augmented with an external resistor when connected to a load. Refer to Section 3.4, "Configuration Straps and Programmable Functions" for additional information.

TABLE 3-4: USB PORT CONTROL PIN DESCRIPTIONS

Num Pins	Symbol	Buffer Type	Description
1	**PRT_CTL1**	I (PU)	Port 1 Power Enable / Overcurrent Sense. As an output, this signal is an active high control signal used to enable power to the downstream port 1. As an input, this signal indicates an overcurrent condition from an external current monitor on USB port 1.
1	**PRT_CTL2**	I (PU)	Port 2 Power Enable / Overcurrent Sense. As an output, this signal is an active high control signal used to enable power to the downstream port 2. As an input, this signal indicates an overcurrent condition from an external current monitor on USB port 2.

TABLE 3-4: USB PORT CONTROL PIN DESCRIPTIONS (CONTINUED)

Num Pins	Symbol	Buffer Type	Description
1	PRT_CTL3	I (PU)	Port 3 Power Enable / Overcurrent Sense. As an output, this signal is an active high control signal used to enable power to the downstream port 3. As an input, this signal indicates an overcurrent condition from an external current monitor on USB port 3.
1	PRT_CTL4	I (PU)	Port 4 Power Enable / Overcurrent Sense. As an output, this signal is an active high control signal used to enable power to the downstream port 4. As an input, this signal indicates an overcurrent condition from an external current monitor on USB port 4.
	GANG_PWR	I (PU)	When pulled high enables gang mode. Gang power pin when used in gang mode.

TABLE 3-5: SPI/UART PIN DESCRIPTIONS

Num Pins	Symbol	Buffer Type	Description
1	SPI_CE_N	O12	Active low SPI chip enable output.
	GPIO7	I/O12	General purpose input/output 7.
	CFG_NON_REM	I	Non-Removable Port Configuration Strap. This configuration strap is used to configure the number of non-removable ports. Refer to Section 3.4.3, "Non-Removable Port Configuration (CFG_NON_REM)" for more information. See Note 3.
1	SPI_CLK	O6	SPI clock output to the serial ROM, when configured for SPI operation.
	UART_RX	I	UART receive pin, when configured for UART operation.
	GPIO4	I/O6	General purpose input/output 4.
	I2C_SLV_CFG0	I	I^2C Slave 0 Configuration Strap. This configuration strap is used to configure I^2C controller 0. Refer to Section 3.4.1, "SPI/SMBus/I2C/UART Configuration (I2C_SLV_CFG[1:0])" for additional information.
1	SPI_DO	O6	SPI data output, when configured for SPI operation.
	UART_TX	O12	UART transmit pin, when configured for UART operation.
	GPIO5	I/O6	General purpose input/output 5.
	I2C_SLV_CFG1	I	I^2C Slave 1 Configuration Strap. This configuration strap is used to configure I^2C controller 1. Refer to Section 3.4.1, "SPI/SMBus/I2C/UART Configuration (I2C_SLV_CFG[1:0])" for additional information.

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TABLE 3-5: SPI/UART PIN DESCRIPTIONS (CONTINUED)

Num Pins	Symbol	Buffer Type	Description
1	**SPI_DI**	IS	SPI data input, when configured for SPI operation.
	GPIO9	I/O12	General purpose input/output 9.
	CFG_BC_EN	I	Battery Charging Configuration Strap. This configuration strap is used to enable battery charging. Refer to Section 3.4.4, "Battery Charging Configuration (CFG_BC_EN)" for more information. See Note 3.

Note 3: Configuration strap values are latched on Power-On Reset (POR) and the rising edge of **RESET_N** (external chip reset). Configuration straps are identified by an underlined symbol name. Signals that function as configurations traps must be augmented with an external resistor when connected to a load. Refer to Section 3.4, "Configuration Straps and Programmable Functions" for additional information.

TABLE 3-6: PROGRAMMABLE FUNCTION PIN DESCRIPTIONS

Num Pins	Symbol	Buffer Type	Description
7	**PROG_FUNC[7:1]**	Note 4	Programmable function pins 7-1. The functions of these pins are configured via the **CFG_STRAP** pin. Refer to Section 3.4.5, "Device Mode / PROG_FUNC[7:1] Configuration (CFG_STRAP)" for additional information.
1	**CFG_STRAP**	I	Device Mode Configuration Strap. This configuration strap is used to set the device mode. Refer to Section 3.4.5, "Device Mode / PROG_FUNC[7:1] Configuration (CFG_STRAP)" for more information. See Note 5.

Note 4: The **PROG_FUNC2** buffer type is I/O6. The **PROG_FUNC7** buffer type is I/O10. All other **PROG_FUNCx** pins have a buffer type of I/O12.

Note 5: Configuration strap values are latched on Power-On Reset (POR) and the rising edge of **RESET_N** (external chip reset). Configuration straps are identified by an underlined symbol name. Signals that function as configurations traps must be augmented with an external resistor when connected to a load. Refer to Section 3.4, "Configuration Straps and Programmable Functions" for additional information.

TABLE 3-7: MISCELLANEOUS PIN DESCRIPTIONS

Num Pins	Symbol	Buffer Type	Description
1	**RESET_N**	IS	The RESET_N pin puts the device into Reset Mode, as the name of the pin and function then align.
1	**XTALI**	ICLK	External 25 MHz crystal input
	CLK_IN	ICLK	External reference clock input. The device may alternatively be driven by a single-ended clock oscillator. When this method is used, **XTALO** should be left unconnected.
1	**XTALO**	OCLK	External 25 MHz crystal output
1	**RBIAS**	AI	A 12.0 kΩ (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings.
1	**ATEST**	AI	Analog test pin. This signal is used for test purposes and must always be connected to ground.

TABLE 3-8: POWER AND GROUND PIN DESCRIPTIONS

Num Pins	Symbol	Buffer Type	Description
4	**VDD33**	P	+3.3 V power and internal regulator input Refer to Section 4.1, "Power Connections" for power connection information.
8	**VDD12**	P	+1.2 V core power Refer to Section 4.1, "Power Connections" for power connection information.
Pad	**VSS**	P	Common ground. This exposed pad must be connected to the ground plane with a via array.

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3.3 Buffer Types

TABLE 3-9: BUFFER TYPES

Buffer Type	Description
I	Input
IS	Schmitt-triggered input
O6	Output with 6 mA sink and 6 mA source
O10	Output with 10 mA sink and 10 mA source
O12	Output with 12 mA sink and 12 mA source
OD12	Open-drain output with 12 mA sink
PU	50 µA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50 µA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
IO-U	Analog input/output as defined in USB specification
AI	Analog input
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power pin

Note: Refer to Section 9.5, "DC Specifications" for individual buffer DC electrical characteristics.

3.4 Configuration Straps and Programmable Functions

Configuration straps are multi-function pins that are used during Power-On Reset (POR) or external chip reset (**RESET_N**) to determine the default configuration of a particular feature. The state of the signal is latched following de-assertion of the reset. Configuration straps are identified by an underlined symbol name. This section details the various device configuration straps and associated programmable pin functions.

Note:	The system designer must guarantee that configuration straps meet the timing requirements specified in Section 9.6.2, "Power-On and Configuration Strap Timing," on page 45 and Section 9.6.3, "Reset and Configuration Strap Timing," on page 46. If configuration straps are not at the correct voltage level prior to being latched, the device may capture incorrect strap values.

3.4.1 SPI/SMBUS/I2C/UART CONFIGURATION (I2C_SLV_CFG[1:0])

The SPI/SMBus/I2C//UART pins can be configured into one of four functional modes:

- SPI Mode
- SMBus Slave Enable Mode
- I2C Bridging Mode
- UART Mode

If 10 kΩ pull-up resistors are detected on **SPI_DO** and **SPI_CLK**, the SPI/SMBus/I2C/UART pins are configured into SMBus Slave Enable Mode. If a 10 kΩ pull-down resistor is detected on **SPI_DO**, the SPI/SMBus/I2C/UART pins are configured into UART Mode. If no pull-ups or pull-downs are detected on **SPI_DO** and **SPI_CLK**, the SPI/SMBus/I2C/UART pins are first configured into SPI Mode. If no valid SPI ROM is detected, the SPI/SMBus/I2C/UART pins are configured into I2C Bridging Mode. The strap settings for these supported modes are detailed in Table 3-10. The individual pin function assignments for each mode are detailed in Table 3-11. For additional device connection information, refer to Section 4.0, "Device Connections".

Note:	The following interfaces cannot be used simultaneously: • UART and SMBus Slave • UART and SPI • SMBus Slave and I2C Bridging interface

TABLE 3-10: SPI/SMBUS/I2C/UART MODE CONFIGURATION SETTINGS

Pin	SPI Mode (Note 6)	SMBus Slave Enable Mode (Note 7)	I2C Bridging Mode (Note 8)	UART Mode
43 (**SPI_DO**)	No pull-up/down	10 kΩ pull-up	No pull-up/down	10 kΩ pull-down
42 (**SPI_CLK**)	No pull-up/down	10 kΩ pull-up	No pull-up/down	No pull-up/down

Note 6: In order to use the SPI interface, an SPI ROM containing a valid signature of `2DFU` (device firmware upgrade) beginning at address 0xFFFA must be present. Refer to Section 7.1, "SPI Master Interface" for additional information.

Note 7: In order to use the SMBus slave interface, the **SPI_DO** and **SPI_CLK** pins must be configured for SMBus Slave Enable Mode *and* **CFG_STRAP** must be configured to Configuration 1, 2, 3, or 6, which programs the **PROG_FUNC4** and **PROG_FUNC5** pins as **SMDAT** and **SMCLK**, respectively. When in Configuration 4 or 5, the SMBus slave interface is not usable. Refer to Section 3.4.5, "Device Mode / PROG_FUNC[7:1] Configuration (CFG_STRAP)" for additional information.

Note 8: In order to use the I2C Bridging interface, the **SPI_DO** and **SPI_CLK** pins must be configured for I2C Bridging Mode *and* **CFG_STRAP** must be configured to Configuration 1, 2, 3, or 6, which programs the **PROG_FUNC4** and **PROG_FUNC5** pins as **SMDAT** and **SMCLK**, respectively. When in Configuration 4 or 5, the I2C Bridging interface is not usable. Additional hub register configuration is also required. Refer to Section 3.4.5, "Device Mode / PROG_FUNC[7:1] Configuration (CFG_STRAP)" and Section 7.3, "I2C Bridge Interface" for additional information.

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TABLE 3-11: SPI/SMBUS/I²C/UART MODE PIN ASSIGNMENTS

Pin	SPI Mode	SMBus Slave Enable Mode	I²C Bridging Mode	UART Mode
45	SPI_CE_N	CFG_NON_REM	CFG_NON_REM	CFG_NON_REM
44	SPI_DI	CFG_BC_EN	CFG_BC_EN	CFG_BC_EN
43	SPI_DO	I2C_SLV_CFG1	-	UART_TX
42	SPI_CLK	I2C_SLV_CFG0	-	UART_RX

3.4.2 PORT DISABLE CONFIGURATION (PRT_DIS_P[4:1] / PRT_DIS_M[4:1])

The **PRT_DIS_P[4:1]** and **PRT_DIS_M[4:1]** configuration straps are used in conjunction to disable the related port (4-1).

For **PRT_DIS_P*x*** (where *x* is the corresponding port 4-1):

0 = Port *x* D+ Enabled

1 = Port *x* D+ Disabled

For **PRT_DIS_M*x*** (where *x* is the corresponding port 4-1):

0 = Port *x* D- Enabled

1 = Port *x* D- Disabled

Note: Both **PRT_DIS_P*x*** and **PRT_DIS_M*x*** (where ***x*** is the corresponding port) must be tied to 3.3 V to disable the associated downstream port. Disabling the USB 2.0 port will also disable the corresponding USB 3.1 Gen 1 port.

3.4.3 NON-REMOVABLE PORT CONFIGURATION (CFG_NON_REM)

The **CFG_NON_REM** configuration strap is used to configure the non-removable port settings of the device to one of five settings. These modes are selected by the configuration of an external resistor on the **CFG_NON_REM** pin. The resistor options are a 200 kΩ pull-down, 200 kΩ pull-up, 10 kΩ pull-down, 10 kΩ pull-up, and 10 Ω pull-down, as shown in Table 3-12.

TABLE 3-12: CFG_NON_REM RESISTOR ENCODING

CFG_NON_REM Resistor Value	Setting
200 kΩ Pull-Down	All ports removable
200 kΩ Pull-Up	Port 1 non-removable
10 kΩ Pull-Down	Port 1, 2 non-removable
10 kΩ Pull-Up	Port 1, 2, 3, non-removable
10 Ω Pull-Down	Port 1, 2, 3, 4 non-removable

3.4.4 BATTERY CHARGING CONFIGURATION (CFG_BC_EN)

The **CFG_BC_EN** configuration strap is used to configure the battery charging port settings of the device to one of five settings. These modes are selected by the configuration of an external resistor on the **CFG_BC_EN** pin. The resistor options are a 200 kΩ pull-down, 200 kΩ pull-up, 10 kΩ pull-down, 10 kΩ pull-up, and 10 Ω pull-down, as shown in Table 3-13.

TABLE 3-13: CFG_BC_EN RESISTOR ENCODING

CFG_BC_EN Resistor Value	Setting
200 kΩ Pull-Down	No battery charging
200 kΩ Pull-Up	Port 1 battery charging
10 kΩ Pull-Down	Port 1, 2 battery charging
10 kΩ Pull-Up	Port 1, 2, 3, battery charging
10 Ω Pull-Down	Port 1, 2, 3, 4 battery charging

3.4.5 DEVICE MODE / PROG_FUNC[7:1] CONFIGURATION (CFG_STRAP)

The **CFG_STRAP** is used to configure the programmable function pins (**PROG_FUNC[7:1]**) into one of six modes. These modes are selected by the configuration of an external resistor on the **CFG_STRAP** pin. The resistor options are a 200 kΩ pull-down, 200 kΩ pull-up, 10 kΩ pull-down, 10 kΩ pull-up, 10 Ω pull-down, and 10 Ω pull-up, as shown in Table 3-14. For details on each device mode, including pin assignments, refer to the following subsections.

TABLE 3-14: CFG_STRAP RESISTOR ENCODING

CFG_STRAP Resistor Value	Mode
200 kΩ Pull-Down	Configuration 1 - Mixed Mode
200 kΩ Pull-Up	Configuration 2 - FlexConnect Mode
10 kΩ Pull-Down	Configuration 3 - Speed Indicator Mode
10 kΩ Pull-Up	Configuration 4 - GPIO Mode (Reserved)
10 Ω Pull-Down	Configuration 5 - Battery Charging / Power Delivery Indicator Mode
10 Ω Pull-Up	Configuration 6 - Full UART Mode

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3.4.5.1 Configuration 1 - Mixed Mode

When the **CFG_STRAP** is configured to this mode, the programmable function pins (**PROG_FUNC[7:1]**) are set to provide an SMBus/I^{2}C interface, 3 GPIOs, and FlexConnect capabilities. Table 3-15 details the **PROG_FUNC[7:1]** pin assignments in this mode.

TABLE 3-15: CONFIGURATION 1 PROG_FUNC[7:1] FUNCTION ASSIGNMENT

Pin	Function	Buffer Type	Description
PROG_FUNC1	GPIO1	I/O12	**General Purpose Input/Output 1**
PROG_FUNC2	GPIO2	I/O6	**General Purpose Input/Output 2**
PROG_FUNC3	GPIO3	I/O12	**General Purpose Input/Output 3**
PROG_FUNC4	SMDAT	OD12	**SMBus/I^{2}C Data** The SMBus/I^{2}C interface acts as SMBus slave or I^{2}C bridge dependent on the device configuration. Refer to Section 3.4.1, "SPI/SMBus/I2C/UART Configuration (I2C_SLV_CFG[1:0])".
PROG_FUNC5	SMCLK	OD12	**SMBus/I^{2}C Clock** The SMBus/I^{2}C interface acts as SMBus slave or I^{2}C bridge dependent on the device configuration. Refer to Section 3.4.1, "SPI/SMBus/I2C/UART Configuration (I2C_SLV_CFG[1:0])".
PROG_FUNC6	FLEXCMD	IS	**FlexConnect Control** 0: Normal Operation (Port 0 upstream, Port 1 downstream) 1: Flex Operation (Port 1 upstream, Port 0 downstream) **Note:** Refer to Section 8.2, "FlexConnect" for additional information.
PROG_FUNC7	USB2_SUSP_IND	O10	**USB2.0 Suspend Indicator** USB2_SUSP_IND can be used as a sideband remote wakeup signal for the host when in USB2.0 suspend. **Note:** Refer to Section 8.5, "Remote Wakeup Indicator" for additional information.

3.4.5.2 Configuration 2 - FlexConnect Mode

When the **CFG_STRAP** is configured to this mode, the programmable function pins (**PROG_FUNC[7:1]**) are set to provide FlexConnect, an SMBus/I2C interface, and other additional features. Table 3-16 details the **PROG_FUNC[7:1]** pin assignments in this mode.

TABLE 3-16: CONFIGURATION 2 PROG_FUNC[7:1] FUNCTION ASSIGNMENT

Pin	Function	Buffer Type	Description
PROG_FUNC1	HOST_TYPE0	O12	**Port 0 USB Host Type** Tri-state: No USB host detected on Port 0 0: USB 3.1 Gen 1 Host detected on Port 0 1: USB 2.0 or USB 1.1 Host detected on Port 0 A USB 2.0 Host is considered detected when the USB 2.0 hub address register holds a non-zero value. A USB 3.1 Gen 1 Host is considered detected when the USB 3.1 Gen 1 hub address register holds a non-zero value.
PROG_FUNC2	HOST_TYPE1	O6	**Port 1 USB Host Type** Tri-state: No USB host detected on Port 1 0: USB 3.1 Gen 1 Host detected on Port 1 1: USB 2.0 or USB 1.1 Host detected on Port 1 A USB 2.0 Host is considered detected when the USB 2.0 hub address register holds a non-zero value. A USB 3.1 Gen 1 Host is considered detected when the USB 3.1 Gen 1 hub address register holds a non-zero value.
PROG_FUNC3	FLEX_STATE_N	O12	**FlexConnect State Compliment Indicator** This signal reflects the inverse of the current state of FLEXCMD. 0: Flex Operation (Port 1 upstream, Port 0 downstream) 1: Normal Operation (Port 0 upstream, Port 1 downstream) **Note:** Refer to Section 8.2, "FlexConnect" for additional information.
PROG_FUNC4	SMDAT	OD12	**SMBus/I2C Data** The SMBus/I2C interface acts as SMBus slave or I2C bridge dependent on the device configuration. Refer to Section 3.4.1, "SPI/SMBus/I2C/UART Configuration (I2C_SLV_CFG[1:0])".
PROG_FUNC5	SMCLK	OD12	**SMBus/I2C Clock** The SMBus/I2C interface acts as SMBus slave or I2C bridge dependent on the device configuration. Refer to Section 3.4.1, "SPI/SMBus/I2C/UART Configuration (I2C_SLV_CFG[1:0])".
PROG_FUNC6	FLEXCMD	IS	**FlexConnect Control** 0: Normal Operation (Port 0 upstream, Port 1 downstream) 1: Flex Operation (Port 1 upstream, Port 0 downstream) **Note:** Refer to the Section 8.2, "FlexConnect" for additional information.
PROG_FUNC7	FLEX_STATE	O10	**FlexConnect State Indicator** This signal reflects the current state of FLEXCMD. 0: Normal Operation (Port 0 upstream, Port 1 downstream) 1: Flex Operation (Port 1 upstream, Port 0 downstream) **Note:** Refer to Section 8.2, "FlexConnect" for additional information.

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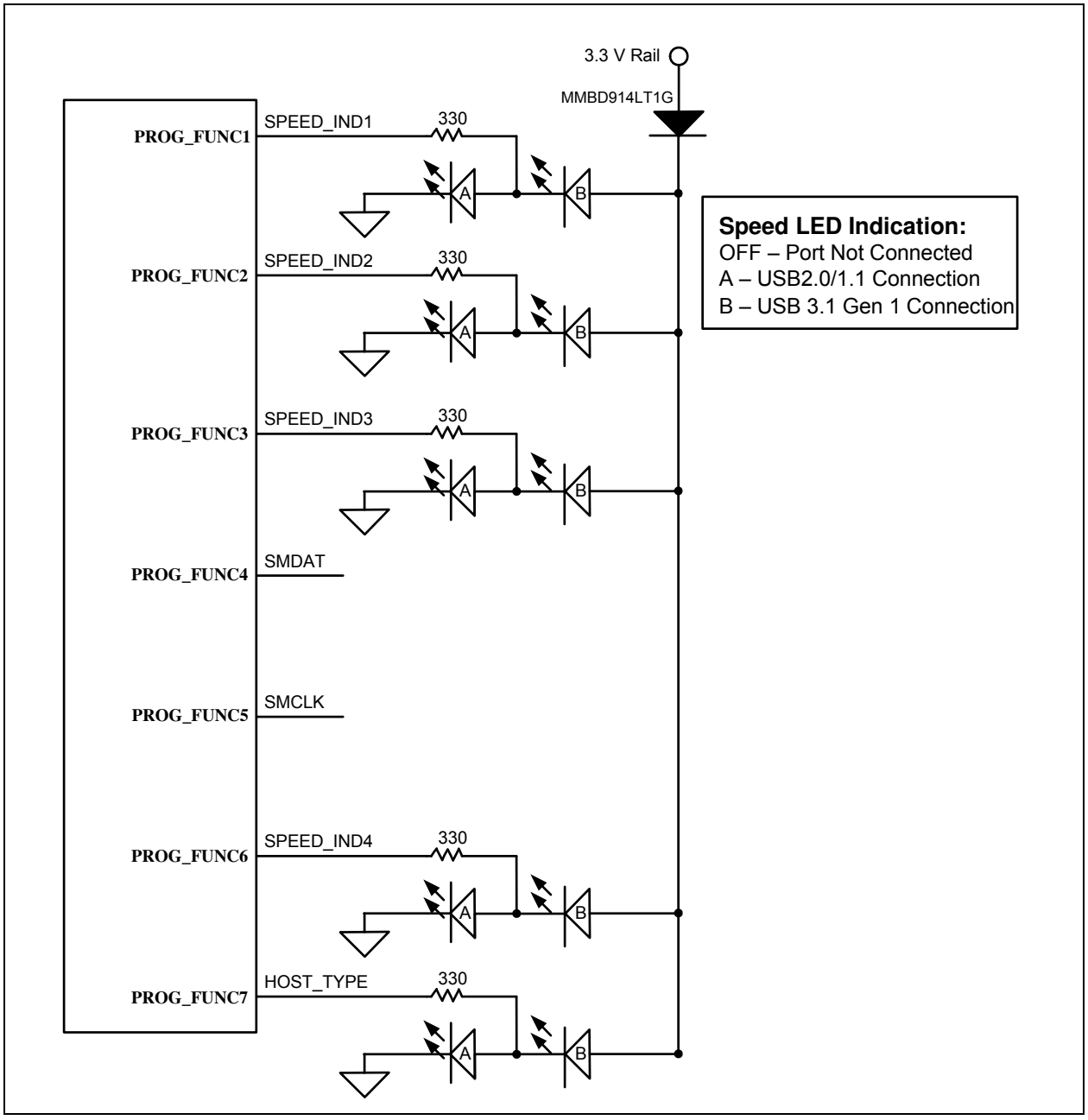
3.4.5.3 Configuration 3 - Speed Indicator Mode

When the **CFG_STRAP** is configured to this mode, the programmable function pins (**PROG_FUNC[7:1]**) are set to indicate speed status, host type, and provide an SMBus/I^{2}C interface. Table 3-17 details the **PROG_FUNC[7:1]** pin assignments in this mode.

TABLE 3-17: CONFIGURATION 3 PROG_FUNC[7:1] FUNCTION ASSIGNMENT

Pin	Function	Buffer Type	Description
PROG_FUNC1	SPEED_IND1	O12	**Port 1 Speed Indicator** Tri-state: Not connected 0: USB 2.0 / USB 1.1 1: USB 3.1 Gen 1
PROG_FUNC2	SPEED_IND2	O6	**Port 2 Speed Indicator** Tri-state: Not connected 0: USB 2.0 / USB 1.1 1: USB 3.1 Gen 1
PROG_FUNC3	SPEED_IND3	O12	**Port 3 Speed Indicator** Tri-state: Not connected 0: USB 2.0 / USB 1.1 1: USB 3.1 Gen 1
PROG_FUNC4	SMDAT	OD12	**SMBus/I^{2}C Data** The SMBus/I^{2}C interface acts as SMBus slave or I^{2}C bridge dependent on the device configuration. Refer to Section 3.4.1, "SPI/SMBus/I2C/UART Configuration (I2C_SLV_CFG[1:0])".
PROG_FUNC5	SMCLK	OD12	**SMBus/I^{2}C Clock** The SMBus/I^{2}C interface acts as SMBus slave or I^{2}C bridge dependent on the device configuration. Refer to Section 3.4.1, "SPI/SMBus/I2C/UART Configuration (I2C_SLV_CFG[1:0])".
PROG_FUNC6	SPEED_IND4	O12	**Port 4 Speed Indicator** Tri-state: Not connected 0: USB 2.0 / USB 1.1 1: USB 3.1 Gen 1
PROG_FUNC7	HOST_TYPE	O10	**Port 0 USB Host Type** Tri-state: No USB host detected on Port 0 0: USB 3.1 Gen 1 Host detected on Port 0 1: USB 2.0 or USB 1.1 Host detected on Port 0 A USB 2.0 Host is considered detected when the USB 2.0 hub address register holds a non-zero value. A USB 3.1 Gen 1 Host is considered detected when the USB 3.1 Gen 1 hub address register holds a non-zero value.

FIGURE 3-2: CONFIGURATION 3 PROG_FUNC[7:1] PIN CONNECTIONS



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3.4.5.4 Configuration 4 - GPIO Mode (Reserved)

When the **CFG_STRAP** is configured to this mode, the programmable function pins (**PROG_FUNC[7:1]**) are set to provide 7 general purpose I/Os that can be used for GPIO bridging. Table 3-18 details the **PROG_FUNC[7:1]** pin assignments in this mode.

TABLE 3-18: CONFIGURATION 4 PROG_FUNC[7:1] FUNCTION ASSIGNMENT

Pin	Function	Buffer Type	Description
PROG_FUNC1	GPIO1	I/O12	**General Purpose Input/Output 1**
PROG_FUNC2	GPIO2	I/O6	**General Purpose Input/Output 2**
PROG_FUNC3	GPIO3	I/O12	**General Purpose Input/Output 3**
PROG_FUNC4	GPIO6	I/O12	**General Purpose Input/Output 4**
PROG_FUNC5	GPIO8	I/O12	**General Purpose Input/Output 5**
PROG_FUNC6	GPIO10	I/O12	**General Purpose Input/Output 6**
PROG_FUNC7	GPIO11	I/O10	**General Purpose Input/Output 7**

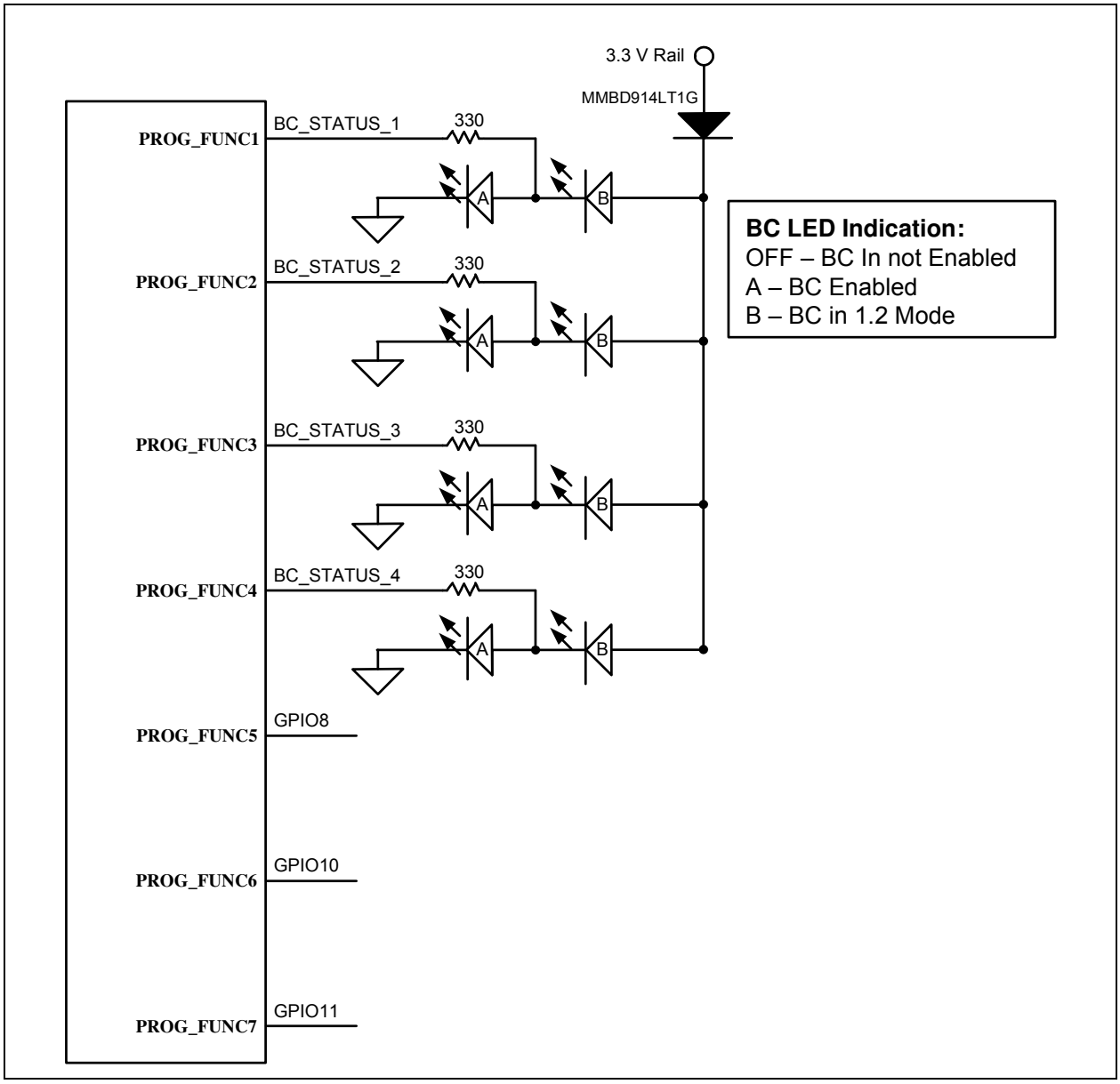
3.4.5.5 Configuration 5 - Battery Charging / Power Delivery Indicator Mode

When the **CFG_STRAP** is configured to this mode, the programmable function pins (**PROG_FUNC[7:1]**) are set to indicate battery charging and 3 general purpose I/Os. Table 3-19 details the **PROG_FUNC[7:1]** pin assignments in this mode.

TABLE 3-19: CONFIGURATION 5 PROG_FUNC[7:1] FUNCTION ASSIGNMENT

Pin	Function	Buffer Type	Description
PROG_FUNC1	BC_IND1	O12	**Port 1 Battery Charging Indicator** Tri-state: Battery Charging not enabled 0: In BC 1.2 Mode 1: Battery Charging enabled
PROG_FUNC2	BC_IND2	O6	**Port 2 Battery Charging Indicator** Tri-state: Battery Charging not enabled 0: In BC 1.2 Mode 1: Battery Charging enabled
PROG_FUNC3	BC_IND3	O12	**Port 3 Battery Charging Indicator** Tri-state: Battery Charging not enabled 0: In BC 1.2 Mode 1: Battery Charging enabled
PROG_FUNC4	BC_IND4	O12	**Port 4 Battery Charging Indicator** Tri-state: Battery Charging not enabled 0: In BC 1.2 Mode 1: Battery Charging enabled
PROG_FUNC5	GPIO8	I/O12	**General Purpose Input/Output 8**
PROG_FUNC6	GPIO10	I/O12	**General Purpose Input/Output 10**
PROG_FUNC7	GPIO11	I/O10	**General Purpose Input/Output 11**

FIGURE 3-3: CONFIGURATION 5 PROG_FUNC[7:1] PIN CONNECTIONS



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3.4.5.6 Configuration 6 - Full UART Mode

When the **CFG_STRAP** is configured to this mode, the programmable function pins (**PROG_FUNC[7:1]**) are set for full UART configuration and also provide an SMBus/I^{2}C interface. In this mode the **PROG_FUNCx** pins are used in conjunction with the **UART_TX** and **UART_RX** pins for a full UART interface. Table 3-20 details the **PROG_FUNC[7:1]** pin assignments in this mode.

Note: When flow control is disabled, UART_nCTS, UART_nDCD, and UART_nDSR must not be left floating. In this case, these pins should include external pull-downs to maintain UART communication in Full UART Mode with no flow control.

TABLE 3-20: CONFIGURATION 6 PROG_FUNC[7:1] FUNCTION ASSIGNMENT

Pin	Function	Buffer Type	Description
PROG_FUNC1	UART_nRTS	I/O12	**UART Request To Send**
PROG_FUNC2	UART_nCTS	I/O6	**UART Clear To Send**
PROG_FUNC3	UART_nDCD	I/O12	**UART Data Carrier Detect**
PROG_FUNC4	SMDAT	OD12	**SMBus/I^{2}C Data** The SMBus/I^{2}C interface acts as SMBus slave or I^{2}C bridge dependent on the device configuration. Refer to Section 3.4.1, "SPI/SMBus/I2C/UART Configuration (I2C_SLV_CFG[1:0])".
PROG_FUNC5	SMCLK	OD12	**SMBus/I^{2}C Clock** The SMBus/I^{2}C interface acts as SMBus slave or I^{2}C bridge dependent on the device configuration. Refer to Section 3.4.1, "SPI/SMBus/I2C/UART Configuration (I2C_SLV_CFG[1:0])".
PROG_FUNC6	UART_nDTR	I/O12	**UART Data Terminal Ready**
PROG_FUNC7	UART_nDSR	I/O10	**UART Data Set Ready**