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4-Port SS/HS USB Controller Hub

Highlights

- USB Hub Feature Controller IC with 4 USB 3.1 Gen 1 / USB 2.0 downstream ports
- USB-IF Battery Charger revision 1.2 support on up & downstream ports (DCP, CDP, SDP)
- USB Link Power Management (LPM) support
- Enhanced OEM configuration options available through either OTP or SPI ROM
- Available in 56-pin (7 x 7 mm) VQFN lead-free, RoHS compliant package
- Commercial and industrial grade temperature support
- Configuration Straps: Predefined configuration of system level functions

Target Applications

- Standalone USB Hubs
- Laptop Docks
- PC Motherboards
- PC Monitor Docks
- Multi-function USB 3.1 Gen 1 Peripherals

Key Benefits

- USB 3.1 Gen 1 compliant 5 Gbps, 480 Mbps, 12 Mbps and 1.5 Mbps operation
 - 5 V tolerant USB 2.0 pins
 - 1.32 V tolerant USB 3.1 Gen 1 pins
 - Integrated termination & pull-up/pull-down resistors
- Supports per port battery charging of most popular battery powered devices
 - USB-IF Battery Charging rev. 1.2 support (DCP, CDP, SDP)
 - Apple® portable product charger emulation
 - Chinese YD/T 1591-2006 charger emulation
 - Chinese YD/T 1591-2009 charger emulation
 - European Union universal mobile charger support
 - Support for Microchip USC100x family of battery charging controllers
 - Supports additional portable devices
- Smart port controller operation
 - Firmware handling of companion port controllers
- On-chip microcontroller
 - Manages I/Os, VBUS, and other signals
- 8 KB RAM, 64 KB ROM
- 8 KB One Time Programmable (OTP) ROM
 - Includes on-chip charge pump
- Configuration programming via OTP ROM, SPI ROM, or SMBus
- **PortSwap**
 - Configurable differential intro-pair signal swapping
- **PHYBoost™**
 - Programmable USB transceiver drive strength for recovering signal integrity
- **VariSense™**
 - Programmable USB receiver sensitivity
- Compatible with Microsoft Windows 8, 7, XP, Apple OS X 10.4+, and Linux hub drivers
- Optimized for low-power operation and low thermal dissipation
- Package
 - 56-pin VQFN (7 x 7 mm)
- Environmental
 - 3 kV HBM JESD22-A114F ESD protection
 - Commercial temperature range (0°C to +70°C)
 - Industrial temperature range (-40°C to +85°C)

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1.0 PREFACE

1.1 General Terms

TABLE 1-1: GENERAL TERMS

Term	Description
ADC	Analog-to-Digital Converter
Byte	8 bits
CDC	Communication Device Class
CSR	Control and Status Registers
DWORD	32 bits
EOP	End of Packet
EP	Endpoint
FIFO	First In First Out buffer
FS	Full-Speed
FSM	Finite State Machine
GPIO	General Purpose I/O
HS	Hi-Speed
HSOS	High Speed Over Sampling
Hub Feature Controller	The Hub Feature Controller, sometimes called a Hub Controller for short is the internal processor used to enable the unique features of the USB Controller Hub. This is not to be confused with the USB Hub Controller that is used to communicate the hub status back to the Host during a USB session.
I ² C	Inter-Integrated Circuit
LS	Low-Speed
lsb	Least Significant Bit
LSB	Least Significant Byte
msb	Most Significant Bit
MSB	Most Significant Byte
N/A	Not Applicable
NC	No Connect
OTP	One Time Programmable
PCB	Printed Circuit Board
PCS	Physical Coding Sublayer
PHY	Physical Layer
PLL	Phase Lock Loop
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
SDK	Software Development Kit
SMBus	System Management Bus
UUID	Universally Unique Identifier
WORD	16 bits

1.2 Reference Documents

1. *UNICODE UTF-16LE For String Descriptors* USB Engineering Change Notice, December 29th, 2004, <http://www.usb.org>
2. *Universal Serial Bus Revision 3.1 Specification*, <http://www.usb.org>
3. *Battery Charging Specification*, Revision 1.2, Dec. 07, 2010, <http://www.usb.org>
4. *I²C-Bus Specification*, Version 1.1, <http://www.nxp.com>
5. *System Management Bus Specification*, Version 1.0, <http://smbus.org/specs>

USB5744

2.0 INTRODUCTION

2.1 General Description

The Microchip USB5744 hub is low-power, OEM configurable, USB 3.1 Gen 1 hub feature controller with 4 downstream ports and advanced features for embedded USB applications. The USB5744 is fully compliant with the *Universal Serial Bus Revision 3.1 Specification* and *USB 2.0 Link Power Management Addendum*. The USB5744 supports 5 Gbps SuperSpeed (SS), 480 Mbps Hi-Speed (HS), 12 Mbps Full-Speed (FS), and 1.5 Mbps Low-Speed (LS) USB downstream devices on all enabled downstream ports.

The USB5744 supports the legacy USB speeds (HS/FS/LS) through a dedicated USB 2.0 hub feature controller that is the culmination of five generations of Microchip hub feature controller design and experience with proven reliability, interoperability, and device compatibility. The SuperSpeed hub feature controller operates in parallel with the USB 2.0 controller, decoupling the 5 Gbps SS data transfers from bottlenecks due to the slower USB 2.0 traffic.

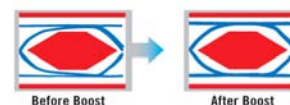
The USB5744 supports downstream battery charging. The USB5744 integrated battery charger detection circuitry supports the USB-IF Battery Charging (BC1.2) detection method and most Apple devices. The USB5744 provides the battery charging handshake and supports the following USB-IF BC1.2 charging profiles:

- DCP: Dedicated Charging Port (Power brick with no data)
- CDP: Charging Downstream Port (1.5A with data)
- SDP: Standard Downstream Port (0.5A with data)
- Custom profiles loaded via SMBus or OTP

Additionally, the USB5744 includes many powerful and unique features such as:

PortSwap, which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.

PHYBoost, which provides programmable levels of Hi-Speed USB signal drive strength in the downstream port transceivers. PHYBoost attempts to restore USB signal integrity in a compromised system environment. The graphic on the right shows an example of Hi-Speed USB eye diagrams before and after PHYBoost signal integrity restoration. in a compromised system environment

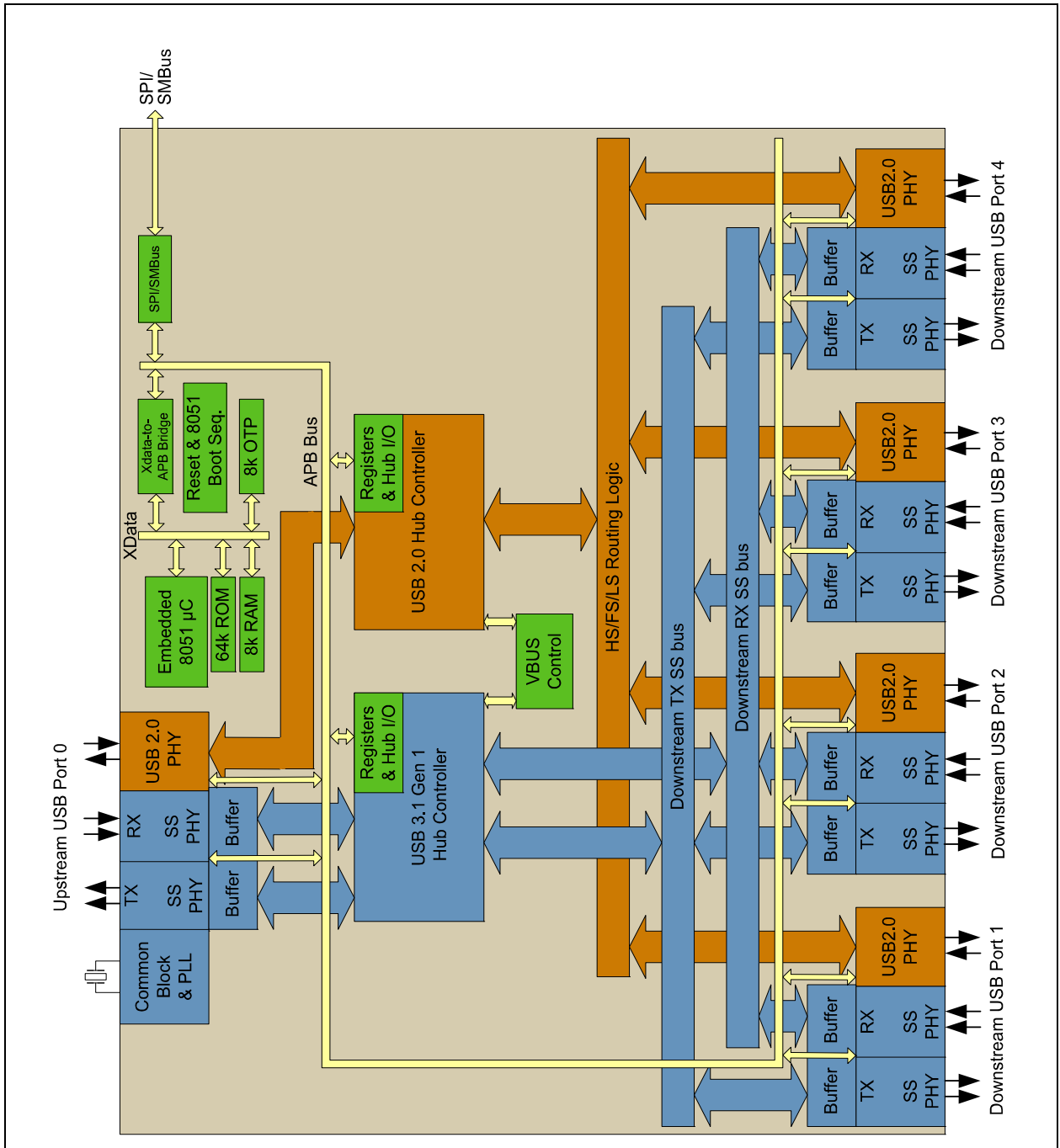


VariSense, which controls the USB receiver sensitivity enabling programmable levels of USB signal receive sensitivity. This capability allows operation in a sub-optimal system environment, such as when a captive USB cable is used.

The USB5744 can be configured for operation through internal default settings. Custom OEM configurations are supported through external SPI ROM or OTP ROM. All port control signal pins are under firmware control in order to allow for maximum operational flexibility, and are available as GPIOs for customer specific use.

The USB5744 is available in commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature ranges. An internal block diagram of the USB5744 is shown in [Figure 2-1](#).

FIGURE 2-1: INTERNAL BLOCK DIAGRAM

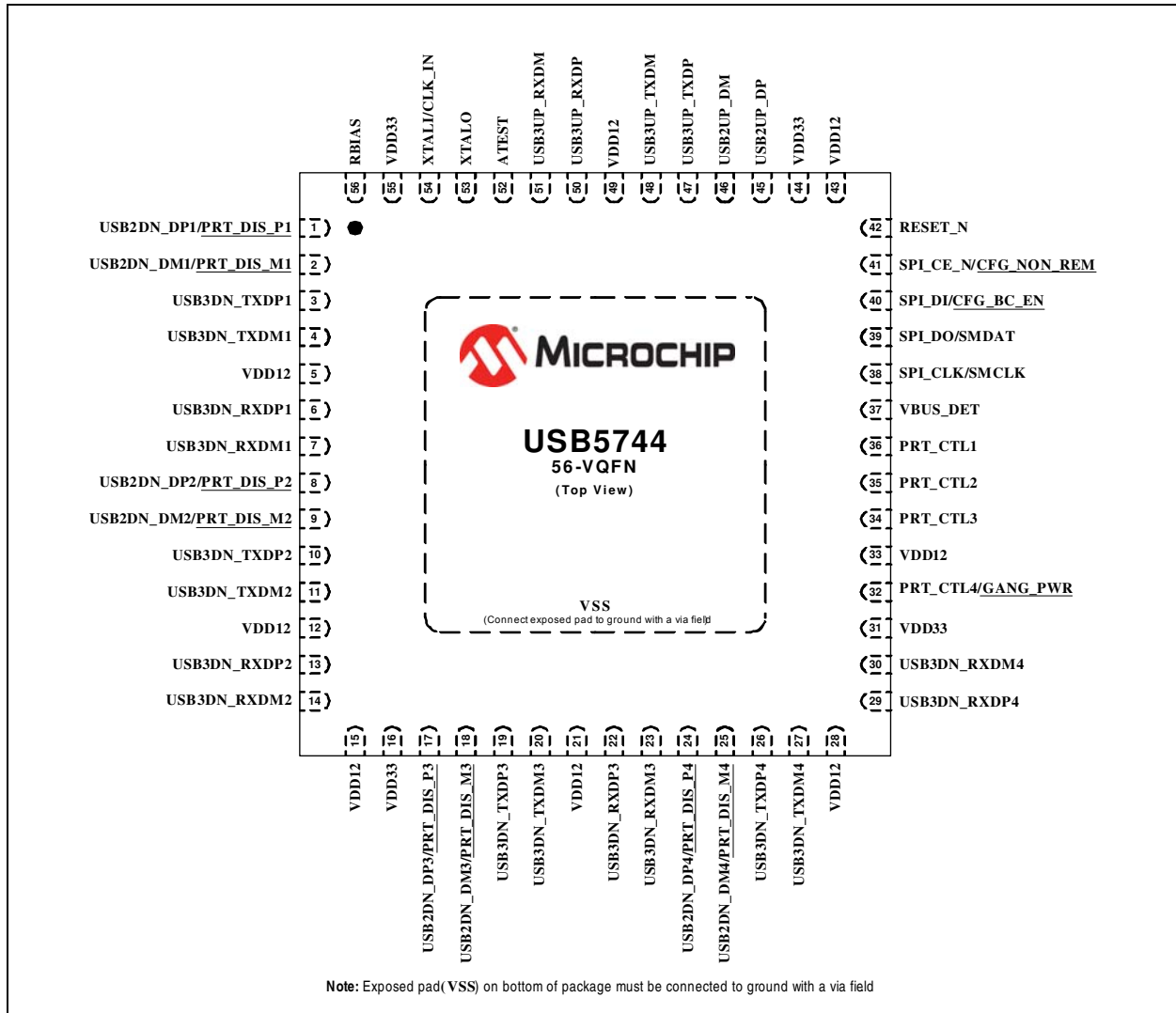


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3.0 PIN DESCRIPTION AND CONFIGURATION

3.1 Pin Assignments

FIGURE 3-1: 56-VQFN PIN ASSIGNMENTS



Note 1: Configuration straps are identified by an underlined symbol name. Signals that function as configurations traps must be augmented with an external resistor when connected to a load. Refer to [Section 3.4, "Configuration Straps and Programmable Functions"](#) for additional information.

Table 3-1 details the package pin assignments in table format.

TABLE 3-1: 56-VQFN PIN ASSIGNMENTS

Pin Number	Pin Name	Pin Number	Pin Name
1	USB2DN_DP1/ <u>PRT_DIS P1</u>	29	USB3DN_RXDP4
2	USB2DN_DM1/ <u>PRT_DIS M1</u>	30	USB3DN_RXDM4
3	USB3DN_TXDP1	31	VDD33
4	USB3DN_TXDM1	32	<u>PRT_CTL4/GANG_PWR</u>
5	VDD12	33	VDD12
6	USB3DN_RXDP1	34	PRT_CTL3
7	USB3DN_RXDM1	35	PRT_CTL2
8	USB2DN_DP2/ <u>PRT_DIS P2</u>	36	PRT_CTL1
9	USB2DN_DM2/ <u>PRT_DIS M2</u>	37	VBUS_DET
10	USB3DN_TXDP2	38	SPI_CLK/SMCLK
11	USB3DN_TXDM2	39	SPI_DO/SMDAT
12	VDD12	40	<u>SPI_DI/CFG_BC_EN</u>
13	USB3DN_RXDP2	41	<u>SPI_CE_N/CFG_NON_REM</u>
14	USB3DN_RXDM2	42	RESET_N
15	VDD12	43	VDD12
16	VDD33	44	VDD33
17	USB2DN_DP3/ <u>PRT_DIS P3</u>	45	USB2UP_DP
18	USB2DN_DM3/ <u>PRT_DIS M3</u>	46	USB2UP_DM
19	USB3DN_TXDP3	47	USB3UP_TXDP
20	USB3DN_TXDM3	48	USB3UP_TXDM
21	VDD12	49	VDD12
22	USB3DN_RXDP3	50	USB3UP_RXDP
23	USB3DN_RXDM3	51	USB3UP_RXDM
24	USB2DN_DP4/ <u>PRT_DIS P4</u>	52	ATEST
25	USB2DN_DM4/ <u>PRT_DIS M4</u>	53	XTALO
26	USB3DN_TXDP4	54	XTALI/CLK_IN
27	USB3DN_TXDM4	55	VDD33
28	VDD12	56	RBIAS

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3.2 Pin Descriptions

This section contains descriptions of the various USB5744 pins. This pin descriptions have been broken into functional groups as follows:

- [USB 3.1 Gen 1 Pin Descriptions](#)
- [USB 2.0 Pin Descriptions](#)
- [USB Port Control Pin Descriptions](#)
- [SPI/SMBus Pin Descriptions](#)
- [Miscellaneous Pin Descriptions](#)
- [Power and Ground Pin Descriptions](#)

The “_N” symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, **RESET_N** indicates that the reset signal is active low. When “_N” is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “Active high” signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

Note: The buffer type for each signal is indicated in the “Buffer Type” column of the pin description tables. A description of the buffer types is provided in [Section 3.3, “Buffer Types,” on page 14](#). For additional information on configuration straps and configurable pins, refer to [Section 3.4, “Configuration Straps and Programmable Functions”](#).

TABLE 3-2: USB 3.1 GEN 1 PIN DESCRIPTIONS

Num Pins	Symbol	Buffer Type	Description
1	USB3UP_TXDP	IO-U	USB 3.1 Gen 1 upstream SuperSpeed transmit data plus.
1	USB3UP_TXDM	IO-U	USB 3.1 Gen 1 upstream SuperSpeed transmit data minus.
1	USB3UP_RXDP	IO-U	USB 3.1 Gen 1 upstream SuperSpeed receive data plus.
1	USB3UP_RXDM	IO-U	USB 3.1 Gen 1 upstream SuperSpeed receive data minus.
4	USBDN_TXDP[4:1]	IO-U	USB 3.1 Gen 1 downstream ports 4-1 SuperSpeed transmit data plus.
4	USBDN_TXDM[4:1]	IO-U	USB 3.1 Gen 1 downstream ports 4-1 SuperSpeed transmit data minus.
4	USBDN_RXDP[4:1]	IO-U	USB 3.1 Gen 1 downstream ports 4-1 SuperSpeed receive data plus.
4	USBDN_RXDM[4:1]	IO-U	USB 3.1 Gen 1 downstream ports 4-1 SuperSpeed receive data minus.

TABLE 3-3: USB 2.0 PIN DESCRIPTIONS

Num Pins	Symbol	Buffer Type	Description
1	USB2UP_DP	IO-U	USB 2.0 upstream data plus (D+).
1	USB2UP_DM	IO-U	USB 2.0 upstream data minus (D-).

TABLE 3-3: USB 2.0 PIN DESCRIPTIONS (CONTINUED)

Num Pins	Symbol	Buffer Type	Description
4	USB2DN_DP[4:1]	IO-U	USB 2.0 downstream ports 4-1 data plus (D+).
	<u>PRT_DIS_P[4:1]</u>	I	Port 4-1 D+ Disable Configuration Strap. These configuration straps are used in conjunction with the corresponding <u>PRT_DIS_M[4:1]</u> straps to disable the related port (4-1). Refer to Section 3.4.2, "Port Disable Configuration (PRT_DIS_P[4:1] / PRT_DIS_M[4:1])" for more information. See Note 2 .
4	USB2DN_DM[4:1]	IO-U	USB 2.0 downstream ports 4-1 data minus (D-).
	<u>PRT_DIS_M[4:1]</u>	I	Port 4-1 D- Disable Configuration Strap. These configuration straps are used in conjunction with the corresponding <u>PRT_DIS_P[4:1]</u> straps to disable the related port (4-1). Refer to Section 3.4.2, "Port Disable Configuration (PRT_DIS_P[4:1] / PRT_DIS_M[4:1])" for more information. See Note 2 .
1	VBUS_DET	IS	This signal detects the state of the upstream bus power. When designing a detachable hub, this pin must be connected to the VBUS power pin of the upstream USB port through a resistor divider (50 kΩ by 100 kΩ) to provide 3.3 V. For self-powered applications with a permanently attached host, this pin must be connected to either 3.3 V or 5.0 V through a resistor divider to provide 3.3 V. In embedded applications, VBUS_DET may be controlled (toggled) when the host desires to renegotiate a connection without requiring a full reset of the device.
	GPIO16	I/O6	General purpose input/output 16.

Note 2: Configuration strap values are latched on Power-On Reset (POR) and the rising edge of **RESET_N** (external chip reset). Configuration straps are identified by an underlined symbol name. Signals that function as configurations traps must be augmented with an external resistor when connected to a load. Refer to [Section 3.4, "Configuration Straps and Programmable Functions"](#) for additional information.

TABLE 3-4: USB PORT CONTROL PIN DESCRIPTIONS

Num Pins	Symbol	Buffer Type	Description
1	PRT_CTL1	I (PU)	Port 1 Power Enable / Overcurrent Sense. As an output, this signal is an active high control signal used to enable power to the downstream port 1. As an input, this signal indicates an overcurrent condition from an external current monitor on USB port 1.
1	PRT_CTL2	I (PU)	Port 2 Power Enable / Overcurrent Sense. As an output, this signal is an active high control signal used to enable power to the downstream port 2. As an input, this signal indicates an overcurrent condition from an external current monitor on USB port 2.

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TABLE 3-4: USB PORT CONTROL PIN DESCRIPTIONS (CONTINUED)

Num Pins	Symbol	Buffer Type	Description
1	PRT_CTL3	I (PU)	Port 3 Power Enable / Overcurrent Sense. As an output, this signal is an active high control signal used to enable power to the downstream port 3. As an input, this signal indicates an overcurrent condition from an external current monitor on USB port 3.
1	PRT_CTL4	I (PU)	Port 4 Power Enable / Overcurrent Sense. As an output, this signal is an active high control signal used to enable power to the downstream port 4. As an input, this signal indicates an overcurrent condition from an external current monitor on USB port 4.
	<u>GANG_PWR</u>	I (PU)	When pulled high enables gang mode. Gang power pin when used in gang mode.

TABLE 3-5: SPI/SMBUS PIN DESCRIPTIONS

Num Pins	Symbol	Buffer Type	Description
1	SPI_CE_N	O12	Active low SPI chip enable output.
	GPIO7	I/O12	General purpose input/output 7.
	<u>CFG_NON_REM</u>	I	Non-Removable Port Configuration Strap. This configuration strap is used to configure the number of non-removable ports. Refer to Section 3.4.3, "Non-Removable Port Configuration (CFG_NON_REM)" for more information. See Note 3 .
1	SPI_CLK	O6	SPI clock output to the serial ROM, when configured for SPI operation.
	SMCLK	OD12	SMBus clock pin, when configured for SMBus slave operation.
	GPIO4	I/O6	General purpose input/output 4.
1	SPI_DO	O6	SPI data output, when configured for SPI operation.
	SMDAT	I/O12	SMBus data pin, when configured for SMBus slave operation.
	GPIO5	I/O6	General purpose input/output 5.
1	SPI_DI	IS	SPI data input, when configured for SPI operation.
	GPIO9	I/O12	General purpose input/output 9.
	<u>CFG_BC_EN</u>	I	Battery Charging Configuration Strap. This configuration strap is used to enable battery charging. Refer to Section 3.4.4, "Battery Charging Configuration (CFG_BC_EN)" for more information. See Note 3 .

Note 3: Configuration strap values are latched on Power-On Reset (POR) and the rising edge of **RESET_N** (external chip reset). Configuration straps are identified by an underlined symbol name. Signals that function as configurations traps must be augmented with an external resistor when connected to a load. Refer to [Section 3.4, "Configuration Straps and Programmable Functions"](#) for additional information.

TABLE 3-6: MISCELLANEOUS PIN DESCRIPTIONS

Num Pins	Symbol	Buffer Type	Description
1	RESET_N	IS	The RESET_N pin puts the device into Reset Mode, as the name of the pin and function then align.
1	XTALI	ICLK	External 25 MHz crystal input
	CLK_IN	ICLK	External reference clock input. The device may alternatively be driven by a single-ended clock oscillator. When this method is used, XTALO should be left unconnected.
1	XTALO	OCLK	External 25 MHz crystal output
1	RBIAS	AI	A 12.0 k Ω (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings.
1	ATEST	AI	Analog test pin.
			This signal is used for test purposes and must always be connected to ground.

TABLE 3-7: POWER AND GROUND PIN DESCRIPTIONS

Num Pins	Symbol	Buffer Type	Description
4	VDD33	P	+3.3 V power and internal regulator input Refer to Section 4.1, "Power Connections" for power connection information.
8	VDD12	P	+1.2 V core power Refer to Section 4.1, "Power Connections" for power connection information.
Pad	VSS	P	Common ground. This exposed pad must be connected to the ground plane with a via array.

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3.3 Buffer Types

TABLE 3-8: BUFFER TYPES

Buffer Type	Description
I	Input
IS	Schmitt-triggered input
O6	Output with 6 mA sink and 6 mA source
O12	Output with 12 mA sink and 12 mA source
OD12	Open-drain output with 12 mA sink
PU	50 μ A (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50 μ A (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
IO-U	Analog input/output as defined in USB specification
AI	Analog input
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power pin

Note: Refer to [Section 9.5, "DC Specifications"](#) for individual buffer DC electrical characteristics.

3.4 Configuration Straps and Programmable Functions

Configuration straps are multi-function pins that are used during Power-On Reset (POR) or external chip reset (**RESET_N**) to determine the default configuration of a particular feature. The state of the signal is latched following de-assertion of the reset. Configuration straps are identified by an underlined symbol name. This section details the various device configuration straps and associated programmable pin functions.

Note: The system designer must guarantee that configuration straps meet the timing requirements specified in [Section 9.6.2, "Power-On and Configuration Strap Timing," on page 34](#) and [Section 9.6.3, "Reset and Configuration Strap Timing," on page 35](#). If configuration straps are not at the correct voltage level prior to being latched, the device may capture incorrect strap values.

3.4.1 SPI/SMBUS CONFIGURATION

The SPI/SMBus pins can be configured into one of two functional modes:

- SPI Mode
- SMBus Slave Mode

If 10 k Ω pull-up resistors are detected on **SPI_DO** and **SPI_CLK**, the SPI/SMBus pins are configured into SMBus Slave Mode. If no pull-ups or pull-downs are detected on **SPI_DO** and **SPI_CLK**, the SPI/SMBus pins are first configured into SPI Mode. The strap settings for these supported modes are detailed in [Table 3-9](#). The individual pin function assignments for each mode are detailed in [Table 3-10](#). For additional device connection information, refer to [Section 4.0, "Device Connections"](#).

TABLE 3-9: SPI/SMBUS MODE CONFIGURATION SETTINGS

Pin	SPI Mode (Note 4)	SMBus Slave Mode
39 (SPI_DO)	No pull-up/down	10 k Ω pull-up
38 (SPI_CLK)	No pull-up/down	10 k Ω pull-up

Note 4: In order to use the SPI interface, an SPI ROM containing a valid signature of $2DFU$ (device firmware upgrade) beginning at address 0xFFFA must be present. Refer to [Section 7.1, "SPI Master Interface"](#) for additional information.

TABLE 3-10: SPI/SMBUS MODE PIN ASSIGNMENTS

Pin	SPI Mode	SMBus Slave Mode
41	SPI_CE_N	<u>CFG_NON_REM</u>
40	SPI_DI	<u>CFG_BC_EN</u>
39	SPI_DO	SMDAT
38	SPI_CLK	SMCLK

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3.4.2 PORT DISABLE CONFIGURATION (PRT_DIS P[4:1] / PRT_DIS M[4:1])

The PRT_DIS P[4:1] and PRT_DIS M[4:1] configuration straps are used in conjunction to disable the related port (4-1).

For PRT_DIS P_x (where *x* is the corresponding port 4-1):

0 = Port *x* D+ Enabled

1 = Port *x* D+ Disabled

For PRT_DIS M_x (where *x* is the corresponding port 4-1):

0 = Port *x* D- Enabled

1 = Port *x* D- Disabled

Note: Both PRT_DIS P_x and PRT_DIS M_x (where *x* is the corresponding port) must be tied to 3.3 V to disable the associated downstream port. Disabling the USB 2.0 port will also disable the corresponding USB 3.1 Gen 1 port.

3.4.3 NON-REMOVABLE PORT CONFIGURATION (CFG_NON_REM)

The CFG_NON_REM configuration strap is used to configure the non-removable port settings of the device to one of five settings. These modes are selected by the configuration of an external resistor on the CFG_NON_REM pin. The resistor options are a 200 kΩ pull-down, 200 kΩ pull-up, 10 kΩ pull-down, 10 kΩ pull-up, and 10 Ω pull-down, as shown in [Table 3-11](#).

TABLE 3-11: CFG_NON_REM RESISTOR ENCODING

<u>CFG_NON_REM</u> Resistor Value	Setting
200 kΩ Pull-Down	All ports removable
200 kΩ Pull-Up	Port 1 non-removable
10 kΩ Pull-Down	Port 1, 2 non-removable
10 kΩ Pull-Up	Port 1, 2, 3, non-removable
10 Ω Pull-Down	Port 1, 2, 3, 4 non-removable

3.4.4 BATTERY CHARGING CONFIGURATION (CFG_BC_EN)

The CFG_BC_EN configuration strap is used to configure the battery charging port settings of the device to one of five settings. These modes are selected by the configuration of an external resistor on the CFG_BC_EN pin. The resistor options are a 200 kΩ pull-down, 200 kΩ pull-up, 10 kΩ pull-down, 10 kΩ pull-up, and 10 Ω pull-down, as shown in [Table 3-12](#).

TABLE 3-12: CFG_BC_EN RESISTOR ENCODING

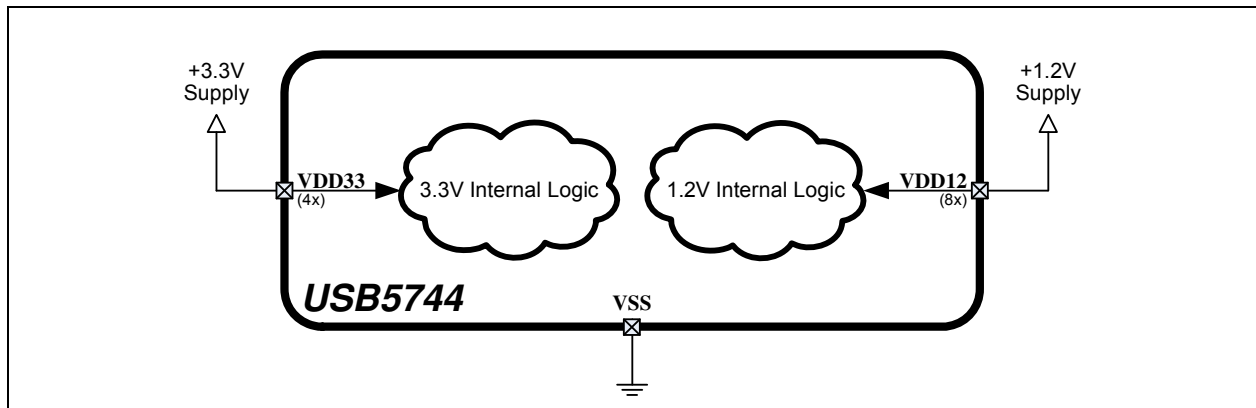
<u>CFG_BC_EN</u> Resistor Value	Setting
200 kΩ Pull-Down	No battery charging
200 kΩ Pull-Up	Port 1 battery charging
10 kΩ Pull-Down	Port 1, 2 battery charging
10 kΩ Pull-Up	Port 1, 2, 3, battery charging
10 Ω Pull-Down	Port 1, 2, 3, 4 battery charging

4.0 DEVICE CONNECTIONS

4.1 Power Connections

Figure 4-1 illustrates the device power connections.

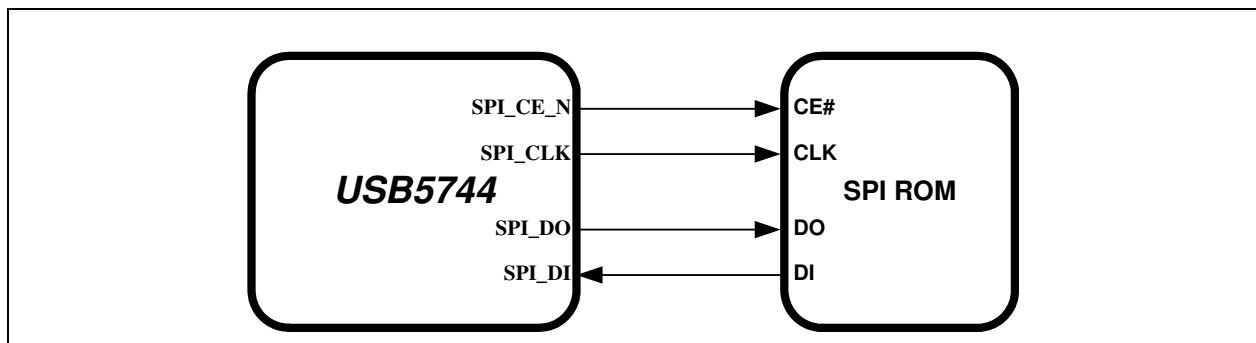
FIGURE 4-1: POWER CONNECTIONS



4.2 SPI ROM Connections

Figure 4-2 illustrates the device SPI ROM connections. Refer to Section 7.1, "SPI Master Interface," on page 23 for additional information on this device interface.

FIGURE 4-2: SPI ROM CONNECTIONS

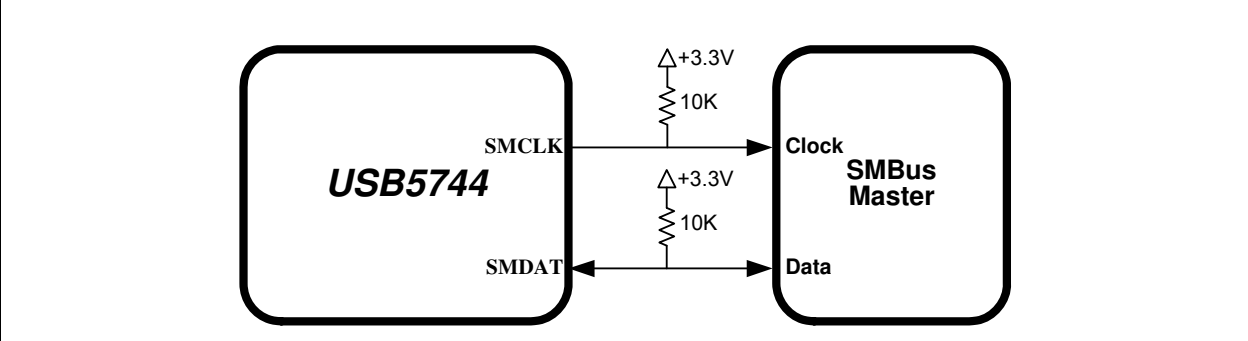


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4.3 SMBus Slave Connections

Figure 4-3 illustrates the device SMBus slave connections. Refer to [Section 7.2, "SMBus Slave Interface,"](#) on page 23 for additional information on this device interface.

FIGURE 4-3: SMBUS SLAVE CONNECTIONS



5.0 MODES OF OPERATION

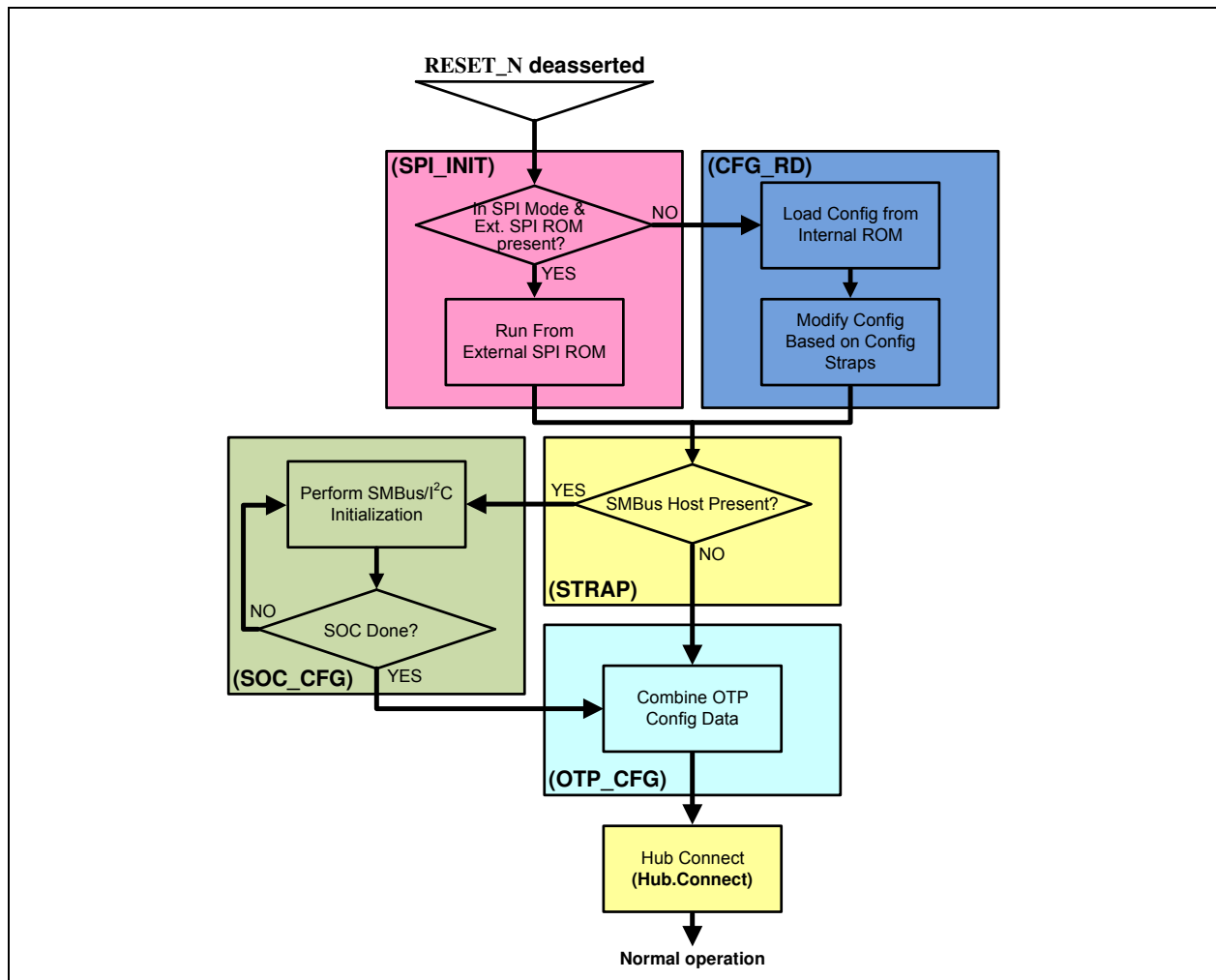
The device provides two main modes of operation: Standby Mode and Hub Mode. These modes are controlled via the **RESET_N** pin, as shown in [Table 5-1](#).

TABLE 5-1: MODES OF OPERATION

RESET_N Input	Summary
0	Standby Mode: This is the lowest power mode of the device. No functions are active other than monitoring the RESET_N input. All port interfaces are high impedance and the PLL is halted. Refer to Section 8.2.2, "External Chip Reset (RESET_N)" for additional information on RESET_N .
1	Hub (Normal) Mode: The device operates as a configurable USB hub with battery charger detection. This mode has various sub-modes of operation, as detailed in Figure 5-1 . Power consumption is based on the number of active ports, their speed, and amount of data received.

The flowchart in [Figure 5-1](#) details the modes of operation and details how the device traverses through the Hub Mode stages (shown in bold). The remaining sub-sections provide more detail on each stage of operation.

FIGURE 5-1: HUB MODE FLOWCHART



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5.1 Boot Sequence

5.1.1 STANDBY MODE

If the **RESET_N** pin is asserted, the hub will be in Standby Mode. This mode provides a very low power state for maximum power efficiency when no signaling is required. This is the lowest power state. In Standby Mode all downstream ports are disabled, the USB data pins are held in a high-impedance state, all transactions immediately terminate (no states saved), all internal registers return to their default state, the PLL is halted, and core logic is powered down in order to minimize power consumption. Because core logic is powered off, no configuration settings are retained in this mode and must be re-initialized after **RESET_N** is negated high.

5.1.2 SPI INITIALIZATION STAGE (SPI_INIT)

The first stage, the initialization stage, occurs on the deassertion of **RESET_N**. In this stage, the internal logic is reset, the PLL locks if a valid clock is supplied, and the configuration registers are initialized to their default state. The internal firmware then checks for an external SPI ROM. The firmware looks for an external SPI flash device that contains a valid signature of "2DFU" (device firmware upgrade) beginning at address 0xFFFFA. If a valid signature is found, then the external ROM is enabled and the code execution begins at address 0x0000 in the external SPI device. If a valid signature is not found, then execution continues from internal ROM (CFG_RD stage).

When using an external SPI ROM, a 1 Mbit, 60 MHz or faster ROM must be used. Both 1- and 2-bit SPI operation are supported. For optimum throughput, a 2-bit SPI ROM is recommended. Both mode 0 and mode 3 SPI ROMs are also supported.

If the system is not strapped for SPI Mode, code execution will continue from internal ROM (CFG_RD stage).

5.1.3 CONFIGURATION READ STAGE (CFG_RD)

In this stage, the internal firmware loads the default values from the internal ROM and then uses the configuration strapping options to override the default values. Refer to [Section 3.4, "Configuration Straps and Programmable Functions"](#) for information on usage of the various device configuration straps.

5.1.4 STRAP READ STAGE (STRAP)

In this stage, the firmware registers the configuration strap settings on the **SPI_DO** and **SPI_CLK** pins. Refer to [Section 3.4.1, "SPI/SMBus Configuration"](#) for information on configuring these straps. If configured for SMBus Slave Mode, the next state will be SOC_CFG. Otherwise, the next state is OTP_CFG.

5.1.5 SOC CONFIGURATION STAGE (SOC_CFG)

In this stage, the SOC can modify any of the default configuration settings specified in the integrated ROM, such as USB device descriptors and port electrical settings.

There is no time limit on this mode. In this stage the firmware will wait indefinitely for the SMBus/I²C configuration. When the SOC has completed configuring the device, it must write to register 0xFF to end the configuration.

5.1.6 OTP CONFIGURATION STAGE (OTP_CFG)

Once the SOC has indicated that it is done with configuration, all configuration data is combined in this stage. The default data, the SOC configuration data, and the OTP data are all combined in the firmware and the device is programmed.

After the device is fully configured, it will go idle and then into suspend if there is no VBUS or Hub.Connect present. Once VBUS is present, and battery charging is enabled, the device will transition to the Battery Charger Detection Stage. If VBUS is present, and battery charging is not enabled, the device will transition to the Connect stage.

5.1.7 HUB CONNECT STAGE (HUB.CONNECT)

Once the CHGDET stage is completed, the device enters the Hub Connect stage. USB connect can be initiated by asserting the VBUS pin function high. The device will remain in the Hub Connect stage indefinitely until the VBUS pin function is deasserted.

5.1.8 NORMAL MODE

Lastly, the hub enters Normal Mode of operation. In this stage full USB operation is supported under control of the USB Host on the upstream port. The device will remain in the normal mode until the operating mode is changed by the system.

If **RESET_N** is asserted low, then Standby Mode is entered. The device may then be placed into any of the designated hub stages. Asserting a soft disconnect on the upstream port will cause the hub to return to the Hub.Connect stage until the soft disconnect is negated.

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6.0 DEVICE CONFIGURATION

The device supports a large number of features (some mutually exclusive), and must be configured in order to correctly function when attached to a USB host controller. The hub can be configured either internally or externally depending on the implemented interface.

Microchip provides a comprehensive software programming tool, Pro-Touch, for configuring the USB5744 functions, registers and OTP memory. All configuration is to be performed via the Pro-Touch programming tool. For additional information on the Pro-Touch programming tool, refer to the Software Libraries within the Microchip USB5744 product page at www.microchip.com/USB5744.

<p>Note: Device configuration straps and programmable pins are detailed in Section 3.4, "Configuration Straps and Programmable Functions," on page 15. Refer to Section 7.0, "Device Interfaces" for detailed information on each device interface.</p>
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6.1 Customer Accessible Functions

The following USB or SMBus accessible functions are available to the customer via the Pro-Touch Programming Tool.

<p>Note: For additional programming details, refer to the Pro-Touch programming tool.</p>
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6.1.1 USB ACCESSIBLE FUNCTIONS

6.1.1.1 OTP Access over USB

The OTP ROM in the device is accessible via the USB bus. All OTP parameters can be modified to the USB Host. The OTP operates in Single Ended mode. For more information, refer to the Microchip USB5744 product page and SDK at www.microchip.com/USB5744

6.1.1.2 Battery Charging Access over USB

The Battery charging behavior of the device can be dynamically changed by the USB Host when something other than the preprogrammed or OTP programmed behavior is desired. For more information, refer to the Microchip USB5744 product page and SDK at www.microchip.com/USB5744

6.1.2 SMBUS ACCESSIBLE FUNCTIONS

OTP access and configuration of specific device functions are possible via the USB5744 SMBus. All OTP parameters can be modified via the SMBus Host. The OTP can be programmed to operate in Single-Ended, Differential, Redundant, or Differential Redundant mode, depending on the level of reliability required. For more information, refer to AN1903 - "Configuration Options for the USB5734 and USB5744" application note at www.microchip.com/AN1903.

7.0 DEVICE INTERFACES

The USB5744 provides multiple interfaces for configuration and external memory access. This section details the various device interfaces and their usage:

- [SPI Master Interface](#)
- [SMBus Slave Interface](#)

Note: For details on how to enable each interface, refer to [Section 3.4.1, "SPI/SMBus Configuration"](#).

For information on device connections, refer to [Section 4.0, "Device Connections"](#). For information on device configuration, refer to [Section 6.0, "Device Configuration"](#).

Microchip provides a comprehensive software programming tool, Pro-Touch, for configuring the USB5744 functions, registers and OTP memory. All configuration is to be performed via the Pro-Touch programming tool. For additional information on the Pro-Touch programming tool, refer to Software Libraries within Microchip USB5744 product page at www.microchip.com/USB5744.

7.1 SPI Master Interface

The device is capable of code execution from an external SPI ROM. When configured for SPI Mode, on power up the firmware looks for an external SPI flash device that contains a valid signature of 2DFU (device firmware upgrade) beginning at address 0xFFFFA. If a valid signature is found, then the external ROM is enabled and the code execution begins at address 0x0000 in the external SPI device. If a valid signature is not found, then execution continues from internal ROM.

Note: For SPI timing information, refer to [Section 9.6.7, "SPI Timing"](#).

7.2 SMBus Slave Interface

The device includes an integrated SMBus slave interface, which can be used to access internal device run time registers or program the internal OTP memory. SMBus slave detection is accomplished by detection of pull-up resistors on both the SMDAT and SMCLK signals. Refer to [Section 3.4.1, "SPI/SMBus Configuration"](#) for additional information.

Note: All device configuration must be performed via the Pro-Touch Programming Tool. For additional information on the Pro-Touch programming tool, refer to Software Libraries within Microchip USB5744 product page at www.microchip.com/USB5744.

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8.0 FUNCTIONAL DESCRIPTIONS

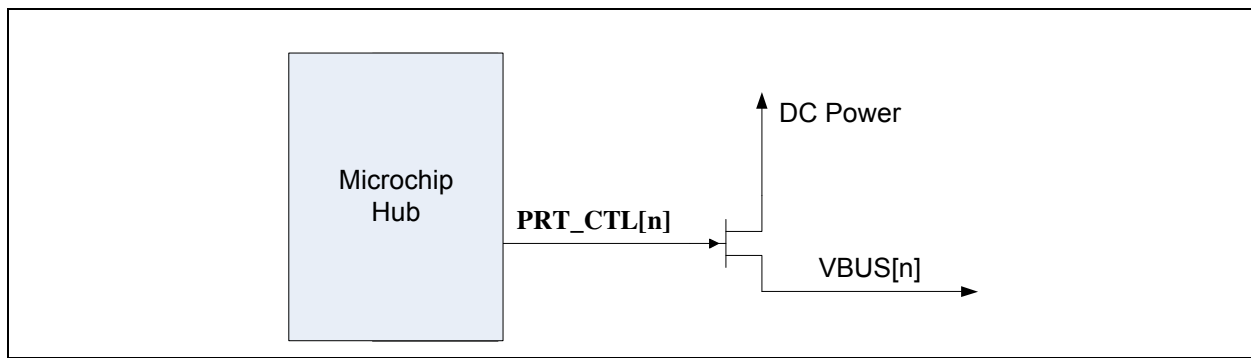
This section details various USB5744 functions, including:

- [Downstream Battery Charging](#)
- [Resets](#)
- [Link Power Management \(LPM\)](#)
- [Port Control Interface](#)

8.1 Downstream Battery Charging

The device can be configured by an OEM to have any of the downstream ports support battery charging. The hub's role in battery charging is to provide acknowledgment to a device's query as to whether the hub system supports USB battery charging. The hub silicon does not provide any current or power FETs or any additional circuitry to actually charge the device. Those components must be provided externally by the OEM.

FIGURE 8-1: BATTERY CHARGING EXTERNAL POWER SUPPLY



If the OEM provides an external supply capable of supplying current per the battery charging specification, the hub can be configured to indicate the presence of such a supply from the device. This indication, via the **PRT_CTL[4:1]** pins, is on a per port basis. For example, the OEM can configure two ports to support battery charging through high current power FETs and leave the other two ports as standard USB ports.

For additional information, refer to the Microchip USB5744 Battery Charging application note on the Microchip.com USB5744 product page at www.microchip.com/USB5744.

8.2 Resets

The device includes the following chip-level reset sources:

- [Power-On Reset \(POR\)](#)
- [External Chip Reset \(RESET_N\)](#)
- [USB Bus Reset](#)

8.2.1 POWER-ON RESET (POR)

A power-on reset occurs whenever power is initially supplied to the device, or if power is removed and reapplied to the device. A timer within the device will assert the internal reset per the specifications listed in [Section 9.6.2, "Power-On and Configuration Strap Timing," on page 34](#).

8.2.2 EXTERNAL CHIP RESET (RESET_N)

A valid hardware reset is defined as assertion of **RESET_N**, after all power supplies are within operating range, per the specifications in [Section 9.6.3, "Reset and Configuration Strap Timing," on page 35](#). While reset is asserted, the device (and its associated external circuitry) enters Standby Mode and consumes minimal current.

Assertion of **RESET_N** causes the following:

1. The PHY is disabled and the differential pairs will be in a high-impedance state.
2. All transactions immediately terminate; no states are saved.
3. All internal registers return to the default state.
4. The external crystal oscillator is halted.
5. The PLL is halted.

Note: All power supplies must have reached the operating levels mandated in [Section 9.2, "Operating Conditions**," on page 30](#), prior to (or coincident with) the assertion of **RESET_N**.

8.2.3 USB BUS RESET

In response to the upstream port signaling a reset to the device, the device performs the following:

Note: The device does not propagate the upstream USB reset to downstream devices.

1. Sets default address to 0.
2. Sets configuration to Unconfigured.
3. Moves device from suspended to active (if suspended).
4. Complies with the USB Specification for behavior after completion of a reset sequence.

The host then configures the device in accordance with the USB Specification.

8.3 Link Power Management (LPM)

The device supports the L0 (On), L1 (Sleep), and L2 (Suspend) link power management states. These supported LPM states offer low transitional latencies in the tens of microseconds versus the much longer latencies of the traditional USB suspend/resume in the tens of milliseconds. The supported LPM states are detailed in [Table 8-1](#).

TABLE 8-1: LPM STATE DEFINITIONS

State	Description	Entry/Exit Time to L0
L2	Suspend	Entry: ~3 ms Exit: ~2 ms (from start of RESUME)
L1	Sleep	Entry: <10 us Exit: <50 us
L0	Fully Enabled (On)	-