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USB5807

7-Port USB 3.1 Gen 1 Hub

Highlights

- USB Hub with 7 USB 3.1 Gen 1 / USB 2.0 downstream ports
- USB-IF Battery Charger revision 1.2 support on up & downstream ports (DCP, CDP, SDP)
- **FlexConnect:** Downstream port able to swap with upstream port, allowing master capable devices to control other devices on the hub
- USB Link Power Management (LPM) support
- Enhanced OEM configuration options available through either OTP or SPI ROM
- Available in 100-pin (12mm x 12mm) VQFN RoHS compliant package
- Commercial and industrial grade temperature support

Target Applications

- Standalone USB Hubs
- Laptop Docks
- PC Motherboards
- PC Monitor Docks
- Multi-function USB 3.1 Gen 1 Peripherals

Key Benefits

- USB 3.1 Gen 1 compliant 5 Gbps, 480 Mbps, 12 Mbps, and 1.5Mbps operation
  - 5V tolerant USB 2.0 pins
  - 1.32V tolerant USB 3.1 Gen 1 pins
  - Integrated termination and pull-up/down resistors
- Supports battery charging of most popular battery powered devices on all ports
  - USB-IF Battery Charging rev. 1.2 support (DCP, CDP, SDP)
  - Apple® portable product charger emulation
  - Chinese YD/T 1591-2006 charger emulation
  - Chinese YD/T 1591-2009 charger emulation
  - European Union universal mobile charger support
  - Support for Microchip UCS100x family of battery charging controllers
  - Supports additional portable devices
- Smart port controller operation
  - Firmware handling of companion port power controllers
- On-chip microcontroller
  - manages I/Os, VBUS, and other signals
- 8 KB RAM, 64 KB ROM
- 8 KB One-Time-Programmable (OTP) ROM
  - Includes on-chip charge pump
- Configuration programming via OTP ROM, SPI ROM, or SMBus
- **FlexConnect**
  - Reversible upstream and downstream Port 1 roles on command
- **PortSwap**
  - Configurable USB 2.0 differential pair signal swap
- **PHYBoost**™
  - Programmable USB transceiver drive strength for recovering signal integrity
- **VariSense**™
  - Programmable USB receive sensitivity
- **Port Split**
  - USB2.0 and USB3.1 Gen1 port operation can be split for custom applications using embedded USB3.x devices in parallel with USB2.0 devices.
- Compatible with Microsoft Windows 10, 8, 7, XP, Apple OS X 10.4+, and Linux hub drivers
- Optimized for low-power operation and low thermal dissipation
- Package
  - 100-pin VQFN (12mm x 12mm)

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1.0 PREFACE

1.1 General Terms

TABLE 1-1: GENERAL TERMS

Term	Description
ADC	Analog-to-Digital Converter
Byte	8 bits
CDC	Communication Device Class
CSR	Control and Status Registers
DWORD	32 bits
EOP	End of Packet
EP	Endpoint
FIFO	First In First Out buffer
FS	Full-Speed
FSM	Finite State Machine
GPIO	General Purpose I/O
HS	Hi-Speed
HSOS	High Speed Over Sampling
Hub Feature Controller	The Hub Feature Controller, sometimes called a Hub Controller for short is the internal processor used to enable the unique features of the USB Controller Hub. This is not to be confused with the USB Hub Controller that is used to communicate the hub status back to the Host during a USB session.
I^2C	Inter-Integrated Circuit
LS	Low-Speed
lsb	Least Significant Bit
LSB	Least Significant Byte
msb	Most Significant Bit
MSB	Most Significant Byte
N/A	Not Applicable
NC	No Connect
OTP	One Time Programmable
PCB	Printed Circuit Board
PCS	Physical Coding Sublayer
PHY	Physical Layer
PLL	Phase Lock Loop
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
SDK	Software Development Kit
SMBus	System Management Bus
UUID	Universally Unique IDentifier
WORD	16 bits

1.2 Reference Documents

1. *UNICODE UTF-16LE For String Descriptors* USB Engineering Change Notice, December 29th, 2004, http://www.usb.org
2. *Universal Serial Bus Revision 3.1 Specification*, http://www.usb.org
3. *Battery Charging Specification*, Revision 1.2, Dec. 07, 2010, http://www.usb.org
4. *I^2C-Bus Specification*, Version 1.1, http://www.nxp.com
5. *System Management Bus Specification*, Version 1.0, http://smbus.org/specs

2.0 INTRODUCTION

2.1 General Description

The Microchip USB5807 hub is a low-power, OEM configurable, USB 3.1 Gen 1 hub controller with 7 downstream ports and advanced features for embedded USB applications. The USB5807 is fully compliant with the Universal Serial Bus Revision 3.1 Specification and USB 2.0 Link Power Management Addendum. The USB5807 supports 5 Gbps SuperSpeed (SS), 480 Mbps Hi-Speed (HS), 12 Mbps Full-Speed (FS), and 1.5 Mbps Low-Speed (LS) USB downstream devices on all enabled downstream ports.

The USB5807 supports the legacy USB speeds (HS/FS/LS) through a dedicated USB 2.0 hub controller that is the culmination of five generations of Microchip hub controller design and experience with proven reliability, interoperability, and device compatibility. The SuperSpeed hub controller operates in parallel with the USB 2.0 hub controller, decoupling the 5 Gbps SS data transfers from bottlenecks due to the slower USB 2.0 traffic.

The USB5807 enables OEMs to configure their system using “Configuration Straps.” These straps simplify the configuration process, assigning default values to USB 3.1 Gen 1 ports and GPIOs. OEMs can disable ports, enable battery charging, and define GPIO functions as default assignments on power-up, removing the need for OTP or external SPI ROM.

The USB5807 supports downstream battery charging via the integrated battery charger detection circuitry, which supports the USB-IF Battery Charging (BC1.2) detection method and most Apple devices. The USB5807 provides the battery charging handshake and supports the following USB-IF BC1.2 charging profiles:

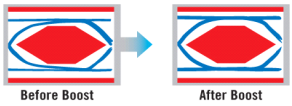
- DCP: Dedicated Charging Port (Power brick with no data)
- CDP: Charging Downstream Port (1.5A with data)
- SDP: Standard Downstream Port (0.5A with data)
- Custom profiles loaded via SMBus or OTP

Additionally, the USB5807 includes many powerful and unique features such as:

FlexConnect, which provides flexible connectivity options. One of the USB5807’s downstream ports can be reconfigured to become the upstream port, allowing master capable devices to control other devices on the hub.

PortSwap, which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.

PHYBoost, which provides programmable levels of Hi-Speed USB signal drive strength in the downstream port transceivers. PHYBoost attempts to restore USB signal integrity in a compromised system environment. The graphic on the right shows an example of Hi-Speed USB eye diagrams before and after PHYBoost signal integrity restoration. in a compromised system environment.



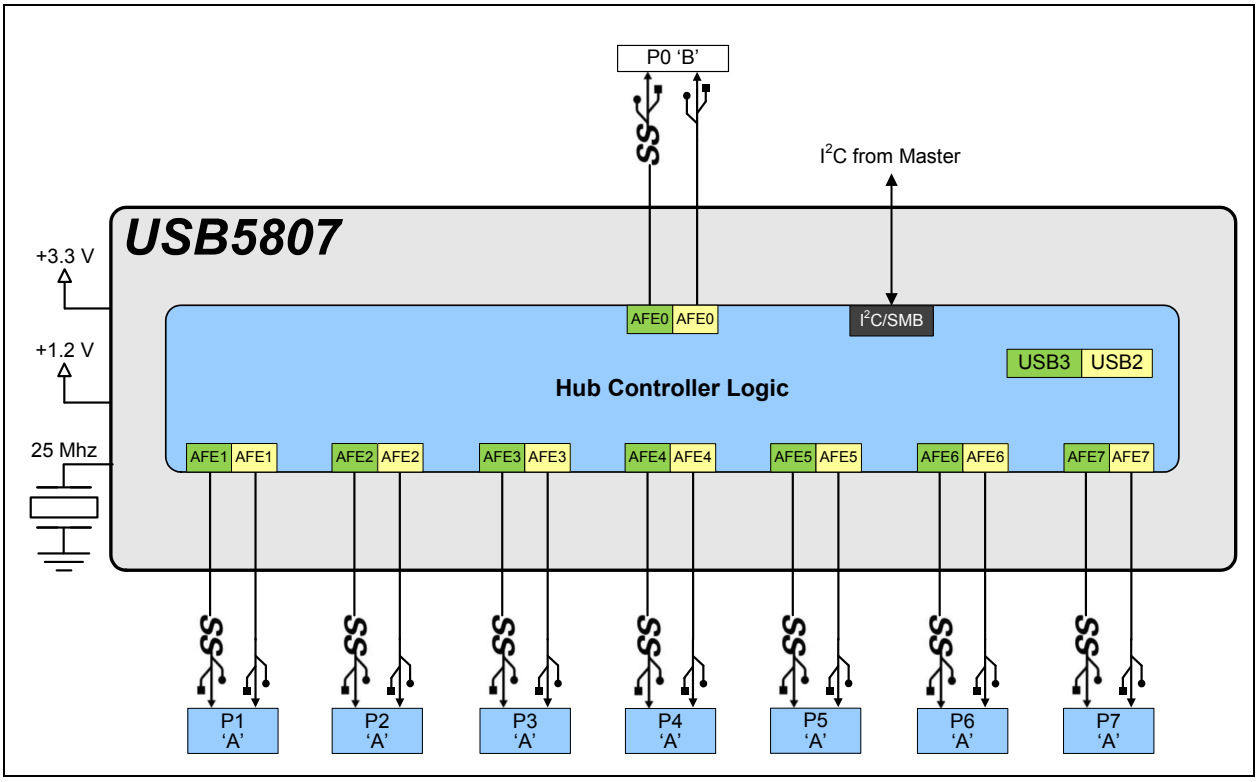
VariSense, which controls the USB receiver sensitivity enabling programmable levels of USB signal receive sensitivity. This capability allows operation in a sub-optimal system environment, such as when a captive USB cable is used.

Port Split, which allows for the USB3.1 Gen1 and USB2.0 portions of downstream ports 5 and 6 to operate independently and enumerate two separate devices in parallel in special applications.

The USB5807 can be configured for operation through internal default settings. Custom OEM configurations are supported through external SPI ROM or OTP ROM. All port control signal pins are under firmware control in order to allow for maximum operational flexibility, and are available as GPIOs for customer specific use.

The USB5807 is available in commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature ranges. An internal block diagram of the USB5807 is shown in Figure 2-1.

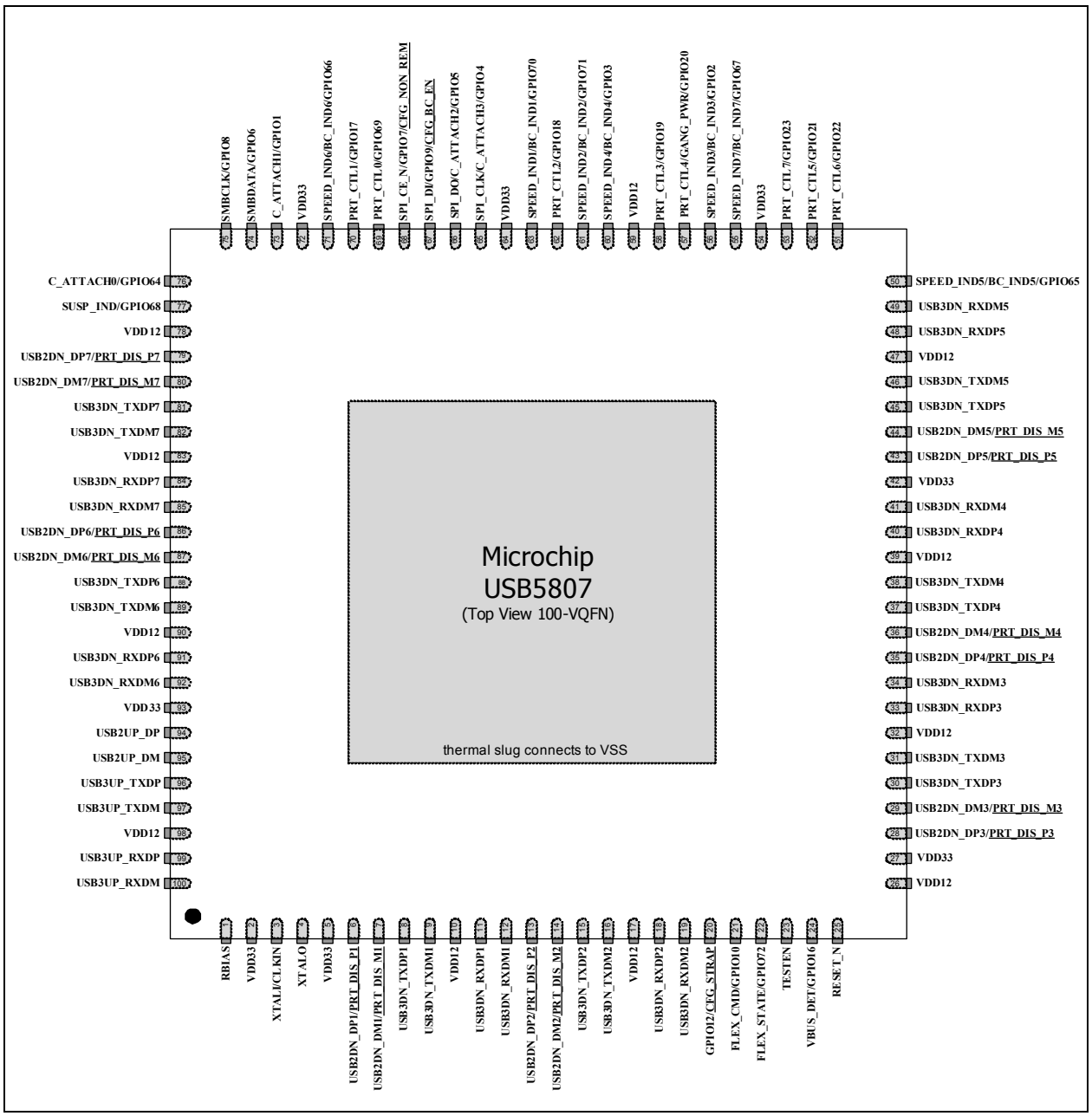
FIGURE 2-1: INTERNAL BLOCK DIAGRAM



3.0 PIN DESCRIPTIONS

3.1 Pin Diagram

FIGURE 3-1: PIN ASSIGNMENTS (TOP VIEW)



Note 1: Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to Section 3.5, Configuration Straps and Programmable Functions

3.2 Pin Symbols

Pin Num.	Pin Name	Reset	Pin Num.	Pin Name	Reset
1	RBIAS	A/P	51	PRT_CTL6/GPIO22	PD-50k
2	VDD33	A/P	52	PRT_CTL5/GPIO21	PD-50k
3	XTALI/CLKIN	A/P	53	PRT_CTL7/GPIO23	PD-50k
4	XTALO	A/P	54	VDD33	A/P
5	VDD33	A/P	55	SPEED_IND7/BC_IND7/GPIO67	Z
6	USB2DN_DP1/PRT_DIS_P1	PD-15k	56	SPEED_IND3/BC_IND3/GPIO2	Z
7	USB2DN_DM1/PRT_DIS_M1	PD-15k	57	PRT_CTL4/GANG_PWR/GPIO20	PD-50k
8	USB3DN_TXDP1	Z	58	PRT_CTL3/GPIO19	PD-50k
9	USB3DN_TXDM1	Z	59	VDD12	A/P
10	VDD12	A/P	60	SPEED_IND4/BC_IND4/GPIO3	Z
11	USB3DN_RXDP1	Z	61	SPEED_IND2/BC_IND2/GPIO71	Z
12	USB3DN_RXDM1	Z	62	PRT_CTL2/GPIO18	PD-50k
13	USB2DN_DP2/PRT_DIS_P2	PD-15k	63	SPEED_IND1/BC_IND1/GPIO70	Z
14	USB2DN_DM2/PRT_DIS_M2	PD-15k	64	VDD33	A/P
15	USB3DN_TXDP2	Z	65	SPI_CLK/C_ATTACH3/GPIO4	Z
16	USB3DN_TXDM2	Z	66	SPI_DO/C_ATTACH2/GPIO5	PD-50k
17	VDD12	A/P	67	SPI_DI/GPIO9/CFG_BC_EN	Z
18	USB3DN_RXDP2	Z	68	SPI_CE_N/GPIO7/CFG_NON_REM	PU-50k
19	USB3DN_RXDM2	Z	69	PRT_CTL0/GPIO69	Z
20	GPIO12/CFG_STRAP	Z	70	PRT_CTL1/GPIO17	PD-50k
21	FLEX_CMD/GPIO10	Z	71	SPEED_IND6/BC_IND6/GPIO66	Z
22	FLEX_STATE/GPIO72	Z	72	VDD33	A/P
23	TESTEN	Z	73	C_ATTACH1/GPIO1	Z
24	VBUS_DET/GPIO16	Z	74	SMBDATA/GPIO6	Z
25	RESET_N	R	75	SMBCLK/GPIO8	Z
26	VDD12	A/P	76	C_ATTACH0/GPIO64	Z
27	VDD33	A/P	77	SUSP_IND/GPIO68	Z
28	USB2DN_DP3/PRT_DIS_P3	PD-15k	78	VDD12	A/P
29	USB2DN_DM3/PRT_DIS_M3	PD-15k	79	USB2DN_DP7/PRT_DIS_P7	PD-15k
30	USB3DN_TXDP3	Z	80	USB2DN_DM7/PRT_DIS_M7	PD-15k
31	USB3DN_TXDM3	Z	81	USB3DN_TXDP7	Z
32	VDD12	A/P	82	USB3DN_TXDM7	Z
33	USB3DN_RXDP3	Z	83	VDD12	A/P
34	USB3DN_RXDM3	Z	84	USB3DN_RXDP7	Z
35	USB2DN_DP4/PRT_DIS_P4	PD-15k	85	USB3DN_RXDM7	Z
36	USB2DN_DM4/PRT_DIS_M4	PD-15k	86	USB2DN_DP6/PRT_DIS_P6	PD-15k
37	USB3DN_TXDP4	Z	87	USB2DN_DM6/PRT_DIS_M6	PD-15k
38	USB3DN_TXDM4	Z	88	USB3DN_TXDP6	Z
39	VDD12	A/P	89	USB3DN_TXDM6	Z
40	USB3DN_RXDP4	Z	90	VDD12	A/P
41	USB3DN_RXDM4	Z	91	USB3DN_RXDP6	Z
42	VDD33	A/P	92	USB3DN_RXDM6	Z
43	USB2DN_DP5/PRT_DIS_P5	PD-15k	93	VDD33	A/P
44	USB2DN_DM5/PRT_DIS_M5	PD-15k	94	USB2UP_DP	PD-1M
45	USB3DN_TXDP5	Z	95	USB2UP_DM	PD-1M
46	USB3DN_TXDM5	Z	96	USB3UP_TXDP	Z
47	VDD12	A/P	97	USB3UP_TXDM	Z
48	USB3DN_RXDP5	Z	98	VDD12	A/P
49	USB3DN_RXDM5	Z	99	USB3UP_RXDP	Z
50	SPEED_IND5/BC_IND5/GPIO65	Z	100	USB3UP_RXDM	Z

The pin reset state definitions are detailed in Table 3-1.

TABLE 3-1: PIN RESET STATE LEGEND

Symbol	Description
A/P	Analog/Power Input
R	Reset Control Input
Z	Hardware disables output driver (high impedance)
PU-50k	Hardware enables internal 50kΩ pull-up
PD-50k	Hardware enables internal 50kΩ pull-down
PD-15k	Hardware enables internal 15kΩ pull-down
PD-1M	Hardware enables internal 1M pull-down

3.3 USB5807 Pin Descriptions

This section contains descriptions of the various USB5807 pins. The pin descriptions have been broken into functional groups as follows:

- USB 3.1 Gen 1 Pin Descriptions
- USB 2.0 Pin Descriptions
- Port Control Pin Descriptions
- SPI Interface
- USB Type-C Connector Controls
- Miscellaneous Pin Descriptions
- Configuration Strap Pin Descriptions
- Power and Ground Pin Descriptions

The "_N" symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, **RESET_N** indicates that the reset signal is active low. When "_N" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of "active low" and "active high" signal. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

TABLE 3-2: USB 3.1 GEN 1 PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
USB 3.1 Gen 1 Upstream D+ TX	**USB3UP_TXDP**	I/O-U	Upstream USB 3.1 Gen 1 Transmit Data Plus
USB 3.1 Gen 1 Upstream D- TX	**USB3UP_TXDM**	I/O-U	Upstream USB 3.1 Gen 1 Transmit Data Minus
USB 3.1 Gen 1 Upstream D+ RX	**USB3UP_RXDP**	I/O-U	Upstream USB 3.1 Gen 1 Receive Data Plus
USB 3.1 Gen 1 Upstream D- RX	**USB3UP_RXDM**	I/O-U	Upstream USB 3.1 Gen 1 Receive Data Minus

TABLE 3-2: USB 3.1 GEN 1 PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
USB 3.1 Gen 1 Ports 7-1 D+ TX	**USB3DN_TXDP[7:1]**	I/O-U	Downstream Super Speed Transmit Data Plus, ports 7 through 1.
USB 3.1 Gen 1 Ports 7-1 D- TX	**USB3DN_TXDM[7:1]**	I/O-U	Downstream Super Speed Transmit Data Minus, ports 7 through 1.
USB 3.1 Gen 1 Ports 7-1 D+ RX	**USB3DN_RXDP[7:1]**	I/O-U	Downstream Super Speed Receive Data Plus, ports 7 through 1.
USB 3.1 Gen 1 Ports 7-1 D- RX	**USB3DN_RXDM[7:1]**	I/O-U	Downstream Super Speed Receive Data Minus, ports 7 through 1.

TABLE 3-3: USB 2.0 PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
USB 2.0 Upstream D+	**USB2UP_DP**	I/O-U	Upstream USB 2.0 Data Plus (D+)
USB 2.0 Upstream D-	**USB2UP_DM**	I/O-U	Upstream USB 2.0 Data Minus (D-)
USB 2.0 Ports 7 D+	**USB2DN_DP[7:1]**	I/O-U	Downstream USB 2.0 Ports 7-1 Data Plus (D+)
USB 2.0 Ports 7 D-	**USB2DN_DM[7:1]**	I/O-U	Downstream USB 2.0 Ports 7-1 Data Minus (D-)
VBUS Detect	**VBUS_DET**	IS	This signal detects the state of the upstream bus power. When designing a detachable hub, this pin must be connected to the VBUS power pin of the upstream USB port through a resistor divider (50 kΩ by 100 kΩ) to provide 3.3 V. For self-powered applications with a permanently attached host, this pin must be connected to either 3.3 V or 5.0 V through a resistor divider to provide 3.3 V. In embedded applications, **VBUS_DET** may be controlled (toggled) when the host desires to renegotiate a connection without requiring a full reset of the device.

TABLE 3-4: PORT CONTROL PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
Port 7 Power Enable / Overcurrent Sense	PRT_CTL7	I/OD12 (PU)	Port 7 Power Enable / Overcurrent Sense. When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 7. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control.
Port 6 Power Enable / Overcurrent Sense	PRT_CTL6	I/OD12 (PU)	Port 6 Power Enable / Overcurrent Sense. When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 6. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control.
Port 5 Power Enable / Overcurrent Sense	PRT_CTL5	I/OD12 (PU)	Port 5 Power Enable / Overcurrent Sense. When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 5. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control.
Port 4 Power Enable / Overcurrent Sense	PRT_CTL4	I/OD12 (PU)	Port 4 Power Enable / Overcurrent Sense. When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 4. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control.

TABLE 3-4: PORT CONTROL PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Port 3 Power Enable / Overcurrent Sense	**PRT_CTL3**	I/OD12 (PU)	Port 3 Power Enable / Overcurrent Sense. When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 3. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control.
Port 2 Power Enable / Overcurrent Sense	**PRT_CTL2**	I/OD12 (PU)	Port 2 Power Enable / Overcurrent Sense. When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 2. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control.
Port 1 Power Enable / Overcurrent Sense	**PRT_CTL1**	I/OD12 (PU)	Port 1 Power Enable / Overcurrent Sense. When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 1. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control.
Port 0 Power Enable / Overcurrent Sense	**PRT_CTL0**	I/OD12 (PU)	Port 0 Power Enable / Overcurrent Sense. When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 0. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control. **Note:** This pin is only used to control port power when FlexConnect is enabled, and Port 0 has exchanged roles with downstream Port 1.

TABLE 3-4: PORT CONTROL PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Gang Power	**GANG_PWR**	I	**GANG_PWR** becomes the port control (PRTCTL) pin for all downstream ports when the hub is configured for ganged port power control mode. All port power controllers should be controlled from this pin when the hub is configured for ganged port power mode.
FlexConnect Control	**FLEX_CMD**	I	FlexConnect control input. When low, the hub will operate in its default state. Port 0 is the upstream port and port 1 is a downstream port. When high, the hub will operate in its flexed state. Port 0 is a downstream port and port 1 is an upstream port.
FlexConnect Indicator	**FLEX_STATE**	O12	FlexConnect indicator output. Reflects the current state of FlexConnect. 0 = Hub is in default mode of operation 1 = Hub is in flexed mode of operation.

TABLE 3-5: SPI INTERFACE

Name	Symbol	Buffer Type	Description
SPI Chip Enable	**SPI_CE_N**	I/O12	This is the active low SPI chip enable output. If the SPI interface is enabled, this pin must be driven high in power-down states.
SPI Clock	**SPI_CLK**	I/O-U	This is the SPI clock out to the serial ROM. If the SPI interface is disabled, by setting the SPI_DIS-ABLE bit in the UTIL_CONFIG1 register, this pin becomes **GPIO4**. If the SPI interface is enabled this pin must be driven low during reset.
SPI Data Output	**SPI_DO**	I/O-U	SPI data output, when configured for SPI operation.
SPI Data Input	**SPI_DI**	I/O-U	SPI data input, when configured for SPI operation.

TABLE 3-6: USB TYPE-C CONNECTOR CONTROLS

Name	Symbol	Buffer Type	Description
USB Type-C Attach Control Input 0-3	C_ATTACH[0:3]	I	USB Type-C attach control input. This pin indicates to the hub when a valid USB Type-C attach has been detected. This pin is used by the hub to enable the USB 3.1 Gen 1 PHY when a Type-C connection is present. When there is no USB Type-C connection present, the USB 3.1 Gen 1 PHY is disabled to reduce power consumption. This pin behaves as follows: - 1: USB Type-C attach detected, turn respective USB 3.1 Gen 1 PHY on. - 0: No USB Type-C attach detected, turn respective USB 3.1 Gen 1 PHY off. When using legacy USB Type-A and Type-B connectors, pull these pins to 3.3V to permanently enable all USB 3.1 PHYs.

TABLE 3-7: MISCELLANEOUS PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
SMBus/I^2C Clock	SMBCLK	I/O12	SMBus/I^2C Clock The SMBus/I^2C interface acts as SMBus slave. For information on how to configure this interface refer to Section 3.5.1, CFG_STRAP Configuration.
SMBus/I^2C Data	SMBDATA	I/O12	SMBus/I^2C Data The SMBus/I^2C interface acts as SMBus slave. For information on how to configure this interface refer to Section 3.5.1, CFG_STRAP Configuration.
USB Port 7-1 Speed Indicator	SPEED_IND[7:1]	O12	USB Port Speed Indicator Indicates the connection speed of the respective port. Tri-state: Not connected 0: USB 2.0 / USB 1.1 1: USB 3.1 Gen 1

TABLE 3-7: MISCELLANEOUS PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
USB Port 7-1 Battery Charging Indicator	**BC_IND[7:1]**	O12	USB Battery Charging Indicator Indicates the connection speed of the respective port. Tri-state: Battery Charging not enabled 0: Battery Charging enabled and successful BC handshake has occurred. 1: Battery Charging enabled, but no BC handshake has occurred.
General Purpose I/O	**GPIO[1:10]**, **GPIO12**, **GPIO[16:23]**, **GPIO[64:72]**	I/O12 (PU/PD)	General Purpose Inputs/Outputs Refer to Section 3.5.5, General Purpose input/Output Configuration (GPIOx) for details.
USB 2.0 Suspend State Indicator	**SUSP_IND**	O12	USB 2.0 Suspend State Indicator **SUSP_IND** can be used as a sideband remote wakeup signal for the host when in USB 2.0 suspend.
Reset Control Input	**RESET_N**	IS	Reset Control Input This pin places the hub into Reset Mode when pulled low.
Bias Resistor	**RBIAS**	I-R	A 12.0 kΩ (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings. Place the resistor as close to the device as possible with a dedicated, low impedance connection to the GND plane.
External 25 MHz Crystal Input	**XTALI**	ICLK	External 25 MHz crystal input
External 25 MHz Reference Clock Input	**CLKIN**	ICLK	External reference clock input. The device may alternatively be driven by a single-ended clock oscillator. When this method is used, **XTALO** should be left unconnected.
External 25 MHz Crystal Output	**XTALO**	OCLK	External 25 MHz crystal output
Test	**TESTEN**	I/O12	Test pin. This signal is used for test purposes and must always be connected to ground.

TABLE 3-8: CONFIGURATION STRAP PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
Device Mode Configuration Strap	**CFG_STRAP**	I	Device Mode Configuration Strap. This configuration strap is used to set the device mode. Refer to Section 3.5.1, CFG_STRAP Configuration for details. See Note 2
Port 7-1 D+ Disable Configuration Strap	**PRT_DIS_P[7:1]**	I	Port 7-1 D+ Disable Configuration Strap. These configuration straps are used in conjunction with the corresponding **PRT_DIS_M[7:1]** straps to disable the related port (7-1). Refer to Section Section 3.5.2, Port Disable Configuration (PRT_DIS_P[7:1] / PRT_DIS_M[7:1]) for more information. See Note 2
Port 7-1 D- Disable Configuration Strap	**PRT_DIS_M[7:1]**	I	Port 7-1 D- Disable Configuration Strap. These configuration straps are used in conjunction with the corresponding **PRT_DIS_P[7:1]** straps to disable the related port (7-1). Refer to Section 3.5.2, Port Disable Configuration (PRT_DIS_P[7:1] / PRT_DIS_M[7:1]) for more information. See Note 2
Non-Removable Ports Configuration Strap	**CFG_NON_REM**	I	Configuration strap to control number of reported non-removal ports. See Section 3.5.3, Non-Removable Port Configuration (CFG_NON_REM) See Note 2
Battery Charging Configuration Strap	**CFG_BC_EN**	I	Configuration strap to control number of BC 1.2 enabled downstream ports. See Section 3.5.4, Battery Charging Configuration (CFG_BC_EN) See Note 2

2: Configuration strap values are latched on Power-On Reset (POR) and the rising edge of **RESET_N** (external chip reset). Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to Section 3.5, Configuration Straps and Programmable Functions for additional information.

TABLE 3-9: POWER AND GROUND PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
+3.3V Power Supply Input	VDD33	P	+3.3 V power and internal regulator input Refer to Section 4.1, Power Connections for power connection information
+1.2V Core Power Supply Input	VDD12	P	+1.2 V core power Refer to Section 4.1, Power Connections for power connection information.
Ground	GND	P	Common ground. This exposed pad must be connected to the ground plane with a via array.

3.4 Buffer Type Descriptions

TABLE 3-10: USB5807 BUFFER TYPE DESCRIPTIONS

BUFFER	DESCRIPTION
I	Input.
IS	Input with Schmitt trigger.
O12	Output buffer with 12 mA sink and 12 mA source.
OD12	Open-drain output with 12 mA sink
PU	50 µA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50 µA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
I/O-U	Analog input/output defined in USB specification.
I-R	RBIAS.

Note: Refer to Section 9.5, DC Specifications for individual buffer DC electrical characteristics.

3.5 Configuration Straps and Programmable Functions

Configuration straps are multi-function pins that are used during Power-On Reset (POR) or external chip reset (**RESET_N**) to determine the default configuration of a particular feature. The state of the signal is latched following de-assertion of the reset. Configuration straps are identified by an underlined symbol name. This section details the various device configuration straps and associated programmable pin functions.

Note:	The system designer must guarantee that configuration straps meet the timing requirements specified in Section 9.6.2, Power-On and Configuration Strap Timing and Section 9.6.3, Reset and Configuration Strap Timing. If configuration straps are not at the correct voltage level prior to being latched, the device may capture incorrect strap values.

3.5.1 CFG_STRAP CONFIGURATION

The **CFG_STRAP** pin is used to place the hub into preset modes of operation. The resistor options are a 200 kΩ pull-down, 200 kΩ pull-up, 10 kΩ pull-down, 10 kΩ pull-up, and 10 Ω pull-down, as shown in Table 3-11.

TABLE 3-11: CFG_STRAP RESISTOR ENCODING

CFG_STRAP Resistor Value	Config	Setting
200 kΩ Pull-Down	CONFIG1	**Speed Indicator Mode + SMBus Interface Disabled** The SMBus interface will be disabled. The following programmable pins will be re-purposed as USB Speed Indicator outputs: Pin 63: **SPEED_IND1** Pin 61: **SPEED_IND2** Pin 56: **SPEED_IND3** Pin 60: **SPEED_IND4** Pin 50: **SPEED_IND5** Pin 71: **SPEED_IND6** Pin 55: **SPEED_IND7** The **SPEED_INDx** pins operate in the following manner: Tri-state: Not connected 0: USB 2.0 / USB 1.1 1: USB 3.1 Gen 1

TABLE 3-11: CFG_STRAP RESISTOR ENCODING (CONTINUED)

CFG_STRAP Resistor Value	Config	Setting
200 kΩ Pull-Up	CONFIG2	**Speed Indicator Mode + SMBus Slave Mode** The SMBus interface will operate in Slave Mode for use with hub configuration. The following programmable pins will be re-purposed as USB Speed Indicator outputs: Pin 63: **SPEED_IND1** Pin 61: **SPEED_IND2** Pin 56: **SPEED_IND3** Pin 60: **SPEED_IND4** Pin 50: **SPEED_IND5** Pin 71: **SPEED_IND6** Pin 55: **SPEED_IND7** The **SPEED_INDx** pins operate in the following manner: Tri-state: Not connected 0: USB 2.0 / USB 1.1 1: USB 3.1 Gen 1
10 kΩ Pull-Down	CONFIG3	Unused, Reserved
10 kΩ Pull-Up	CONFIG4	Unused, Reserved
10 Ω Pull-Down	CONFIG5	**Battery Charging Indicator Mode** The following programmable pins will be re-purposed as USB Battery Charging Indicator outputs: Pin 63: **BC_IND1** Pin 61: **BC_IND2** Pin 56: **BC_IND3** Pin 60: **BC_IND4** Pin 50: **BC_IND5** Pin 71: **BC_IND6** Pin 55: **BC_IND7** The **BC_INDx** pins operate in the following manner: Tri-state: Battery Charging not enabled 0: Battery Charging enabled and successful BC handshake has occurred. 1: Battery Charging enabled, but no BC handshake has occurred.
10 Ω Pull-Up	CONFIG6	Unused, Reserved

3.5.2 PORT DISABLE CONFIGURATION (PRT_DIS_P[7:1] / PRT_DIS_M[7:1])

The **PRT_DIS_P[7:1]** and **PRT_DIS_M[7:1]** configuration straps are used in conjunction to disable the related port (7-1).

For **PRT_DIS_P*x*** (where *x* is the corresponding port 7-1):

0 = Port *x* D+ Enabled

1 = Port *x* D+ Disabled

For **PRT_DIS_M*x*** (where *x* is the corresponding port 7-1):

0 = Port *x* D- Enabled

1 = Port *x* D- Disabled

Note:	Both **PRT_DIS_P*x*** and **PRT_DIS_M*x*** (where *x* is the corresponding port) must be tied to 3.3 V to disable the associated downstream port. Disabling the USB 2.0 port will also disable the corresponding USB 3.1 Gen 1 port.

3.5.3 NON-REMOVABLE PORT CONFIGURATION (CFG_NON_REM)

The **CFG_NON_REM** configuration strap is used to configure the non-removable port settings of the device to one of five settings. These modes are selected by the configuration of an external resistor on the **CFG_NON_REM** pin. The resistor options are a 200 kΩ pull-down, 200 kΩ pull-up, 10 kΩ pull-down, 10 kΩ pull-up, 10 Ω pull-down and 10 Ω pull-up as shown in Table 3-12.

TABLE 3-12: CFG_NON_REM RESISTOR ENCODING

CFG_NON_REM Resistor Value	Setting
200 kΩ Pull-Down	All ports removable
200 kΩ Pull-Up	Port 1 non-removable
10 kΩ Pull-Down	Port 1, 2 non-removable
10 kΩ Pull-Up	Port 1, 2, 3, non-removable
10 Ω Pull-Down	Port 1, 2, 3, 4 non-removable
10 Ω Pull-Up	Port 1, 2, 3, 4, 5, 6, 7 non-removable

3.5.4 BATTERY CHARGING CONFIGURATION (CFG_BC_EN)

The **CFG_BC_EN** configuration strap is used to configure the battery charging port settings of the device to one of five settings. These modes are selected by the configuration of an external resistor on the **CFG_BC_EN** pin. The resistor options are a 200 kΩ pull-down, 200 kΩ pull-up, 10 kΩ pull-down, 10 kΩ pull-up, 10 Ω pull-down and 10 Ω pull-up as shown in Table 3-13.

TABLE 3-13: CFG_BC_EN RESISTOR ENCODING

CFG_BC_EN Resistor Value	Setting
200 kΩ Pull-Down	No battery charging
200 kΩ Pull-Up	Port 1 battery charging
10 kΩ Pull-Down	Port 1, 2 battery charging
10 kΩ Pull-Up	Port 1, 2, 3, battery charging
10 Ω Pull-Down	Port 1, 2, 3, 4 battery charging
10 Ω Pull-Up	Port 1, 2, 3, 4, 5, 6, 7 battery charging

3.5.5 GENERAL PURPOSE INPUT/OUTPUT CONFIGURATION (GPIO*x*)

General Purpose Inputs/Outputs may be used for application specific purposes. Any given GPIO may operate as an input or an output. Inputs can apply an internal 50kΩ pull-down or pull-up resistor. Outputs may drive low or drive high (3.3V). GPIOs may be configured and manipulated via SMBus.

3.5.5.1 SMBus configuration

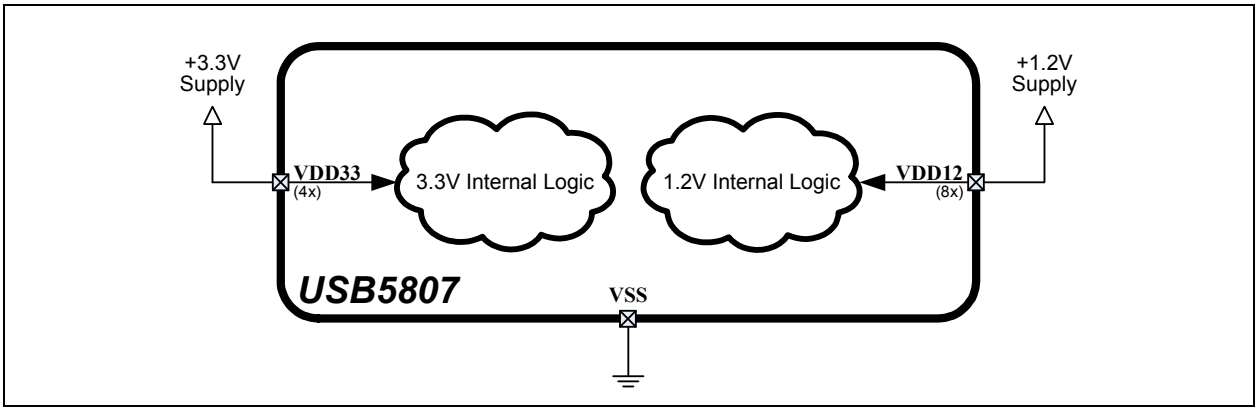
The SMBus slave interface may be used to write to internal registers that configure the state of the GPIO. Refer to the “Configuration Options for Microchip USB58xx and USB59xx Hubs” application note for additional details.

4.0 DEVICE CONNECTIONS

4.1 Power Connections

Figure 4-1 illustrates the device power connections.

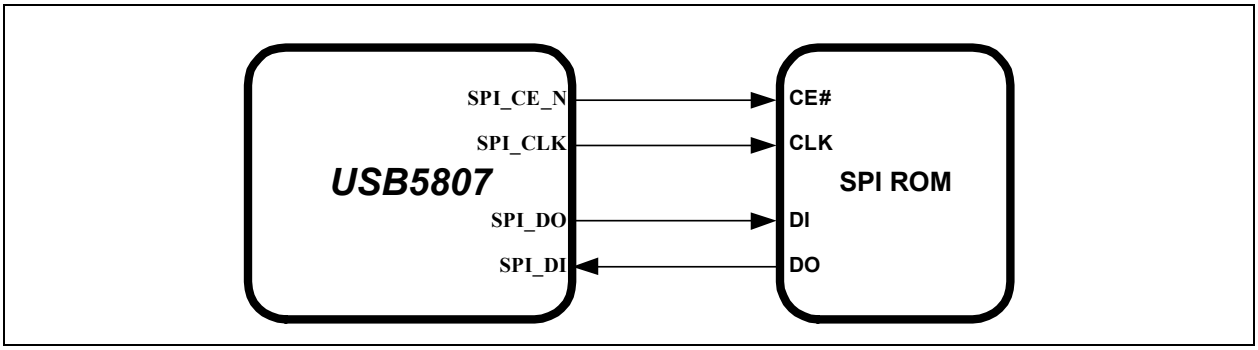
FIGURE 4-1: DEVICE POWER CONNECTIONS



4.2 SPI ROM Connections

Figure 4-2 illustrates the device SPI ROM connections. Refer to **Section 7.1 "SPI Master Interface"** for additional information on this device interface.

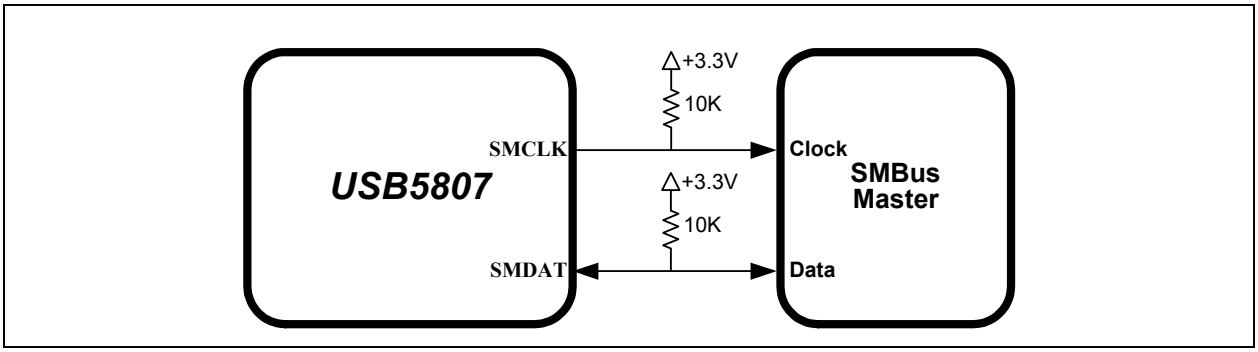
FIGURE 4-2: SPI ROM CONNECTIONS



4.3 SMBus Slave Connections

Figure 4-3 illustrates the device SMBus slave connections. Refer to **Section 7.2 "SMBus Slave Interface"** for additional information on this device interface.

FIGURE 4-3: SMBUS SLAVE CONNECTIONS



5.0 MODES OF OPERATION

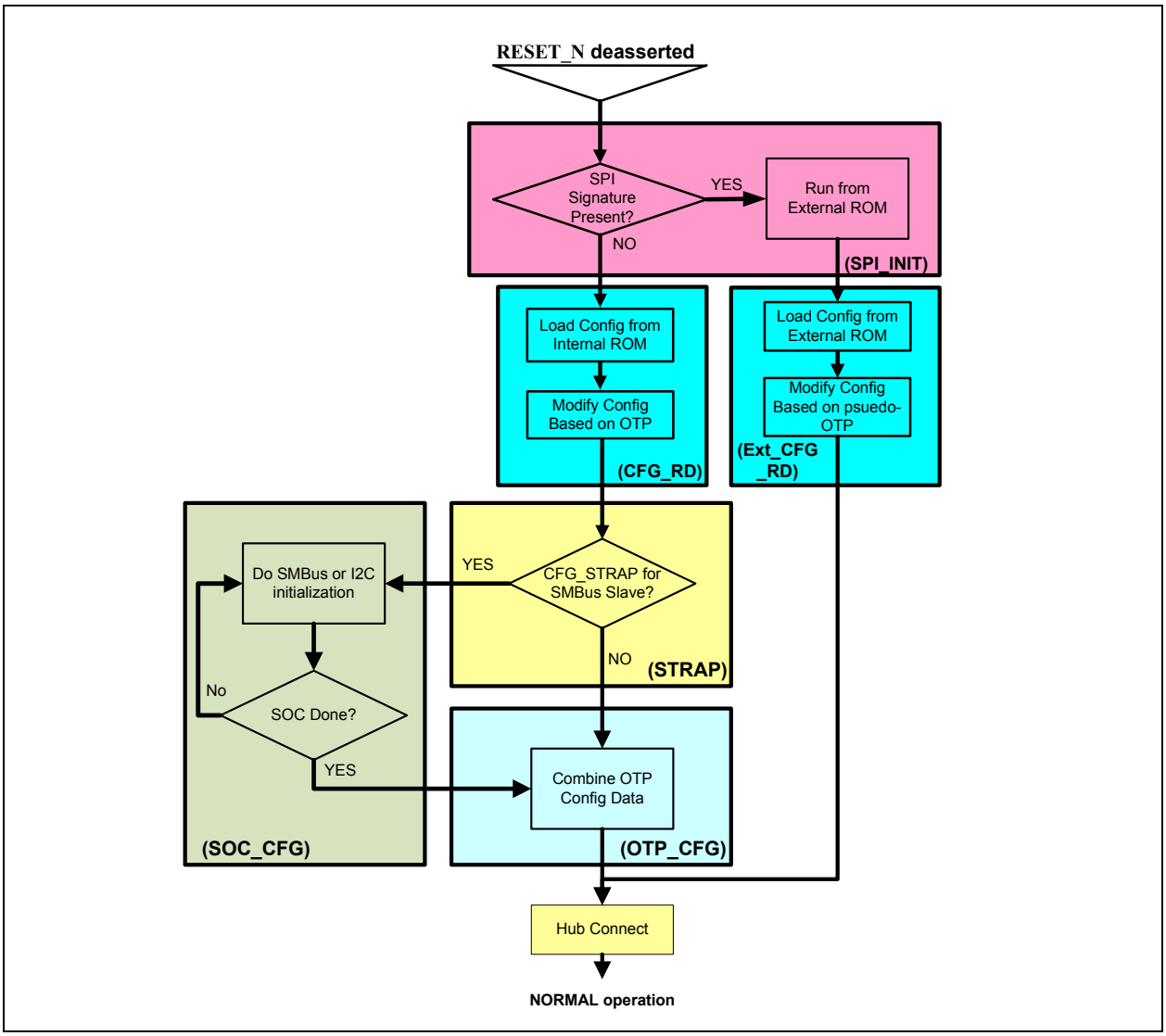
The device provides two main modes of operation: Standby Mode and Hub Mode. These modes are controlled via the RESET_N pin, as shown in Table 5-1.

TABLE 5-1: MODES OF OPERATION

RESET_N Input	Summary
0	**Standby Mode**: This is the lowest power mode of the device. No functions are active other than monitoring the RESET_N input. All port interfaces are high impedance and the PLL is halted. Refer to Section 8.4.2, External Chip Reset (RESET_N) for additional information on RESET_N.
1	**Hub (Normal) Mode**: The device operates as a configurable USB hub with battery charger detection. This mode has various sub-modes of operation, as detailed in Figure 5-1. Power consumption is based on the number of active ports, their speed, and amount of data transferred.

The flowchart in Figure 5-1 details the modes of operation and how the device traverses through the Hub Mode stages (shown in bold). The remaining sub-sections provide more detail on each stage of operation.

FIGURE 5-1: HUB BOOT FLOWCHART



5.1 Standby Mode

If the **RESET_N** pin is asserted, the hub will be in Standby Mode. This mode provides a very low power state for maximum power efficiency when no signaling is required. This is the lowest power state. In Standby Mode all downstream ports are disabled, the USB data pins are held in a high-impedance state, all transactions immediately terminate (no states saved), all internal registers return to their default state, the PLL is halted, and core logic is powered down in order to minimize power consumption. Because core logic is powered off, no configuration settings are retained in this mode and must be re-initialized after **RESET_N** is negated high.

5.2 SPI Initialization Stage (SPI_INIT)

The first stage, the initialization stage, occurs on the deassertion of **RESET_N**. In this stage, the internal logic is reset, the PLL locks if a valid clock is supplied, and the configuration registers are initialized to their default state. The internal firmware then checks for an external SPI ROM. The firmware looks for an external SPI flash device that contains a valid signature of “2DFU” (device firmware upgrade) beginning at address 0xFFFA. If a valid signature is found, then the external ROM is enabled and the code execution begins at address 0x0000 in the external SPI device. If a valid signature is not found, then execution continues from internal ROM (CFG_RD stage).

When using an external SPI ROM, a 1 Mbit, 60 MHz or faster ROM must be used. Both 1- and 2-bit SPI operation are supported. For optimum throughput, a 2-bit SPI ROM is recommended. Both mode 0 and mode 3 SPI ROMs are also supported.

If the system is not strapped for SPI Mode, code execution will continue from internal ROM (CFG_RD stage).

5.3 Configuration Read Stage (CFG_RD)

In this stage, the internal firmware loads the default values from the internal ROM and then uses the configuration strapping options to override the default values. Refer to Section 3.5, Configuration Straps and Programmable Functions for information on usage of the various device configuration straps.

5.4 Strap Read Stage (STRAP)

In this stage, the firmware registers the configuration strap settings and checks the state of **CFG_STRAP**. If **CFG_STRAP** is set for CONFIG2, then the hub will check the state of the **SMBDATA** and **SMBCLK** pins. If 10k pull-up resistors are detected on both pins, the device will enter the SOC_CFG stage. If 10k pull-up resistors are not detected on both pins, the hub will transition to the OTP_CFG stage instead.

5.5 SOC Configuration Stage (SOC_CFG)

In this stage, the SOC can modify any of the default configuration settings specified in the integrated ROM, such as USB device descriptors and port electrical settings.

There is no time limit on this mode. In this stage the firmware will wait indefinitely for the SMBus/I^2C configuration. When the SOC has completed configuring the device, it must write to register 0xFF to end the configuration.

5.6 OTP Configuration Stage (OTP_CFG)

Once the SOC has indicated that it is done with configuration, all configuration data is combined in this stage. The default data, the SOC configuration data, and the OTP data are all combined in the firmware and the device is programmed.

After the device is fully configured, it will go idle and then into suspend if there is no VBUS or Hub.Connect present. Once VBUS is present, and battery charging is enabled, the device will transition to the Battery Charger Detection Stage. If VBUS is present, and battery charging is not enabled, the device will transition to the Connect stage.

5.7 Hub Connect Stage (Hub.Connect)

Once the CHGDET stage is completed, the device enters the Hub Connect stage. USB connect can be initiated by asserting the VBUS pin function high. The device will remain in the Hub Connect stage indefinitely until the VBUS pin function is deasserted.

5.8 Normal Mode

Lastly, the hub enters Normal Mode of operation. In this stage full USB operation is supported under control of the USB Host on the upstream port. The device will remain in the normal mode until the operating mode is changed by the system.