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6-Port USB 3.1 Gen 1 Smart Hub with Support for Multiple USB Type-C™ UFP and DFP

Highlights

- USB Hub Feature Controller Hub with:
 - 2 USB 3.1 Gen 1 USB Type-C™ downstream ports
 - 2 USB 3.1 Gen 1 legacy downstream ports
 - 2 USB 2.0 legacy downstream ports
 - USB Type-C upstream port
- USB-IF Battery Charger revision 1.2 support on up & downstream ports (DCP, CDP, SDP)
- **FlexConnect**: Downstream port able to swap with upstream port, allowing master capable devices to control other devices on the hub
- Internal Hub Feature Controller device enables:
 - USB to I²C/SPI/GPIO bridge endpoint support
 - USB to internal hub register write and read
- USB Link Power Management (LPM) support
- Enhanced OEM configuration options available through either OTP or SPI ROM
- Available in 100-pin (12mm x 12mm) VQFN RoHS compliant package
- Commercial and industrial grade temperature support

Target Applications

- Standalone USB Hubs
- Laptop Docks
- PC Motherboards
- PC Monitor Docks
- Multi-function USB 3.1 Gen 1 Peripherals

Key Benefits

- USB 3.1 Gen 1 compliant 5 Gbps, 480 Mbps, 12 Mbps, and 1.5Mbps operation
 - 5V tolerant USB 2.0 pins
 - 1.32V tolerant USB 3.1 Gen 1 pins
 - Integrated termination and pull-up/down resistors
- Native USB Type-C Support
 - Integrated Multiplexer on USB Type-C enabled ports
 - USB 3.1 Gen 1 PHYs are disabled until a valid USB Type-C attach is detected, saving idle power

- Supports battery charging of most popular battery powered devices on all ports
 - USB-IF Battery Charging rev. 1.2 support (DCP, CDP, SDP)
 - Apple® portable product charger emulation
 - Chinese YD/T 1591-2006 charger emulation
 - Chinese YD/T 1591-2009 charger emulation
 - European Union universal mobile charger support
 - Support for Microchip UCS100x family of battery charging controllers
 - Supports additional portable devices
- Smart port controller operation
 - Firmware handling of companion port power controllers
- On-chip microcontroller
 - manages I/Os, VBUS, and other signals
- 8 KB RAM, 64 KB ROM
- 8 KB One-Time-Programmable (OTP) ROM
 - Includes on-chip charge pump
- Configuration programming via OTP ROM, SPI ROM, or SMBus
- **FlexConnect**
 - Reversible upstream and downstream Port 1 roles on command
- **PortSwap**
 - Configurable USB 2.0 differential pair signal swap
- **PHYBoost™**
 - Programmable USB transceiver drive strength for recovering signal integrity
- **VariSense™**
 - Programmable USB receive sensitivity
- **Port Split**
 - USB2.0 and USB3.1 Gen1 port operation can be split for custom applications using embedded USB3.x devices in parallel with USB2.0 devices.
- USB Power Delivery Billboard Device Support
 - Internal port can enumerate as a Power Delivery Billboard device to communicate Power Delivery Alternate Mode negotiation failure cases to USB host
- Compatible with Microsoft Windows 10, 8, 7, XP, Apple OS X 10.4+, and Linux hub drivers
- Optimized for low-power operation and low thermal dissipation
- Package
 - 100-pin VQFN (12mm x 12mm)

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1.0 PREFACE

1.1 General Terms

TABLE 1-1: GENERAL TERMS

Term	Description
ADC	Analog-to-Digital Converter
Byte	8 bits
CDC	Communication Device Class
CSR	Control and Status Registers
DWORD	32 bits
EOP	End of Packet
EP	Endpoint
FIFO	First In First Out buffer
FS	Full-Speed
FSM	Finite State Machine
GPIO	General Purpose I/O
HS	Hi-Speed
HSOS	High Speed Over Sampling
Hub Feature Controller	The Hub Feature Controller, sometimes called a Hub Controller for short is the internal processor used to enable the unique features of the USB Controller Hub. This is not to be confused with the USB Hub Controller that is used to communicate the hub status back to the Host during a USB session.
I²C	Inter-Integrated Circuit
LS	Low-Speed
lsb	Least Significant Bit
LSB	Least Significant Byte
msb	Most Significant Bit
MSB	Most Significant Byte
N/A	Not Applicable
NC	No Connect
OTP	One Time Programmable
PCB	Printed Circuit Board
PCS	Physical Coding Sublayer
PHY	Physical Layer
PLL	Phase Lock Loop
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
SDK	Software Development Kit
SMBus	System Management Bus
UUID	Universally Unique Identifier
WORD	16 bits

1.2 Reference Documents

1. *UNICODE UTF-16LE For String Descriptors* USB Engineering Change Notice, December 29th, 2004, <http://www.usb.org>
2. *Universal Serial Bus Revision 3.1 Specification*, <http://www.usb.org>
3. *Battery Charging Specification*, Revision 1.2, Dec. 07, 2010, <http://www.usb.org>
4. *I²C-Bus Specification*, Version 1.1, <http://www.nxp.com>
5. *System Management Bus Specification*, Version 1.0, <http://smbus.org/specs>

2.0 INTRODUCTION

2.1 General Description

The Microchip USB5926 hub is a low-power, OEM configurable, USB 3.1 Gen 1 hub controller with 6 downstream ports and advanced features for embedded USB applications. The USB5926 is fully compliant with the Universal Serial Bus Revision 3.1 Specification and USB 2.0 Link Power Management Addendum. The USB5926 supports 5 Gbps Super-Speed (SS), 480 Mbps Hi-Speed (HS), 12 Mbps Full-Speed (FS), and 1.5 Mbps Low-Speed (LS) USB downstream devices on all enabled downstream ports.

The USB5926 supports the legacy USB speeds (HS/FS/LS) through a dedicated USB 2.0 hub controller that is the culmination of five generations of Microchip hub controller design and experience with proven reliability, interoperability, and device compatibility. The SuperSpeed hub controller operates in parallel with the USB 2.0 hub controller, decoupling the 5 Gbps SS data transfers from bottlenecks due to the slower USB 2.0 traffic.

The USB5926 hub feature controller enables OEMs to configure their system using “Configuration Straps.” These straps simplify the configuration process, assigning default values to USB 3.1 Gen 1 ports and GPIOs. OEMs can disable ports, enable battery charging, and define GPIO functions as default assignments on power-up, removing the need for OTP or external SPI ROM.

The USB5926 supports downstream battery charging via the integrated battery charger detection circuitry, which supports the USB-IF Battery Charging (BC1.2) detection method and most Apple devices. The USB5926 provides the battery charging handshake and supports the following USB-IF BC1.2 charging profiles:

- DCP: Dedicated Charging Port (Power brick with no data)
- CDP: Charging Downstream Port (1.5A with data)
- SDP: Standard Downstream Port (0.5A with data)
- Custom profiles loaded via SMBus or OTP

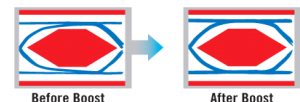
Additionally, the USB5926 includes many powerful and unique features such as:

The Hub Feature Controller, which provides an internal USB device dedicated for use as a USB to I²C/UART/SPI/GPIO interface, allowing external circuits or devices to be monitored, controlled, or configured via the USB interface.

FlexConnect, which provides flexible connectivity options. One of the USB5926’s downstream ports can be reconfigured to become the upstream port, allowing master capable devices to control other devices on the hub.

PortSwap, which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.

PHYBoost, which provides programmable levels of Hi-Speed USB signal drive strength in the downstream port transceivers. PHYBoost attempts to restore USB signal integrity in a compromised system environment. The graphic on the right shows an example of Hi-Speed USB eye diagrams before and after PHYBoost signal integrity restoration. in a compromised system environment.



VariSense, which controls the USB receiver sensitivity enabling programmable levels of USB signal receive sensitivity. This capability allows operation in a sub-optimal system environment, such as when a captive USB cable is used.

Port Split, which allows for the USB3.1 Gen1 and USB2.0 portions of downstream ports 3 and 4 to operate independently and enumerate two separate devices in parallel in special applications.

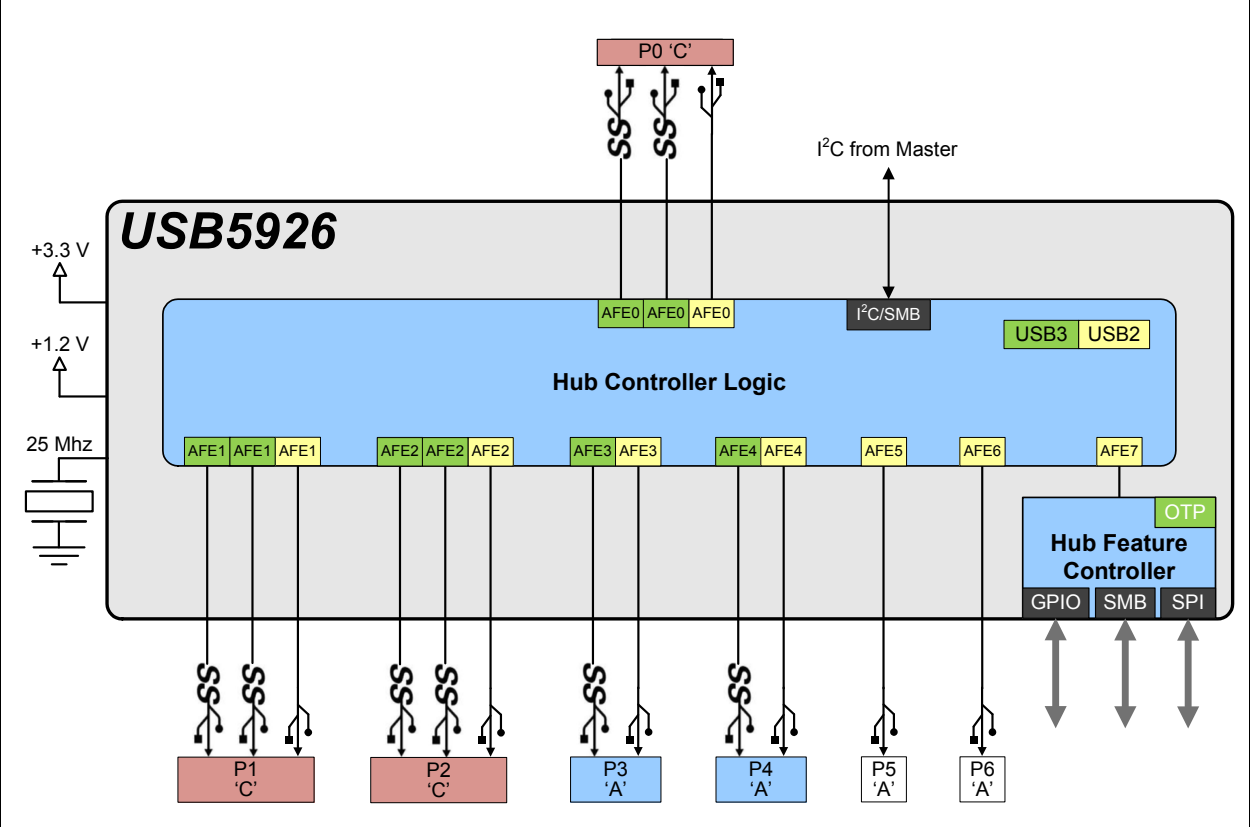
USB Power Delivery Billboard Device, which allows an internal device to enumerate as a Billboard class device when a Power Delivery Alternate Mode negotiation has failed. The Billboard device will enumerate temporarily to the host PC when a failure occurs, as indicated by a digital signal from an external Power Delivery controller.

The USB5926 can be configured for operation through internal default settings. Custom OEM configurations are supported through external SPI ROM or OTP ROM. All port control signal pins are under firmware control in order to allow for maximum operational flexibility, and are available as GPIOs for customer specific use.

The USB5926 is available in commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature ranges. An internal block diagram of the USB5926 is shown in [Figure 2-1](#).

USB5926

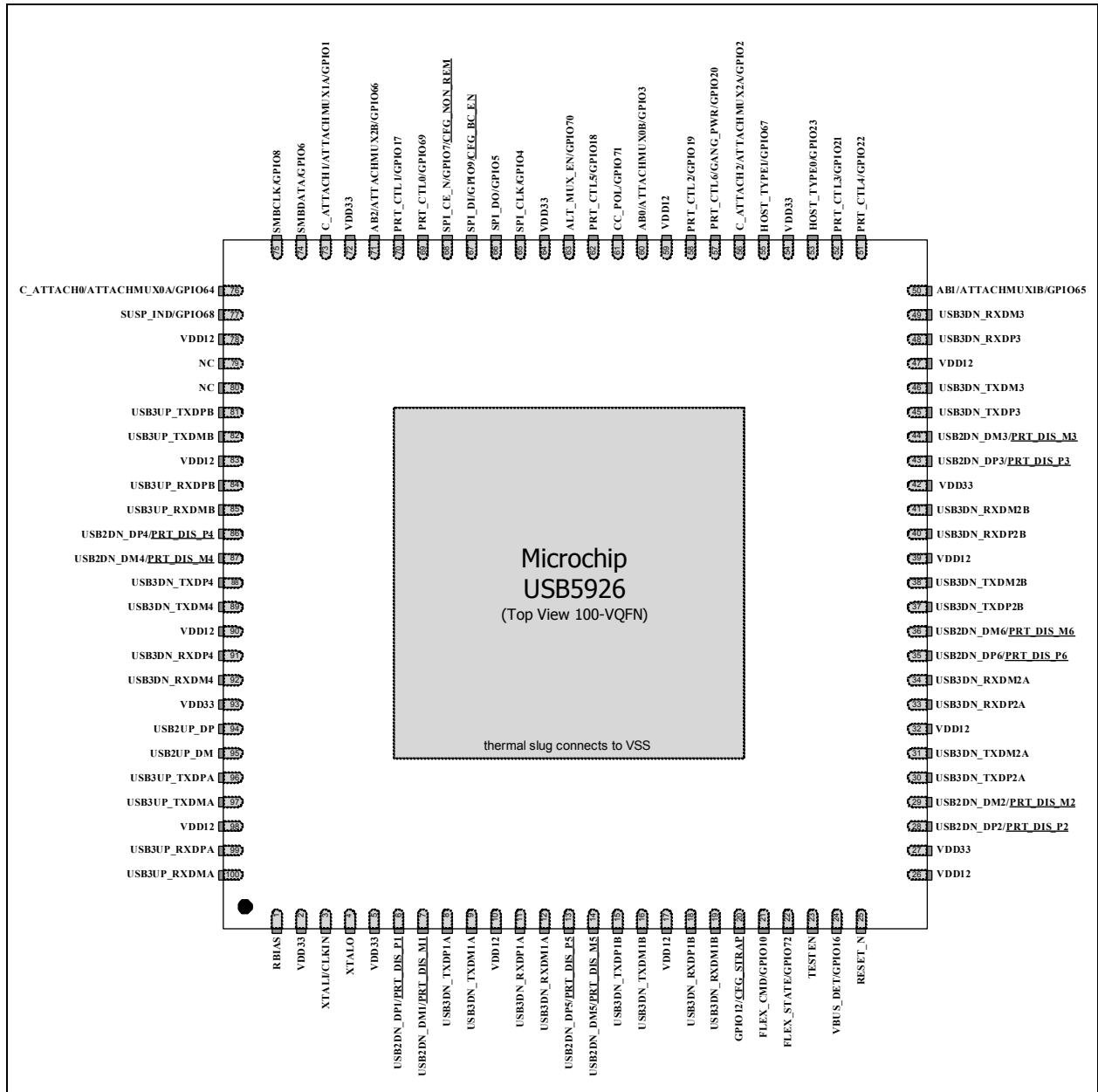
FIGURE 2-1: INTERNAL BLOCK DIAGRAM



3.0 PIN DESCRIPTIONS

3.1 Pin Diagram

FIGURE 3-1: PIN ASSIGNMENTS (TOP VIEW)



Note 1: Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to [Section 3.5, Configuration Straps and Programmable Functions](#)

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3.2 Pin Symbols

Pin Num.	Pin Name	Reset	Pin Num.	Pin Name	Reset
1	RBIAS	A/P	51	PRT_CTL4/GPIO22	PD-50k
2	VDD33	A/P	52	PRT_CTL3/GPIO21	PD-50k
3	XTALI/CLKIN	A/P	53	HOST_TYPE0/GPIO23	PD-50k
4	XTALO	A/P	54	VDD33	A/P
5	VDD33	A/P	55	HOST_TYPE1/GPIO67	Z
6	USB2DN_DP1/PRT_DIS_P1	PD-15k	56	C_ATTACH2/ATTACHMUX2A/GPIO2	Z
7	USB2DN_DM1/PRT_DIS_M1	PD-15k	57	PRT_CTL6/GANG_PWR/GPIO20	PD-50k
8	USB3DN_TXDP1A	Z	58	PRT_CTL2/GPIO19	PD-50k
9	USB3DN_TXDM1A	Z	59	VDD12	A/P
10	VDD12	A/P	60	AB0/ATTACHMUX0B/GPIO3	Z
11	USB3DN_RXDP1A	Z	61	CC_POL/GPIO71	Z
12	USB3DN_RXDM1A	Z	62	PRT_CTL5/GPIO18	PD-50k
13	USB2DN_DP5/PRT_DIS_P5	PD-15k	63	ALT_MUX_EN/GPIO70	Z
14	USB2DN_DM5/PRT_DIS_M5	PD-15k	64	VDD33	A/P
15	USB3DN_TXDP1B	Z	65	SPI_CLK/GPIO4	Z
16	USB3DN_TXDM1B	Z	66	SPI_DO/GPIO5	PD-50k
17	VDD12	A/P	67	SPI_DI/GPIO9/CFG_BC_EN	Z
18	USB3DN_RXDP1B	Z	68	SPI_CE_N/GPIO7/CFG_NON_REM	PU-50k
19	USB3DN_RXDM1B	Z	69	PRT_CTL0/GPIO69	Z
20	GPIO12/CFG_STRAP	Z	70	PRT_CTL1/GPIO17	PD-50k
21	FLEX_CMD/GPIO10	Z	71	AB2/ATTACHMUX2B/GPIO66	Z
22	FLEX_STATE/GPIO72	Z	72	VDD33	A/P
23	TESTEN	Z	73	C_ATTACH1/ATTACHMUX1A/GPIO1	Z
24	VBUS_DET/GPIO16	Z	74	SMBDATA/GPIO6	Z
25	RESET_N	R	75	SMBCLK/GPIO8	Z
26	VDD12	A/P	76	C_ATTACH0/ATTACHMUX0A/GPIO64	Z
27	VDD33	A/P	77	SUSP_IND/GPIO68	Z
28	USB2DN_DP2/PRT_DIS_P2	PD-15k	78	VDD12	A/P
29	USB2DN_DM2/PRT_DIS_M2	PD-15k	79	NC	PD-15k
30	USB3DN_TXDP2A	Z	80	NC	PD-15k
31	USB3DN_TXDM2A	Z	81	USB3UP_TXDPB	Z
32	VDD12	A/P	82	USB3UP_TXDMB	Z
33	USB3DN_RXDP2A	Z	83	VDD12	A/P
34	USB3DN_RXDM2A	Z	84	USB3UP_RXDPB	Z
35	USB2DN_DP6/PRT_DIS_P6	PD-15k	85	USB3UP_RXDMB	Z
36	USB2DN_DM6/PRT_DIS_M6	PD-15k	86	USB2DN_DP4/PRT_DIS_P4	PD-15k
37	USB3DN_TXDP2B	Z	87	USB2DN_DM4/PRT_DIS_M4	PD-15k
38	USB3DN_TXDM2B	Z	88	USB3DN_TXDP4	Z
39	VDD12	A/P	89	USB3DN_TXDM4	Z
40	USB3DN_RXDP2B	Z	90	VDD12	A/P
41	USB3DN_RXDM2B	Z	91	USB3DN_RXDP4	Z
42	VDD33	A/P	92	USB3DN_RXDM4	Z
43	USB2DN_DP3/PRT_DIS_P3	PD-15k	93	VDD33	A/P
44	USB2DN_DM3/PRT_DIS_M3	PD-15k	94	USB2UP_DP	PD-1M
45	USB3DN_TXDP3	Z	95	USB2UP_DM	PD-1M
46	USB3DN_TXDM3	Z	96	USB3UP_TXDPA	Z
47	VDD12	A/P	97	USB3UP_TXDMA	Z
48	USB3DN_RXDP3	Z	98	VDD12	A/P
49	USB3DN_RXDM3	Z	99	USB3UP_RXDPA	Z
50	AB1/ATTACHMUX1B/GPIO65	Z	100	USB3UP_RXDMA	Z

The pin reset state definitions are detailed in [Table 3-1](#).

TABLE 3-1: PIN RESET STATE LEGEND

Symbol	Description
A/P	Analog/Power Input
R	Reset Control Input
Z	Hardware disables output driver (high impedance)
PU-50k	Hardware enables internal 50kΩ pull-up
PD-50k	Hardware enables internal 50kΩ pull-down
PD-15k	Hardware enables internal 15kΩ pull-down
PD-1M	Hardware enables internal 1M pull-down

3.3 USB5926 Pin Descriptions

This section contains descriptions of the various USB5926 pins. The pin descriptions have been broken into functional groups as follows:

- [USB 3.1 Gen 1 Pin Descriptions](#)
- [USB 2.0 Pin Descriptions](#)
- [Port Control Pin Descriptions](#)
- [SPI Interface](#)
- [USB Type-C Connector Controls](#)
- [Miscellaneous Pin Descriptions](#)
- [Configuration Strap Pin Descriptions](#)
- [Power and Ground Pin Descriptions](#)

The “_N” symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, **RESET_N** indicates that the reset signal is active low. When “_N” is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signal. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

TABLE 3-2: USB 3.1 GEN 1 PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
USB 3.1 Gen 1 Upstream A D+ TX	USB3UP_TXDPA	I/O-U	Upstream USB Type-C “Orientation A” USB 3.1 Gen 1 Transmit Data Plus
USB 3.1 Gen 1 Upstream A D- TX	USB3UP_TXDMA	I/O-U	Upstream USB Type-C “Orientation A” USB 3.1 Gen 1 Transmit Data Minus
USB 3.1 Gen 1 Upstream A D+ RX	USB3UP_RXDPA	I/O-U	Upstream USB Type-C “Orientation A” USB 3.1 Gen 1 Receive Data Plus

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TABLE 3-2: USB 3.1 GEN 1 PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
USB 3.1 Gen 1 Upstream A D- RX	USB3UP_RXDMA	I/O-U	Upstream USB Type-C “Orientation A” USB 3.1 Gen 1 Receive Data Minus
USB 3.1 Gen 1 Upstream B D+ TX	USB3UP_TXDPB	I/O-U	Upstream USB Type-C “Orientation B” USB 3.1 Gen 1 Transmit Data Plus
USB 3.1 Gen 1 Upstream B D- TX	USB3UP_TXDMB	I/O-U	Upstream USB Type-C “Orientation B” USB 3.1 Gen 1 Transmit Data Minus
USB 3.1 Gen 1 Upstream B D+ RX	USB3UP_RXDPB	I/O-U	Upstream USB Type-C “Orientation B” USB 3.1 Gen 1 Receive Data Plus
USB 3.1 Gen 1 Upstream B D- RX	USB3UP_RXDMB	I/O-U	Upstream USB Type-C “Orientation B” USB 3.1 Gen 1 Receive Data Minus
USB 3.1 Gen 1 Ports 4-3 D+ TX	USB3DN_TXDP[4:3]	I/O-U	Downstream Super Speed Transmit Data Plus, ports 4 through 3.
USB 3.1 Gen 1 Ports 4-3 D- TX	USB3DN_TXDM[4:3]	I/O-U	Downstream Super Speed Transmit Data Minus, ports 4 through 3.
USB 3.1 Gen 1 Ports 4-3 D+ RX	USB3DN_RXDP[4:3]	I/O-U	Downstream Super Speed Receive Data Plus, ports 4 through 3.
USB 3.1 Gen 1 Ports 4-3 D- RX	USB3DN_RXDM[4:3]	I/O-U	Downstream Super Speed Receive Data Minus, ports 4 through 3.
USB 3.1 Gen 1 Ports 2-1 A D+ TX	USB3DN_TXDP[2:1]A	I/O-U	Downstream USB Type-C “Orientation A” Super Speed Transmit Data Plus, ports 2 through 1.
USB 3.1 Gen 1 Ports 2-1 A D- TX	USB3DN_TXDM[2:1]A	I/O-U	Downstream USB Type-C “Orientation A” Super Speed Transmit Data Minus, ports 2 through 1.
USB 3.1 Gen 1 Ports 2-1 A D+ RX	USB3DN_RXDP[2:1]A	I/O-U	Downstream USB Type-C “Orientation A” Super Speed Receive Data Plus, ports 2 through 1.
USB 3.1 Gen 1 Ports 2-1 A D- RX	USB3DN_RXDM[2:1]A	I/O-U	Downstream USB Type-C “Orientation A” Super Speed Receive Data Minus, ports 2 through 1.
USB 3.1 Gen 1 Ports 2-1 B D+ TX	USB3DN_TXDP[2:1]B	I/O-U	Downstream USB Type-C “Orientation B” Super Speed Transmit Data Plus, ports 2 through 1.

TABLE 3-2: USB 3.1 GEN 1 PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
USB 3.1 Gen 1 Ports 2-1 B D- TX	USB3DN_TXDM[2:1]B	I/O-U	Downstream USB Type-C “Orientation B” Super Speed Transmit Data Minus, ports 2 through 1.
USB 3.1 Gen 1 Ports 2-1 B D+ RX	USB3DN_RXDP[2:1]B	I/O-U	Downstream USB Type-C “Orientation B” Super Speed Receive Data Plus, ports 2 through 1.
USB 3.1 Gen 1 Ports 2-1 B D- RX	USB3DN_RXDM[2:1]B	I/O-U	Downstream USB Type-C “Orientation B” Super Speed Receive Data Minus, ports 2 through 1.

TABLE 3-3: USB 2.0 PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
USB 2.0 Upstream D+	USB2UP_DP	I/O-U	Upstream USB 2.0 Data Plus (D+)
USB 2.0 Upstream D-	USB2UP_DM	I/O-U	Upstream USB 2.0 Data Minus (D-)
USB 2.0 Ports 6 D+	USB2DN_DP[6:1]	I/O-U	Downstream USB 2.0 Ports 6-1 Data Plus (D+)
USB 2.0 Ports 6 D-	USB2DN_DM[6:1]	I/O-U	Downstream USB 2.0 Ports 6-1 Data Minus (D-)
VBUS Detect	VBUS_DET	IS	<p>This signal detects the state of the upstream bus power.</p> <p>When designing a detachable hub, this pin must be connected to the VBUS power pin of the upstream USB port through a resistor divider (50 kΩ by 100 kΩ) to provide 3.3 V.</p> <p>For self-powered applications with a permanently attached host, this pin must be connected to either 3.3 V or 5.0 V through a resistor divider to provide 3.3 V.</p> <p>In embedded applications, VBUS_DET may be controlled (toggled) when the host desires to renegotiate a connection without requiring a full reset of the device.</p>

TABLE 3-4: PORT CONTROL PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
Port 6 Power Enable / Overcurrent Sense	PRT_CTL6	I/OD12 (PU)	<p>Port 6 Power Enable / Overcurrent Sense.</p> <p>When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 6.</p> <p>This pin will change to an output and be driven low when the port is disabled by configuration or by the host control.</p>
Port 5 Power Enable / Overcurrent Sense	PRT_CTL5	I/OD12 (PU)	<p>Port 5 Power Enable / Overcurrent Sense.</p> <p>When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 5.</p> <p>This pin will change to an output and be driven low when the port is disabled by configuration or by the host control.</p>
Port 4 Power Enable / Overcurrent Sense	PRT_CTL4	I/OD12 (PU)	<p>Port 4 Power Enable / Overcurrent Sense.</p> <p>When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 4.</p> <p>This pin will change to an output and be driven low when the port is disabled by configuration or by the host control.</p>
Port 3 Power Enable / Overcurrent Sense	PRT_CTL3	I/OD12 (PU)	<p>Port 3 Power Enable / Overcurrent Sense.</p> <p>When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 3.</p> <p>This pin will change to an output and be driven low when the port is disabled by configuration or by the host control.</p>

TABLE 3-4: PORT CONTROL PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Port 2 Power Enable / Overcurrent Sense	PRT_CTL2	I/OD12 (PU)	<p>Port 2 Power Enable / Overcurrent Sense.</p> <p>When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 2.</p> <p>This pin will change to an output and be driven low when the port is disabled by configuration or by the host control.</p>
Port 1 Power Enable / Overcurrent Sense	PRT_CTL1	I/OD12 (PU)	<p>Port 1 Power Enable / Overcurrent Sense.</p> <p>When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 1.</p> <p>This pin will change to an output and be driven low when the port is disabled by configuration or by the host control.</p>
Port 0 Power Enable / Overcurrent Sense	PRT_CTL0	I/OD12 (PU)	<p>Port 0 Power Enable / Overcurrent Sense.</p> <p>When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 0.</p> <p>This pin will change to an output and be driven low when the port is disabled by configuration or by the host control.</p> <p>Note: This pin is only used to control port power when FlexConnect is enabled, and Port 0 has exchanged roles with downstream Port 1.</p>
Gang Power	GANG_PWR	I	<p>GANG_PWR becomes the port control (PRTCTL) pin for all downstream ports when the hub is configured for ganged port power control mode. All port power controllers should be controlled from this pin when the hub is configured for ganged port power mode.</p>
FlexConnect Control	FLEX_CMD	I	<p>FlexConnect control input.</p> <p>When low, the hub will operate in its default state. Port 0 is the upstream port and port 1 is a downstream port.</p> <p>When high, the hub will operate in its flexed state. Port 0 is a downstream port and port 1 is an upstream port.</p>

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TABLE 3-4: PORT CONTROL PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
FlexConnect Indicator	FLEX_STATE	O12	FlexConnect indicator output. Reflects the current state of FlexConnect. 0 = Hub is in default mode of operation 1 = Hub is in flexed mode of operation.

TABLE 3-5: SPI INTERFACE

Name	Symbol	Buffer Type	Description
SPI Chip Enable	SPI_CE_N	I/O12	This is the active low SPI chip enable output. If the SPI interface is enabled, this pin must be driven high in power-down states.
SPI Clock	SPI_CLK	I/O-U	This is the SPI clock out to the serial ROM. If the SPI interface is disabled, by setting the SPI_DIS-ABLE bit in the UTIL_CONFIG1 register, this pin becomes GPIO4 . If the SPI interface is enabled this pin must be driven low during reset.
SPI Data Output	SPI_DO	I/O-U	SPI data output, when configured for SPI operation.
SPI Data Input	SPI_DI	I/O-U	SPI data input, when configured for SPI operation.

TABLE 3-6: USB TYPE-C CONNECTOR CONTROLS

Name	Symbol	Buffer Type	Description
USB Type-C Attach Control Input 0-2	C_ATTACH[0:2]	I	<p>“Type-C Control Mode 1” USB Type-C attach control input.</p> <p>This pin indicates to the hub when a valid USB Type-C attach has been detected. This pin is used by the hub to enable the USB 3.1 Gen 1 PHY when a Type-C connection is present. When there is no USB Type-C connection present, the USB 3.1 Gen 1 PHY is disabled to reduce power consumption.</p> <p>The polarity of this input is controlled via the CC_POL pin. If CC_POL is low, this pin behaves as follows:</p> <ul style="list-style-type: none"> - 1: USB Type-C attach detected, turn respective USB 3.1 Gen 1 PHY on. - 0: No USB Type-C attach detected, turn respective USB 3.1 Gen 1 PHY off. <p>If CC_POL is high, this pin behaves as follows:</p> <ul style="list-style-type: none"> - 1: No USB Type-C attach detected, turn respective USB3.1 Gen 1 PHY off. - 0: USB Type-C attach detected, turn respective USB3.1 Gen 1 PHY on. <p>When using legacy USB Type-A and Type-B connectors, pull these pins to 3.3V to permanently enable all USB 3.1 PHYs.</p>
USB Type-C Orientation Control Input 0-2	AB[0:2]	I	<p>“Type-C Control Mode 1” USB Type-C orientation control input.</p> <p>This pin signals to the hub the orientation of the USB Type-C connector. The hub enables the appropriate USB 3.1 Gen 1 PHY based upon the polarity of this signal, and the assertion of the associated C_ATTACH[0:2] pin.</p> <p>The polarity of this input is controlled via the CC_POL pin. If CC_POL is low, this pin behaves as follows:</p> <ul style="list-style-type: none"> - 1: Enable USB 3.1 Gen 1 PHY A. - 0: Enable USB 3.1 Gen 1 PHY B. <p>If CC_POL is high, this pin behaves as follows:</p> <ul style="list-style-type: none"> - 1: Enable USB 3.1 Gen 1 PHY B. - 0: Enable USB 3.1 Gen 1 PHY A.

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TABLE 3-6: USB TYPE-C CONNECTOR CONTROLS (CONTINUED)

Name	Symbol	Buffer Type	Description
USB Type-C Alternative Orientation A Attach 0-2	ATTACH_MUX[0:2]A	I	<p>“Type-C Control Mode 2” Alternative USB Type-C attach for “Orientation A” USB Type-C connections.</p> <p>This mode of control is an alternative to the C_ATTACH[0:2] and AB[0:2] pins. To select this mode, the ALT_MUX_EN pin must be high.</p> <p>When this pin asserted, the hub enables the “Orientation A” USB 3.1 Gen 1 PHY of the associated port. When there is no USB Type-C connection present and this pin is not asserted, the associated USB 3.1 Gen 1 PHY is disabled to reduce power consumption.</p> <p>The polarity of this input is controlled via the CC_POL pin.</p> <p>If CC_POL is low, this pin behaves as follows:</p> <ul style="list-style-type: none"> - 1: USB Type-C attach detected, turn respective “Orientation A” USB 3.1 Gen 1 PHY on. - 0: No USB Type-C attach detected, turn respective “Orientation A” USB 3.1 Gen 1 PHY off. <p>If CC_POL is high, this pin behaves as follows:</p> <ul style="list-style-type: none"> - 1: No USB Type-C attach detected, turn respective “Orientation A” USB 3.1 Gen 1 PHY off. - 0: USB Type-C attach detected, turn respective “Orientation A” USB 3.1 Gen 1 PHY on.

TABLE 3-6: USB TYPE-C CONNECTOR CONTROLS (CONTINUED)

Name	Symbol	Buffer Type	Description
USB Type-C Alternative Orientation B Attach 0-2	ATTACH_MUX[0:2]B	I	<p>“Type-C Control Mode 2” USB Type-C attach for “Orientation B” USB Type-C connections.</p> <p>This mode of control is an alternative to the C_ATTACH[0:2] and AB[0:2] pins. To select this mode, the ALT_MUX_EN pin must be high.</p> <p>When this pin asserted, the hub enables the “Orientation B” USB 3.1 Gen 1 PHY of the associated port. When there is no USB Type-C connection present and this pin is not asserted, the associated USB 3.1 Gen 1 PHY is disabled to reduce power consumption.</p> <p>The polarity of this input is controlled via the CC_POL pin.</p> <p>If CC_POL is low, this pin behaves as follows:</p> <ul style="list-style-type: none"> - 1: USB Type-C attach detected, turn respective “Orientation B” USB 3.1 Gen 1 PHY on. - 0: No USB Type-C attach detected, turn respective “Orientation B” USB 3.1 Gen 1 PHY off. <p>If CC_POL is high, this pin behaves as follows:</p> <ul style="list-style-type: none"> - 1: No USB Type-C attach detected, turn respective “Orientation B” USB 3.1 Gen 1 PHY off. - 0: USB Type-C attach detected, turn respective “Orientation A” USB 3.1 Gen 1 PHY on.
Attach Polarity Control	CC_POL	I	<p>USB C_ATTACH polarity control input.</p> <p>If this pin is low, the C_ATTACH[0:2], AB[0:2], ATTACH_MUX[0:2]A, and ATTACH_MUX[0:2]B pins are active high.</p> <p>If this pin is high, the C_ATTACH[0:2], AB[0:2], ATTACH_MUX[0:2]A, and ATTACH_MUX[0:2]B pins are active low.</p> <p>This pin has an internal pull-down enabled. If the desired strapping is to pull this pin low, then this pin may be left unconnected.</p>

TABLE 3-6: USB TYPE-C CONNECTOR CONTROLS (CONTINUED)

Name	Symbol	Buffer Type	Description
USB Type-C Control Mode Selection	ALT_MUX_EN	I	<p>USB Type-C control mode selection.</p> <p>If this pin is low, the hub operates in “Type-C Control Mode 1”. In “Type-C Control Mode 1”, the C_ATTACH[0:2] and AB[0:2] pin functions are used.</p> <p>If this pin is high, the hub operates in “Type-C Control Mode 2”. In “Type-C Control Mode 2”, the ATTACH_MUX[0:2]A and ATTACH_MUX[0:2]B pin functions are used.</p> <p>This pin has an internal pull-down enabled. If the desired mode is “Type-C Control Mode 1”, then this pin may be left unconnected.</p>

TABLE 3-7: MISCELLANEOUS PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
SMBus/I ² C Clock	SMBCLK	I/O12	<p>SMBus/I²C Clock</p> <p>The SMBus/I²C interface acts as SMBus slave or I²C bridge dependent on the device configuration.</p> <p>For information on how to configure this interface refer to Section 3.5.1, CFG_STRAP Configuration.</p>
SMBus/I ² C Data	SMBDATA	I/O12	<p>SMBus/I²C Data</p> <p>The SMBus/I²C interface acts as SMBus slave or I²C bridge dependent on the device configuration.</p> <p>For information on how to configure this interface refer to Section 3.5.1, CFG_STRAP Configuration.</p>
USB Host Port 1-0 Speed Indicator	HOST_TYPE_[1:0]	O12	<p>USB Host Port Speed Indicator</p> <p>Tri-state: Not connected 0: USB 2.0 / USB 1.1 1: USB 3.1 Gen 1</p>
General Purpose I/O	GPIO[1:10], GPIO12, GPIO[16:23], GPIO[64:72]	I/O12 (PU/PD)	<p>General Purpose Inputs/Outputs</p> <p>Refer to Section 3.5.5, General Purpose input/Output Configuration (GPIOx) for details.</p>
USB 2.0 Suspend State Indicator	SUSP_IND	O12	<p>USB 2.0 Suspend State Indicator</p> <p>SUSP_IND can be used as a sideband remote wakeup signal for the host when in USB 2.0 suspend.</p>

TABLE 3-7: MISCELLANEOUS PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Reset Control Input	RESET_N	IS	Reset Control Input This pin places the hub into Reset Mode when pulled low.
Bias Resistor	RBIAS	I-R	A 12.0 k Ω (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings. Place the resistor as close to the device as possible with a dedicated, low impedance connection to the GND plane.
External 25 MHz Crystal Input	XTALI	ICLK	External 25 MHz crystal input
External 25 MHz Reference Clock Input	CLKIN	ICLK	External reference clock input. The device may alternatively be driven by a single-ended clock oscillator. When this method is used, XTALO should be left unconnected.
External 25 MHz Crystal Output	XTALO	OCLK	External 25 MHz crystal output
Test	TESTEN	I/O12	Test pin. This signal is used for test purposes and must always be connected to ground.
No Connect	NC	-	No connect. For proper operation, this signal must be left unconnected.

TABLE 3-8: CONFIGURATION STRAP PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
Device Mode Configuration Strap	<u>CFG_STRAP</u>	I	Device Mode Configuration Strap. This configuration strap is used to set the device mode. Refer to Section 3.5.1, CFG_STRAP Configuration for details. See Note 2
Port 6-1 D+ Disable Configuration Strap	<u>PRT_DIS_P[6:1]</u>	I	Port 6-1 D+ Disable Configuration Strap. These configuration straps are used in conjunction with the corresponding <u>PRT_DIS_M[6:1]</u> straps to disable the related port (6-1). Refer to Section 3.5.2, Port Disable Configuration (PRT_DIS_P[6:1] / PRT_DIS_M[6:1]) for more information. See Note 2
Port 6-1 D- Disable Configuration Strap	<u>PRT_DIS_M[6:1]</u>	I	Port 6-1 D- Disable Configuration Strap. These configuration straps are used in conjunction with the corresponding <u>PRT_DIS_P[6:1]</u> straps to disable the related port (6-1). Refer to Section 3.5.2, Port Disable Configuration (PRT_DIS_P[6:1] / PRT_DIS_M[6:1]) for more information. See Note 2
Non-Removable Ports Configuration Strap	<u>CFG_NON_REM</u>	I	Configuration strap to control number of reported non-removal ports. See Section 3.5.3, Non-Removable Port Configuration (CFG_NON_REM) See Note 2
Battery Charging Configuration Strap	<u>CFG_BC_EN</u>	I	Configuration strap to control number of BC 1.2 enabled downstream ports. See Section 3.5.4, Battery Charging Configuration (CFG_BC_EN) See Note 2

2: Configuration strap values are latched on Power-On Reset (POR) and the rising edge of **RESET_N** (external chip reset). Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. Refer to [Section 3.5, Configuration Straps and Programmable Functions](#) for additional information.

TABLE 3-9: POWER AND GROUND PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
+3.3V Power Supply Input	VDD33	P	+3.3 V power and internal regulator input Refer to Section 4.1, Power Connections for power connection information
+1.2V Core Power Supply Input	VDD12	P	+1.2 V core power Refer to Section 4.1, Power Connections for power connection information.
Ground	GND	P	Common ground. This exposed pad must be connected to the ground plane with a via array.

3.4 Buffer Type Descriptions

TABLE 3-10: USB5926 BUFFER TYPE DESCRIPTIONS

BUFFER	DESCRIPTION
I	Input.
IS	Input with Schmitt trigger.
O12	Output buffer with 12 mA sink and 12 mA source.
OD12	Open-drain output with 12 mA sink
PU	50 μ A (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50 μ A (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
I/O-U	Analog input/output defined in USB specification.
I-R	RBIAS.

Note: Refer to [Section 9.5, DC Specifications](#) for individual buffer DC electrical characteristics.

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3.5 Configuration Straps and Programmable Functions

Configuration straps are multi-function pins that are used during Power-On Reset (POR) or external chip reset (**RESET_N**) to determine the default configuration of a particular feature. The state of the signal is latched following deassertion of the reset. Configuration straps are identified by an underlined symbol name. This section details the various device configuration straps and associated programmable pin functions.

Note: The system designer must guarantee that configuration straps meet the timing requirements specified in [Section 9.6.2, Power-On and Configuration Strap Timing](#) and [Section 9.6.3, Reset and Configuration Strap Timing](#). If configuration straps are not at the correct voltage level prior to being latched, the device may capture incorrect strap values.

3.5.1 CFG_STRAP CONFIGURATION

The CFG_STRAP pin is used to place the hub into preset modes of operation. The resistor options are a 200 k Ω pull-down, 200 k Ω pull-up, 10 k Ω pull-down, 10 k Ω pull-up, and 10 Ω pull-down, as shown in [Table 3-11](#).

TABLE 3-11: CFG_STRAP RESISTOR ENCODING

<u>CFG_STRAP</u> Resistor Value	Config	Setting
200 k Ω Pull-Down	CONFIG1	I²C Bridging Mode The SMBus interface will operate in Master Mode for use with USB to I ² C bridging function. For more information on USB to I ² C bridging with the USB5806, refer to the “USB to I ² C Using Microchip USB 3.1 Gen 1 Hubs” application note.
200 k Ω Pull-Up	CONFIG2	SMBus Slave Mode The SMBus interface will operate in Slave Mode for use with hub configuration.
10 k Ω Pull-Down	CONFIG3	Unused, Reserved
10 k Ω Pull-Up	CONFIG4	Unused, Reserved
10 Ω Pull-Down	CONFIG5	Unused, Reserved
10 Ω Pull-Up	CONFIG6	Unused, Reserved

3.5.2 PORT DISABLE CONFIGURATION (PRT_DIS_P[6:1] / PRT_DIS_M[6:1])

The PRT_DIS_P[6:1] and PRT_DIS_M[6:1] configuration straps are used in conjunction to disable the related port (6-1).

For PRT_DIS_P_x (where x is the corresponding port 6-1):

- 0 = Port x D+ Enabled
- 1 = Port x D+ Disabled

For PRT_DIS_M_x (where x is the corresponding port 6-1):

- 0 = Port x D- Enabled
- 1 = Port x D- Disabled

Note: Both PRT_DIS_P_x and PRT_DIS_M_x (where x is the corresponding port) must be tied to 3.3 V to disable the associated downstream port. Disabling the USB 2.0 port will also disable the corresponding USB 3.1 Gen 1 port.

3.5.3 NON-REMOVABLE PORT CONFIGURATION (CFG_NON_REM)

The CFG_NON_REM configuration strap is used to configure the non-removable port settings of the device to one of five settings. These modes are selected by the configuration of an external resistor on the CFG_NON_REM pin. The resistor options are a 200 kΩ pull-down, 200 kΩ pull-up, 10 kΩ pull-down, 10 kΩ pull-up, 10 Ω pull-down and 10 Ω pull-up as shown in [Table 3-12](#).

TABLE 3-12: CFG_NON_REM RESISTOR ENCODING

<u>CFG_NON_REM</u> Resistor Value	Setting
200 kΩ Pull-Down	All ports removable
200 kΩ Pull-Up	Port 3 non-removable
10 kΩ Pull-Down	Port 3, 4 non-removable
10 kΩ Pull-Up	Port 3, 4, 5, non-removable
10 Ω Pull-Down	Port 3, 4, 5, 6 non-removable
10 Ω Pull-Up	Reserved

3.5.4 BATTERY CHARGING CONFIGURATION (CFG_BC_EN)

The CFG_BC_EN configuration strap is used to configure the battery charging port settings of the device to one of five settings. These modes are selected by the configuration of an external resistor on the CFG_BC_EN pin. The resistor options are a 200 kΩ pull-down, 200 kΩ pull-up, 10 kΩ pull-down, 10 kΩ pull-up, 10 Ω pull-down and 10 Ω pull-up as shown in [Table 3-13](#).

TABLE 3-13: CFG_BC_EN RESISTOR ENCODING

<u>CFG_BC_EN</u> Resistor Value	Setting
200 kΩ Pull-Down	No battery charging
200 kΩ Pull-Up	Port 1 battery charging
10 kΩ Pull-Down	Port 1, 2 battery charging
10 kΩ Pull-Up	Port 1, 2, 3, battery charging
10 Ω Pull-Down	Port 1, 2, 3, 4 battery charging
10 Ω Pull-Up	Port 1, 2, 3, 4, 5, 6 battery charging

3.5.5 GENERAL PURPOSE INPUT/OUTPUT CONFIGURATION (GPIO_x)

General Purpose Inputs/Outputs may be used for application specific purposes. Any given GPIO may operate as an input or an output. Inputs can apply an internal 50kΩ pull-down or pull-up resistor. Outputs may drive low or drive high (3.3V). GPIOs may be configured and manipulated during runtime (while enumerated to a host) in one of two ways:

- SMBus configuration
- USB to GPIO bridging

3.5.5.1 SMBus configuration

The SMBus slave interface may be used to write to internal registers that configure the state of the GPIO. Refer to the “Configuration Options for Microchip USB58xx and USB59xx Hubs” application note for additional details.

3.5.5.2 USB to GPIO Bridging

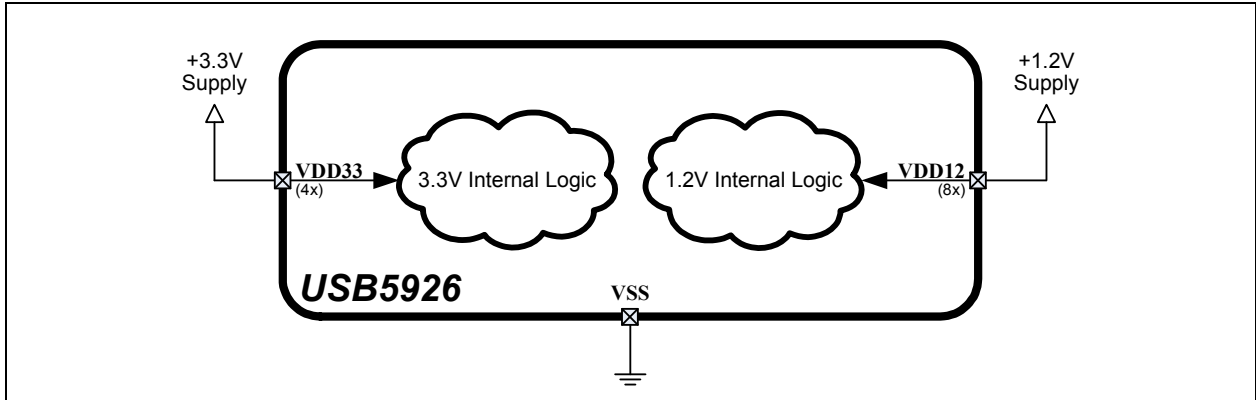
USB to GPIO Bridging may be used to write to internal registers that configure the state of the GPIO. USB to GPIO bridging operates via host communication to the hub’s internal Hub Feature Controller. Refer to the “USB to GPIO Bridging for Microchip USB3.1 Gen 1 Hubs” application note for additional details.

4.0 DEVICE CONNECTIONS

4.1 Power Connections

Figure 4-1 illustrates the device power connections.

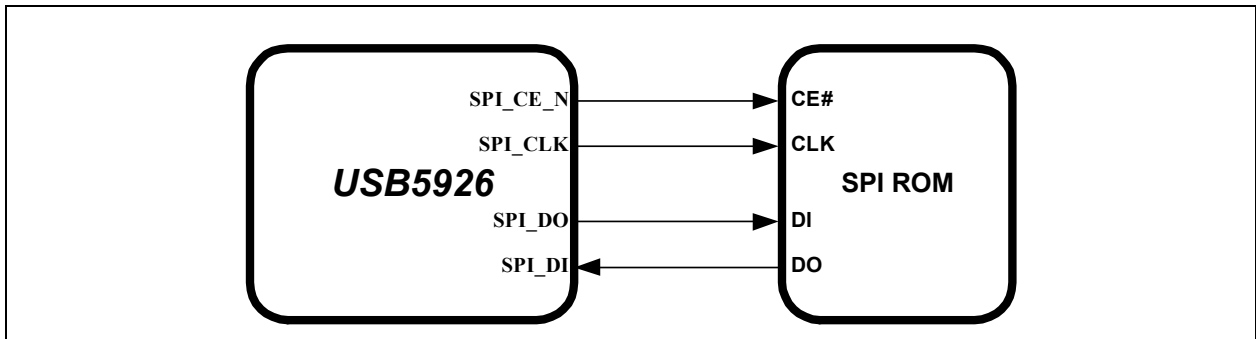
FIGURE 4-1: DEVICE POWER CONNECTIONS



4.2 SPI ROM Connections

Figure 4-2 illustrates the device SPI ROM connections. Refer to [Section 7.1 “SPI Master Interface”](#) for additional information on this device interface.

FIGURE 4-2: SPI ROM CONNECTIONS



4.3 SMBus Slave Connections

Figure 4-3 illustrates the device SMBus slave connections. Refer to [Section 7.2 “SMBus Slave Interface”](#) for additional information on this device interface.

FIGURE 4-3: SMBUS SLAVE CONNECTIONS

