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USBF129

USB Firmware Memory

Features

- Preprogrammed with binary image 129 for automotive usage. See “FlexConnect Firmware for USB84604” application note for complete feature set.
- Targeted for USB 2.0 High-Speed infotainment applications including:
  - Integration with head unit systems
  - First, second, and third row USB media hubs
- Memory Size:
  - 512 KByte (4 Mbit)
- Single Voltage Read and Write Operations
  - 2.7-3.6V
- Serial Interface Architecture
  - SPI Compatible: Mode 0 and Mode 3
- High Speed Clock Frequency
  - 30MHz
- READ Support
  - Fast-Read Dual-Output
  - Fast-Read Single I/O
- Superior Reliability
  - Endurance: 100,000 Cycles
  - Greater than 20 years Data Retention
- Ultra-Low Power Consumption:
  - Active Read Current: 5 mA (typical)
  - Standby Current: 5 µA (typical)
  - Power-down Mode Standby Current: 3 µA (typical)
- Flexible Erase Capability
  - Uniform 4 KByte sectors
  - Uniform 64 KByte overlay blocks
- Page Program Mode
  - 256 Bytes/Page
- Fast Erase and Page-Program:
  - Chip-Erase Time: 250 ms (typical)
  - Sector-Erase Time: 40 ms (typical)
  - Block-Erase Time: 80 ms (typical)
  - Page-Program Time: 4 ms/ 256 bytes (typical)
- End-of-Write Detection
  - Software polling the BUSY bit in Status Register
- Hold Pin (HOLD#)
  - Suspend a serial sequence without deselecting the device
- Write Protection (WP#)
  - Enables/Disables the Lock-Down function of the status register
- Software Write Protection
  - Write protection through Block-Protection bits in status register
- Temperature Range
  - Industrial: -40°C to +85°C
- Packages Available
  - 8-lead SOIC (150 mils)
  - Other packages available upon request.
- All devices are RoHS compliant
- Automotive Grade 3

Product Description

USBF129, a USB Firmware memory chip, is a companion to the Microchip Automotive USB Smart Hub devices: USB84604 and USB84602. It is factory preprogrammed with version 129 of the binary firmware, which contains application firmware and default hub configuration settings. The USBF129 memory function assures proper functionality, providing for decreased development time and engineering resource, and overall faster time to market. Full custom programming alternatives are available upon request.

The USB Firmware memory family features a four-wire, SPI-compatible interface that allows for a low pin-count package, which occupies less board space and ultimately lowers total system costs. It is manufactured with proprietary, high-performance CMOS SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches ideal for applications requiring high quality and reliability.

USBF129 is offered in 8-lead SOIC. Alternate low profile package is available upon request. See Figure 2-1 for the pin assignments.

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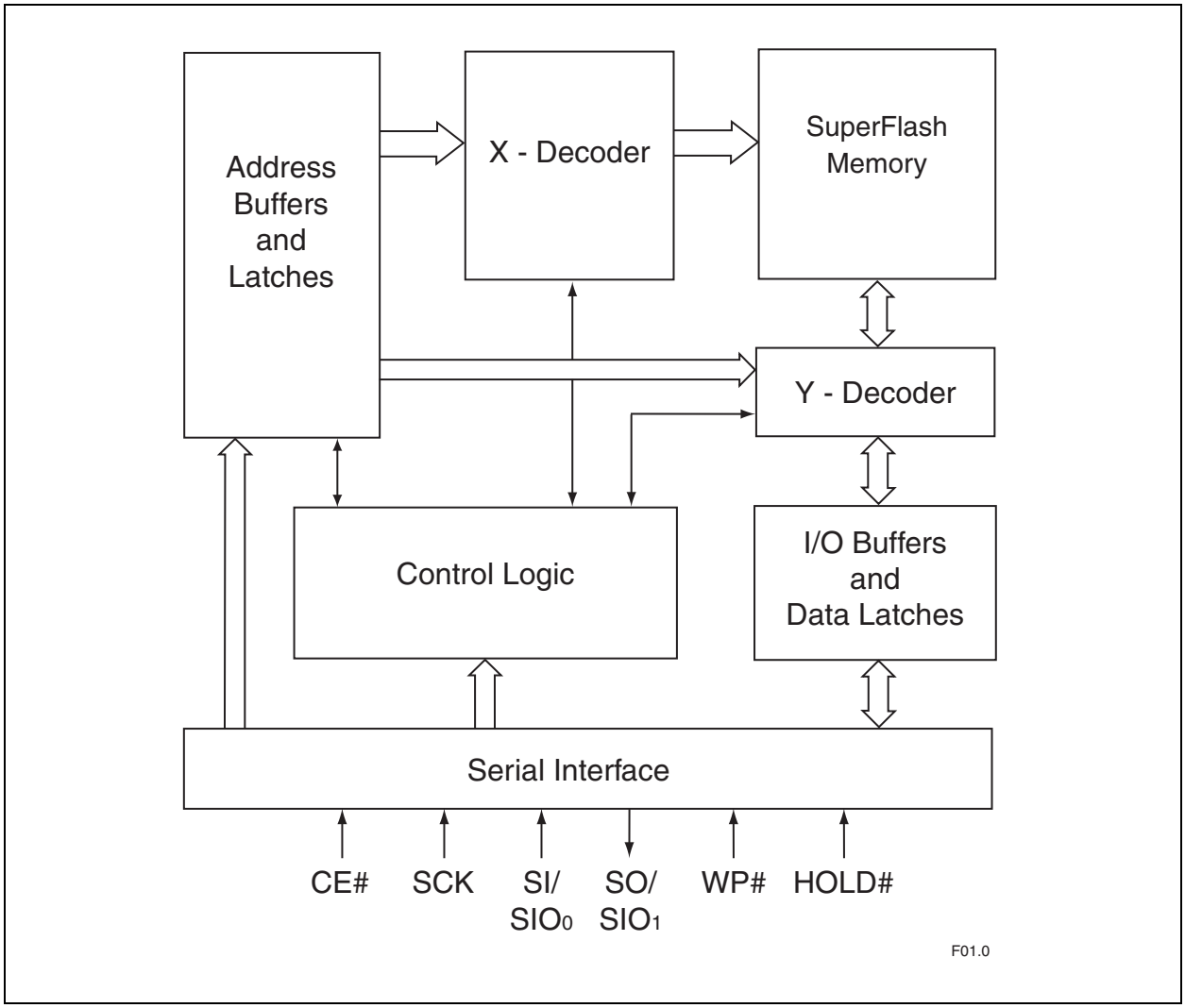
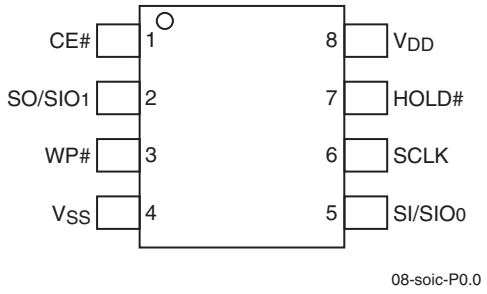
1.0 FUNCTIONAL BLOCKS

FIGURE 1-1: FUNCTIONAL BLOCK DIAGRAM



2.0 PIN ASSIGNMENTS

FIGURE 2-1: PIN ASSIGNMENTS



8-Lead SOIC

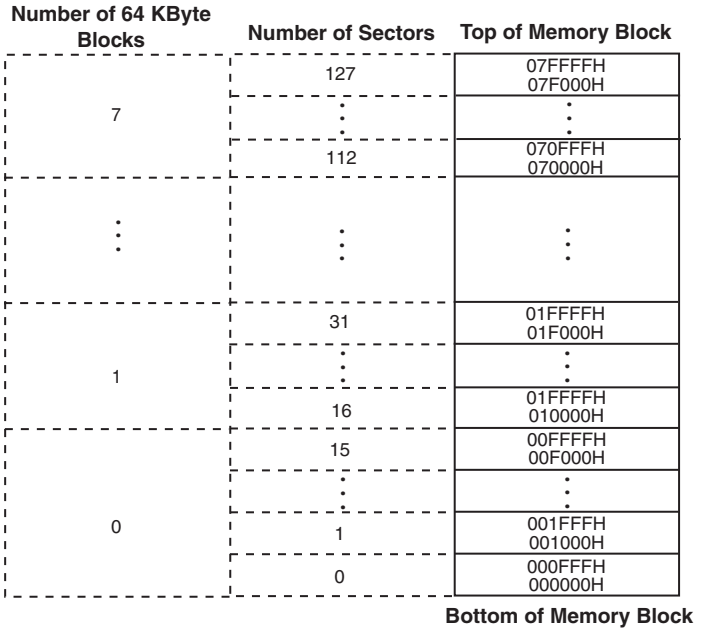
TABLE 2-1: PIN DESCRIPTION

Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the input/output timing of the serial interface. Commands, addresses, or input data are latched on the rising edge of the clock input, while output data is shifted out on the falling edge of the clock input.
SI	Serial Data Input	To transfer commands, addresses, or data serially into the device. Inputs are latched on the rising edge of the serial clock.
SO	Serial Data Output	To transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock.
$SIO_{[0:1]}$	Serial Data Input/ Output for Dual I/O Mode	To transfer commands, addresses, or data serially into the device, or data out of the device. Inputs are latched on the rising edge of the serial clock. Data is shifted out on the falling edge of the serial clock. These pins are used in Dual I/O mode
CE#	Chip Enable	The device is enabled by a high to low transition on CE#. CE# must remain low for the duration of any command sequence. The device is deselected and placed in Standby mode when CE# is high.
WP#	Write Protect	The Write Protect (WP#) pin is used to enable/disable BPL bit in the status register.
HOLD#	Hold	To temporarily stop serial communication with USB Firmware memory while device is selected.
V_{DD}	Power Supply	To provide power supply voltage: 2.7-3.6V
V_{SS}	Ground	

3.0 MEMORY ORGANIZATION

USBF129 SuperFlash memory arrays are organized in 128 uniform 4 KByte sectors, with 8 64 KByte overlay erasable blocks.

FIGURE 3-1: MEMORY MAP

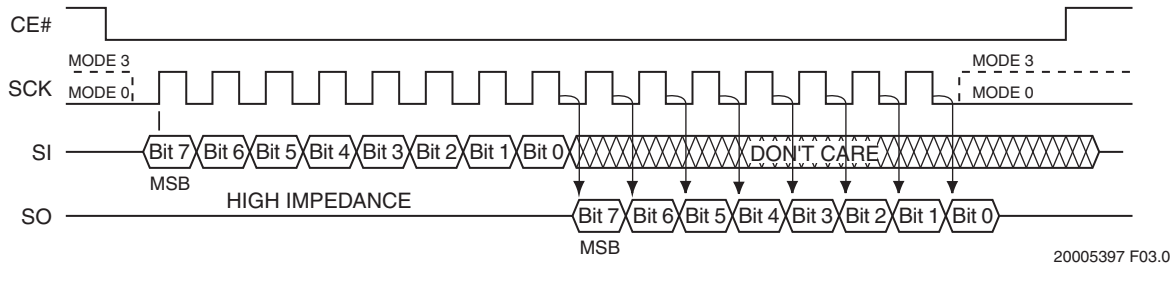


4.0 DEVICE OPERATION

USBF129 is accessed through the SPI (Serial Peripheral Interface) bus compatible protocol. The SPI bus consist of four control lines: Chip Enable (CE#) is used to select the device, and data is accessed through the Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK).

The USBF129 supports both Mode 0 (0,0) and Mode 3 (1,1) of SPI bus operations. The difference between the two modes, as shown in Figure 4-1, is the state of the SCK signal when the bus master is in Stand-by mode and no data is being transferred. The SCK signal is low for Mode 0 and SCK signal is high for Mode 3. For both modes, the Serial Data In (SI) is sampled at the rising edge of the SCK clock signal and the Serial Data Output (SO) is driven after the falling edge of the SCK clock signal.

FIGURE 4-1: SPI PROTOCOL



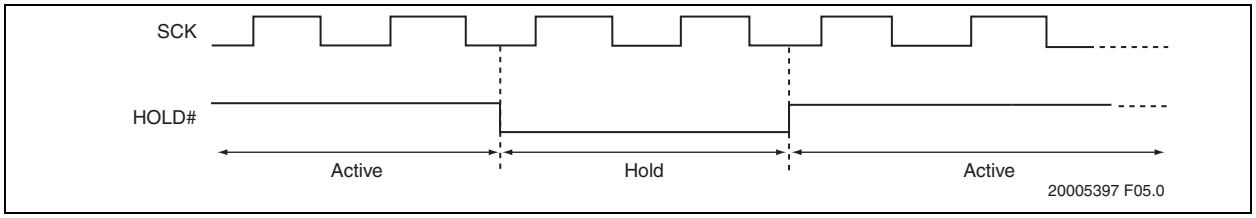
4.0.1 HOLD

In the hold mode, serial sequences underway with the device are paused without resetting the clocking sequence. To activate the HOLD# mode, CE# must be in active low state. The HOLD# mode begins when the SCK active low state coincides with the falling edge of the HOLD# signal. The Hold mode ends when the rising edge of the HOLD# signal coincides with the SCK active low state. HOLD# must not rise or fall when SCK logic level is high. See Figure 4-2 for Hold Condition waveform.

Once the device enters Hold mode, SO will be in high-impedance state while SI and SCK can be V_{IL} or V_{IH}.

If CE# is driven active high during a Hold condition, the device returns to standby mode. The device can then be re-initiated with the command sequences listed in Table 5-1. As long as HOLD# signal is low, the memory remains in the Hold condition. To resume communication with the device, HOLD# must be driven active high, and CE# must be driven active low. See Figure 4-2 for Hold timing.

FIGURE 4-2: HOLD CONDITION WAVEFORM



4.1 Write Protection

USBF129 provides software Write protection. The Write Protect pin (WP#) enables or disables the lock-down function of the status register. The Block-Protection bits (BP0, BP1, BP2, TB, and BPL) in the status register provide Write protection to the memory array and the status register. See Table 4-3 for the Block-Protection description.

4.1.1 WRITE PROTECT PIN (WP#)

The Write Protect (WP#) pin enables the lock-down function of the BPL bit (bit 7) in the status register. When WP# is driven low, the execution of the Write-Status-Register (WRSR) instruction is determined by the value of the BPL bit (see Table 4-1). When WP# is high, the lock-down function of the BPL bit is disabled.

TABLE 4-1: CONDITIONS TO EXECUTE WRITE-STATUS-REGISTER (WRSR) INSTRUCTION

WP#	BPL	Execute WRSR Instruction
L	1	Not Allowed
L	0	Allowed
H	X	Allowed

4.2 Status Register

The software status register provides status on whether the flash memory array is available for any Read or Write operation, whether the device is Write enabled, and the state of the Memory Write protection.

During an internal Erase or Program operation, the status register may be read only to determine the completion of an operation in progress. Table 4-2 describes the function of each bit in the software status register.

TABLE 4-2: SOFTWARE STATUS REGISTER

Bit	Name	Function	Default at Power-up	Read/Write
0	BUSY	1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	1 = Device is memory Write enabled 0 = Device is not memory Write enabled	0	R
2	BP0[1]	Indicate current level of block write protection (See Table 4-3)	0 or 1	R/W
3	BP1[1]	Indicate current level of block write protection (See Table 4-3)	0 or 1	R/W
4	BP2[1]	Indicate current level of block write protection (See Table 4-3)	0 or 1	R/W
5	TB[1]	1 = 1/8, 1/4, or 1/2 Bottom Memory Blocks are protected (See Table 4-3) 0 = 1/8, 1/4, or 1/2 Top Memory Blocks are protected	0 or 1	R/W
6	RES	Reserved for future use	0	N/A
7	BPL[1]	1 = BP0, BP1, BP2, TB, and BPL are read-only bits 0 = BP0, BP1, BP2, TB, and BPL are read/writable	0 or 1	R/W

1. BP0, BP1, BP2, TB, and BPL bits are non-volatile memory bits.

4.2.1 BUSY (BIT 0)

The Busy bit determines whether there is an internal Erase or Program operation in progress. A ‘1’ for the Busy bit indicates the device is busy with an operation in progress. A ‘0’ indicates the device is ready for the next valid operation.

4.2.2 WRITE ENABLE LATCH (WEL–BIT 1)

The Write-Enable-Latch bit indicates the status of the internal Write-Enable-Latch memory. If the WEL bit is set to ‘1’, it indicates the device is Write enabled. If the bit is set to ‘0’ (reset), it indicates the device is not Write enabled and does not accept any Write (Program/ Erase) commands. The Write-Enable-Latch bit is automatically reset under the following conditions:

- Power-up
- Write-Disable (WRDI) instruction completion
- Page-Program instruction completion
- Sector-Erase instruction completion
- 64 KByte Block-Erase instruction completion
- Chip-Erase instruction completion
- Write-Status-Register instruction completion

4.2.3 BLOCK-PROTECTION (BP0, BP1, BP2, AND TB–BITS 2, 3, 4, AND 5)

The Block-Protection (BP0, BP1, BP2, and TB) bits define the size of the memory area to be software protected against any memory Write (Program or Erase) operation, see Table 4-3. The Write-Status-Register (WRSR) instruction is used to program the BP0, BP1, BP2, and TB bits as long as WP# is high or the Block-Protect-Lock (BPL) bit is ‘0’. Chip-Erase can only be executed if Block-Protection bits are all ‘0’. BP0, BP1, and BP2 select the protected area and TB allocates the protected area to the higher-order address area (Top Blocks) or lower-order address area (Bottom Blocks).

4.2.4 BLOCK PROTECTION LOCK-DOWN (BPL–BIT 7)

When the WP# pin is driven low (V_{IL}), it enables the Block-Protection-Lock-Down (BPL) bit. When BPL is set to '1', it prevents any further alteration of the BP0, BP1, BP2, TB, and BPL bits. When the WP# pin is driven high (V_{IH}), the BPL bit has no effect and its value is 'Don't Care'.

TABLE 4-3: SOFTWARE STATUS REGISTER BLOCK PROTECTION

Protection Level	Status Register Bit				Protected Memory Address
	TB	BP2	BP1	BP0	
0 (Full Memory Array unprotected)	X	0	0	0	None
T1 (1/8 Top Memory Block protected)	0	0	0	1	070000H-07FFFFH
T2 (1/4 Top Memory Block protected)	0	0	1	0	060000H-07FFFFH
T3 (1/2 Top Memory Block protected)	0	0	1	1	040000H-07FFFFH
B1 (1/8 Bottom Memory Block protected)	1	0	0	1	000000H-00FFFFH
B2 (1/4 Bottom Memory Block protected)	1	0	1	0	000000H-01FFFFH
B3 (1/2 Bottom Memory Block protected)	1	0	1	1	000000H-03FFFFH
4 (Full Memory Block protected)	X	1	X	X	000000H-07FFFFH

5.0 INSTRUCTIONS

Instructions are used to read, write (Erase and Program), and configure the USBF129 devices. The instruction bus cycles are 8 bits each for commands (Op Code), data, and addresses. The Write-Enable (WREN) instruction must be executed prior to Sector-Erase, Block-Erase, Page-Program, Write-Status-Register, or Chip-Erase instructions. The complete instructions are provided in Table 5-1. All instructions are synchronized off a high-to-low transition of CE#. Inputs will be accepted on the rising edge of SCK starting with the most significant bit. CE# must be driven low before an instruction is entered and must be driven high after the last bit of the instruction has been shifted in (except for Read, Read-ID, and Read-Status-Register instructions). Any low-to-high transition on CE#, before receiving the last bit of an instruction bus cycle, will terminate the instruction in progress and return the device to standby mode. Instruction commands (Op Code), addresses, and data are all input from the most significant bit (MSB) first.

TABLE 5-1: DEVICE OPERATION INSTRUCTIONS

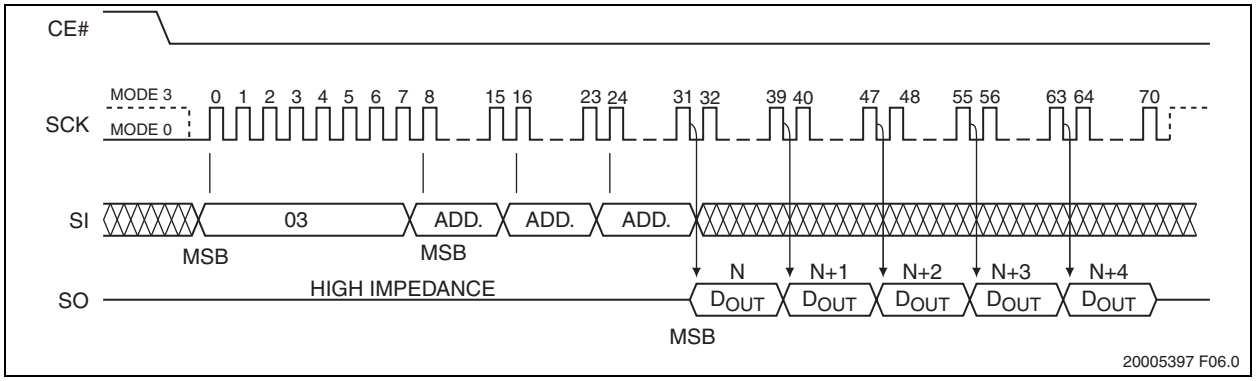
Instruction	Description	Op Code Cycle[1]	Address Cycle(s)[2]	Dummy Cycle(s)	Data Cycle(s)	Maximum Frequency
Read	Read Memory	0000 0011b (03H)	3	0	1 to ∞	25 MHz
High-Speed Read	Read Memory at Higher Speed	0000 1011b (0BH)	3	1	1 to ∞	30 MHz
Fast-Read Dual-Output	Read Memory with Dual Output	0011 1011b (3BH)	3	1[3]	1 to ∞[3]	
Fast-Read Dual I/O	Read Memory with Dual Address Input and Data Output	1011 1011b (BBH)	3[3]	1[3]	1 to ∞[3]	
4 KByte Sector-Erase[4]	Erase 4 KByte of memory array	0010 0000b (20H) 1101 0111b (D7H)	3	0	0	
64 KByte Block-Erase[5]	Erase 64 KByte block of memory array	1101 1000b (D8H)	3	0	0	
Chip-Erase	Erase Full Memory Array	0110 0000b (60H) or 1100 0111b (C7H)	0	0	0	
Page-Program	To program up to 256 Bytes	0000 0010b (02H)	3	0	1 to 256	
RDSR[6]	Read-Status-Register	0000 0101b (05H)	0	0	1 to ∞	
WRSR	Write-Status-Register	0000 0001b (01H)	0	0	1	
WREN	Write-Enable	0000 0110b (06H)	0	0	0	
WRDI	Write-Disable	0000 0100b (04H)	0	0	0	
RDID[7, 8]	Read-ID	1010 1011b (ABH)	3	0	1 to ∞	
JEDEC-ID	JEDEC ID Read	1001 1111b (9FH)	0	0	4 to ∞	
DPD	Deep Power-Down Mode	1011 1001b (B9H)	0	0	0	
RDPD[8]	Release from Deep Power-Down or Read ID	1010 1011b (ABH)	0	0	0	

1. One bus cycle is eight clock periods.
2. Address bits above the most significant bit of each density can be V_{IL} or V_{IH}.
3. One bus cycle is four clock periods in Dual Operation
4. 4 KByte Sector-Erase addresses: use A_{MS}-A_{12}, remaining addresses are don't care but must be set either at V_{IL} or V_{IH}.
5. 64 KByte Block-Erase addresses: use A_{MS}-A_{16}, remaining addresses are don't care but must be set either at V_{IL} or V_{IH}.
6. The Read-Status-Register is continuous with ongoing clock cycles until terminated by a low to high transition on CE#.
7. Device ID is read after three dummy address bytes. The Device ID output stream is continuous until terminated by a low-to-high transition on CE#.
8. The instructions Release from Deep Power down and Read-ID are similar instructions (ABH). Executing Read-ID requires the ABH instruction, followed by 24 dummy address bits to retrieve the Device ID. Release from Deep Power-Down only requires the instruction ABH.

5.1 Read

The Read instruction, 03H, supports up to 25 MHz Read. The device outputs a data stream starting from the specified address location. The data stream is continuous through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer automatically increments until the highest memory address is reached. Once the highest memory address is reached, the address pointer automatically increments to the beginning (wrap-around) of the address space. Once the data from the address location 7FFFFH is read, the next output is from address location 000000H. The Read instruction is initiated by executing an 8-bit command, 03H, followed by address bits A_{23}-A_0. CE# must remain active low for the duration of the Read cycle. See Figure 5-1 for the Read sequence.

FIGURE 5-1: READ SEQUENCE

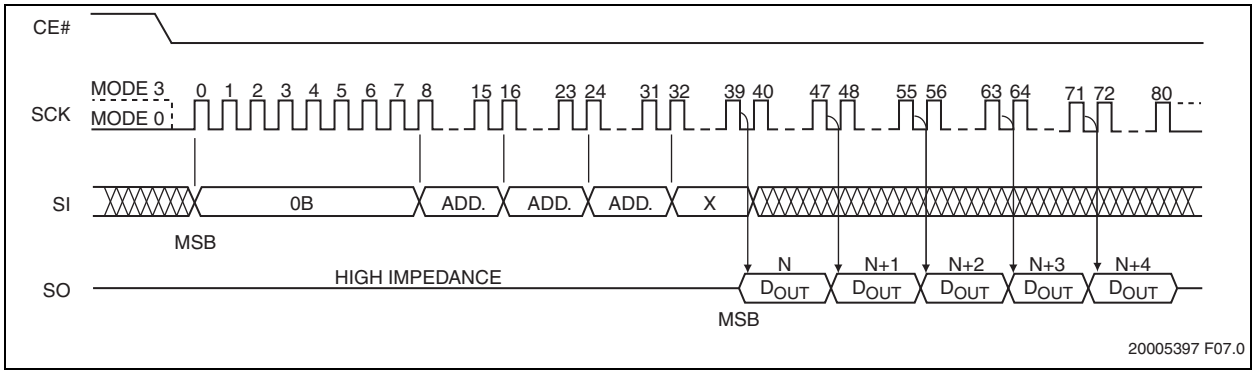


5.2 High-Speed-Read

The High-Speed-Read instruction supporting up to 30 MHz Read is initiated by executing an 8-bit command, 0BH, followed by address bits [A_{23}-A_0] and a dummy byte. CE# must remain active low for the duration of the High-Speed-Read cycle. See Figure 5-2 for the High-Speed-Read sequence.

Following a dummy cycle, the High-Speed-Read instruction outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically increment to the beginning (wrap-around) of the address space. Once the data from address location 7FFFFH is read, the next output will be from address location 000000H.

FIGURE 5-2: HIGH-SPEED-READ SEQUENCE

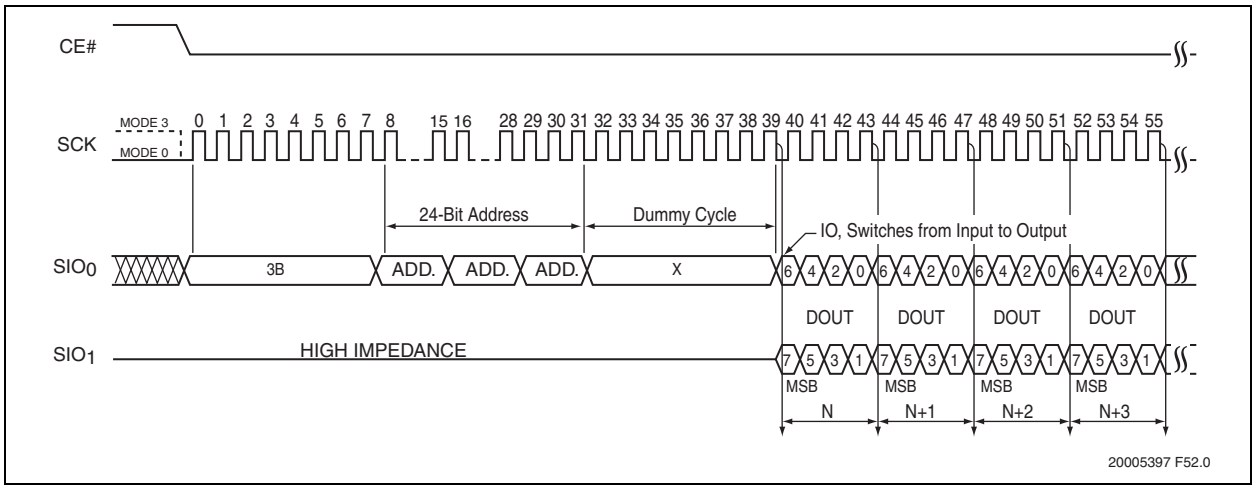


5.3 Fast-Read Dual Output

The Fast-Read Dual-Output (3BH) instruction outputs data up to 30 MHz from the SIO_0 and SIO_1 pins. To initiate the instruction, execute an 8-bit command (3BH) followed by address bits A23-A0 and a dummy byte on SI/SIO_0. Following a dummy cycle, the Fast-Read Dual-Output instruction outputs the data starting from the specified address location on the SIO_1 and SIO_0 lines. SIO_1 outputs, per clock sequence, odd data bits D7, D5, D3, and D1; and SIO_0 outputs even data bits D6, D4, D2, and D0. CE# must remain active low for the duration of the Fast-Read Dual-Output instruction cycle. See Figure 5-3 for the Fast-Read Dual-Output sequence.

The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer automatically increments to the beginning (wraparound) of the address space. Once the data from address location 7FFFFH has been read the next output will be from address location 000000H.

FIGURE 5-3: FAST-READ DUAL OUTPUT SEQUENCE



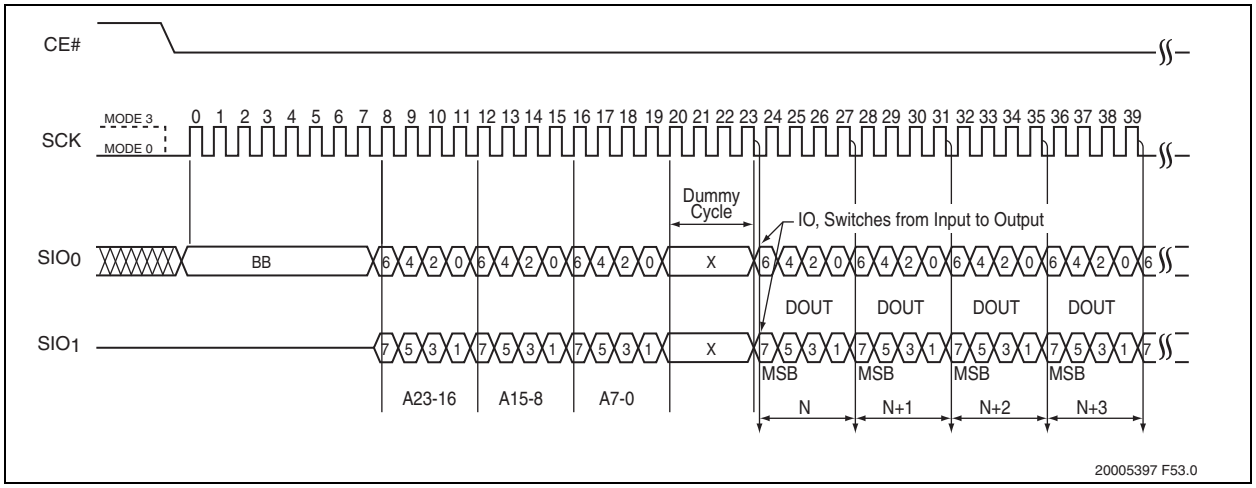
5.4 Fast-Read Dual I/O

The Fast-Read Dual I/O (BBH) instruction reduces the total number of input clock cycles, which results in faster data access. The device is first selected by driving Chip Enable CE# low. Fast-Read Dual I/O is initiated by executing an 8-bit command (BBH) on SI/SIO_0, thereafter, the device accepts address bits A23-A0 and a dummy byte on SI/SIO_0 and SO/SIO_1. It offers the capability to input address bits A23-A0 at a rate of two bits per clock. Odd address bits A23 through A1 are input on SIO_1 and even address bits A22 through A0 are input on SIO_0, alternately For example, the most significant bit is input first followed by A23/22, A21/A20, and so on. Each bit is latched at the same rising edge of the Serial Clock (SCK). The input data during the dummy clocks is “don’t care”. However, the SIO_0 and SIO_1 pin must be in high-impedance prior to the falling edge of the first data output clock.

Following a dummy cycle, the Fast-Read Dual I/O instruction outputs the data starting from the specified address location on the SIO_1 and SIO_0 lines. SIO_1 outputs, per clock sequence, odd data bits D7, D5, D3, and D1; and SIO_0 outputs even data bits D6, D4, D2, and D0 per clock edge. CE# must remain active low for the duration of the Fast-Read Dual I/O instruction cycle. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#.

The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer automatically increments to the beginning (wraparound) of the address space. Once the data from address location 7FFFFH is read, the next output is from address location 000000H. See Figure 5-4 for the Fast-Read Dual I/O sequence.

FIGURE 5-4: FAST-READ DUAL I/O SEQUENCE



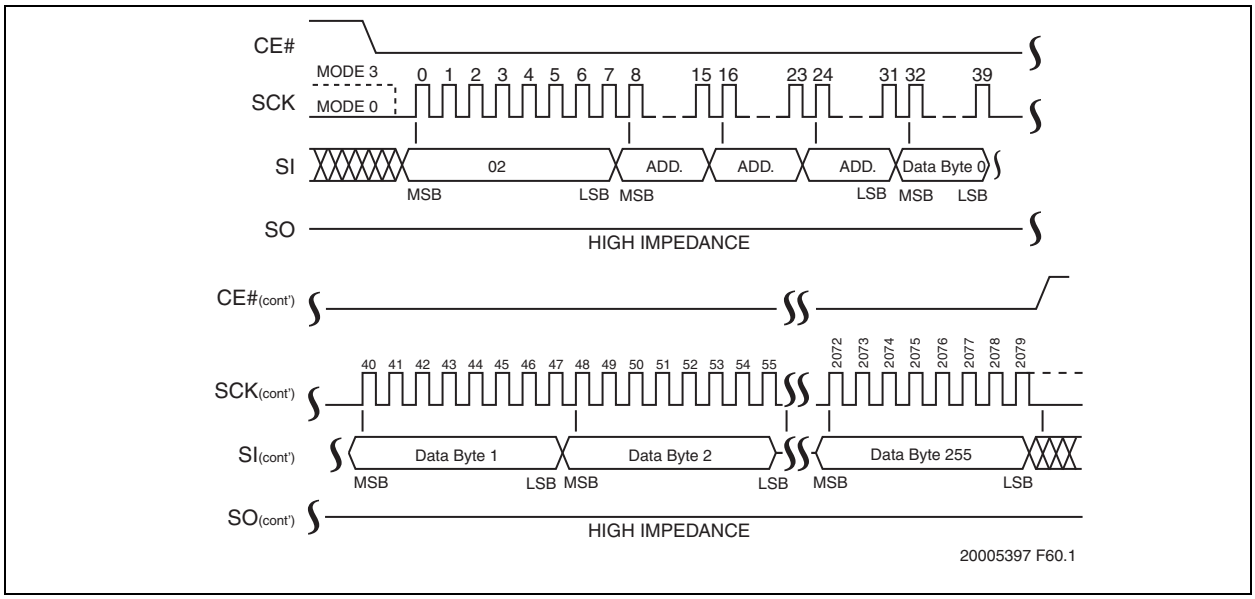
5.5 Page-Program

The Page-Program instruction programs up to 256 Bytes of data in the memory. The data for the selected page address must be in the erased state (FFH) before initiating the Page-Program operation. A Page-Program applied to a protected memory area will be ignored. Prior to the program operation, execute the WREN instruction.

To execute a Page-Program operation, the host drives CE# low, then sends the Page-Program command cycle (02H), three address cycles, followed by the data to be programmed, and then drives CE# high. The programmed data must be between 1 to 256 Bytes and in whole byte increments; sending less than a full byte will cause the partial byte to be ignored. Poll the BUSY bit in the Status register, or wait T_{PP}, for the completion of the internal, self-timed, Page-Program operation. See Figure 5-5 for the Page-Program sequence and Figure 6-8 for the Page-Program flow chart.

When executing Page-Program, the memory range for the USBF129 is divided into 256-Byte page boundaries. The device handles the shifting of more than 256 Bytes of data by maintaining the last 256 Bytes as the correct data to be programmed. If the target address for the Page-Program instruction is not the beginning of the page boundary (A[7:0] are not all zero), and the number of bytes of data input exceeds or overlaps the end of the address of the page boundary, the excess data inputs wrap around and will be programmed at the start of that target page.

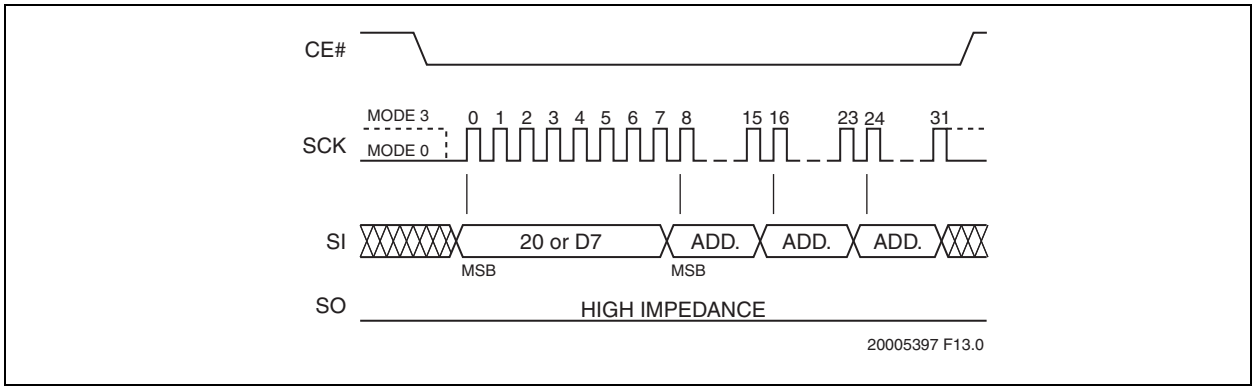
FIGURE 5-5: PAGE-PROGRAM SEQUENCE



5.6 Sector-Erase

The Sector-Erase instruction clears all bits in the selected 4 KByte sector to FFH. A Sector-Erase instruction applied to a protected memory area will be ignored. Prior to any Write operation, the Write-Enable (WREN) instruction must be executed. CE# must remain active low for the duration of any command sequence. The Sector-Erase instruction is initiated by executing an 8-bit command, 20H or D7H, followed by address bits [A_{23}-A_0]. Address bits [A_{MS}-A_{12}] (A_{MS} = Most Significant address) are used to determine the sector address (SA_X), remaining address bits can be V_{IL} or V_{IH}. CE# must be driven high before the instruction is executed. Poll the BUSY bit in the Software Status register, or wait T_{SE}, for the completion of the internal self-timed Sector-Erase cycle. See Figure 5-6 for the Sector-Erase sequence and Figure 6-9 for the flow chart.

FIGURE 5-6: SECTOR-ERASE SEQUENCE

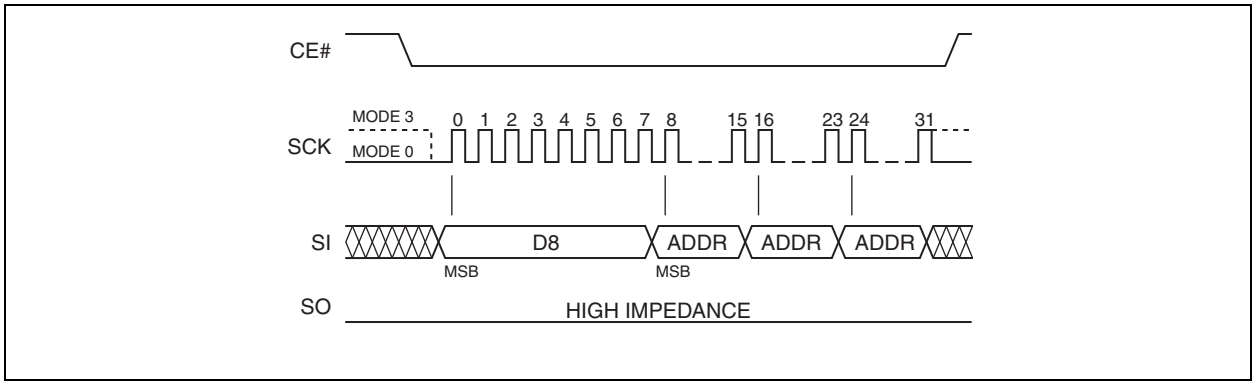


5.7 64-KByte Block-Erase

The 64-KByte Block-Erase instruction clears all bits in the selected 64 KByte block to FFH. Applying this instruction to a protected memory area results in the instruction being ignored. Prior to any Write operation, the Write-Enable (WREN) instruction must be executed. CE# must remain active low for the duration of any command sequence.

Initiate the 64-Byte Block-Erase instruction by executing an 8-bit command, D8H, followed by address bits [A_{23}-A_0]. Address bits [A_{MS}-A_{16}] (A_{MS} = Most Significant Address) determine the block address (BA_X), remaining address bits can be V_{IL} or V_{IH}. CE# must be driven high before executing the instruction. Poll the Busy bit in the software status register or wait T_{BE} for the completion of the internal self-timed Block-Erase cycle. See Figure 5-7 for the 64-KByte Block-Erase sequences and Figure 6-9 for the flow chart.

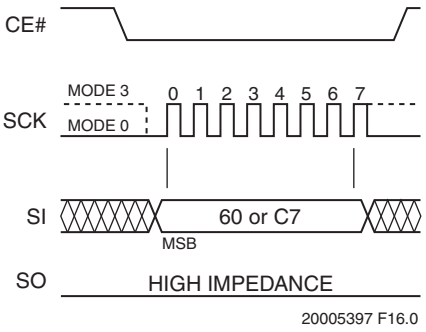
FIGURE 5-7: 64-KBYTE BLOCK-ERASE SEQUENCE



5.8 Chip-Erase

The Chip-Erase instruction clears all bits in the device to FFH. A Chip-Erase instruction is ignored if any of the memory area is protected. Prior to any Write operation, the Write-Enable (WREN) instruction must be executed. CE# must remain active low for the duration of the Chip-Erase instruction sequence. Initiate the Chip-Erase instruction by executing an 8-bit command, 60H or C7H. CE# must be driven high before the instruction is executed. Poll the BUSY bit in the Software Status register, or wait T_{SCE}, for the completion of the internal self-timed Chip-Erase cycle. See Figure 5-8 for the Chip-Erase sequence and Figure 6-10 for the flow chart.

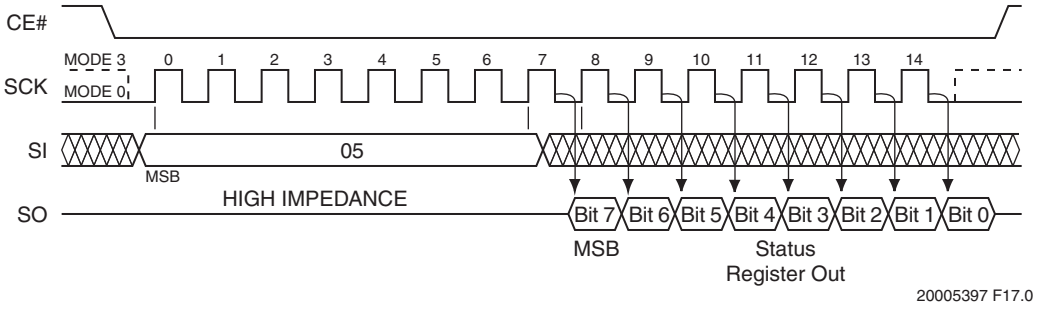
FIGURE 5-8: CHIP-ERASE SEQUENCE



5.9 Read-Status-Register (RDSR)

The Read-Status-Register (RDSR) instruction, 05H, allows reading of the status register. The status register may be read at any time even during a Write (Program/Erase) operation. When a Write operation is in progress, the Busy bit may be checked before sending any new commands to assure that the new commands are properly received by the device. CE# must be driven low before the RDSR instruction is entered and remain low until the status data is read. Read-Status-Register is continuous with ongoing clock cycles until it is terminated by a low-to-high transition of the CE#. See Figure 5-9 for the RDSR instruction sequence.

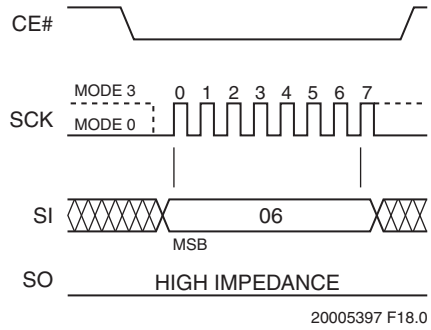
FIGURE 5-9: READ-STATUS-REGISTER (RDSR) SEQUENCE



5.10 Write-Enable (WREN)

The Write-Enable (WREN) instruction, 06H, sets the Write-Enable-Latch bit in the Status Register to '1' allowing Write operations to occur. The WREN instruction must be executed prior to any Write (Program/Erase) operation. The WREN instruction may also be used to allow execution of the Write-Status-Register (WRSR) instruction; however, the Write-Enable-Latch bit in the Status Register will be cleared upon the rising edge CE# of the WRSR instruction. CE# must be driven low before entering the WREN instruction, and CE# must be driven high before executing the WREN instruction. See Figure 5-10 for the WREN instruction sequence.

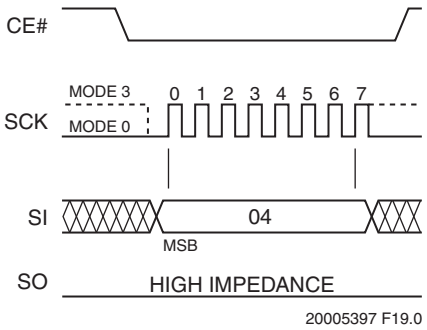
FIGURE 5-10: WRITE ENABLE (WREN) SEQUENCE



5.11 Write-Disable (WRDI)

The Write-Disable (WRDI) instruction, 04H, resets the Write-Enable-Latch bit to '0', thus preventing any new Write operations. CE# must be driven low before entering the WRDI instruction, and CE# must be driven high before executing the WRDI instruction. See Figure 5-11 for the WRDI instruction sequence.

FIGURE 5-11: WRITE DISABLE (WRDI) SEQUENCE

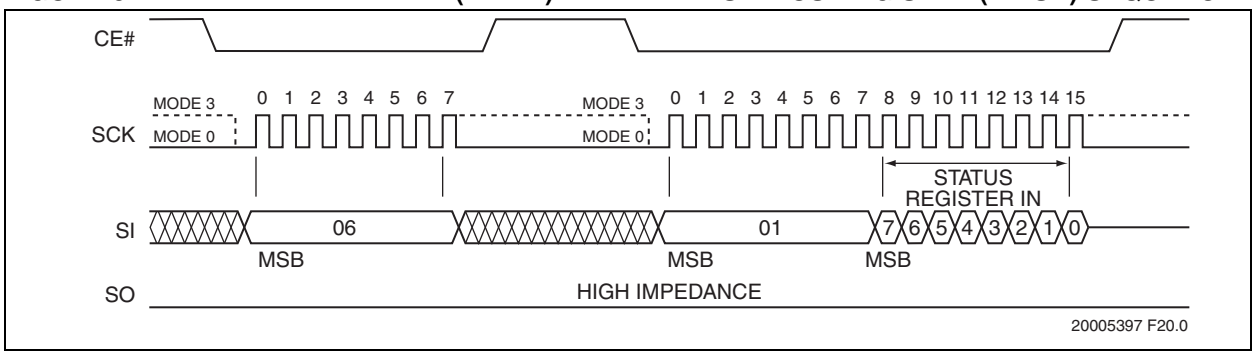


5.12 Write-Status-Register (WRSR)

The Write-Status-Register instruction writes new values to the BP0, BP1, BP2, TB, and BPL bits of the status register. CE# must be driven low before the command sequence of the WRSR instruction is entered and driven high before the WRSR instruction is executed. Poll the BUSY bit in the Software Status register, or wait T_{WRSR}, for the completion of the internal, self-timed Write-Status-Register cycle. See Figure 5-12 for WREN and WRSR instruction sequences and Figure 6-11 for the WRSR flow chart.

Executing the Write-Status-Register instruction will be ignored when WP# is low and BPL bit is set to '1'. When the WP# is low, the BPL bit can only be set from '0' to '1' to lock-down the status register, but cannot be reset from '1' to '0'. When WP# is high, the lock-down function of the BPL bit is disabled and the BPL, BP0, BP1, BP2, and TB bits in the status register can all be changed. As long as BPL bit is set to '0' or WP# pin is driven high (V_{IH}) prior to the low-to-high transition of the CE# pin at the end of the WRSR instruction, the bits in the status register can all be altered by the WRSR instruction. In this case, a single WRSR instruction can set the BPL bit to '1' to lock down the status register as well as altering the BP0, BP1, BP2, and TB bits at the same time. See Table 4-1 for a summary description of WP# and BPL functions.

FIGURE 5-12: WRITE-ENABLE (WREN) AND WRITE-STATUS-REGISTER (WRSR) SEQUENCE



5.13 Power-Down

The Deep Power-Down (DPD) instruction puts the device in the lowest power consumption mode – the Deep Power-Down mode. This instruction is ignored if the device is busy with an internal write operation. While the device is in DPD mode, all instructions are ignored except for the Release Deep Power-Down instruction or Read ID.

To initiate deep power-down, input the Deep Power-Down instruction (B9H) while driving CE# low. CE# must be driven high before executing the DPD instruction. After driving CE# high, the device requires a delay of T_{DPD} before the standby current I_{SB} is reduced to the deep power-down current I_{DPD}. See Figure 5-13 for the DPD instruction sequence.

Exit the power-down state using the Release from Deep Power-Down or Read ID instruction. CE# must be driven low before sending the Release from Deep Power-Down command cycle (ABH), and then driving CE# high. The device will return to Standby mode and be ready for the next instruction after T_{SBR}. See Figure 5-14. for the Release from Deep Power-Down sequence.

FIGURE 5-13: DEEP POWER-DOWN SEQUENCE

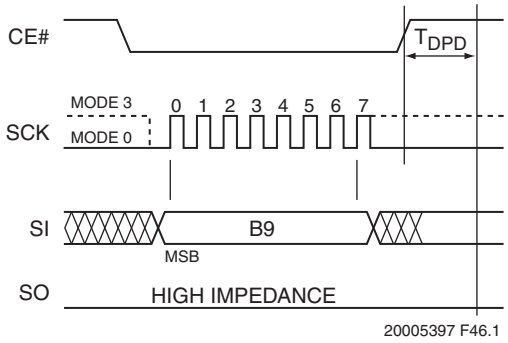
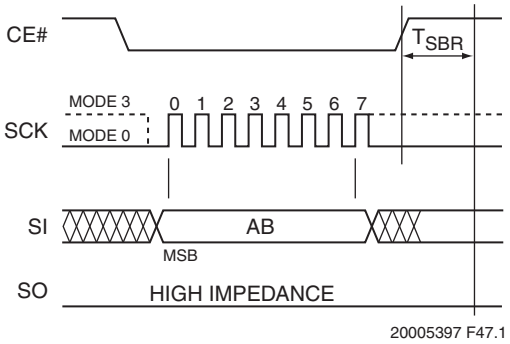


FIGURE 5-14: RELEASE FROM DEEP POWER-DOWN SEQUENCE



5.14 Read-ID

The Read-ID instruction identifies the device as USBF129. See Table 5-2.

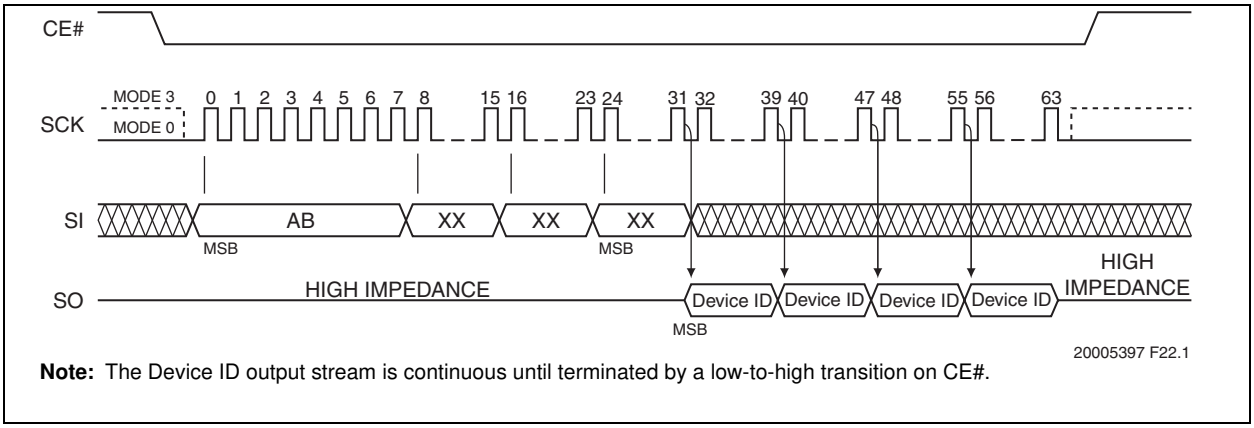
The device ID information is read by executing an 8-bit command, ABH, followed by 24 dummy address bits.

Following the Read-ID instruction, and 24 address dummy bits, the device ID continues to output with continuous clock input until terminated by a low-to-high transition on CE#.

TABLE 5-2: PRODUCT IDENTIFICATION

	Address	Data
USBF129 ID	XXXXXXH	6EH

FIGURE 5-15: READ-ID SEQUENCE



Note: The Device ID output stream is continuous until terminated by a low-to-high transition on CE#.

5.15 JEDEC Read-ID

The JEDEC Read-ID instruction identifies the device ID information of USBF129. The device information can be read by executing the 8-bit command, 9FH. Following the JEDEC Read-ID instruction, 32-bit device ID information is output from the device. The Device ID information is assigned by the manufacturer and contains the Device ID 1 in the first byte, the type of memory in the second byte, the memory capacity of the device in the third byte, and a reserved code in the fourth byte. The 4-Byte code outputs repeatedly with continuous clock input until a low-to-high transition on CE#. See Figure 5-16 for the instruction sequence. The JEDEC Read ID instruction is terminated by a low to high transition on CE# at any time during data output.

FIGURE 5-16: JEDEC READ-ID SEQUENCE

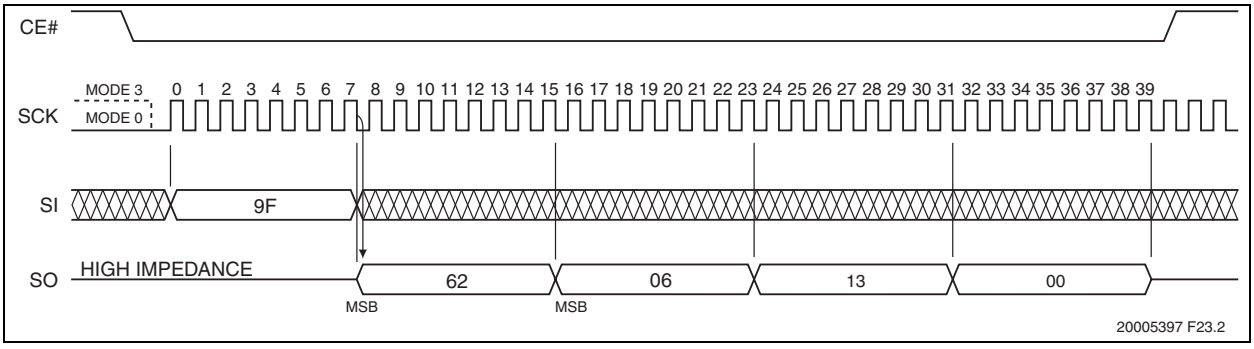


TABLE 5-3: JEDEC READ-ID DATA-OUT

Product	Device ID			
	Device ID 1 (Byte 1)	Memory Type (Byte 2)	Memory Capacity (Byte 3)	Reserved Code (Byte 4)
USBF129	62H	06H	13H	00H

6.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -55°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -2.0V to V_{DD}+2.0V
Package Power Dissipation Capability (T_A = 25°C) 1.0W
Surface Mount Solder Reflow Temperature . . . . . 260°C for 10 seconds
Output Short Circuit Current[1] . . . . . 50 mA

1. Output shorted for no more than one second. No more than one output shorted at a time.

TABLE 6-1: OPERATING RANGE

Range	Ambient Temp	V_{DD}
Industrial	-40°C to +85°C	2.7 - 3.6V
Automotive Grade 3	-40°C to +85°C	2.7 - 3.6V

TABLE 6-2: AC CONDITIONS OF TEST

Input Rise/Fall Time	Output Load
5ns	C_L = 30 pF

6.1 Power-Up Specifications

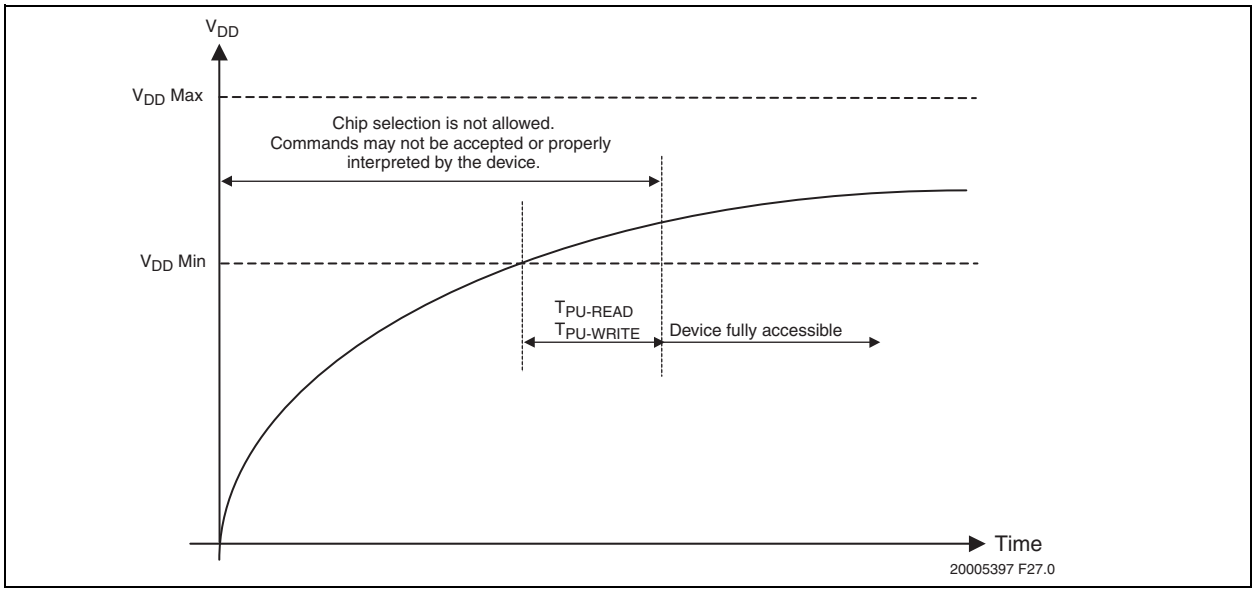
All functionalities and DC specifications are specified for a V_{DD} ramp rate of greater than 1V per 100 ms (0V to 3.3V in less than 330 ms). See Table 6-3 and Figure 6-2 for more information.

TABLE 6-3: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	V_{DD} Min to Read Operation	100	µs
$T_{PU-WRITE}$[1]	V_{DD} Min to Write Operation	100	µs

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

FIGURE 6-1: POWER-UP TIMING DIAGRAM



6.2 Hardware Data Protection

USBF129 provides a power-up reset function. To ensure that the power reset circuit will operate correctly, the device must meet the conditions shown in Figure 6-2 and Table 6-4. Microchip does not guarantee the data in the event of an instantaneous power failure that occurs during a Write operation.

FIGURE 6-2: POWER-DOWN TIMING DIAGRAM

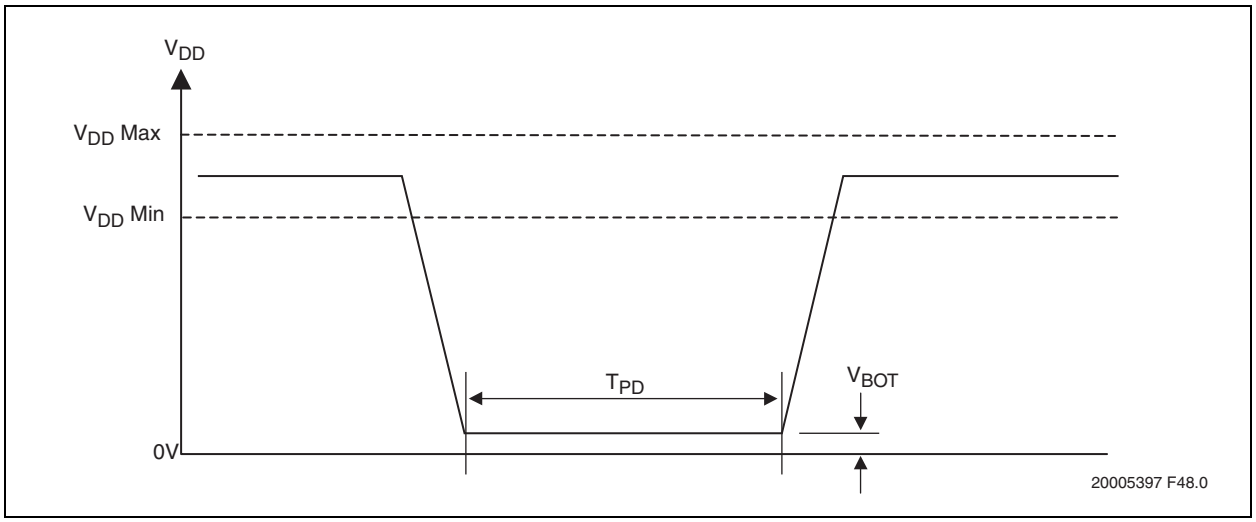


TABLE 6-4: RECOMMENDED SYSTEM POWER-DOWN TIMINGS

Symbol	Parameter	Min	Max	Units
T_{PD}	Power-down time	10		ms
V_{BOT}	Power-down voltage		0.2	V

6.3 Software Data Protection

USBF129 prevents unintentional operations by not recognizing commands under the following conditions:

- After inputting a Write command, if the rising CE# edge timing is not in a bus cycle (8 CLK units of SCK)
- When the Page-Program data is not in 1-byte increments
- If the Write Status Register instruction is input for two bus cycles or more.

6.4 Decoupling Capacitor

A 0.1µF ceramic capacitor must be provided for each device and connected between V_{DD} and V_{SS} to ensure that the device will operate correctly.

6.5 DC Characteristics

TABLE 6-5: DC OPERATING CHARACTERISTICS

Symbol	Parameter	Limits				Test Conditions
		Min	Typ[1]	Max	Units	
I_{DDR}	Read Current			6	mA	CE#=0.1 V_{DD}/0.9 V_{DD}@25 MHz, SO=open; Single I/O
I_{DDR2}	Read Current			10	mA	CE#=0.1 V_{DD}/0.9V_{DD}@30 MHz, SO=open
I_{DDR3}	Read Current			12	mA	CE#=0.1 V_{DD}/0.9V_{DD}@30 MHz, SO=open; Dual I/O;
I_{DDW}	Program and Erase Current			15	mA	CE#=V_{DD}
I_{SB}	Standby Current			50	µA	CE#=V_{DD}, V_{IN}=V_{DD} or V_{SS}
I_{DPD}	Deep Power-Down			10	µA	CE#=V_{DD}, V_{IN}=V_{DD} or V_{SS}
I_{LI}	Input Leakage Current			2	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current			2	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IL}	Input Low Voltage	-0.3		0.3	V	V_{DD}=V_{DD} Min
V_{IH}	Input High Voltage	0.7 V_{DD}		V_{DD}+0.3	V	V_{DD}=V_{DD} Max
V_{OL}	Output Low Voltage			0.2	V	I_{OL}=100 µA, V_{DD}=V_{DD} Min
V_{OH}	Output High Voltage	V_{DD}-0.2			V	I_{OH}=-100 µA, V_{DD}=V_{DD} Min

1. Value characterized, not fully tested in production.

TABLE 6-6: CAPACITANCE (T_A = 25°C, F=1 MHz, OTHER PINS OPEN)

Parameter	Description	Test Condition	Maximum
C_{OUT}[1]	Output Pin Capacitance	V_{OUT} = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 6-7: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	100,000	Cycles	JEDEC Standard A117
	Status Register Write Cycle	100,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	20	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

6.6 AC Characteristics

TABLE 6-8: AC OPERATING CHARACTERISTICS

Symbol	Parameter	Limits - 25 MHz			Limits - 30 MHz			Units
		Min		Max	Min		Max	
F_{CLK}[1]	Serial Clock Frequency			25			30	MHz
T_{SCKH}	Serial Clock High Time	18			15.5			ns
T_{SCKL}	Serial Clock Low Time	18			15.5			ns
T_{SCKR}	Serial Clock Rise Time			5			5	ns
T_{SCKF}	Serial Clock Fall Time			5			5	ns
T_{CES}[2]	CE# Active Setup Time	8			8			ns
T_{CEH}[2]	CE# Active Hold Time	8			8			ns
T_{CHS}[2]	CE# Not Active Setup Time	8			8			ns
T_{CHH}[2]	CE# Not Active Hold Time	8			8			ns
T_{CPH}	CE# High Time	25			25			ns
T_{CHZ}	CE# High to High-Z Output			8			8	ns
T_{CLZ}	SCK Low to Low-Z Output	0			0			ns
T_{DS}	Data In Setup Time	2			2			ns
T_{DH}	Data In Hold Time	5			5			ns
T_{HLS}	HOLD# Low Setup Time	5			5			ns
T_{HHS}	HOLD# High Setup Time	5			5			ns
T_{HLH}	HOLD# Low Hold Time	5			5			ns
T_{HHH}	HOLD# High Hold Time	5			5			ns
T_{HZ}	HOLD# Low to High-Z Output			9			9	ns
T_{LZ}	HOLD# High to Low-Z Output			9			9	ns
T_{OH}	Output Hold from SCK Change	1			1			ns
T_V	Output Valid from SCK			11			11	ns
T_{WPS}	WP# Setup Time	20			20			ns
T_{WPH}	WP# Hold Time	20			20			ns
T_{WRSR}	Status Register Write Time			10			15	ms
T_{DPD}	CE# High to Deep Power-Down			3			3	µs
T_{SBR}	Deep Power-Down (CE# High) to Standby Mode			3			3	µs
T_{SE}	Sector-Erase		40	150		40	150	ms
T_{BE}	Block-Erase		80	250		80	250	ms
T_{CE}	Chip-Erase		0.25	2		0.25	2	s
T_{PP}	Page-Program (256 Byte)		4	5		4	5	ms

1. Maximum clock frequency for Read instruction, 03H, is 25 MHz
2. Relative to SCK

FIGURE 6-3: SERIAL OUTPUT TIMING DIAGRAM

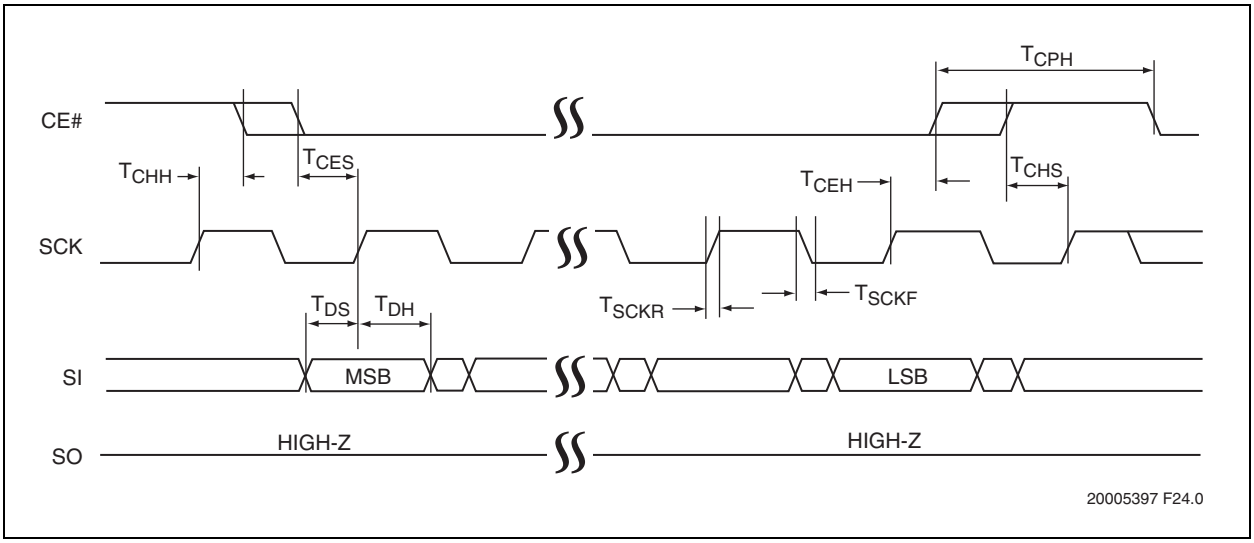


FIGURE 6-4: SERIAL INPUT TIMING DIAGRAM

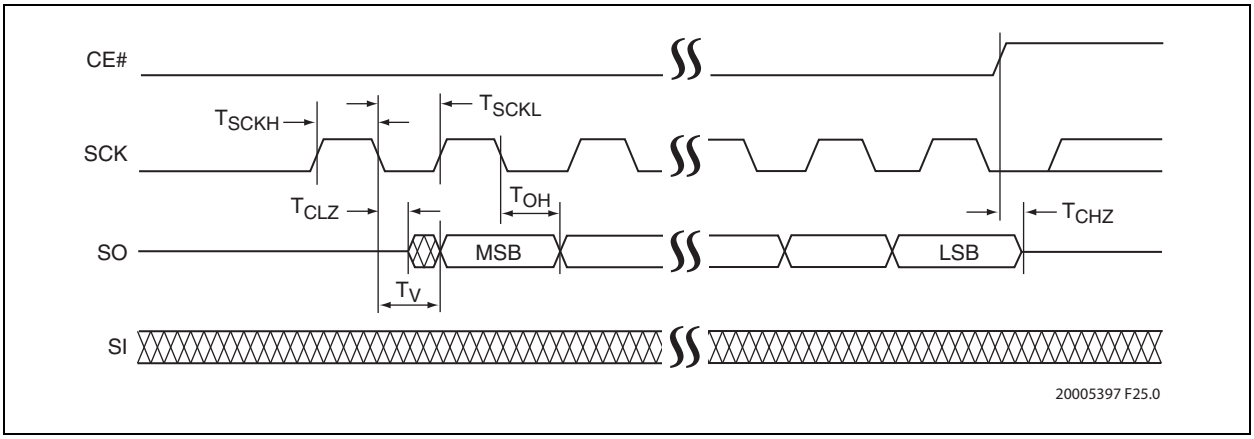


FIGURE 6-5: HOLD TIMING DIAGRAM