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General Description

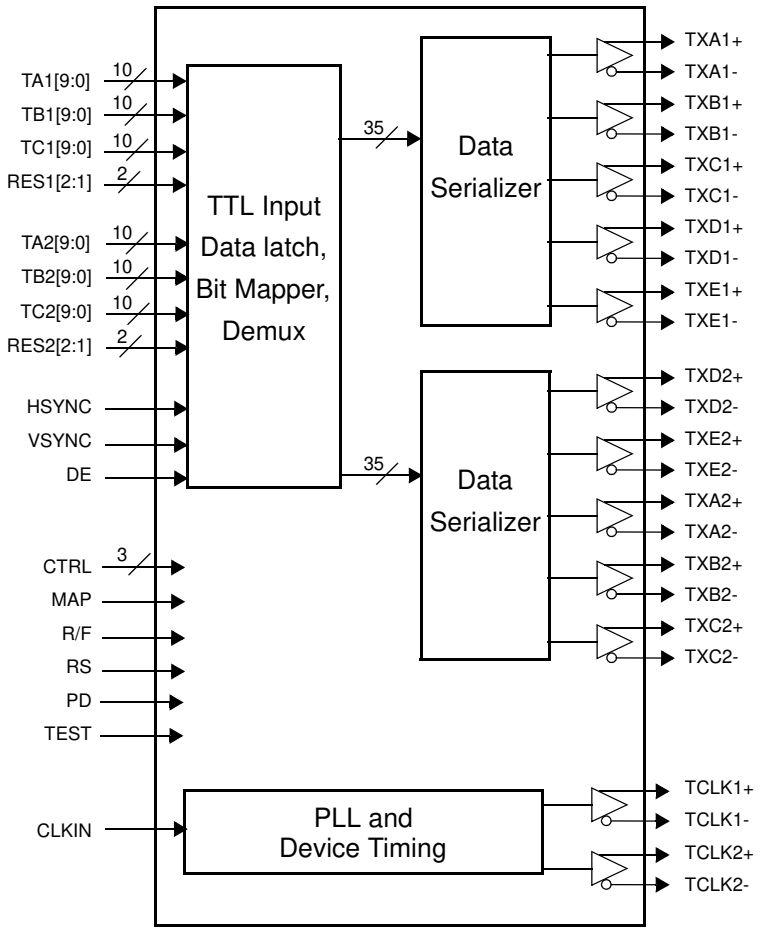
The V105A LVDS display interface transmitter is designed to support pixel data transmission between a video processing engine and a digital video display. The dual channel LVDS output supports pixel rates up to 150 MHz, enabling compatibility with 1080p and WUXGA display resolutions.

Total 67-bit LVCMOS/LVTTL input is provided. The V105A converts the 67 bit parallel input data into two 5-pair LVDS (Low Voltage Differential Signaling) serial data outputs, in odd/even pixel format. Input data can be clocked on the rising or falling edge of the input clock (selectable). In video applications the 35 data bits are normally divided into 10 bits for each R, G and B channel and 5 control bits (which includes VSYNC, HSYNC and DE).

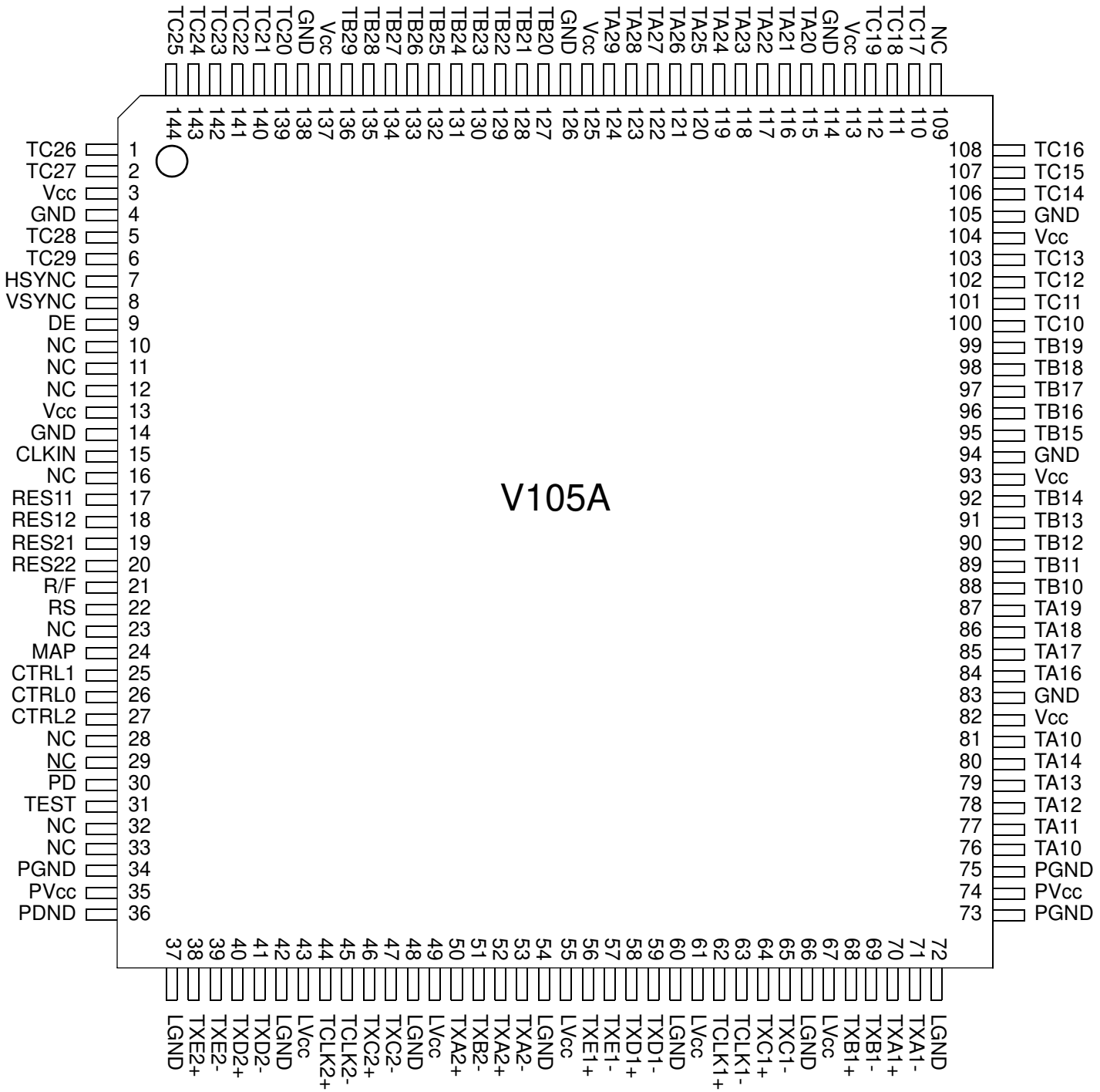
Features

- Dual 32+3-bit LVTTL input supports up to 150 MHz pixel rate.
- Dual pixel, LVDS output supports 150 MHz pixel rate (compatible with 1080p and WUXGA resolution)
- Internal PLL requires no external loop filter
- Selectable rising or falling clock edge for data alignment
- Compatible with Spread Spectrum clock source
- Reduced LVDS output voltage swing mode (selectable) to minimize EMI
- Single 3.3 V supply
- Low power consumption CMOS design
- Power down mode
- Available in 144 pin LQFP package (14x14mm body size)

Block Diagram



Pin Assignment



Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
70, 71	TXA1+, TXA1-	LVDS OUT	LVDS Serial Data Output Pairs, Channel 1
68, 69	TXB1+, TXB1-		
64, 65	TXC1+, TXC1-		
58, 59	TXD1+, TXD1-		
56, 57	TXE1+, TXE1-		
52, 53	TXA2+, TXA2-		LVDS Serial Data Output Pairs, Channel 2
50,51	TXB2+, TXB2-		
46, 47	TXC2+, TXC2-		
40, 41	TXD2+, TXD2-		
38,39	TXE2+, TXE2-		
62, 63	TCLK1+, TCLK1-	LVDS OUT	LVDS Reference Clock Output Pair
44, 45	TCLK2+, TCLK2-		
76, 77, 78, 79, 80, 81, 84, 85, 86, 87	TA10 ~TA19	IN	CMOS/TTL (or small signal) Data Bit Inputs, Channel 1
88, 89, 90, 91, 92, 95, 96, 97, 98, 99	TB10 ~ TB19		
100, 101, 102, 103, 106, 107, 108, 110, 111, 112	TC10 ~TC19		
17, 18	RES11, RES12	IN	Control Input, Channel 1
115, 116,117, 118, 119, 120, 121, 122, 123, 124	TA20 ~ TA29	IN	CMOS/TTL (or small signal) Data Bit Inputs, Channel 2
127, 128, 129, 130, 131, 132, 133, 134, 135, 136	TB20 ~ TB29		
139, 140, 141, 142, 143, 144, 1, 2, 5, 6	TC20 ~ TC29		
19, 20	RES21, RES22	IN	Control Input, Channel 2
7	HSYNC	IN	HSYNC InputI
8	VSYNC	IN	VSYNC Input
9	DE	IN	DE Input
25, 26, 27	CTRL0 ~ CTRL2	IN	MODE Selection
24	MAP	IN	MAP MODE Selection
30	PD	IN	High: Normal device operation Low: Power down; all outputs become high impedance
31	TEST	IN	Reserved: tie to High or Low

Pin Number	Pin Name	Pin Type	Pin Description
22	RS	IN	Voltage level on this pin sets LVDS output swing voltage and data input swing voltage; refer to the table at the bottom of this page.
21	R/F	IN	Input Clock triggering edge select. High: Rising edge; Low: Falling edge.
3, 13,82, 93, 104, 113, 125, 137	V_{CC}	Power	Power supply pins for TTL inputs and digital circuitry
15	CLKIN	IN	Clock Input
4, 14, 83, 94, 105, 114, 126, 138	GND	Ground	Ground pins for TTL inputs and digital circuitry
43, 49, 55, 61, 67	LV_{CC}	Power	Power supply pins for LVDS outputs
37, 42, 48, 54, 60, 66, 72	LGND	Ground	Ground pins for LVDS outputs
35, 74	PV_{CC}	Power	Power supply pins for PLL circuitry
34, 36, 73, 75	PGND	Ground	Ground pins for PLL circuitry
10, 11, 12, 16, 23, 28, 29, 32, 33, 109	NC		Reserved

RS Input Voltage LVDS Output Swing CMOS/TTL Input Configuration (Input Voltage Swing)

RS Input Voltage	LVDS Output Swing	CMOS/TTL Input Configuration (Input Voltage Swing
V_{CC}	350 mV	Standard Input and Output Configuration[1]
0.6 ~ 1.4 V (V_{REF}[1])	350 mV	Small Input Swing, Standard Output Swing Configuration[1]
GND	200 mV	Standard Input Swing, Reduced Output Swing Configuration[1]

1. Refer to DC Electrical Characteristics.

External Components

Decoupling capacitors should be used for all power pins.

Absolute Maximum Ratings

Item	Rating[1]
Supply Voltage, V_{CC}	-0.3 V to +4.0 V
CMOS/TTL Input Voltage	-0.3 V to Vcc+0.3 V
CMOS/TTL Output Voltage	-0.3 V to Vcc+0.3 V
LVDS Driver Output Voltage	-0.3 V to Vcc+0.3 V
Storage Temperature	-55 to +150°C
Junction Temperature	+125°C
LeadTemperature (10 seconds)	+260°C
Maximum Power Dissipation @ 25°C	1.15 W

1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

Recommended Operation Conditions

Symbol	Parameter			Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage			+3	+3.3	+3.6	V
TA	Ambient Operating Temperature			0		+70	°C
CLK	CTRL<1:0> = LL (Dual-in/Dual-out)		Input	20		135	MHz
			LVDS Output	20		135	MHz
	CTRL<1:0> = LH (Dual-in/Single-out)		Input	10		67.5	MHz
			LVDS Output	20		135	MHz
	CTRL<1:0> = HL (Single-in/Dual-out)	Single Edge Input (CTRL<2> = L)	Input	40		150	MHz
			LVDS Output	20		75	MHz
		Double Edge Input (CTRL<2> = H)	Input	20		135	MHz
			LVDS Output	20		135	MHz
	CTRL<1:0> = HH (Single-in/Single-out)	Distribution Off (CTRL<2> = L)	Input	20		135	MHz
			LVDS Output	20		135	MHz
		Distribution On (CTRL<2> = H)	Input	20		135	MHz
			LVDS Output	20		135	MHz

DC Electrical Characteristics

V_{DD}=3.3 V ±10%, Ambient temperature 0 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
CMOS/TTL Inputs, Standard Configuration						
Input High Voltage	V_{IH}	RS=V_{CC} or GND	2.00		V_{CC}	V
Input Low Voltage	V_{IL}	RS=V_{CC} or GND	GND		0.80	V
Input Current	I_{INC}	0V<V_{IN}<V_{CC}			±10	µA
CMOS/TTL Inputs, Small Input Swing Configuration						
Max Input Swing Voltage	V_{CCQ}[1]	V_{REF} = V_{RS} = $V_{CCQ/2}$	1.2		2.8	V
Input Reference Voltage into pin RS	V_{REF}			$V_{CCQ/2}$		V
High Level Input Voltage (for small input swing condition)	V_{SH}[2]	V_{REF}=$V_{CCQ/2}$	$V_{CCQ/2}$ +0.1V			V
Low Level Input Voltage (for small input swing condition)	V_{SL}[2]	V_{REF}=$V_{CCQ/2}$			$V_{CCQ/2}$ -0.1V	V

1. V_{CCQ} voltage defines the max voltage of the small swing input and is not an actual input into the device.
2. Small input swing voltage is applied to TA1[9:0], TB1[9:0], TC1[9:0], RES1[2:1], TA2[9:0],TB2[9:0], TC2[9:0], RES2[2:1], HSYNC, VSYNC, DE, and CLKIN.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
LVDS Transmitter DC Specifications						
Differential Output Voltage, R_L = 100Ω	V_{OD}	Normal swing RS = V_{CC}	250	350	450	mV
		Reduced swing RS = GND	100	200	300	mV
Change in V_{OD} Between Complimentary Output States	DV_{OD}	RL = 100Ω			35	mV
Common Mode Voltage	V_{OC}		1.125	1.250	1.375	V
Change in V_{OC} Between Complimentary Output States	DV_{OC}				35	mV
Output Short Circuit Current	I_{OS}	V_{OUT} = 0V, R_L = 100Ω			-24	mA
Output Tri-State Current	I_{OZ}	$\overline{PD}$ = 0V, V_{OUT} = 0V to V_{CC}			±10	µA

Parameter	Symbol	Conditions			Typ	Max	Units
Supply Current Transmitter Supply Current (worst case pattern)	I_{TCCW}	CLKIN = 65MHz	R_L = 100Ω C_L = 5pF R_S = V_{CC}	CTRL<1:0> = HH Single-in/Single-out CTRL<2> = L Distribution Off		41	mA
		CLKIN = 85MHz				54	mA
		CLKIN = 135MHz				86	mA
		CLKIN = 65MHz		CTRL<1:0> = HH Single-in/Single-out CTRL<2> = H Distribution On		68	mA
		CLKIN = 85MHz				89	mA
		CLKIN = 135MHz				141	mA
		CLKIN = 65MHz		CTRL<1:0> = HL Single-in/Dual-out CTRL<2> = L DDR Input Off		37	mA
		CLKIN = 85MHz				38	mA
		CLKIN = 135MHz				77	mA
		CLKIN = 150MHz				85	mA
		CLKIN = 65MHz		CTRL<1:0> = HL Single-in/Dual-out CTRL<2> = L DDR Input On		54	mA
		CLKIN = 85MHz				71	mA
		CLKIN = 135MHz				113	mA
		CLKIN = 32.5MHz		CTRL<1:0> = LH Dual-in/Single-out		35	mA
		CLKIN = 42.5MHz				46	mA
		CLKIN = 67.5MHz				73	mA
		CLKIN = 65MHz		CTRL<1:0> = LL Dual-in/Dual-out		80	mA
		CLKIN = 85MHz				104	mA
		CLKIN = 135MHz				164	mA
Transmitter Power Down Supply Current	I_{TCCS}	$\overline{PDWN}$ = L, All Inputs = Fixed L or H				10	µA

AC Electrical Characteristics

V_{DD}=3.3 V ±10%, Ambient temperature 0 to +70°C, Mode=135 MHz

Parameter	Symbol	Min.	Typ.	Max.	Units
Switching Characteristics					
CLK IN Transition Time	t_{TCIT}			1.0	ns
CLK IN Period	t_{TCP}	6.7		100.0	ns
CLK IN High Time[1]	t_{TCH}	2.59	3.7	4.81	ns
CLK IN Low Time[1]	t_{TCL}	2.59	3.7	4.81	ns
CLK IN to TCLK± Delay	t_{TCD}		22.2		ns
TTL Data Setup to CLK IN	t_{TS}	2.5			ns
TTL Data Hold from CLK IN	t_{TH}	0			ns
LVDS Transition Time	t_{LVT}		0.6	1.5	ns
Output Data Position0	t_{TOP1}	-0.2	0.0	0.2	ns
Output Data Position1	t_{TOP0}	0.907	1.057	1.207	ns
Output Data Position2	t_{TOP6}	1.814	2.114	2.414	ns
Output Data Position3	t_{TOP5}	2.721	3.171	3.621	ns
Output Data Position4	t_{TOP4}	3.628	4.228	4.828	ns
Output Data Position5	t_{TOP3}	4.535	5.285	6.035	ns
Output Data Position6	t_{TOP2}	5.442	6.342	7.242	ns
Phase Lock Loop Set	t_{TPLL}			10.0	ms

1. See figure 1.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θJ_A	Still air		53		°C/W
	θJ_A	1 m/s air flow		40		°C/W
	θJ_A	3 m/s air flow		33		°C/W
Thermal Resistance Junction to Case	θJ_C			8		°C/W

AC Timing Diagrams

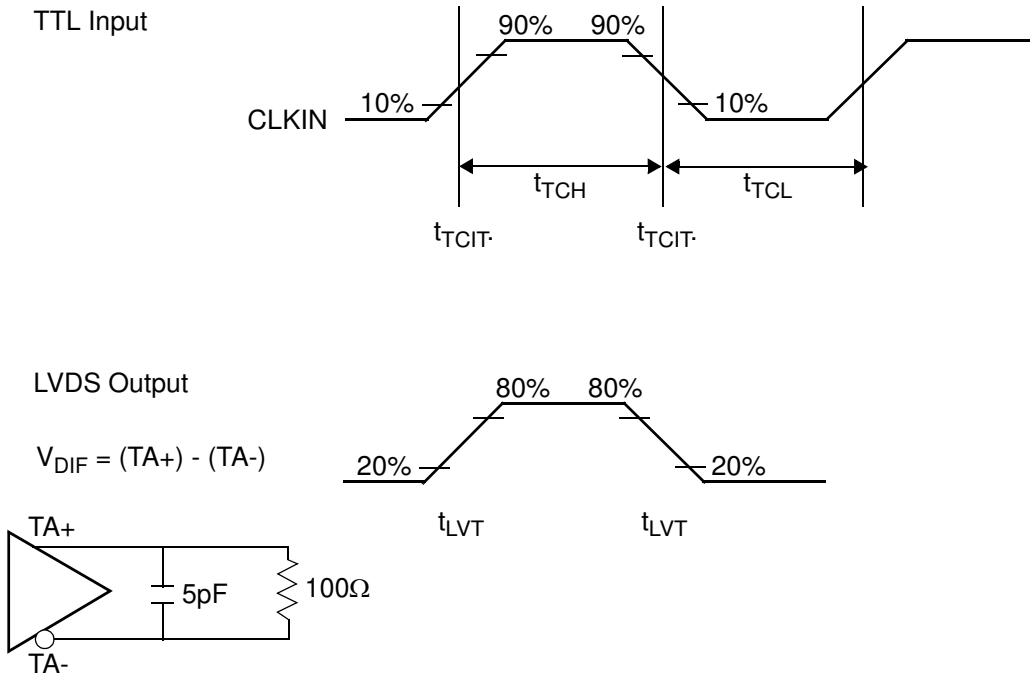
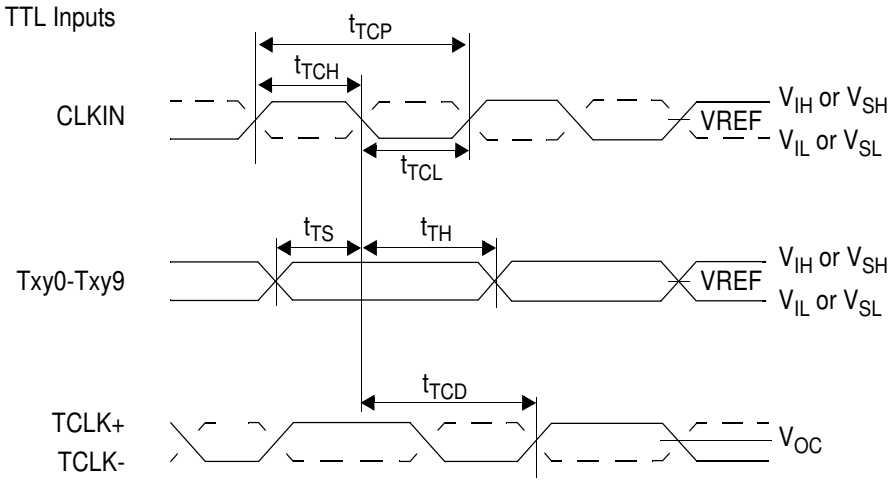


Figure 1.



NOTE: CLKIN for R/F = GND, solid line
CLKIN for R/F = VCC, dashed line

Figure 2.

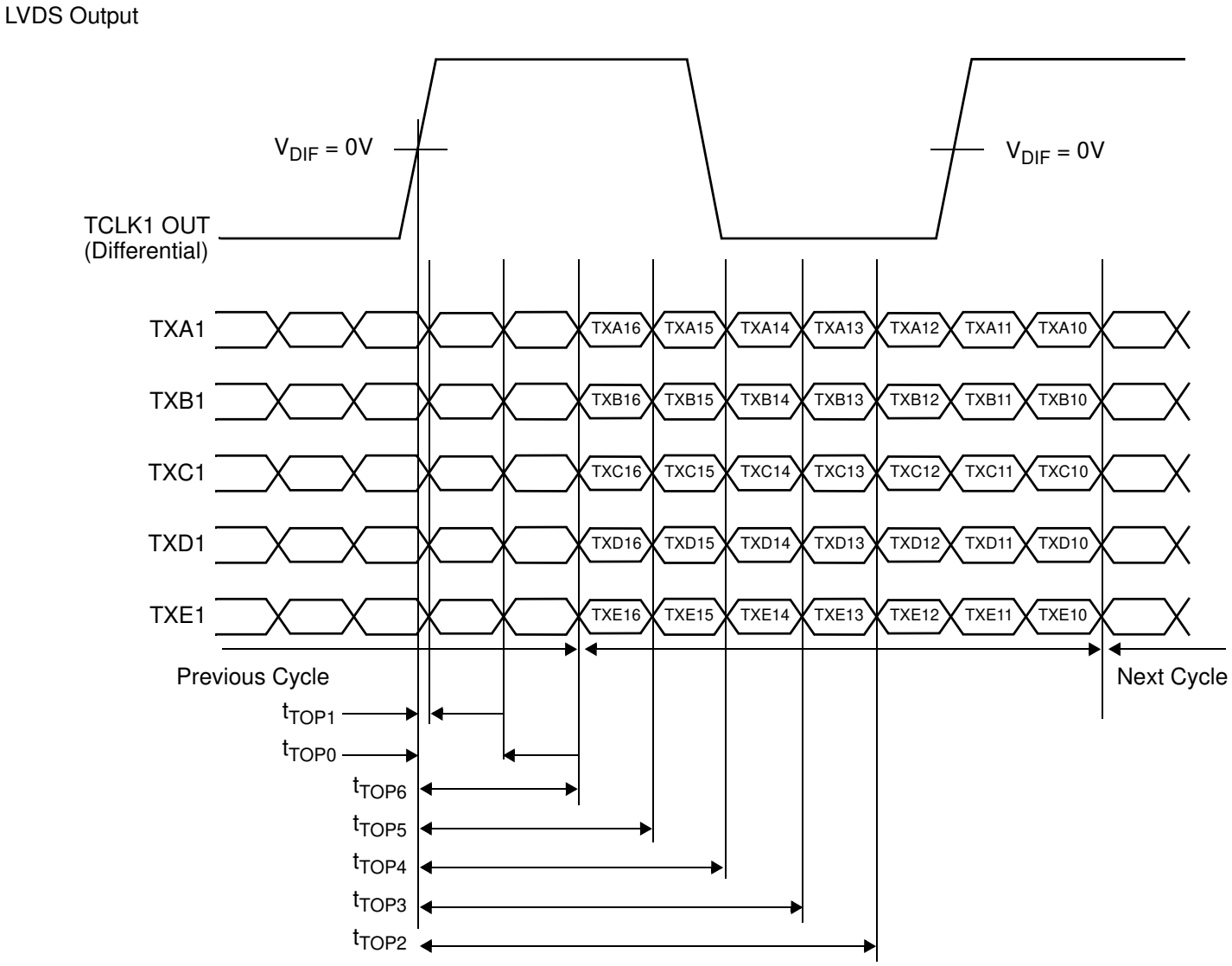

LVDS Output
V_{DIF} = 0V
V_{DIF} = 0V
TCLK1 OUT
(Differential)
TXA1
TXA16 TXA15 TXA14 TXA13 TXA12 TXA11 TXA10
TXB1
TXB16 TXB15 TXB14 TXB13 TXB12 TXB11 TXB10
TXC1
TXC16 TXC15 TXC14 TXC13 TXC12 TXC11 TXC10
TXD1
TXD16 TXD15 TXD14 TXD13 TXD12 TXD11 TXD10
TXE1
TXE16 TXE15 TXE14 TXE13 TXE12 TXE11 TXE10
Previous Cycle
Next Cycle
t_{TOP1}
t_{TOP0}
t_{TOP6}
t_{TOP5}
t_{TOP4}
t_{TOP3}
t_{TOP2}

Figure 3.

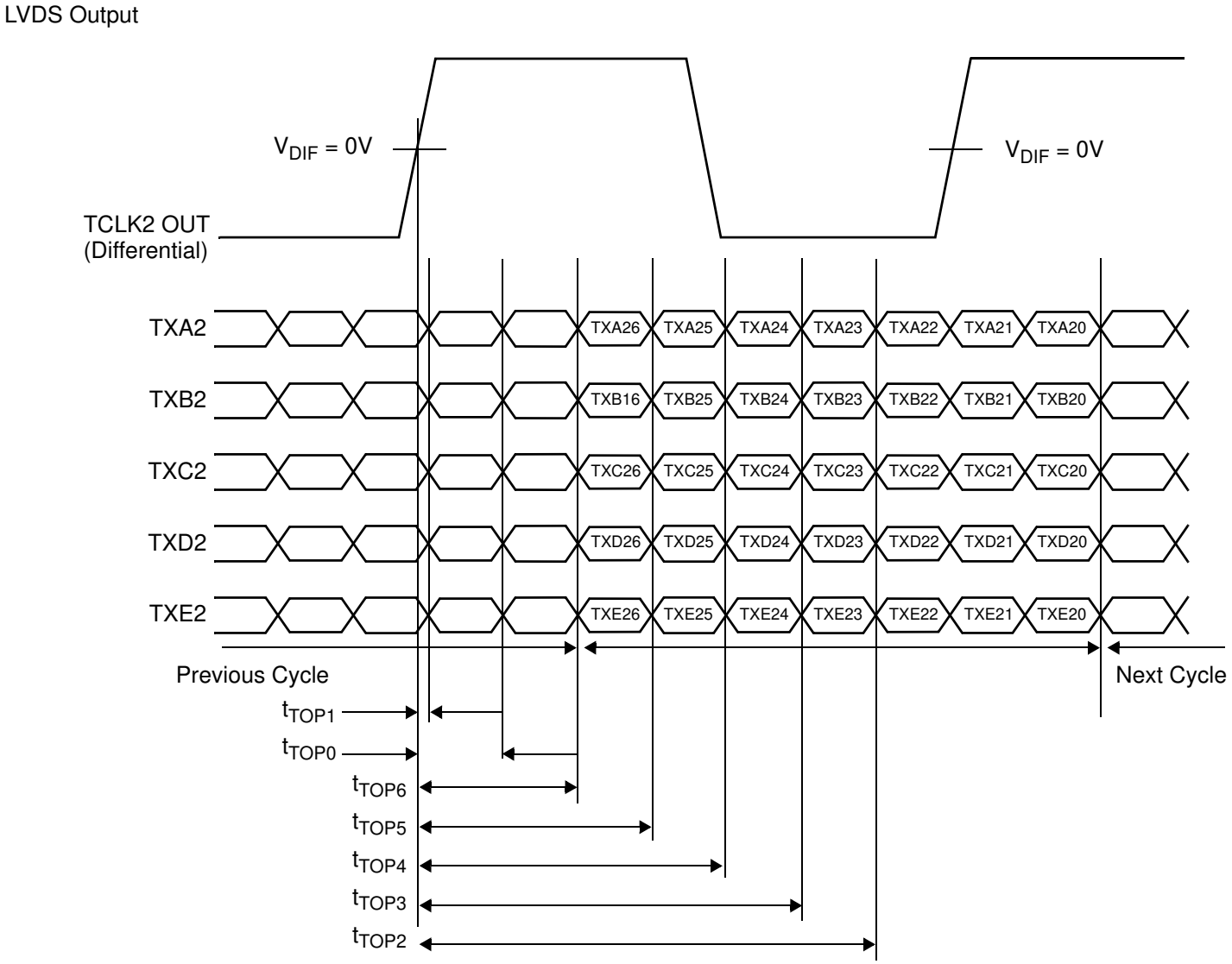

LVDS Output
V_{DIF} = 0V
V_{DIF} = 0V
TCLK2 OUT
(Differential)
TXA2
TXA26 TXA25 TXA24 TXA23 TXA22 TXA21 TXA20
TXB2
TXB16 TXB25 TXB24 TXB23 TXB22 TXB21 TXB20
TXC2
TXC26 TXC25 TXC24 TXC23 TXC22 TXC21 TXC20
TXD2
TXD26 TXD25 TXD24 TXD23 TXD22 TXD21 TXD20
TXE2
TXE26 TXE25 TXE24 TXE23 TXE22 TXE21 TXE20
Previous Cycle
Next Cycle
t_{TOP1}
t_{TOP0}
t_{TOP6}
t_{TOP5}
t_{TOP4}
t_{TOP3}
t_{TOP2}

Figure 4.

Phase Lock Loop Time

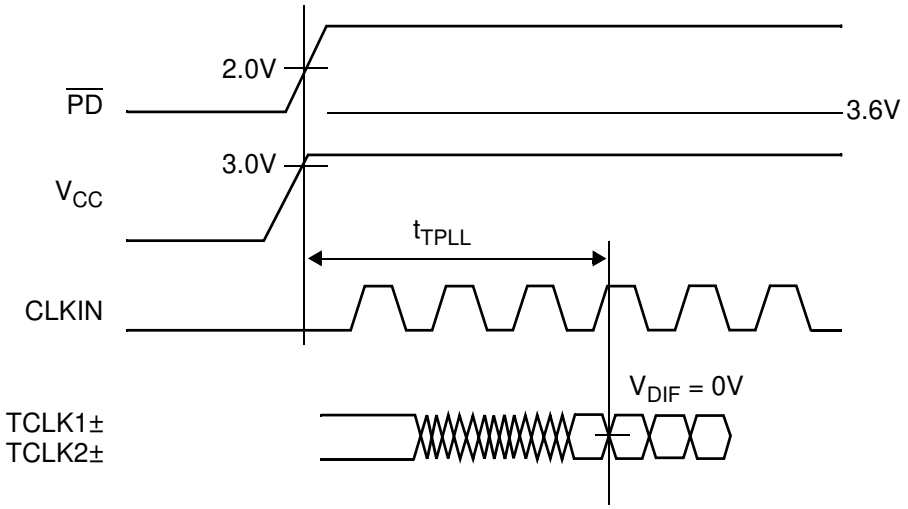
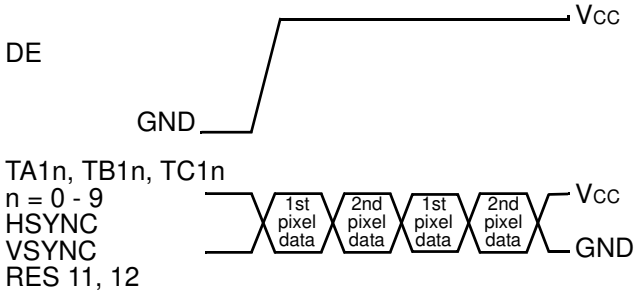


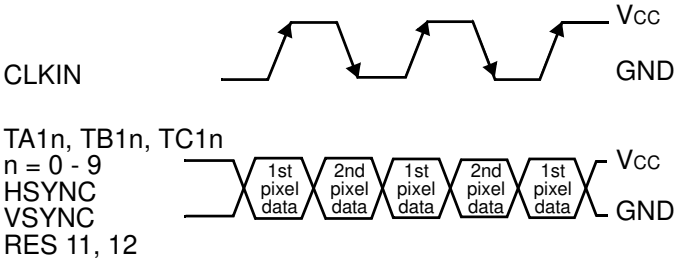
Figure 5.

LVDS Output Data Mapping

Single-In, Dual-Out (DDR Off); MODE<2:0> = LHL



Single-In, Dual-Out (DDR On) CTRL<2:0> = HHL



NOTE: CTRL2 = H (Double Edge Input)
CLKIN for R/F = VCC, solid line
CLKIN for R/F = GND, dashed line

Figure 6.

Single-in/ Single-out Distribution Off: CTRL<2:0> = LHH

LVDS Output Data	MAP = 1	MAP = 0
TXA1[0]	TA14	TA12
TXA1[1]	TA15	TA13
TXA1[2]	TA16	TA14
TXA1[3]	TA17	TA15
TXA1[4]	TA18	TA16
TXA1[5]	TA19	TA17
TXA1[6]	TB14	TB12
TXB1[0]	TB15	TB13
TXB1[1]	TB16	TB14
TXB1[2]	TB17	TB15
TXB1[3]	TB18	TB16
TXB1[4]	TB19	TB17
TXB1[5]	TC14	TC12
TXB1[6]	TC15	TC13
TXC1[0]	TC16	TC14
TXC1[1]	TC17	TC15
TXC1[2]	TC18	TC16
TXC1[3]	TC19	TC17
TXC1[4]	HSYNC	HSYNC
TXC1[5]	VSYNC	VSYNC
TXC1[6]	DE	DE
TXD1[0]	TA12	TA18
TXD1[1]	TA13	TA19
TXD1[2]	TB12	TB18
TXD1[3]	TB13	TB19
TXD1[4]	TC12	TC18
TXD1[5]	TC13	TC19
TXD1[6]	RES11	RES11
TXE1[0]	TA10	TA10
TXE1[1]	TA11	TA11
TXE1[2]	TB10	TB10
TXE1[3]	TB11	TB11
TXE1[4]	TC10	TC10
TXE1[5]	TC11	TC11
TXE1[6]	RES12	RES12

Single-in/ Single-out Distribution On: CTRL<2:0> = HHH

First Link			Second Link		
LVDS Output Data	**MAP = 1**	**MAP = 0**	**LVDS Output Data**	**MAP = 1**	**MAP = 0**
TXA1[0]	TA14	TA12	TXA2[0]	TA14	TA12
TXA1[1]	TA15	TA13	TXA2[1]	TA15	TA13
TXA1[2]	TA16	TA14	TXA2[2]	TA16	TA14
TXA1[3]	TA17	TA15	TXA2[3]	TA17	TA15
TXA1[4]	TA18	TA16	TXA2[4]	TA18	TA16
TXA1[5]	TA19	TA17	TXA2[5]	TA19	TA17
TXA1[6]	TB14	TB12	TXA2[6]	TB14	TB12
TXB1[0]	TB15	TB13	TXB2[0]	TB15	TB13
TXB1[1]	TB16	TB14	TXB2[1]	TB16	TB14
TXB1[2]	TB17	TB15	TXB2[2]	TB17	TB15
TXB1[3]	TB18	TB16	TXB2[3]	TB18	TB16
TXB1[4]	TB19	TB17	TXB2[4]	TB19	TB17
TXB1[5]	TC14	TC12	TXB2[5]	TC14	TC12
TXB1[6]	TC15	TC13	TXB2[6]	TC15	TC13
TXC1[0]	TC16	TC14	TXC2[0]	TC16	TC14
TXC1[1]	TC17	TC15	TXC2[1]	TC17	TC15
TXC1[2]	TC18	TC16	TXC2[2]	TC18	TC16
TXC1[3]	TC19	TC17	TXC2[3]	TC19	TC17
TXC1[4]	HSYNC	HSYNC	TXC2[4]	HSYNC	HSYNC
TXC1[5]	VSYNC	VSYNC	TXC2[5]	VSYNC	VSYNC
TXC1[6]	DE	DE	TXC2[6]	DE	DE
TXD1[0	TA12	TA18	TXD2[0]	TA12	TA18
TXD1[1]	TA13	TA19	TXD2[1]	TA13	TA19
TXD1[2]	TB12	TB18	TXD2[2]	TB12	TB18
TXD1[3]	TB13	TB19	TXD2[3]	TB13	TB19
TXD1[4]	TC12	TC18	TXD2[4]	TC12	TC18
TXD1[5]	TC13	TC19	TXD2[5]	TC13	TC19
TXD1[6]	RES11	RES11	TXD2[6]	RES11	RES11
TXE1[0]	TA10	TA10	TXE2[0]	TA10	TA10
TXE1[1]	TA11	TA11	TXE2[1]	TA11	TA11
TXE1[2]	TB10	TB10	TXE2[2]	TB10	TB10
TXE1[3]	TB11	TB11	TXE2[3]	TB11	TB11
TXE1[4]	TC10	TC10	TXE2[4]	TC10	TC10
TXE1[5]	TC11	TC11	TXE2[5]	TC11	TC11
TXE1[6]	RES12	RES12	TXE2[6]	RES12	RES12

Single-in/ Dual-out DDR On or OFF: CTRL<2:0> = HHL or LHL

First Pixel Data			Second Pixel Data		
LVDS Output Data	**MAP = 1**	**MAP = 0**	**LVDS Output Data**	**MAP = 1**	**MAP = 0**
TXA1[0]	TA14	TA12	TXA2[0]	TA14	TA12
TXA1[1]	TA15	TA13	TXA2[1]	TA15	TA13
TXA1[2]	TA16	TA14	TXA2[2]	TA16	TA14
TXA1[3]	TA17	TA15	TXA2[3]	TA17	TA15
TXA1[4]	TA18	TA16	TXA2[4]	TA18	TA16
TXA1[5]	TA19	TA17	TXA2[5]	TA19	TA17
TXA1[6]	TB14	TB12	TXA2[6]	TB14	TB12
TXB1[0]	TB15	TB13	TXB2[0]	TB15	TB13
TXB1[1]	TB16	TB14	TXB2[1]	TB16	TB14
TXB1[2]	TB17	TB15	TXB2[2]	TB17	TB15
TXB1[3]	TB18	TB16	TXB2[3]	TB18	TB16
TXB1[4]	TB19	TB17	TXB2[4]	TB19	TB17
TXB1[5]	TC14	TC12	TXB2[5]	TC14	TC12
TXB1[6]	TC15	TC13	TXB2[6]	TC15	TC13
TXC1[0]	TC16	TC14	TXC2[0]	TC16	TC14
TXC1[1]	TC17	TC15	TXC2[1]	TC17	TC15
TXC1[2]	TC18	TC16	TXC2[2]	TC18	TC16
TXC1[3]	TC19	TC17	TXC2[3]	TC19	TC17
TXC1[4]	HSYNC	HSYNC	TXC2[4]	HSYNC	HSYNC
TXC1[5]	VSYNC	VSYNC	TXC2[5]	VSYNC	VSYNC
TXC1[6]	DE	DE	TXC2[6]	DE	DE
TXD1[0	TA12	TA18	TXD2[0]	TA12	TA18
TXD1[1]	TA13	TA19	TXD2[1]	TA13	TA19
TXD1[2]	TB12	TB18	TXD2[2]	TB12	TB18
TXD1[3]	TB13	TB19	TXD2[3]	TB13	TB19
TXD1[4]	TC12	TC18	TXD2[4]	TC12	TC18
TXD1[5]	TC13	TC19	TXD2[5]	TC13	TC19
TXD1[6]	RES11	RES11	TXD2[6]	RES11	RES11
TXE1[0]	TA10	TA10	TXE2[0]	TA10	TA10
TXE1[1]	TA11	TA11	TXE2[1]	TA11	TA11
TXE1[2]	TB10	TB10	TXE2[2]	TB10	TB10
TXE1[3]	TB11	TB11	TXE2[3]	TB11	TB11
TXE1[4]	TC10	TC10	TXE2[4]	TC10	TC10
TXE1[5]	TC11	TC11	TXE2[5]	TC11	TC11
TXE1[6]	RES12	RES12	TXE2[6]	RES12	RES12

Dual-in/ Single-out: CTRL<2:0> = HLH or LLH

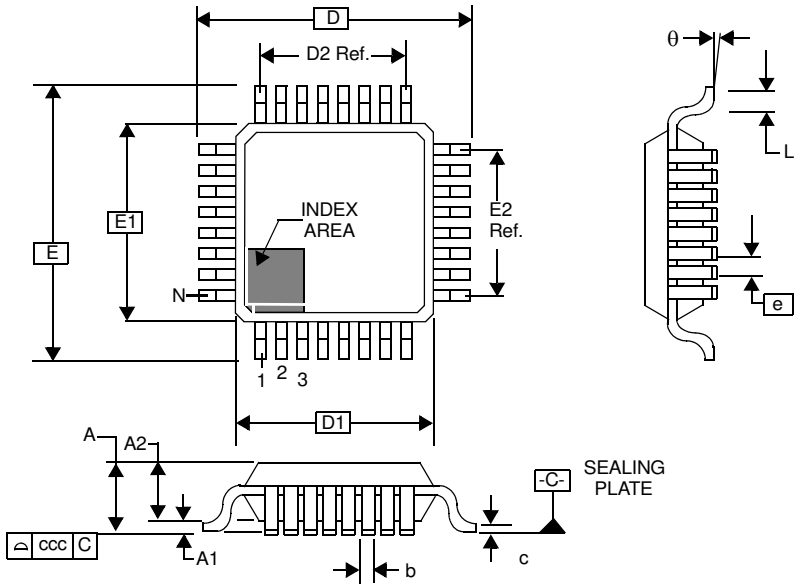
First Pixel Data			Second Pixel Data		
LVDS Output Data	**MAP = 1**	**MAP = 0**	**LVDS Output Data**	**MAP = 1**	**MAP = 0**
TXA1[0](n)	TA14	TA12	TXA1[0](n+1)	TA24	TA22
TXA1[1](n)	TA15	TA13	TXA1[1](n+1)	TA25	TA23
TXA1[2](n)	TA16	TA14	TXA1[2(]n+1)	TA26	TA24
TXA1[3](n)	TA17	TA15	TXA1[3](n+1)	TA27	TA25
TXA1[4](n)	TA18	TA16	TXA1[4](n+1)	TA28	TA26
TXA1[5](n)	TA19	TA17	TXA1[5](n+1)	TA29	TA27
TXA1[6](n)	TB14	TB12	TXA1[6](n+1)	TB24	TB22
TXB1[0](n)	TB15	TB13	TXB1[0](n+1)	TB25	TB23
TXB1[1](n)	TB16	TB14	TXB1[1](n+1)	TB26	TB24
TXB1[2](n)	TB17	TB15	TXB1[2](n+1)	TB27	TB25
TXB1[3](n)	TB18	TB16	TXB1[3](n+1)	TB28	TB26
TXB1[4](n)	TB19	TB17	TXB1[4](n+1)	TB29	TB27
TXB1[5](n)	TC14	TC12	TXB1[5](n+1)	TC24	TC22
TXB1[6](n)	TC15	TC13	TXB1[6](n+1)	TC25	TC23
TXC1[0](n)	TC16	TC14	TXC1[0](n+1)	TC26	TC24
TXC1[1](n)	TC17	TC15	TXC1[1](n+1)	TC27	TC25
TXC1[2](n)	TC18	TC16	TXC1[2](n+1)	TC28	TC26
TXC1[3](n)	TC19	TC17	TXC1[3](n+1)	TC29	TC27
TXC1[4](n)	HSYNC	HSYNC	TXC1[4](n+1)	HSYNC	HSYNC
TXC1[5](n)	VSYNC	VSYNC	TXC1[5](n+1)	VSYNC	VSYNC
TXC1[6](n)	DE	DE	TXC1[6](n+1)	DE	DE
TXD1[0](n)	TA12	TA18	TXD1[0](n+1)	TA22	TA28
TXD1[1](n)	TA13	TA19	TXD1[1](n+1)	TA23	TA29
TXD1[2](n)	TB12	TB18	TXD1[2](n+1)	TB22	TB28
TXD1[3](n)	TB13	TB19	TXD1[3](n+1)	TB23	TB29
TXD1[4](n)	TC12	TC18	TXD1[4](n+1)	TC22	TC28
TXD1[5](n)	TC13	TC19	TXD1[5](n+1)	TC23	TC29
TXD1[6](n)	RES11	RES11	TXD1[6](n+1)	RES21	RES21
TXE1[0](n)	TA10	TA10	TXE1[0](n+1)	TA20	TA20
TXE1[1](n)	TA11	TA11	TXE1[1](n+1)	TA21	TA21
TXE1[2](n)	TB10	TB10	TXE1[2](n+1)	TB20	TB20
TXE1[3](n)	TB11	TB11	TXE1[3](n+1)	TB21	TB21
TXE1[4](n)	TC10	TC10	TXE1[4](n+1)	TC20	TC20
TXE1[5](n)	TC11	TC11	TXE1[5](n+1)	TC21	TC21
TXE1[6](n)	RES12	RES12	TXE1[6](n+1)	RES22	RES22

Dual-in/ Dual-out: CTRL<2:0> = HLL or LLL

First Pixel Data			Second Pixel Data		
LVDS Output Data	**MAP = 1**	**MAP = 0**	**LVDS Output Data**	**MAP = 1**	**MAP = 0**
TXA1[0]	TA14	TA12	TXA2[0]	TA24	TA22
TXA1[1]	TA15	TA13	TXA2[1]	TA25	TA23
TXA1[2]	TA16	TA14	TXA2[2]	TA26	TA24
TXA1[3]	TA17	TA15	TXA2[3]	TA27	TA25
TXA1[4]	TA18	TA16	TXA2[4]	TA28	TA26
TXA1[5]	TA19	TA17	TXA2[5]	TA29	TA27
TXA1[6]	TB14	TB12	TXA2[6]	TB24	TB22
TXB1[0]	TB15	TB13	TXB2[0]	TB25	TB23
TXB1[1]	TB16	TB14	TXB2[1]	TB26	TB24
TXB1[2]	TB17	TB15	TXB2[2]	TB27	TB25
TXB1[3]	TB18	TB16	TXB2[3]	TB28	TB26
TXB1[4]	TB19	TB17	TXB2[4]	TB29	TB27
TXB1[5]	TC14	TC12	TXB2[5]	TC24	TC22
TXB1[6]	TC15	TC13	TXB2[6]	TC25	TC23
TXC1[0]	TC16	TC14	TXC2[0]	TC26	TC24
TXC1[1]	TC17	TC15	TXC2[1]	TC27	TC25
TXC1[2]	TC18	TC16	TXC2[2]	TC28	TC26
TXC1[3]	TC19	TC17	TXC2[3]	TC29	TC27
TXC1[4]	HSYNC	HSYNC	TXC2[4]	HSYNC	HSYNC
TXC1[5]	VSYNC	VSYNC	TXC2[5]	VSYNC	VSYNC
TXC1[6]	DE	DE	TXC2[6]	DE	DE
TXD1[0	TA12	TA18	TXD2[0]	TA22	TA28
TXD1[1]	TA13	TA19	TXD2[1]	TA23	TA29
TXD1[2]	TB12	TB18	TXD2[2]	TB22	TB28
TXD1[3]	TB13	TB19	TXD2[3]	TB23	TB29
TXD1[4]	TC12	TC18	TXD2[4]	TC22	TC28
TXD1[5]	TC13	TC19	TXD2[5]	TC23	TC29
TXD1[6]	RES11	RES11	TXD2[6]	RES21	RES21
TXE1[0]	TA10	TA10	TXE2[0]	TA20	TA20
TXE1[1]	TA11	TA11	TXE2[1]	TA21	TA21
TXE1[2]	TB10	TB10	TXE2[2]	TB20	TB20
TXE1[3]	TB11	TB11	TXE2[3]	TB21	TB21
TXE1[4]	TC10	TC10	TXE2[4]	TC20	TC20
TXE1[5]	TC11	TC11	TXE2[5]	TC21	TC21
TXE1[6]	RES12	RES12	TXE2[6]	RES22	RES22

Package Outline and Package Dimensions (144-pin LQFP)

Package dimensions are kept current with JEDEC Publication No. 95, variation ACD.

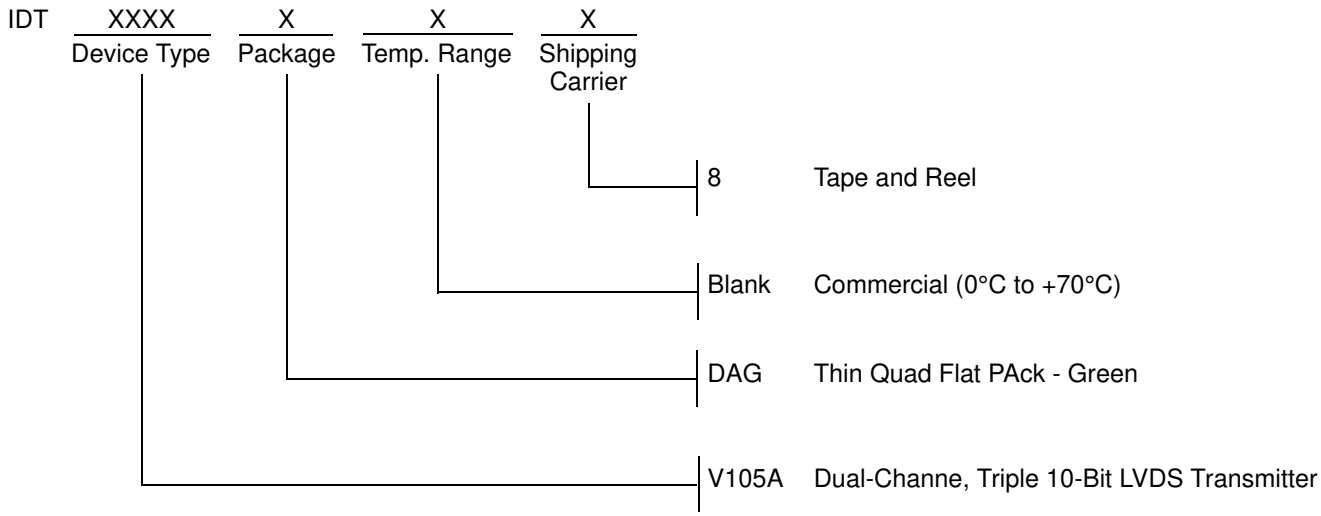


ALL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches[1] COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
N	144		144	
A	—	1.60	—	.063
A1	0.05	0.15	.002	.006
A2	1.35	1.45	.053	.057
b	0.17	0.27	.007	.011
c	0.09	0.20	.004	.008
D	22.00 BASIC		.866 BASIC	
D1	20.00 BASIC		.787 BASIC	
D2	17.50 Ref.		.689 Ref.	
E	22.00 BASIC		.866 BASIC	
E1	20.00 BASIC		.787 BASIC	
E2	17.50 Ref.		.689 Ref.	
e	0.50 BASIC		.02 BASIC	
L	0.45	0.75	.018	.03
q	0°	7°	0°	7°
ccc	—	0.08	—	.003

1. For reference only. Controlling dimensions are in mm.

Ordering Information



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