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VINCULUM

BINDING USB TECHNOLOGIES

Future Technology Devices International Ltd.

V2-EVAL

Vinculum II Evaluation Board

Datasheet

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Table of Contents

1 Introduction

The following document details the features and specifications of the V2-EVAL board. The V2-EVAL is a hardware platform designed to support easy evaluation of FTDI's Vinculum-II (VNC2) series of embedded USB host controller devices.

The V2-Eval kit includes the following hardware items as standard

- 1 x V2-Eval base board.
- 1 x 5V/1A mains adapter PSU – UK, US, European and Japanese versions available.
- 1 x USB A/B cable to connect to a host PC in programming / terminal emulation or debugging modes.
- 1 x USB gender changer for USB slave mode applications.

NOTE:

The V2-EVAL kit requires a VNC2 based daughterboard module to be installed into the V2-EVAL base board socket site, in order to enable development with the kit.

Daughterboard modules are sold separately, with 3 versions available for 32-pin, 48-pin and 64-pin package devices. Daughterboard modules can be purchased from FTDI or via our website http://www.ftdichip.com.

Before you proceed:
Please check that all the contents of the package are not damaged.

Ensure that your kit includes a proper version of the power supply, depending on the region where you live. Eval application software and project examples can be downloaded from: http://www.ftdichip.com

1.1 Handling the board

Static discharge precaution – Without proper anti-static handling the board can be damaged. Therefore, take anti-static precautions while handling the board.

1.2 Environmental requirements

The V2-Eval Board must be stored between -40°C and 80°C. The recommended operating temperature is between 0°C and 55°C

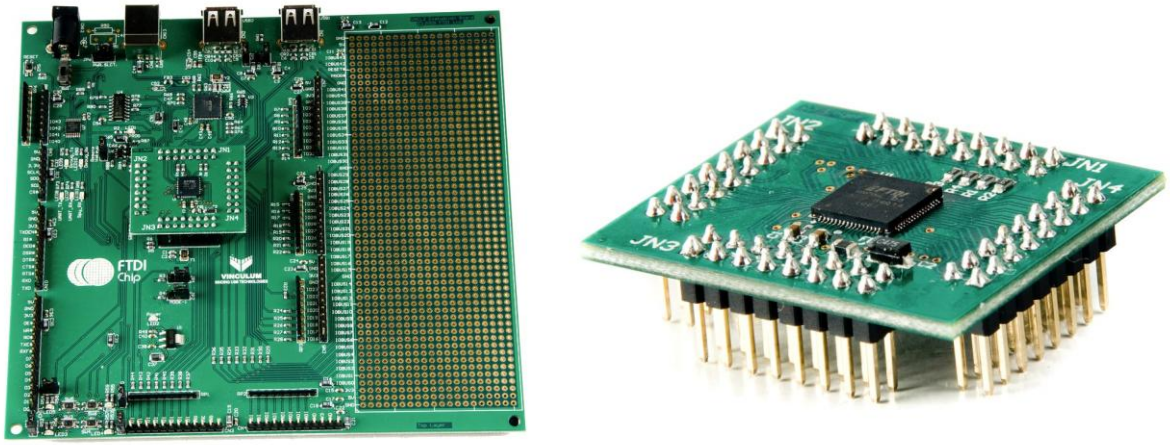

Figure 1.1 - V2-EVAL Motherboard(left) with Daughterboard Module(right)

1.3 Part Numbers

Part Number	Description
V2-EVAL	V2-EVAL kit with base board, power supply and cables.
V2-EVAL-EXT32	VNC2 daughterboard module with 32-pin QFN VNC2 device for use with V2-EVAL.
V2-EVAL-EXT48	VNC2 daughterboard module with 48-pin QFN VNC2 device for use with V2-EVAL.
V2-EVAL-EXT64	VNC2 daughterboard module with 64-pin QFN VNC2 device for use with V2-EVAL.

Table 1.0 Part Numbers

1.4 References

The document contains references to the following websites and documents. Links to most documents are available from the FTDI website, http://www.ftdichip.com.

Document Name	Description
1. FT_000138	Vinculum-II Embedded Dual USB Host Controller IC Data Sheet.
2. FT_000060	FT4232H Data Sheet.
3. AN_137	Vinculum-II IO Cell Description.
4. AN_138	Vinculum-II Debug Interface Description.
5. AN_139	Vinculum-II IO Mux Explained.
6. AN_140	Vinculum-II PWM Example.
7. FT_000006	Vinculum Firmware User Manual.
8. USB 2.0	Universal Serial Bus Specification Revision 2.0 USB Implementers Forum http://www.usb.org.

Table 1.1 Document References

1.5 Acronyms and Abbreviations

Terms	Description
FIFO	First In First Out.
GPIO	General Purpose Input Output.
I/O	Input / Output.
MISO	Master In Slave Out.
MOSI	Master Out Slave In.
SPI	Serial Peripheral Interface.
UART	Universal Asynchronous Receiver/Transmitter.
USB	Universal Serial Bus.
VNC2	Vinculum-II.

Table 1.2 Acronyms and Abbreviations

2 Board Description

V2-Eval Board is intended for use as a hardware platform to enable easy evaluation of FTDI's Vinculum-II VNC2 series of embedded USB Host / Slave controllers. The V2-Eval Board includes all the necessary components required by a user to begin developing USB Host / Slave system applications based on the VNC2 device.

2.1 V2-EVAL Board Features

- VNC2 – Embedded USB Host / Slave chip accessible via daughterboard.
- Selection of VNC2 daughterboards to support 32-pin, 48-pin and 64-pin QFN packages.
- Two USB type A connectors for connecting to USB slave peripherals.
- VNC2 IO port connectors grouped by port name/or function.
- FT42232H –USB to quad channel UART device for VNC2 programming & debug functions.
- One USB type B connector for connection to PC host via FT4232H.
- 4 User-programmable LEDs.
- 4 User-programmable push button switches.

2.2 Specifications

- Board supply voltage: 4.75V … 5.25V.
- Board supply current: 60mA (with no USB devices on USB1 or USB2 port).
- IO connectors power output: 5V/150mA, 3.3V/150mA.
- Base board dimensions: 167mm x 156mm x 1.5mm (L x W x H).
- VNC2 daughterboard dimensions: 37.9mm x 32.48mm x 10.0mm (L x W x H).

3 V2-Eval Board Components and Interfaces

This chapter describes the operational and connectivity information for the V2-Eval board major components and interfaces.

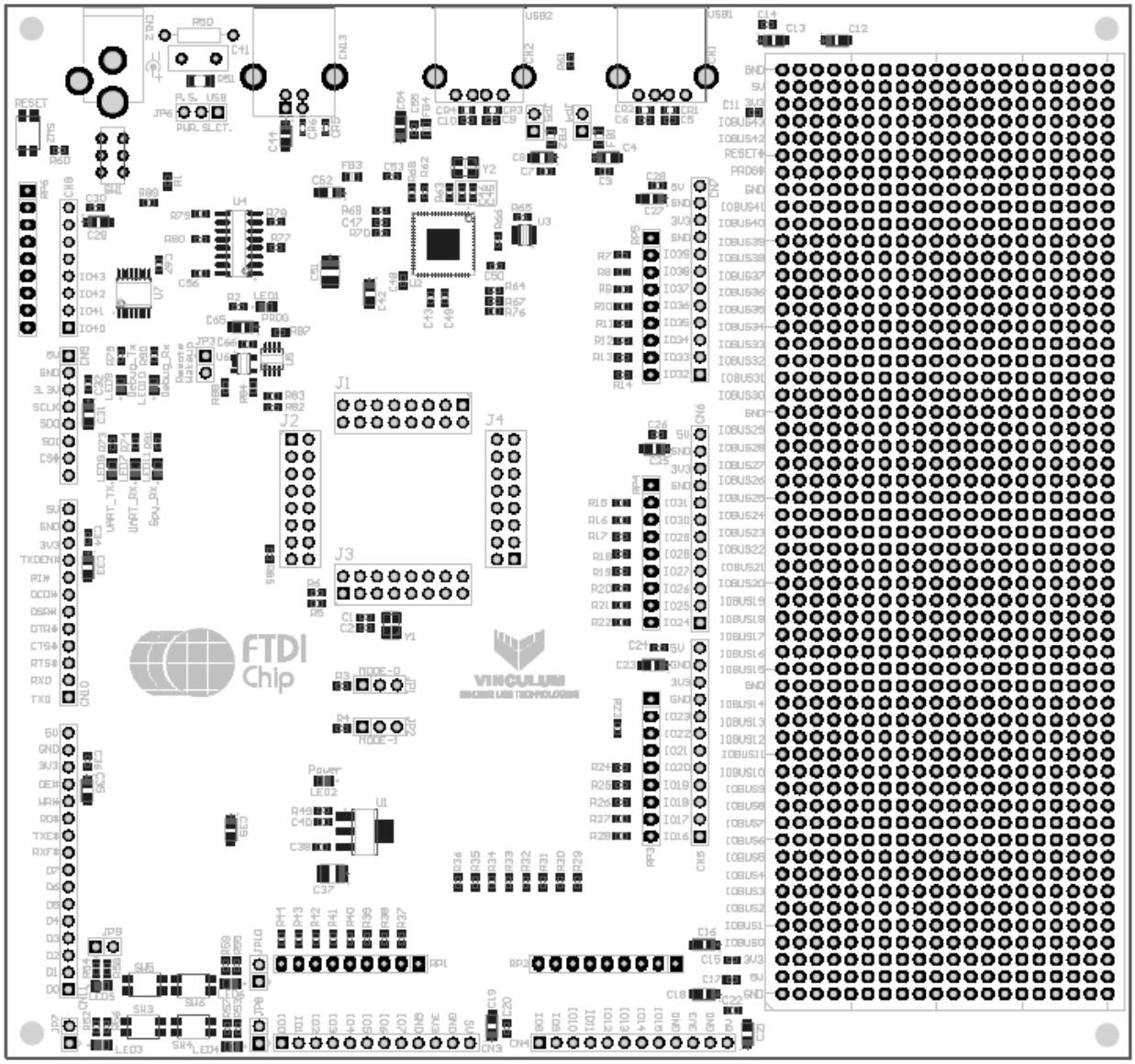

Figure 3.1 V2-EVAL Board Layout

3.1 Block Diagram

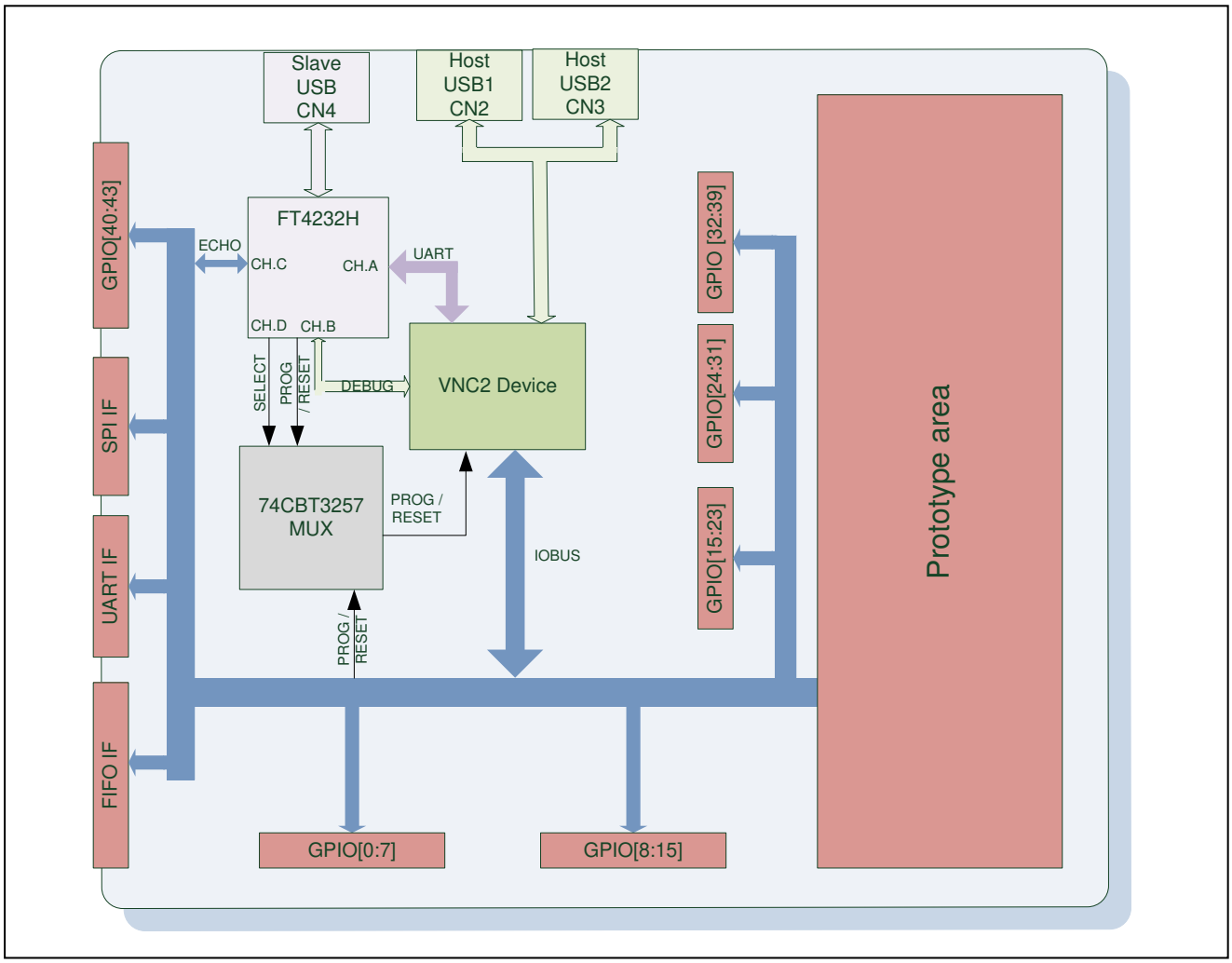

Figure 3.2 V2-EVAL Board Block Diagram

3.1.1 Components.

Component	Board designator	Description
USB-UART bridge	U2	FT4232H USB ⇔ Quad UART/FIFO device.
Configuration memory	U3	9356 Serial SPI EEPROM for FT4232H configuration data.
IO multiplexer	U4	74CBT3257 4-bit, 1to2, FET Multiplexer/Demultiplexer.
3.3V regulator	U1	AIC1735-33 Ultra low dropout 3.3V voltage regulator.
Dual port buffer	U5	SN74LVC2G125 dual port buffer used to convert bi-directional debug signal into separate TX and RX signals.
Inverter	U6	SN74LVC1G14 inverter device used to invert the TXDEN output from FT4232H to control output enable signal for dual port buffer.
12MHz crystal	Y2	12MHz crystal for FT4232H.
Single 5V DC power supply	CN12	Board adapter for included 5V DC power supply.
Power switch	SW1	Power On/Off switch.
Power source select	JP6	Power source selection jumper.
Reset button	SW2	Push-button switch for manual reset of VNC2 device.
Keyboard	SW3-SW6	Four user push-button switches.
User LEDs	LED3-LED6	Four green user LEDs.
PROG LED	LED1	Red LED.
Power LED	LED2	Green LED.
UART RX LED	LED7	Green LED.
UART TX LED	LED8	Red LED.
Debug TX	LED9	Red LED.
Debug RX	LED10	Green LED.
SPI_RX	LED11	Green LED.
LEDs enable jumpers	JP7-JP10	Enable/disable user-defined LEDs.
GPIO I/O Jumpers	JP1, JP2	GPIO I/O jumpers .
REMOTE WAKEUP	JP3	VNC2 remote wakeup jumper.
VBUS jumpers	JP4, JP5	USB1, USB2 power bus enable jumpers.

Table 3.1 V2-Eval Board Components

3.1.2 Interfaces.

Component	Board designator	Description
USB1, USB2 (1)	CN1, CN2	VNC2 USB host ports 1&2.
USB Type B	CN13	FT4232H USB Slave connection.
VNC2 Socket	J1 -J4	Daughterboard connectors for VNC2 Daughterboard.
SPI (2)	CN9	VNC2 SPI interface pins.
UART (2)	CN10	VNC2 UART interface pins.
FIFO (2)	CN11	VNC2 FIFO interface pins.
IOBUS[7..0] (2)	CN3	VNC2 IOBUS [7:0] port pins.
IOBUS[8..15] (2)	CN4	VNC2 IOBUS [8:15] port pins.
IOBUS[16..23] (2)	CN5	VNC2 IOBUS [16:23] port pins.
IOBUS[24..31] (2)	CN6	VNC2 IOBUS [24:31] port pins.
IOBUS[32..39] (2)	CN7	VNC2 IOBUS [32:39] port pins.
IOBUS[40..43] (2)	CN8	VNC2 IOBUS [40:43] port pins.
Prototyping area (2)	P1	All of VNC2 IO ports and PROG#, RESET# pins are brought on to this area.

Notes

(1) Gender changer required when ports are configured as slave ports by VNC2 firmware, to enable connection to a USB host port.

(2) Those pins are shared between different areas and connectors on the board. You can use only one device at time connected to those pins.

Table 3.2 V2-Eval Board Interfaces

4 Initial Board Set-up & Test

4.1 Installing VNC2 Daughterboard

Prior to first powering the board, users must ensure that the daughterboard module hosting the VNC2 chip is correctly installed on to the main V2-Eval board. The V2-Eval board has 4 socket connectors, J1-J4, onto which the VNC2 daughterboard module is installed.

On the VNC2 daughterboard module, connector JN1 connects to corresponding socket J1, JN2 connects to socket J2, JN3 connects to socket J3 and JN4 connects to J4 on the V2-Eval board.

Warning!

Please check that the VNC2 daughterboard module is correctly installed onto the V2-Eval board prior to power-up. Incorrect installation can cause the VNC2 to not function.

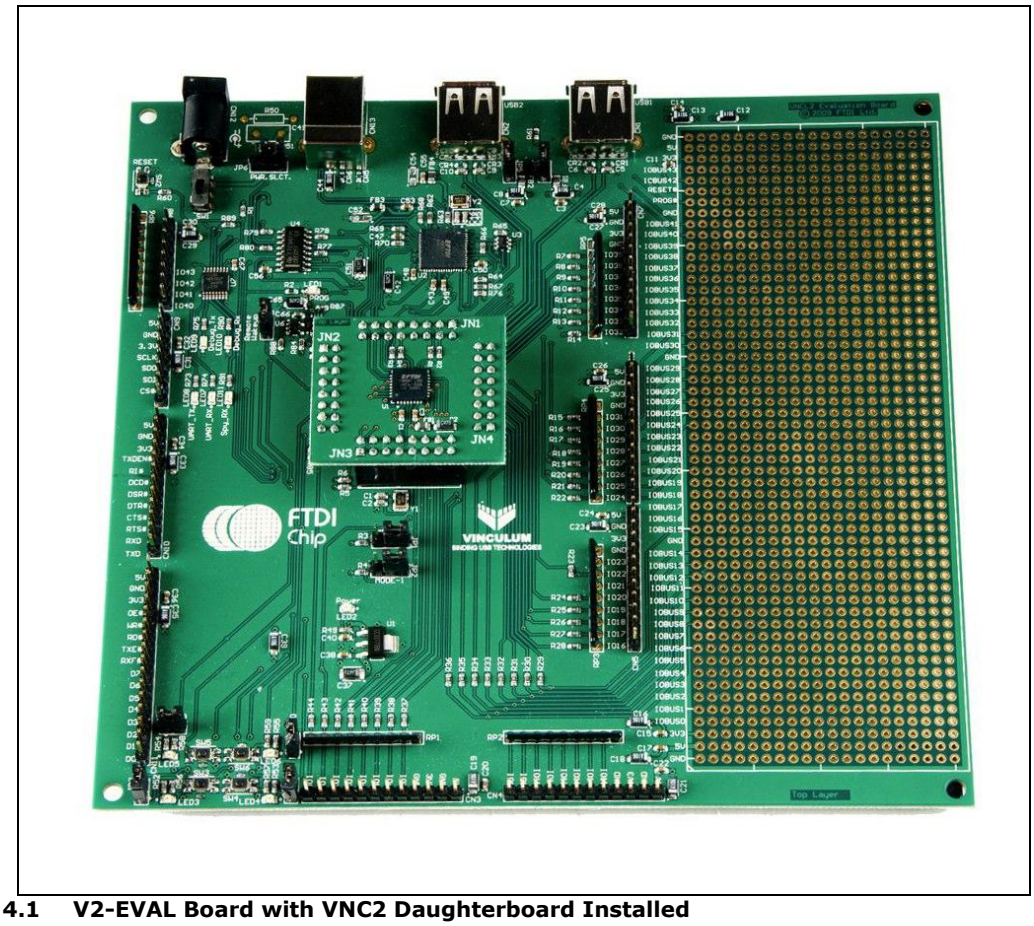

Figure 4.1 V2-EVAL Board with VNC2 Daughterboard Installed

4.2 Testing the board.

Ensure that the Power Select jumper JP6 is in 'P.S.' position (pins 2 & 3 shorted), to enable the board to be powered from the external power adapter.

Connect the 5V DC/1A power supply included in V2-Eval Kit to the external input power adapter connector (CN12), connect USB A/B cable to USB B connector (CN13) on V2-Eval Board and to a free USB port on host PC. Switch SW1 to the ON position (towards board edge). LED2 – POWER should now be on.

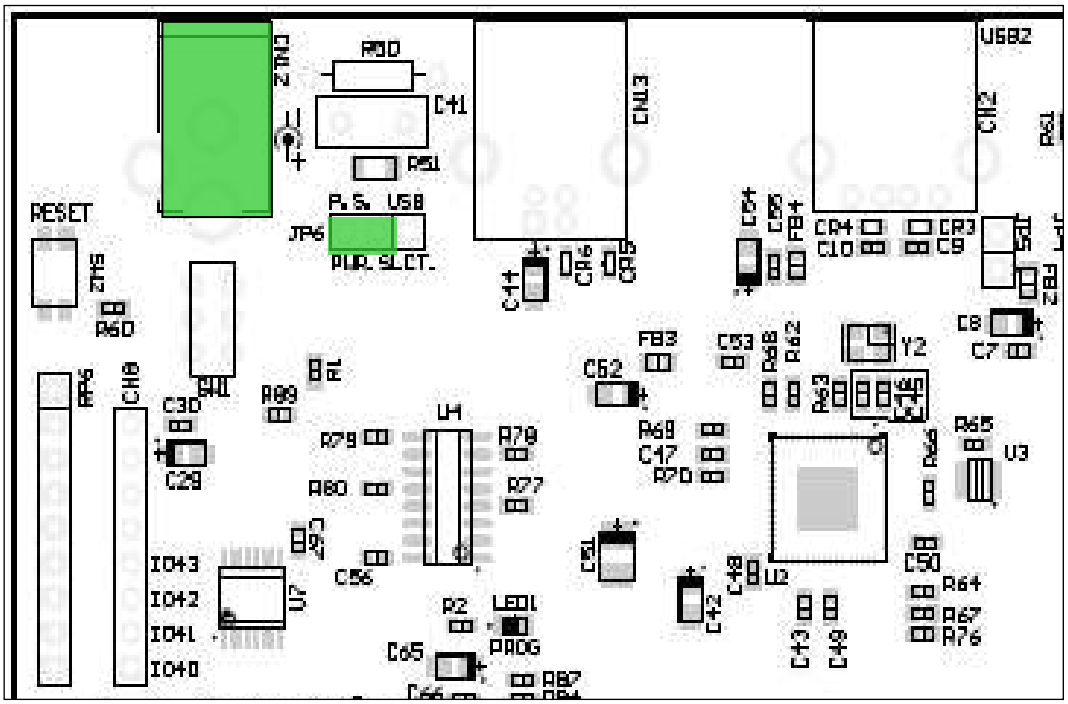

Figure 4.2 Power connector with Jumper JP6

The PCB circuitry will draw power either directly from the board 5V supply or from a 3.3V regulator that is powered by this 5V supply. This includes the VNC2 daughterboard module that is installed on the board. Upon power up, the power LED (LED2) will illuminate.

5 Detailed Description of Board Components.

5.1 Power Select Jumper JP6.

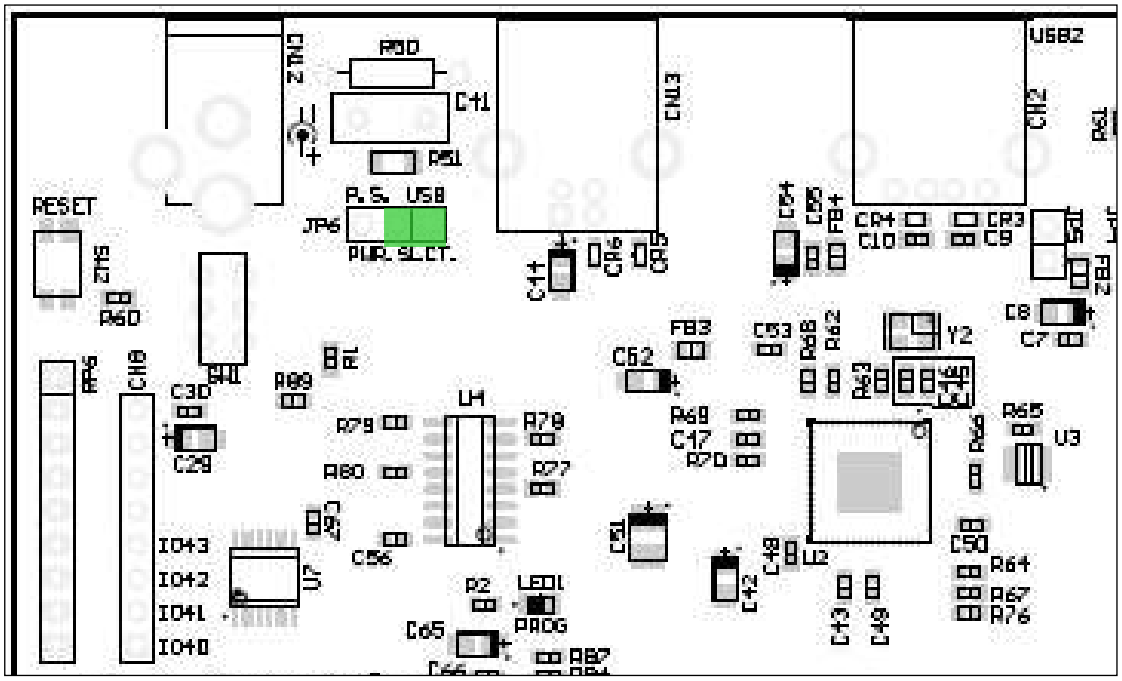

Figure 5.1 Power Select Jumper Configuration for USB Power

V2-Eval Board can draw its power either from the external 5V/1A DC Power Supply or from the USB interface when connected to a USB host via the B type connector (CN13). To enable USB power supply feature, switch the jumper JP6 to USB position, pins 1&2 shorted (pin 1 has a rectangle shaped pad on the bottom side of the board).

Warning!

Please remember that every device connected to the PC through USB port can draw NO MORE than 500mA from the USB host PC 5V power bus.

5.2 GPIO BUS Connectors

The V2-EVAL board features a set of 6 connectors providing access to GPIO capable pins on the VNC2 device. The GPIO pins are distributed across 6 connectors. The configuration of each connector is outlined in subsequent sections. Further each connector has a 5V and 3.3V power and GND pins.

5.2.1 GPIO [0:7] Connector CN3

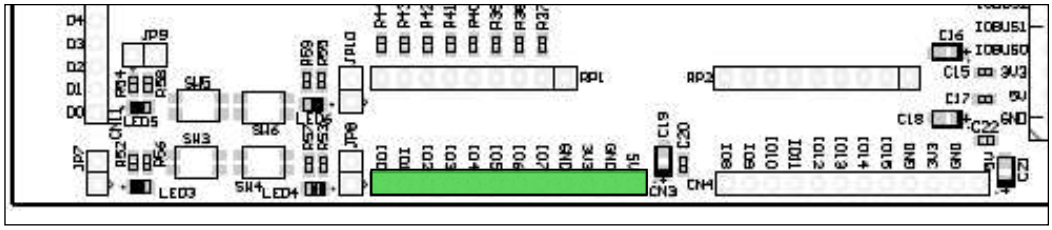

Figure 5.2 GPIO[0:7] Connector CN3

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
GPIO0 (3)	1	11	11	11	IO	GPIO data bit 0
GPIO1 (3)	2	12	12	12	IO	GPIO data bit 1
GPIO2 (3)	3	14	13	13	IO	GPIO data bit 2
GPIO3 (3)	4	15	14	14	IO	GPIO port, data bit 3
GPIO4 (3)	5	-	-	15	IO	GPIO port, data bit 4
GPIO5 (3)	6	-	-	16	IO	GPIO port, data bit 5
GPIO6 (3)	7	-	-	17	IO	GPIO port, data bit 6
GPIO7 (3)	8	-	-	18	IO	GPIO port, data bit 7
GND	9	-	-	-	-	Ground pin
3.3V(4)	10	-	-	-	-	3.3V power rail.
GND	11	-	-	-	-	Ground pin
5V(5)	12	-	-	-	-	5V power rail.

Notes:

(3) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels.
The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(4) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(5) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

Table 5.1 GPIO[0:7] port connector CN3

5.2.2 GPIO [8:15] Connector CN4

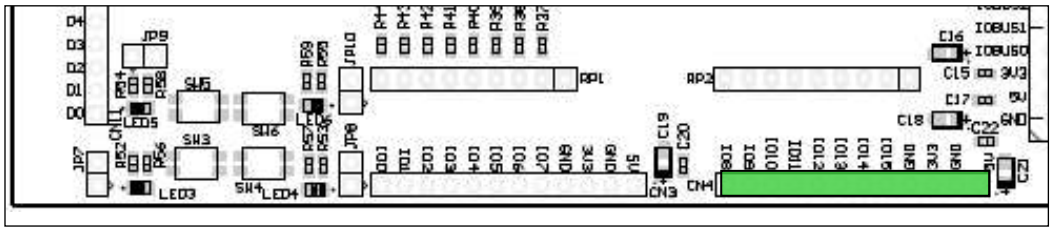

Figure 5.3 GPIO[8:15] Connector CN4

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
GPIO8 (6)	1	-	-	19	IO	GPIO port, data bit 8
GPIO9 (6)	2	-	-	20	IO	GPIO port, data bit 9
GPIO10 (6)	3	-	-	22	IO	GPIO port, data bit 10
GPIO11 (6)	4	-	-	23	IO	GPIO port, data bit11
GPIO12 (6)	5	-	-	24	IO	GPIO port, data bit 12
GPIO13 (6)	6	-	-	25	IO	GPIO port, data bit 13
GPIO14 (6)	7	-	-	26	IO	GPIO port, data bit 14
GPIO15 (6)	8	-	-	27	IO	GPIO port, data bit 15
GND	9	-	-	-	-	Ground pin
3.3V(7)	10	-	-	-	-	3.3V power rail.
GND	11	-	-	-	-	Ground pin
5V(8)	12	-	-	-	-	5V power rail.

Notes:

(6) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels.
The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(7) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(8) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

Table 5.2 GPIO[8:15] connector CN4

5.2.3 GPIO [16:23] Connector CN5

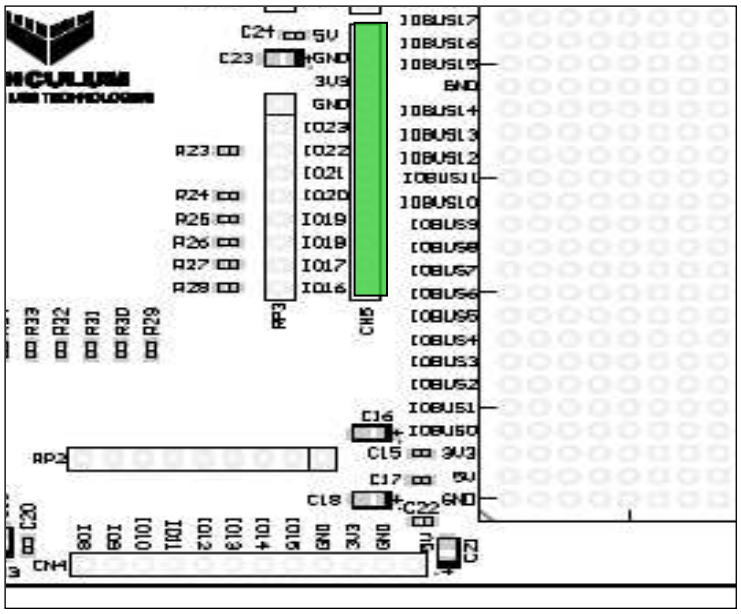

Figure 5.4 GPIO[16:23] Connector CN5

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
GPIO16 (9)	1	-	-	27	IO	GPIO port, data bit 16
GPIO17 (9)	2	-	46	28	IO	GPIO port, data bit 17
GPIO18 (9)	3	-	45	29	IO	GPIO port, data bit 18
GPIO19 (9)	4	-	48	31	IO	GPIO port, data bit19
GPIO20 (9)	5	23	31	32	IO	GPIO port, data bit 20
GPIO21 (9)	6	24(10)	32(10)	39	IO	GPIO port, data bit 21
GPIO22 (9)	7	25	33	40	IO	GPIO port, data bit 22
GPIO23 (9)	8	26(10)	34 (10)	41	IO	GPIO port, data bit 23
GND	9	-	-	-	-	Ground pin
3.3V(11)	10	-	-	-	-	3.3V power rail.
GND	11	-	-	-	-	Ground pin
5V(12)	12	-	-	-	-	5V power rail.

Notes:

(9) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels.
The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(10) The following pins are only accessible on VNC2 when the onboard multiplexer select input is high. See section 6.4 for details.

(11) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(12) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

Table 5.3 GPIO port connector CN5

5.2.4 GPIO [24:31] Connector CN6

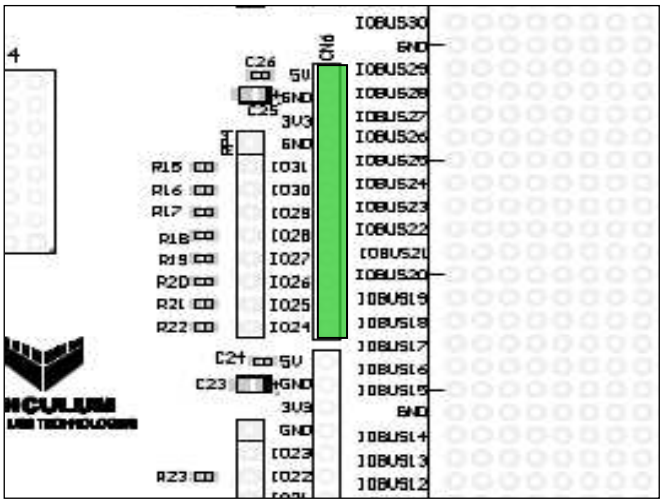

Figure 5.5 GPIO[24:31] Connector CN6

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
GPIO24 (13)	1	-	35	43	IO	GPIO port, data bit 24
GPIO25 (13)	2	-	36	44	IO	GPIO port, data bit 25
GPIO26 (13)	3	-	37	45	IO	GPIO port, data bit 26
GPIO27 (13)	4	-	38	46	IO	GPIO port, data bit 27
GPIO28 (13)	5	-	41	47	IO	GPIO port, data bit 28
GPIO29 (13)	6	-	42	48	IO	GPIO port, data bit 29
GPIO30 (13)	7	-	43	49	IO	GPIO port, data bit 30
GPIO31 (13)	8	-	44	50	IO	GPIO port, data bit 31
GND	9	-	-	-	-	Ground pin
3.3V(14)	10		-	-	-	3.3V power rail.
GND	11		-	-	-	Ground pin
5V(15)	12		-	-	-	5V power rail.

Notes:

(13) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels.
The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(14) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(15) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from power supply and no more than 50mA when the board is powered from USB bus.

Table 5.4 GPIO port connector CN6

5.2.5 GPIO [32:39] Connector CN7

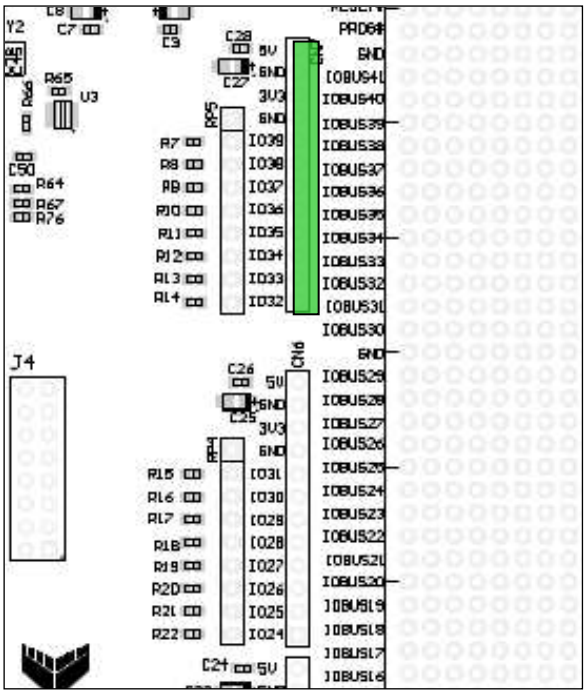

Figure 5.6 GPIO[32:39] Connector CN7

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
GPIO32 (16)	1	29	15	51	IO	GPIO port, data bit 32
GPIO33 (16)	2	30	16	52	IO	GPIO port, data bit 33
GPIO34 (16)	3	31	18	55	IO	GPIO port, data bit 34
GPIO35 (16)	4	32	19	56	IO	GPIO port, data bit 35
GPIO36 (16)	5	-	-	57	IO	GPIO port, data bit 36
GPIO37 (16)	6	-	-	58	IO	GPIO port, data bit 37
GPIO38 (16)	7	-	-	59	IO	GPIO port, data bit 38
GPIO39 (16)	8	-	-	60	IO	GPIO port, data bit 39
GND	9	-	-	-	-	Ground pin
3.3V(17)	10	-	-	-	-	3.3V power rail.
GND	11	-	-	-	-	Ground pin
5V(18)	12	-	-	-	-	5V power rail.

Notes:

(16) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels. The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(17) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(18) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from power supply and no more than 50mA when the board is powered from USB power bus.

Table 5.5 GPIO port connector CN7

5.2.6 GPIO [40:43] Connector CN8

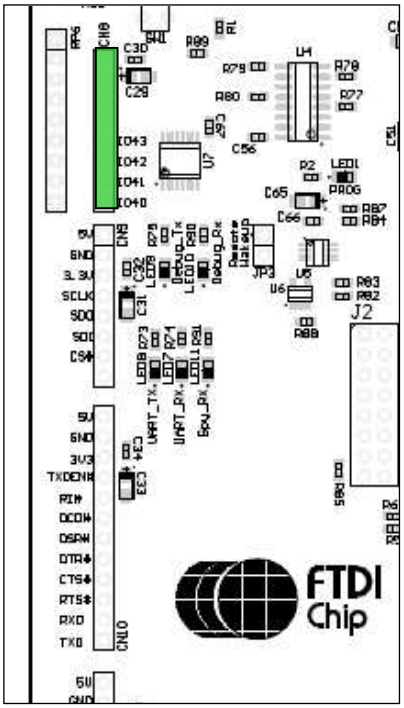

Figure 5.7 GPIO[32:39] Connector CN8

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
GPIO40 (19)	1	-	20	61	IO	GPIO port, data bit 40
GPIO41 (19)	2	-	21	62	IO	GPIO port, data bit 41
GPIO42 (19)	3	-	22	63	IO	GPIO port, data bit 42
GPIO43 (19)	4	-	23	64	IO	GPIO port, data bit 43
GND	5	-	-	-	-	Ground pin
3.3V(20)	6	-	-	-	-	3.3V power rail.
GND	7	-	-	-	-	Ground pin
5V(21)	8	-	-	-	-	5V power rail.

Notes:

(19) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels. The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(20) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(21) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

Table 5.6 GPIO port connector CN8

5.3 SPI Connector C9

Table 5.7 details connector pinout for the SPI connector C9. A full description of each signal is available in the VNC2 data sheet.

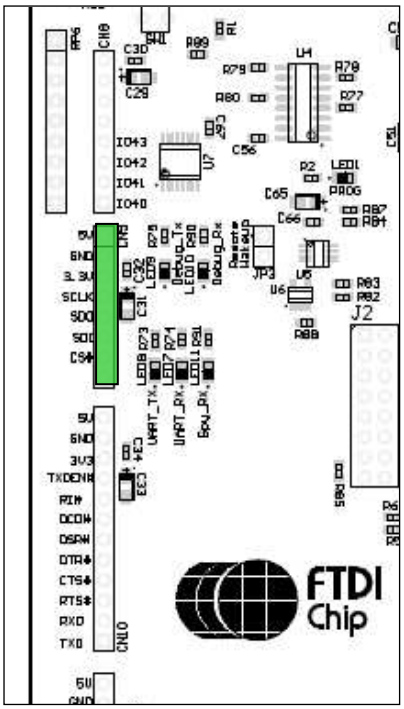

Figure 5.8 SPI Connector CN9

Signal name	Connector pin	VCN2 Pin No		IO type	Description
		48-PIN	64-PIN		
5V(22)	1	-	-	-	5V power rail.
GND	2	-	-	-	Ground pin
3.3V(23)	3	-	-	-	3.3V power rail.
SCLK (24)	4	20	61	Input	SPI CLK Input
SDO (24)	5	21	62	Output	SPI Master out slave in
SDI(24)	6	22	63	Input	SDI Master in slave out
CS# (24)	7	23	64	Output	Active low slave chip select 0 from master to slave 0
GND	8	-	-	-	Ground pin

Notes:

(22) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(23) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(24) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels..
The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

Table 5.7 SPI Port Connector CN9

5.4 UART Interface Connector C10

Table 5.8 details connector pinout for the UART connector C10. A full description of each signal is available in the VNC2 data sheet.

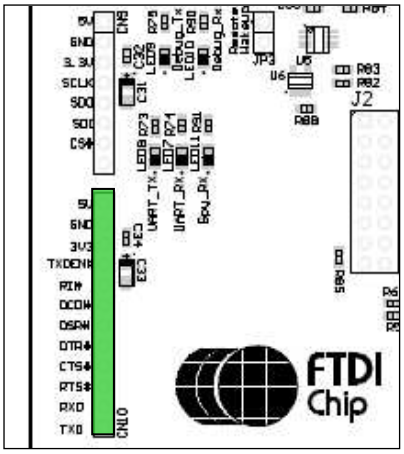

Figure 5.9 UART Connector CN10

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
TXD [25]	1	23	31	39	Output	Transmit data
RXD [25]	2	24[26]	32[26]	40	Input	Receive data
RTS# [25]	3	25	33	41	Output	Request to Send Control Output / Handshake signal.
CTS# [25]	4	26[26]	34[26]	42	Input	Clear to Send Input / Handshake signal.
DTR# [25]	5		35	43	Output	Data Terminal Ready Output / Handshake signal.
DSR# [25]	6		36	44	Input	Data Set Ready Input / Handshake signal.
DCD# [25]	7		37	45	Input	Data Carrier Detect Control Input
RI# [25]	8		38	46	Input	Ring Indicator Control Input
TXDEN#[25]	9		-	47	Output	Transmit Data Enable
3.3V[27]	10		-	-	-	3.3V power rail.
GND	11		-	-	-	Ground pin
5V[28]	12		-	-	-	5V power rail.

Notes:

(25) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels..
The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(26) The following pins are only accessible on VNC2 when the onboard multiplexer select input is high. See section 6.4 for details.

(27) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from power supply and no more than 50mA when the board is powered from USB power bus.

(28) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from power supply and no more than 50mA when the board is powered from USB power bus.

Table 5.8 UART Interface Connector CN10

5.5 FIFO Interface Connector CN11

Table 5.9 details connector pinout for the FIFO connector C11. A full description of each signal is available in the VNC2 data sheet.

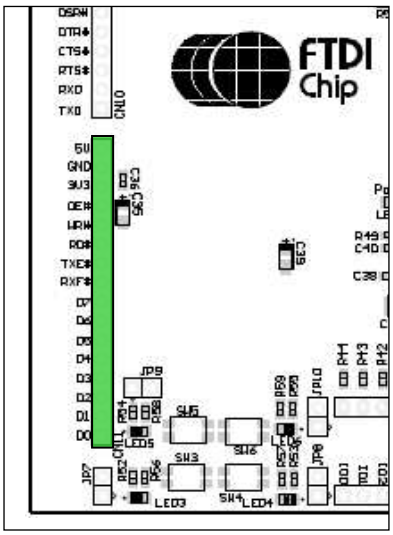

Figure 5.10 FIFO Connector CN11

Signal name	Connector pin	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
D0 (29)	1	-	-	15	IO	FIFO data bit 0, bidirectional
D1 (29)	2	-	-	16	IO	FIFO data bit 1, bidirectional
D2 (29)	3	-	-	17	IO	FIFO data bit 2, bidirectional
D3 (29)	4	-	-	18	IO	FIFO data bit 3, bidirectional
D4 (29)	5	-	-	19	IO	FIFO data bit 4, bidirectional
D5 (29)	6	-	-	20	IO	FIFO data bit 5, bidirectional
D6 (29)	7	-	-	22	IO	FIFO data bit 6, bidirectional
D7 (29)	8	-	-	23	IO	FIFO data bit 7, bidirectional
RXF#	9	-	-	24	Output	FIFO receive full output
TXE#	10	-	-	25	Output	FIFO transmitter buffer empty output
RD#	11	-	-	26	Input	FIFO read enable input
WR#	12	-	-	27	Input	FIFO write enable input
OE#	13	-	-	28	Input	FIFO output enable – synchronous FIFO only
3.3V(30)	14	-	-	-	-	3.3V power rail.
GND	15	-	-	-	-	Ground pin
5V(31)	16	-	-	-	-	5V power rail.

Notes:

(29) All VNC2's IO pins can be driven from 3.3V LVTTL TTL logic levels. The use of these pins for GPIO is set by the IOMUX on the VNC2 device. The pins are shared by other connectors on the board. Care should be taken to ensure that pins are not driven from other headers on the board.

(30) This pin is connected to 3.3V regulator output. External device can draw no more than 100mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

(31) This pin is connected to the board's 5V power rail. External device can draw no more than 250mA when board is powered from an external power supply and no more than 50mA when the board is powered from USB bus.

Table 5.9 FIFO Interface Connector CN11

5.6 Prototyping area

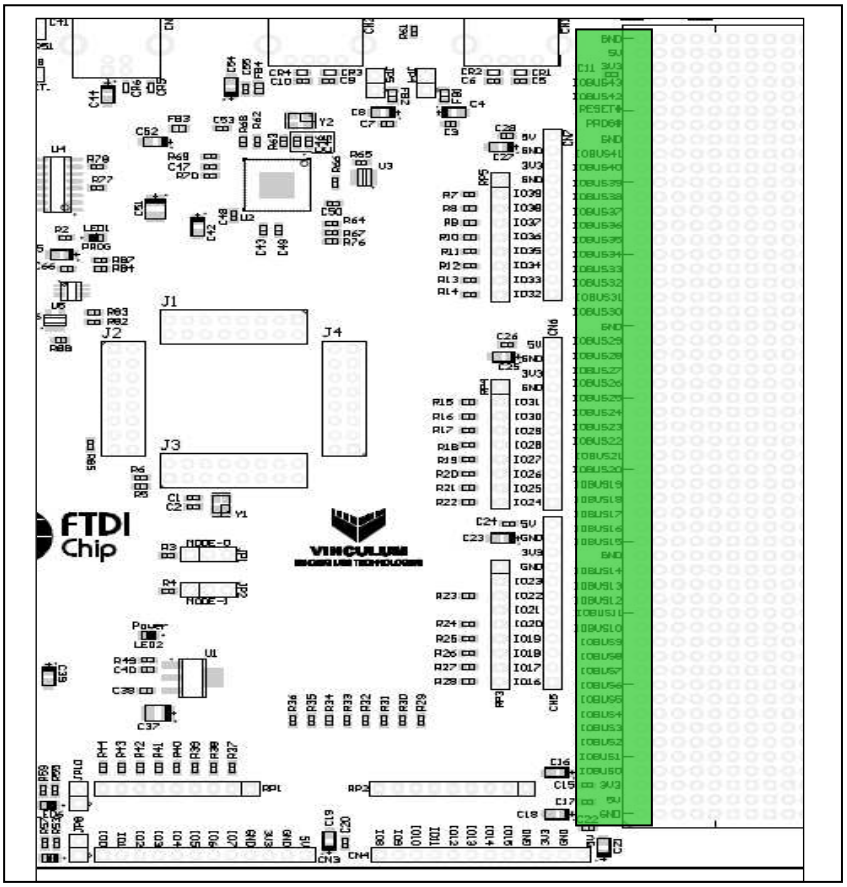

Figure 5.11 Prototyping area P1

A prototype area consisting of an array of 1100, 0.1-inch pitch holes is provided. The area can be used to create custom circuitry and connect components to the V2-EVAL board. The prototyping area includes connections to the 5V, 3.3 V planes and ground planes. The silk-screen text on the board indicates which holes are connected to which signals. Only the first column is connected to VNC2 IO ports, power and ground planes. All the other holes are not connected to anything on the board.

Signal pins are shared between other IO connectors on the board. For more information refer to the V2-Eval Board schematics.

Connector pin number	Silk Screen Signal Label	VCN2 Pin No			IO type	Description
		32-PIN	48-PIN	64-PIN		
1	GND	-	-	-	-	Ground pin
2	5V [32]	-	-	-	-	5V power rail. Can be used to power external devices
3	3.3V[33]	-	-	-	-	3.3V power rail. Can be used to power external devices
4	IOBUS0[34]	11	11	11	IO	IOBUS port Data Bit 0. Debug port – default configuration.
5	IOBUS1[34]	12	12	12	IO	IOBUS port Data Bit 1.
6	IOBUS2[34]	14	13	13	IO	IOBUS port Data Bit 2.
7	IOBUS3[34]	15	14	14	IO	IOBUS port Data Bit 3.
8	IOBUS4[34]	-	-	15	IO	IOBUS port Data Bit 4.
9	IOBUS5[34]	-	-	16	IO	IOBUS port Data Bit 5.
10	IOBUS6[34]	-	-	17	IO	IOBUS port Data Bit 6.
11	IOBUS7[34]	-	-	18	IO	IOBUS port Data Bit 7.
12	IOBUS8[34]	-	-	19	IO	IOBUS port Data Bit 8.
13	IOBUS9[34]	-	-	20	IO	IOBUS port Data Bit 9.
14	IOBUS10[34]	-	-	22	IO	IOBUS port Data Bit 10.
15	IOBUS11[34]	-	-	23	IO	IOBUS port Data Bit 11.
16	IOBUS12[34]	-	-	24	IO	IOBUS port Data Bit 12.
17	IOBUS13[34]	-	-	25	IO	IOBUS port Data Bit 13.
18	IOBUS14[34]	-	-	26	IO	IOBUS port Data Bit 14.
19	GND	-	-	-	-	Ground pin
20	IOBUS15[34]	-	-	27	IO	IOBUS port Data Bit 15.
21	IOBUS16[34]	-	-	27	IO	IOBUS port Data Bit 16.
22	IOBUS17[34]	-	46	28	IO	IOBUS port Data Bit 17.
23	IOBUS18[34]	-	45	29	IO	IOBUS port Data Bit 18.
24	IOBUS19[34]	-	48	31	IO	IOBUS port Data Bit 19.
25	IOBUS20[34]	23	31	32	IO	IOBUS port Data Bit 20.
26	IOBUS21[34]	24[35]	32[35]	39	IO	IOBUS port Data Bit 21.
27	IOBUS22[34]	25	33	40	IO	IOBUS port Data Bit 22.
28	IOBUS23[34]	26[35]	34[35]	41	IO	IOBUS port Data Bit 23.
29	IOBUS24[34]	-	35	43	IO	IOBUS port Data Bit 24.
30	IOBUS25[34]	-	36	44	IO	IOBUS port Data Bit 25.
31	IOBUS26[34]	-	37	45	IO	IOBUS port Data Bit 26.
32	IOBUS27[34]	-	38	46	IO	IOBUS port Data Bit 27.
33	IOBUS28[34]	-	41	47	IO	IOBUS port Data Bit 28.
34	IOBUS29[34]	-	42	48	IO	IOBUS port Data Bit 29.
35	GND	-	-	-		
36	IOBUS30[34]	-	43	49	IO	IOBUS port Data Bit 30.
37	IOBUS31[34]	-	44	50	IO	IOBUS port Data Bit 31.
38	IOBUS32[34]	29	15	51	IO	IOBUS port Data Bit 32.
39	IOBUS33[34]	30	16	52	IO	IOBUS port Data Bit 33.
40	IOBUS34[34]	31	18	55	IO	IOBUS port Data Bit 34.
41	IOBUS35[34]	32	19	56	IO	IOBUS port Data Bit 35.