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V385A

8-BIT LVDS TRANSMITTER FOR VIDEO

General Description

The V385A transmitter converts 28 bits of 3.3 V CMOS/TTL into 4 Low Voltage Differential Signaling (LVDS) data streams while the transmit clock input is transmitted in parallel with the data streams over a fifth LVDS link.

Compared to the V385, the V385A provides an extended clock frequency range of 12-90 MHz, rather than 20-85 MHz. Other performance improvements have been incorporated as well.

The V385A can be programmed for rising edge or falling edge clocks through pin R_FB.

Pin Assignment

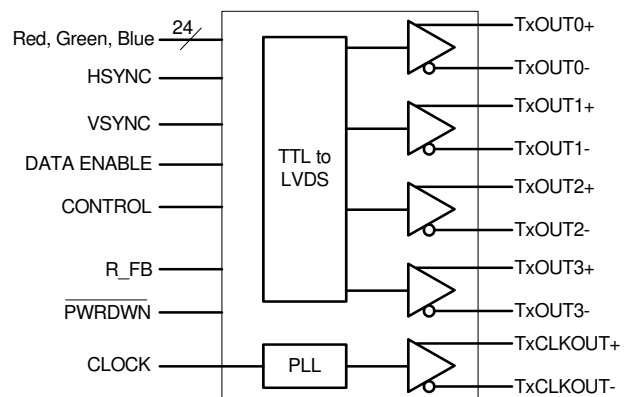
VCC	1	56	TxIN4
TxIN5	2	55	TxIN3
TxIN6	3	54	TxIN2
TxIN7	4	53	GND
GND	5	52	TxIN1
TxIN8	6	51	TxIN0
TxIN9	7	50	TxIN27
TxIN10	8	49	LVDS_GND
VCC	9	48	TxOUT0-
TxIN11	10	47	TxOUT0+
TxIN12	11	46	TxOUT1-
TxIN13	12	45	TxOUT1+
GND	13	44	LVDS_VCC
TxIN14	14	43	LVDS_GND
TxIN15	15	42	TxOUT2-
TxIN16	16	41	TxOUT2+
R_FB	17	40	TxCLKOUT-
TxIN17	18	39	TxCLKOUT+
TxIN18	19	38	TxOUT3-
TxIN19	20	37	TxOUT3+
GND	21	36	LVDS_GND
TxIN20	22	35	PLL_GND
TxIN21	23	34	PLL_VCC
TxIN22	24	33	PLL_GND
TxIN23	25	32	PWRDWN
VCC	26	31	TxCLKIN
TxIN24	27	30	TxIN26
TxIN25	28	29	GND

56-pin TSSOP

Features

- Extended clock frequency range of 12 to 90 MHz
- Convert 28 bits of 3.3 V CMOS/TTL into 4 LVDS streams
- Up to 2.52 Gbps throughput or 315 Megabytes/sec bandwidth
- Spread spectrum compatible
- Supports SD, HD and VGA graphics applications
- LVDS voltage swing of 350 mV for low EMI
- On-chip PLL requires no external components
- Single 3.3 V low-power CMOS design
- Operating temperature of -10 to +70°C
- Programmable rising or falling edge strobe
- Power-down control function
- Compatible with TIA/EIA-644 LVDS standards
- Packaged in a 56-pin TSSOP (Pb free available)
- Pin and function compatible with the National DS90C385, TI SN65LVDS93 and Thine THC63LVDM83, but with extended clock frequency and operating temperature range

Block Diagram





Pin Descriptions

Pin	Pin Type	Pin Name	Pin Description/Name
1	Power	VCC	3.3V Power
2	CMOS/TTL	TxIN5	Parallel digital video input pins (TxIN0..27).
3	CMOS/TTL	TxIn6	Parallel digital video input pins (TxIN0..27).
4	CMOS/TTL	TxIn7	Parallel digital video input pins (TxIN0..27).
5	Ground	GND	Ground
6	CMOS/TTL	TxIN8	Parallel digital video input pins (TxIN0..27).
7	CMOS/TTL	TxIN9	Parallel digital video input pins (TxIN0..27).
8	CMOS/TTL	TxIN10	Parallel digital video input pins (TxIN0..27).
9	Power	VCC	3.3V Power
10	CMOS/TTL	TxIN11	Parallel digital video input pins (TxIN0..27).
11	CMOS/TTL	TxIN12	Parallel digital video input pins (TxIN0..27).
12	CMOS/TTL	TxIN13	Parallel digital video input pins (TxIN0..27).
13	Ground	GND	Ground
14	CMOS/TTL	TxIN14	Parallel digital video input pins (TxIN0..27).
15	CMOS/TTL	TxIN15	Parallel digital video input pins (TxIN0..27).
16	CMOS/TTL	TxIN16	Parallel digital video input pins (TxIN0..27).
17	CMOS/TTL	R_FB	Programmable strobe select input pin (R_FB). High = rising edge; Low = falling edge.
18	CMOS/TTL	TxIN17	Parallel digital video input pins (TxIN0..27).
19	CMOS/TTL	TxIN18	Parallel digital video input pins (TxIN0..27).
20	CMOS/TTL	TxIN19	Parallel digital video input pins (TxIN0..27).
21	Ground	GND	Ground
22	CMOS/TTL	TxIN20	Parallel digital video input pins (TxIN0..27).
23	CMOS/TTL	TxIN21	Parallel digital video input pins (TxIN0..27).
24	CMOS/TTL	TxIN22	Parallel digital video input pins (TxIN0..27).
25	CMOS/TTL	TxIN23	Parallel digital video input pins (TxIN0..27).
26	Power	VCC	3.3V Power
27	CMOS/TTL	TxIN24	Parallel digital video input pins (TxIN0..27).
28	CMOS/TTL	TxIN25	Parallel digital video input pins (TxIN0..27).
29	Ground	GND	Ground
30	CMOS/TTL	TxIN26	Parallel digital video input pins (TxIN0..27).
31	CMOS/TTL	TxCLKIN	Clock input (TxCLKIN)
32	CMOS/TTL	PWRDWN	Active low. Powerdown tri-states outputs.
33	Ground	PLL_GND	Ground
34	Power	PLL_VCC	3.3V Power
35	Ground	PLL_GND	Ground
36	Ground	LVDS_GND	Ground



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Pin	Pin Type	Pin Name	Pin Description/Name
37	LVDS	TxOUT3+	LVDS output (+)
38	LVDS	TxOUT3-	LVDS output (-)
39	LVDS	TxCLKOUT+	LVDS output (+)
40	LVDS	TxCLKOUT-	LVDS output (-)
41	LVDS	TxOUT2+	LVDS output (+)
42	LVDS	TxOUT2-	LVDS output (-)
43	Ground	LVDS_GND	Ground
44	Power	LVDS_VCC	3.3V Power
45	LVDS	TxOUT1+	LVDS output (+)
46	LVDS	TxOUT1-	LVDS output (-)
47	LVDS	TxOUT0+	LVDS output (+)
48	LVDS	TxOUT0-	LVDS output (-)
49	Ground	LVDS_GND	Ground
50	CMOS/TTL	TxIN27	Parallel digital video input pins (TxIN0..27).
51	CMOS/TTL	TxIn0	Parallel digital video input pins (TxIN0..27).
52	CMOS/TTL	TxIn1	Parallel digital video input pins (TxIN0..27).
53	Ground	GND	Ground
54	CMOS/TTL	TxIn2	Parallel digital video input pins (TxIN0..27).
55	CMOS/TTL	TxIn3	Parallel digital video input pins (TxIN0..27).
56	CMOS/TTL	TxIn4	Parallel digital video input pins (TxIN0..27).

External Components

The V385A requires no external components.



Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the V385A. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	-0.3 V to +4 V
All Inputs and Outputs	-0.3 V to VCC+0.3 V
Electrostatic Discharge (EIAJ, 0Ω, 200 pF)	> 500 V
Ambient Operating Temperature	-10 to +70°C
Storage Temperature	-65 to +150°C
Junction Temperature	150°C
Maximum Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-10		+70	°C
Power Supply Voltage (measured in respect to GND)	3.0	3.3	3.6	V

Electrical Characteristics

VDD=3.3 V ±10%, Ambient temperature -10 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Freq.
CMOS/TTL DC Specifications							
Input High Voltage	V _{IH}		2.00		VCC	V	
Input Low Voltage	V _{IL}		GND		0.80	V	
Input Current	I _{IN}	GND<VIN<VCC			±10	μA	
Power-down Current	I _{PD}	No switching for input pins			10	μA	
LVDS DC Specifications							
Differential Output Voltage	V _{OD}	R _L = 100 ohms	250	345	450	mV	
Change in V _{OD} Between Complimentary Output States	ΔV _{OD}				35	mV	
Common Mode Voltage	V _{CM}		1.125	1.250	1.375	V	
Change in V _{CM} Between Complimentary Output States	ΔV _{CM}				35	mV	
Output Short Circuit Current	I _{OS}	V _{OD} =0V		3.5	5	mA	
Output Tri-State Current	I _{OZ}	Power Down#=0V		±1	±10	μA	



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Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Freq.
Recommended Transmitter Input Characteristics							
TxCLK IN Transition Time	TCIT				5	ns	
TxCLK IN Period	TCIP		11.11	T	83.333	ns	
TxCLK IN High Time	TCIH		0.35T	0.5T	0.65T	ns	
TxCLK IN Low Time	TCIL		0.35T	0.5T	0.65T	ns	
TxIN Transition Time	TXIT		1.5		6	ns	
Transmitter Switching Characteristics							
LVDS Low-to-High Time	LLHT			0.75	1.4	ns	
LVDS High-to-Low Time	LHLT			0.75	1.4	ns	
Transmitter Output Pulse Position	TPPos0	Bit0	-0.2	0	0.2	ns	85 MHz
	TPPos1	Bit1	T/7-0.2	T/7	T/7+0.2	ns	85 MHz
	TPPos2	Bit2	2T/7-0.2	2T/7	2T/7+0.2	ns	85 MHz
	TPPos3	Bit3	3T/7-0.2	3T/7	3T/7+0.2	ns	85 MHz
	TPPos4	Bit4	4T/7-0.2	4T/7	4T/7+0.2	ns	85 MHz
	TPPos5	Bit5	5T/7-0.2	5T/7	5T/7+0.2	ns	85 MHz
	TPPos6	Bit6	6T/7-0.2	6T/7	6T/7+0.2	ns	85 MHz
Transmitter Phase Loop Set	TPLLS				10	ms	
TxIN Setup to TxCLK IN	TSTC		2.5			ns	
TxIN Hold to TxCLK IN	THTC		0.5			ns	
TxCLK IN to TxCLK OUT Delay	TCCD		10		30	ns	

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		84		°C/W
	θ_{JA}	1 m/s air flow		76		°C/W
	θ_{JA}	3 m/s air flow		67		°C/W
Thermal Resistance Junction to Case	θ_{JC}			50		°C/W



AC Timing Diagrams

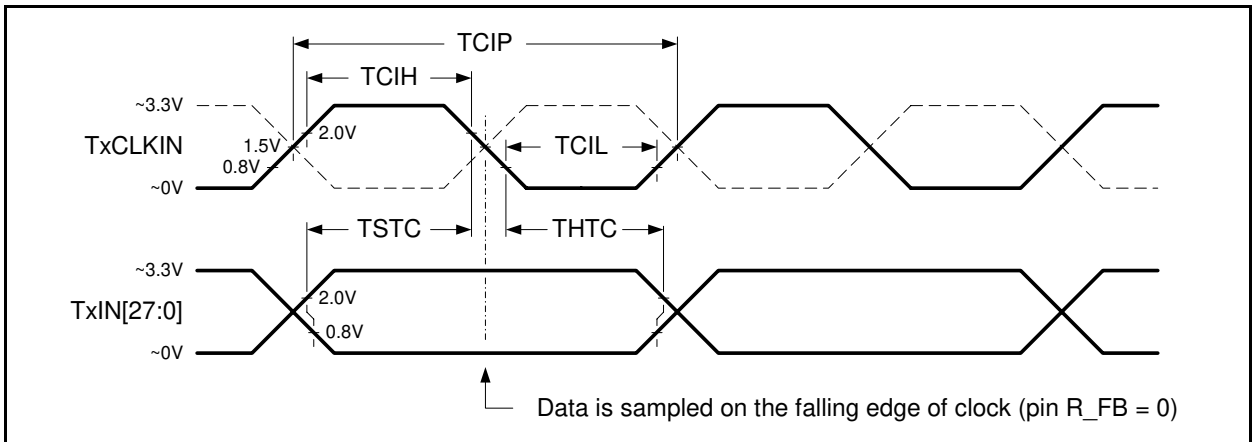


Figure AC1. Transmitter Setup/Hold and High/Low Times (Falling Edge Strobe or R_FB=0)

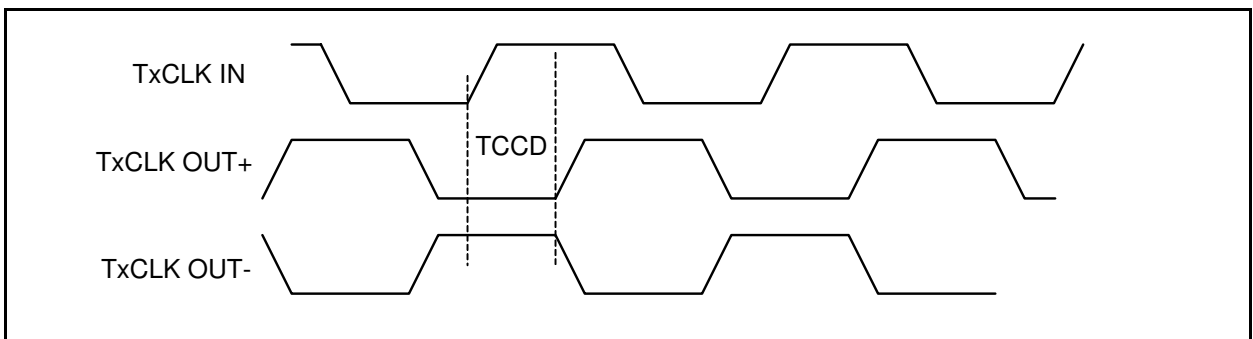


Figure AC2. Clock IN to Clock OUT Delay (Rising Edge Strobe or R_FB=1)

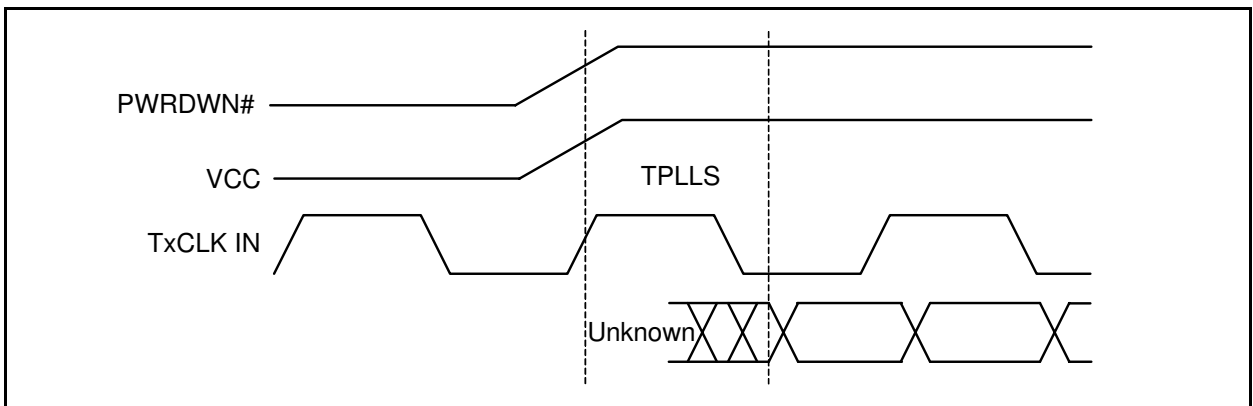


Figure AC3. Phase Lock Loop Set Time



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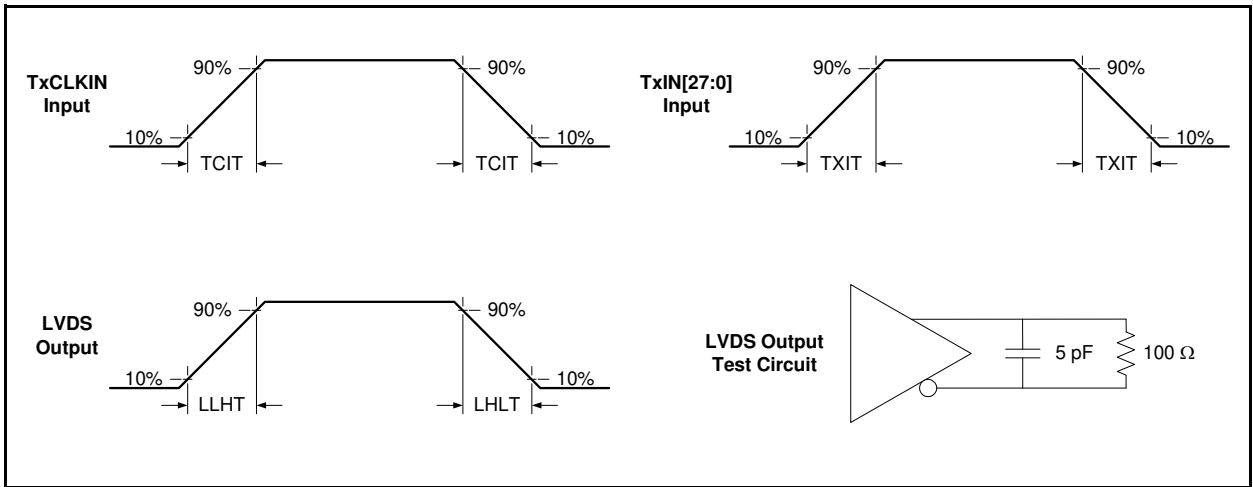


Figure AC4. Transmitter Device Transition Times and Load

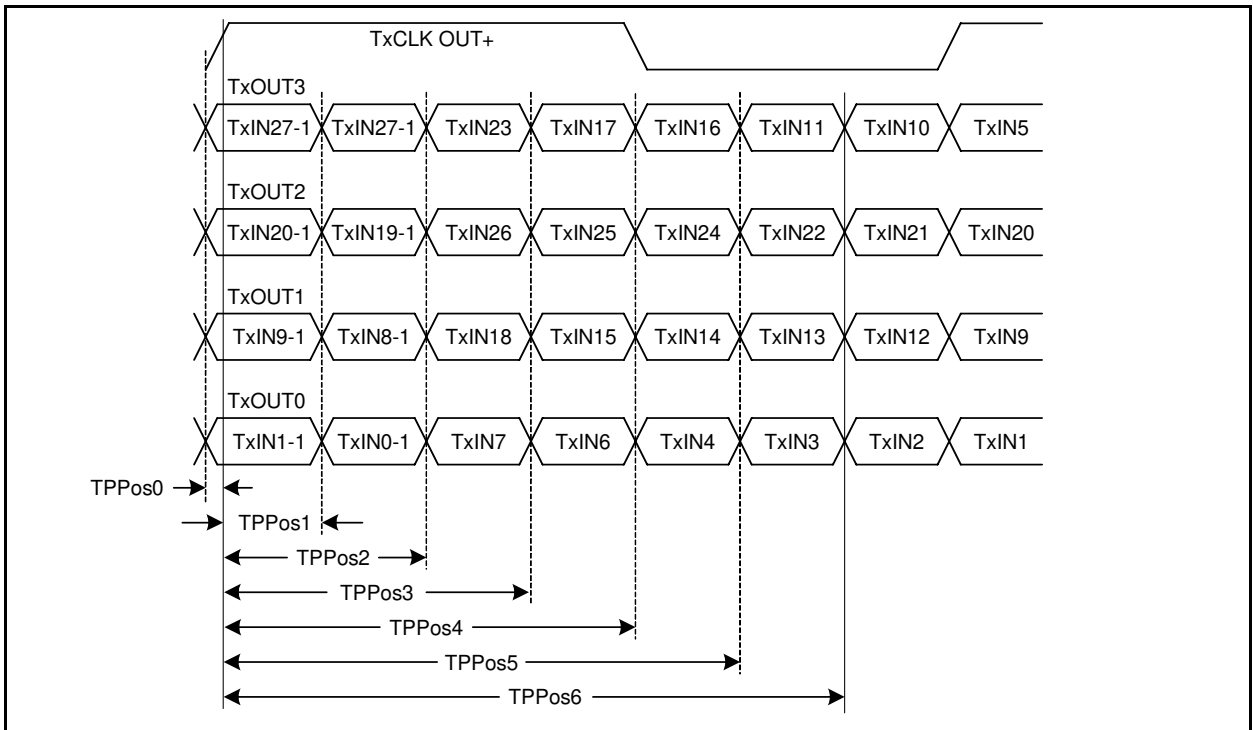


Figure AC5. Transmitter LVDS Output Pulse Position Measurement

