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# Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





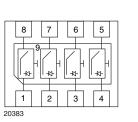


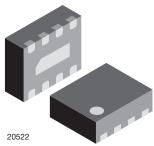
**GREEN** (5-2008)



## Vishay Semiconductors

### 4-Channel EMI-Filter with ESD-Protection





#### **FEATURES**

- Ultra compact LLP1713-9L package
- Low package profile of 0.6 mm
- 4-channel EMI-filter
- · Low leakage current
- Line resistance  $R_S = 100 \Omega$
- Typical cut off frequency f<sub>3dB</sub> = 100 MHz
- ESD-protection acc. IEC 61000-4-2 ± 30 kV contact discharge ± 30 kV air discharge
- e4 precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- Material categorization: For definitions of compliance please see www.vishav.com/doc?99912



**MARKING** (example only)



Dot = pin 1 marking Y = type code (see table below) XX = date code

ORDERING INFORMATION					
DEVICE NAME	DEVICE NAME ORDERING CODE		MINIMUM ORDER QUANTITY		
VEMI45AA-HNH	VEMI45AA-HNH-GS08	3000	15 000		

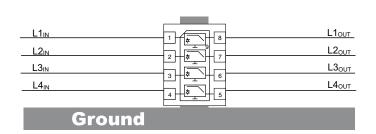
PACKAGE DATA						
DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VEMI45AA-HNH	LLP1713-9L	Α	3.7 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	260 °C/10 s at terminals

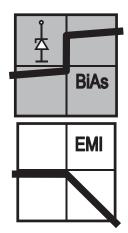
ABSOLUTE MAXIMUM RATINGS						
PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT		
Peak pulse current	All I/O pin to pin 9; acc. IEC 61000-4-5; $t_p = 8/20 \mu s$ ; single shot	I <sub>PPM</sub>	4	Α		
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	V	± 30	kV		
LSD illillullity	Air discharge acc. IEC 61000-4-2; 10 pulses	<b>V</b> ESD	V <sub>ESD</sub> ± 30			
Operating temperature	Junction temperature	TJ	- 40 to + 125	°C		
Storage temperature		T <sub>STG</sub>	- 55 to + 150	°C		



#### **APPLICATION NOTE**

With the VEMI45AA-HNH 4 different signal or data lines can be filtered and clamped to ground. Due to the different clamping levels in forward and reverse direction the clamping behaviour is <u>Bidirectional</u> and <u>Asymmetric</u> (BiAs).





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The 4 independent EMI-filter are placed between

pin 1 and pin 8,

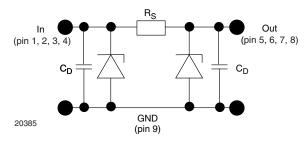
pin 2 and pin 7,

pin 3 and pin 6 and

pin 4 and pin 5.

They all are connected to a common ground pin 9 on the backside of the package.

The circuit diagram of one EMI-filter-channel shows two identical Z-diodes at the input to ground and the output to ground. These Z-diodes are characterized by the breakthrough voltage level ( $V_{BR}$ ) and the diode capacitance ( $C_D$ ). Below the breakthrough voltage level the Z-diodes can be considered as capacitors. Together with these capacitors and the line resistance  $R_S$  between input and output the device works as a low pass filter. Low frequency signals ( $f < f_{3dB}$ ) pass the filter while high frequency signals ( $f > f_{3dB}$ ) will be shorted to ground through the diode capacitances  $C_D$ .



Each filter is symmetrical so that both ports can be used as input or output.



<b>ELECTRICAL CHARACTERISTICS</b> All inputs (pin 1, 2, 3, and 4) to ground (pin 9) (T <sub>amb</sub> = 25 °C, unless otherwise specified)							
PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Protection paths	Number of channels which can be protected	N <sub>channel</sub>	-	-	4	channel	
Reverse stand off voltage	Max. reverse working voltage	V <sub>RWM</sub>	-	-	5	V	
Reverse voltage	at I <sub>R</sub> = 1 μA	V <sub>R</sub>	5	-	-	V	
Reverse current	at V <sub>R</sub> = V <sub>RWM</sub>	I <sub>R</sub>	-	-	1	μΑ	
Reverse break down voltage	at I <sub>R</sub> = 1 mA	$V_{BR}$	6	-	-	V	
Pos. clamping voltage	at I <sub>PP</sub> = 1 A applied at the input, measured at the output; acc. IEC 61000-4-5	V <sub>C-out</sub>	-	-	7	V	
	at $I_{PP} = I_{PPM} = 4$ A applied at the input, measured at the output; acc. IEC 61000-4-5	V <sub>C-out</sub>	-	-	8	V	
Neg. clamping voltage	at I <sub>PP</sub> = - 1 A applied at the input, measured at the output; acc. IEC 61000-4-5	V <sub>C-out</sub>	- 1	-	-	V	
	at I <sub>PP</sub> = I <sub>PPM</sub> = - 4 A applied at the input, measured at the output; acc. IEC 61000-4-5	V <sub>C-out</sub>	- 1.2	-	-	V	
Input capacitance	at V <sub>R</sub> = 0 V; f = 1 MHz	C <sub>IN</sub>	-	60	-	pF	
	at V <sub>R</sub> = 2.5 V; f = 1 MHz	C <sub>IN</sub>	-	36	-	pF	
ESD-clamping voltage	at ± 30 kV ESD-pulse acc. IEC 61000-4-2	V <sub>CESD</sub>	-	7.5	-	V	
Line resistance	Measured between input and output; I <sub>S</sub> = 10 mA	R <sub>S</sub>	90	100	110	Ω	
Cut-off frequency	$V_{IN} = 0 \text{ V}$ ; measured in a 50 $\Omega$ system	f <sub>3dB</sub>	-	100	-	MHz	

### **TYPICAL CHARACTERISTICS** (T<sub>amb</sub> = 25 °C, unless otherwise specified)

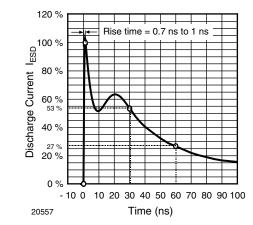


Fig. 1 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330  $\Omega$ /150 pF)

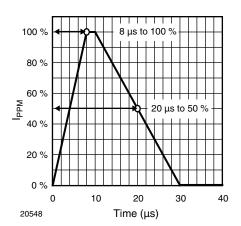


Fig. 2 - 8/20 µs Peak Pulse Current Wave Form acc. IEC 61000-4-5



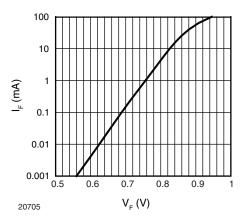


Fig. 3 - Typical Forward Current I<sub>F</sub> vs. Forward Voltage V<sub>F</sub>

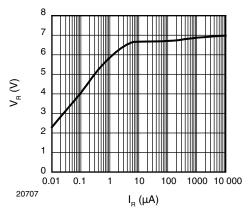


Fig. 4 - Typical Reverse Voltage  $V_R$  vs. Reverse Current  $I_R$ 

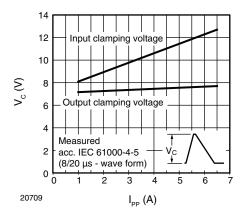


Fig. 5 - Typical Peak Clamping Voltage  $V_{C}$  vs. Peak Pulse Current  $I_{PP}$ 

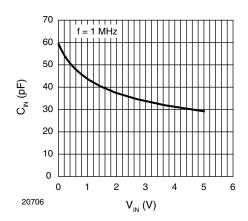


Fig. 6 - Typical Input Capacitance  $C_{\text{IN}}$  vs. Input Voltage  $V_{\text{IN}}$ 

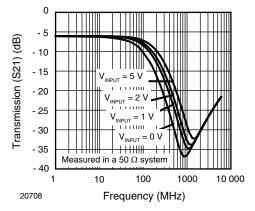
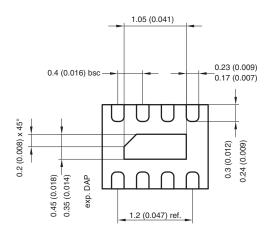
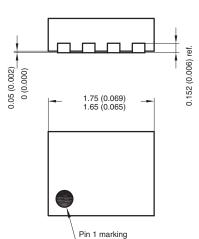
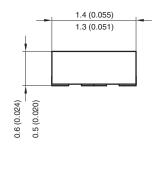


Fig. 7 - Typical Small Signal Transmission (S21) at  $\,$  Z $_{O}$  = 50  $\,$   $\Omega$ 

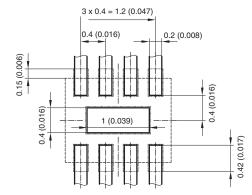
### PACKAGE DIMENSIONS in millimeters (inches): LLP1713-9L

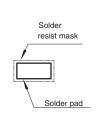






#### Foot print recommendation:





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