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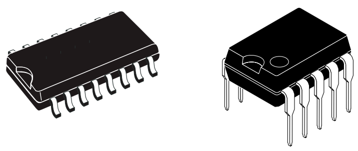
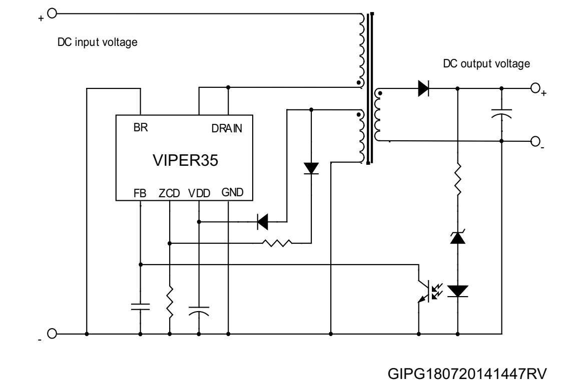
Quasi-resonant high performance off line high voltage converter

Datasheet - production data



SO16 N SDIP10

Figure 1. Basic application schematic



Features

- 800 V avalanche-rugged power MOSFET allowing ultra wide range input V_{AC} to be achieved
- Embedded HV start-up and senseFET
- Built-in soft-start
- Quasi-resonant current mode PWM controller with drain current limit (I_{Dlim})
- Multifunction ZCD pin:
  – Zero-current detection
  – OCP threshold (I_{Dlim}) setup
  – Output OVP (auto-restart)
  – Feed-forward compensation
- Support isolated flyback topology with opto-coupler
- Frequency limit:
  – 136 kHz (L type), 225 kHz (H type)
- Less than 30 mW @ 230 V_{AC} in no-load condition
- Brown-out set through resistor divider
- Short-circuit protection (auto-restart)
- Hysteretic thermal shutdown

Applications

- Auxiliary power supply
- Adapter/charger for PDA, camcorders, shavers, tablet, video games, STB
- Supplies for industrial systems, metering, appliances

Description

The device is a high voltage converter, which smartly integrates an 800 V rugged power MOSFET with a quasi-resonant current mode PWM control. This IC meets severe energy saving standards as it has very low consumption and operates in burst mode under light load conditions.

The device features the brown-out enabling the IC to set the switch-off and switch-on threshold independently one of each other. The quasi-resonant operation reduces the level of EMI and the quantity of components in the application.

The quasi-resonant operation reduces the switching losses and improves power conversion efficiency. The device features high level protections such as: output overvoltage, short-circuit and thermal shutdown with hysteresis. After the removal of a fault condition, the IC is automatically restarted.

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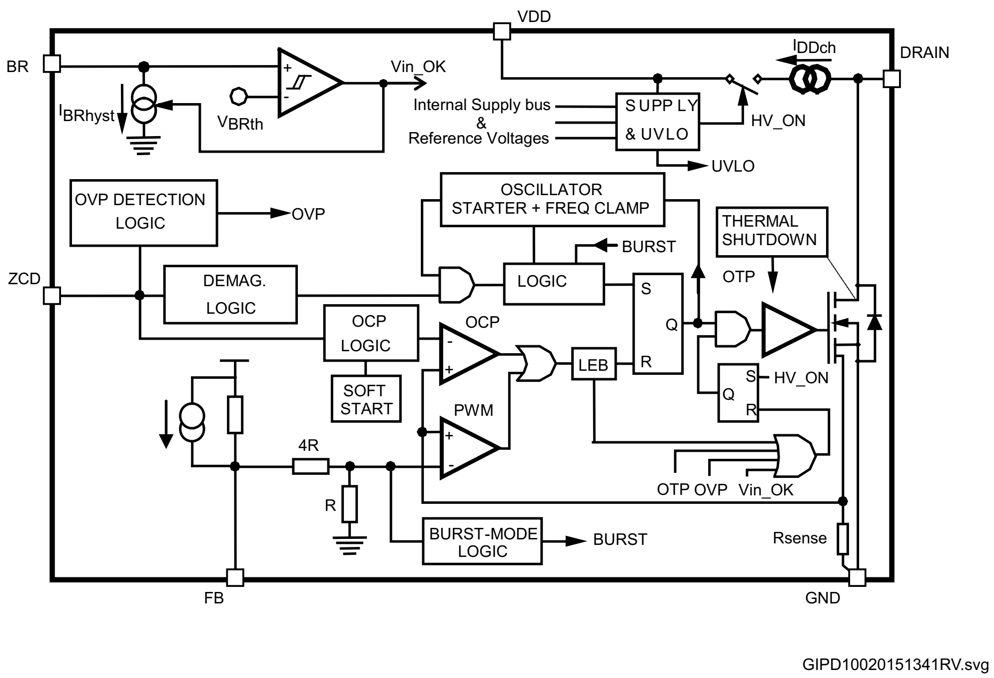
1 Block diagram

Figure 2. Block diagram



2 Typical output power

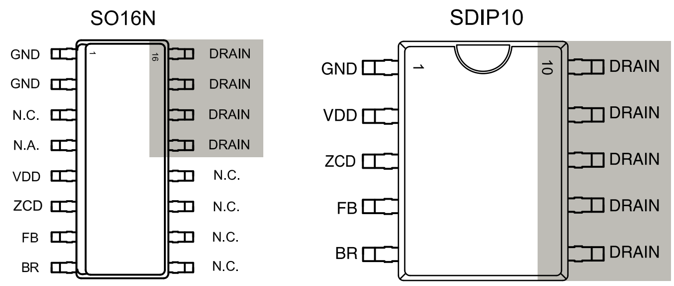
Table 1. Typical power

Part number	230 V_{AC}		85-265 V_{AC}	
	Adapter(1)	Open frame(2)	Adapter(1)	Open frame(2)
VIPER35	20 W	22 W	15 W	16 W

1. Typical continuous power in non-ventilated enclosed adapter measured at 50 °C ambient.
2. Maximum practical continuous power in an open frame design at 50 °C ambient, with adequate heatsinking.

3 Pin settings

Figure 3. Connection diagram



Note: The copper area for heat dissipation has to be designed under the DRAIN pins.

Table 2. Pin description

SO16N	SDIP10	Name	Function
1, 2	1	GND	Device ground and source of the power MOSFET.
3	-	N.C.	Not internally connected. It can be connected to GND.
4	-	N.A.	Not available for user. This pin is mechanically connected to the controller die pad of the frame. In order to improve the noise immunity it should be connected to GND (pin 1, 2).
5	2	VDD	Supply voltage of the control section. This pin provides the charging current of the external capacitor during the power-up.
6	3	ZCD	Multifunction pin: 1. Zero-current detection for quasi-resonant operations. 2. Drain current limit ($I_{Dlim)}$ setup for overcurrent protection (R_{LIM}). 3. Feed-forward compensation (R_{FF}) setup. 4. Output overvoltage protection (resistor divider R_{OVP} / R_{LIM}) setup.
7	4	FB	Control input for duty cycle control. Internal current generator provides bias current for loop regulation. A voltage below the threshold V_{FBbm} activates the burst-mode operation. A level close to the threshold V_{FBlin} means that the cycle-by-cycle overcurrent set-point is close.
8	5	BR	Brown-out protection input with hysteresis. A voltage below the threshold V_{BRth} shuts down (not latch) the device and lowers the power consumption. The device operation restarts as the voltage exceeds the threshold V_{BRth} + V_{BRhyst}. It must be connected to ground when it is not used.
9 to 12	-	N.C.	Not internally connected. These pins must be left floating in order to get a safe clearance distance.
13 to 16	6 to 10	DRAIN	High voltage drain pin. The built-in high voltage switched start-up bias current is drawn from this pin. Pins connected to the metal frame facilitate heat dissipation.

4 Electrical ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min.	Max.	
V_{DRAIN}	Drain-to-source (ground) voltage		800	V
E_{AV}	Repetitive avalanche energy (limited by T_J = 150 °C)		5	mJ
I_{AR}	Repetitive avalanche current (limited by T_J = 150 °C)		1.5	A
I_{DRAIN}	Single pulse drain current		3	A
V_{ZCD}	Input pin voltage (with I_{ZCD} = 1 mA)	-0.3	Self limited	V
V_{FB}	Input pin voltage	-0.3	5.5	V
V_{BR}	Input pin voltage (with I_{BR} = 0.25 mA)	-0.3	Self limited	V
V_{DD}	Supply voltage	-0.3	Self limited	V
I_{DD}	Input current		25	mA
P_{TOT}	Power dissipation at T_A < 60 °C		1.5	W
T_J	Operating junction temperature range	-40	150	°C
T_{STG}	Storage temperature	-55	150	°C

Table 4. Thermal data

Symbol	Parameter	Max. value		Unit
		SDIP10	SO16N	
R_{thJP}	Thermal resistance junction pin (dissipated power = 1 W)	35	35	°C/W
R_{thJA}	Thermal resistance junction ambient (dissipated power = 1 W)	100	110	°C/W
R_{thJA}	Thermal resistance junction ambient (1) (dissipated power = 1 W)	85	80	°C/W

1. When mounted on a standard single side FR4 board with 100 mm^2 (0.155 sq inch) of Cu (35 µm thick).

T_J = -40 to 125 °C, V_{DD} = 14 V [a] (unless otherwise specified)

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BVDSS}	Breakdown voltage	I_{DRAIN} = 1 mA, V_{FB} = GND T_J = 25 °C	800			V
I_{OFF}	Off-state drain current	V_{DRAIN} = 800 V V_{FB} = GND, T_J = 25 °C			60	uA
$R_{DS(on)}$	Drain-source on-state resistance	I_{DRAIN} = 0.4 A, VFB = 3 V V_{BR} = GND, T_J = 25 °C			4.5	Ω
		I_{DRAIN} = 0.4 A, VFB = 3 V V_{BR} = GND, T_J = 125 °C			9	Ω
C_{OSS}	Effective (energy related) output capacitance	V_{DRAIN} = 0 to 640 V		17		pF

T_J = -40 to 125 °C (unless otherwise specified)

Table 6. Supply section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Voltage						
V_{DRAIN_START}	Drain-source start voltage		60	80	100	V
I_{DDch1}	Start-up charging current (power-up)	V_{DRAIN} = 120 V V_{BR} = GND V_{FB} = GND V_{DD} = 4 V	-2	-3	-4	mA
I_{DDch2}	Start-up charging current (auto-restart)	V_{DRAIN} = 120 V V_{BR} = GND V_{FB} = GND V_{DD} = 5 V, after fault	-0.4	-0.6	-0.8	mA
V_{DD}	Operating voltage range	After turn-on	8.5		23.5	V
$V_{DDclamp}$	Clamp voltage	I_{DD} = 20 mA	23.5			V
V_{DDon}	V_{DD} start-up threshold	V_{DRAIN} = 120 V V_{BR} = GND V_{FB} = GND	13	14	15	V
V_{DDoff}	V_{DD} undervoltage shutdown threshold		7.5	8	8.5	V
$V_{DD(RESTART)}$	V_{DD} restart voltage threshold		4	4.5	5	V

a. Adjust V_{DD} above V_{DDon} start-up threshold before setting 14 V.

Table 6. Supply section (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Current						
I_{DD0}	Operating supply current, not switching	V_{FB} = GND V_{BR} = GND V_{DD} = 10 V[1]		0.6	0.7	mA
I_{DD1}	Operating supply current switching	V_{DRAIN} = 120 V V_{DD} = 16 V ZCD switching @100 kHz Resistive load:100 Ω V_{FB} = 2.5 V		2	3	mA
I_{DD_FAULT}	Operating supply current with protection tripping	VDD = 10 V			400	uA
I_{DDoff}	Operating supply current	$V_{DD} < V_{DDoff}$			270	uA

1. Adjust V_{DD} above V_{DDon} start-up threshold before setting 10 V.

T_J = -40 to 125 °C (unless otherwise specified)

Table 7. Controller section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Feedback pin						
V_{FBolp}	Overload shutdown threshold		4.5	4.8	5.2	V
V_{FBlin}	Linear dynamics upper limit		3.1	3.3	3.5	V
V_{FBbm}	Burst mode threshold	Voltage falling	0.56	0.6	0.64	V
$V_{FBbmhys}$	Burst mode hysteresis	Voltage rising		100		mV
I_{FB}	Feedback sourced current	V_{FB} = 0.3 V	-150	-215	-280	µA
		3.3 V < V_{FB} < 4 V	-2.5	-3	-3.5	µA
$R_{FB(DYN)}$	Dynamic resistance	V_{FB} > 2.5 V	12		25	kΩ
H_{FB}	$\Delta V_{FB} / \Delta I_D$		0.5		2	V/A

Table 7. Controller section (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
ZCD pin						
V_{ZCDCLh}	Upper clamp voltage	I_{ZCD} = 1 mA	5	5.5	6	V
V_{ZCDAth}	Arming voltage threshold	Positive-going edge	0.75	0.8	0.85	V
V_{ZCDTth}	Triggering voltage threshold	Negative-going edge	0.55	0.6	0.65	V
I_{ZCD}	Internal pull-up	$V_{FB} < V_{FBlin}$	-7.5	-10	-12.5	µA
t_{DELAY}	Turn-on delay after ZCD trigger			300		ns
t_{BLANK}	Turn-on inhibit time after MOSFET turn-off	V_{ZCD} < 1 V		6.3		µs
		V_{ZCD} >1 V		2.5		µs
Current limitation						
I_{Dlim}	Drain current limitation	V_{FB} = 4 V I_{ZCD} = -10 µA T_J = 25 °C	0.95	1	1.05	A
		V_{FB} = 4 V I_{ZCD} = - 55 µA T_J = 25 °C	0.68	0.8	0.92	A
		V_{FB} = 4 V I_{ZCD} = - 105 µA T_J = 25 °C	0.55	0.65	0.75	A
t_{SS}	Soft-start time	VIPER35L			3.5	ms
		VIPER35H			4.2	ms
t_{SU}	Start-up time	VIPER35L	7.5		15	ms
		VIPER35H	9.5		18	ms
t_{ON_MIN}	Minimum turn-on time		220	400	480	ns
t_d	Propagation delay	(1)		100		ns
t_{LEB}	Leading edge blanking	(1)		300		ns
I_{D_BM}	Peak drain current during burst mode	V_{FB} = 0.6 V	120	170	220	mA

Table 7. Controller section (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Overvoltage protection						
V_{OVP}	Overvoltage threshold		3.8	4.2	4.6	V
t_{STROBE}	Strobe time			2.2		µs
Oscillator section						
F_{OSClim}	Internal frequency limit	VIPER35L	122	136	150	kHz
		VIPER35H	200	225	250	kHz
$F_{STARTER}$	Starter frequency	V_{FB} = 1 V $V_{ZCD} < V_{ZCDTth}$ $t < t_{SU}$		1/4 F_{OSClim}		kHz
		V_{FB} =1 V $V_{ZCD} < V_{ZCDTth}$ $t > t_{SU}$		1/8 F_{OSClim}		kHz
Brown-out protection						
V_{BRth}	Brown-out threshold	Voltage falling	0.41	0.45	0.49	A
V_{BRHyst}	Voltage hysteresis above V_{BRth}		40	50	60	mV
I_{BRHyst}	Current hysteresis		7		12	µA
$V_{BRclamp}$	Clamp voltage	I_{BR} = 250 µA		3		V
V_{DIS}	Brown-out disable voltage		50		150	mV
Thermal shutdown						
T_{SD}	Thermal shutdown temperature	(1)	150	160		°C
T_{HYST}	Thermal shutdown hysteresis	(1)		30		°C

1. Specification assured by design, characterization and statistical correlation.

5 Typical electrical characteristics

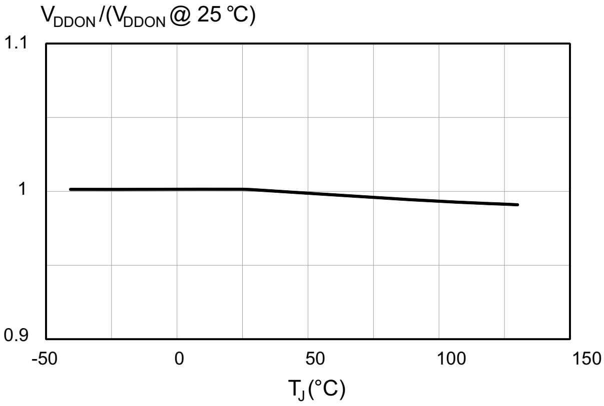


Figure 4. V_{DDon} vs T_J

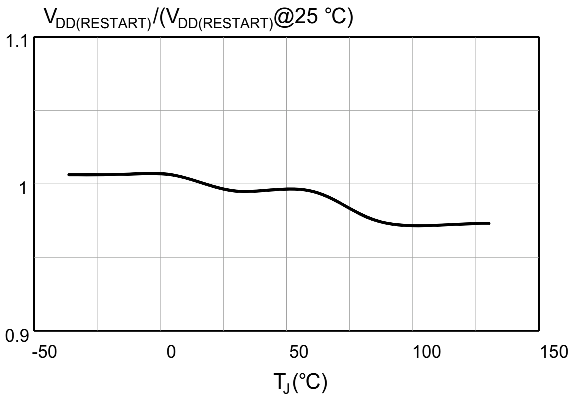


Figure 5. $V_{DD(RESTART)}$ vs T_J

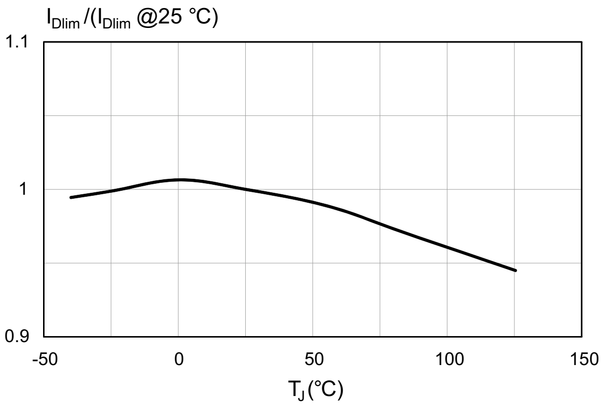


Figure 6. I_{Dlim} vs T_J

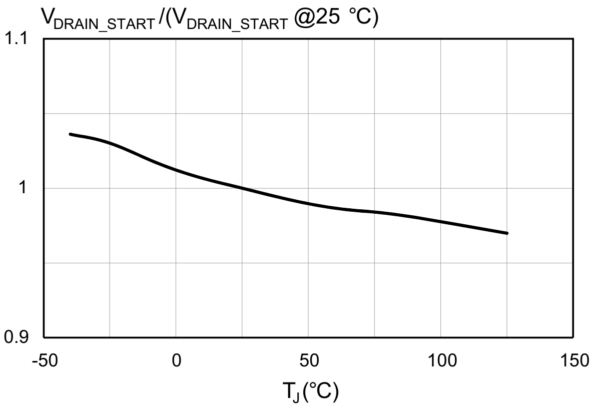


Figure 7. V_{DRAIN_START} vs T_J

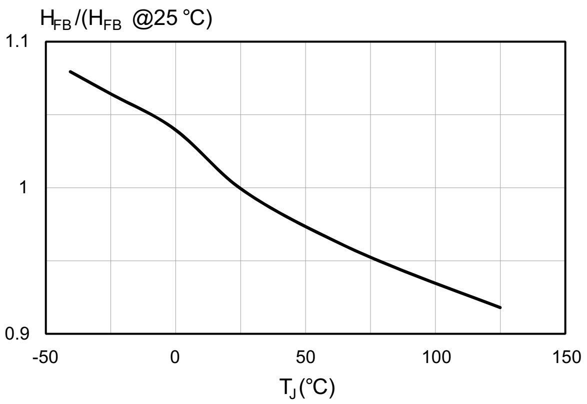


Figure 8. H_{FB} vs T_J

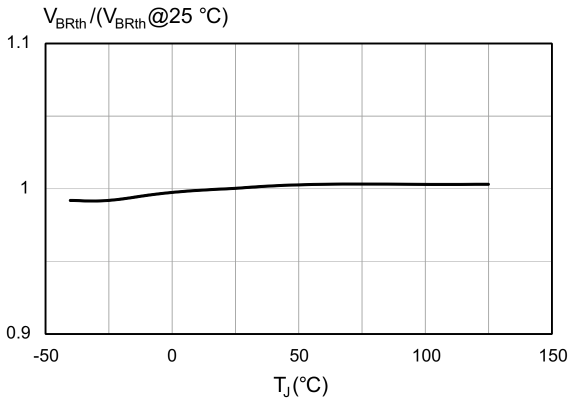


Figure 9. V_{BRth} vs T_J

Figure 10. V_{BRhyst} vs T_J

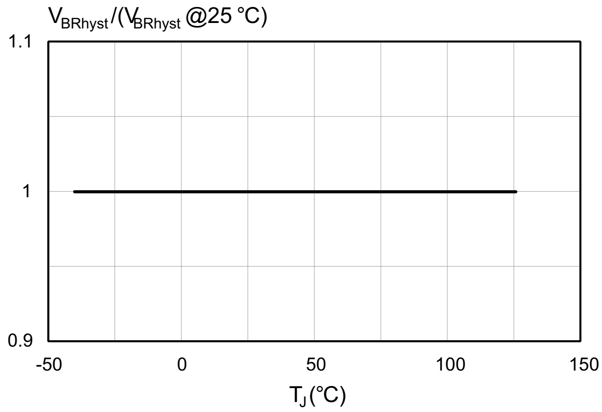


Figure 11. I_{BRhys} vs T_J

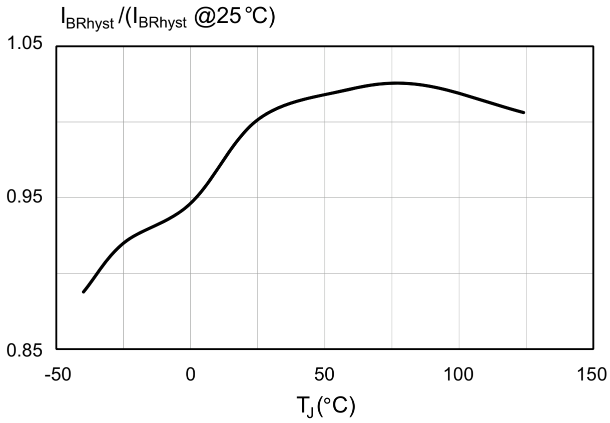


Figure 12. I_{DD0} vs T_J

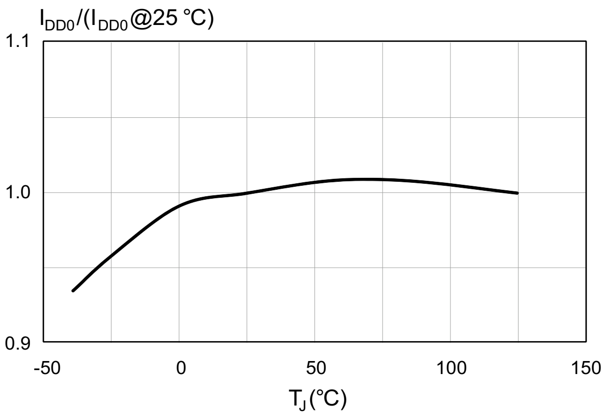


Figure 13. I_{DD1} vs T_J

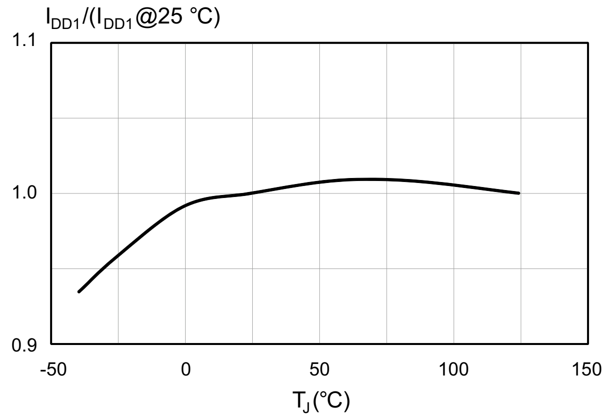


Figure 14. V_{ZCD} vs I_{ZCD}

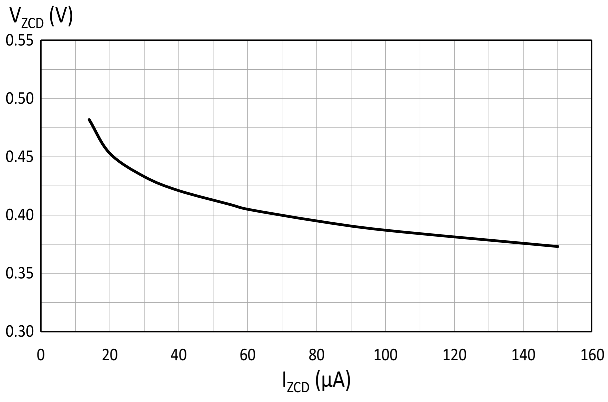


Figure 15. I_{Dlim} vs I_{ZCD}

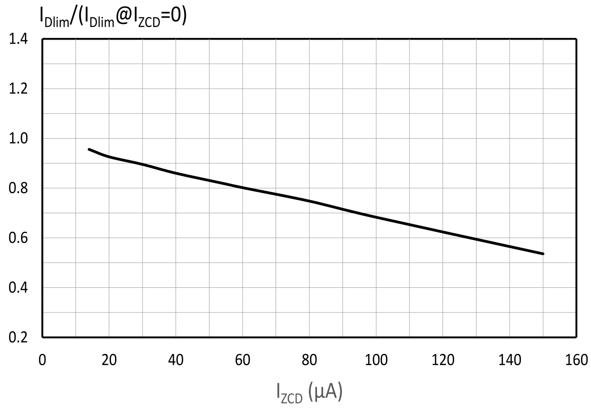


Figure 16. $R_{DS(on)}$ vs T_J

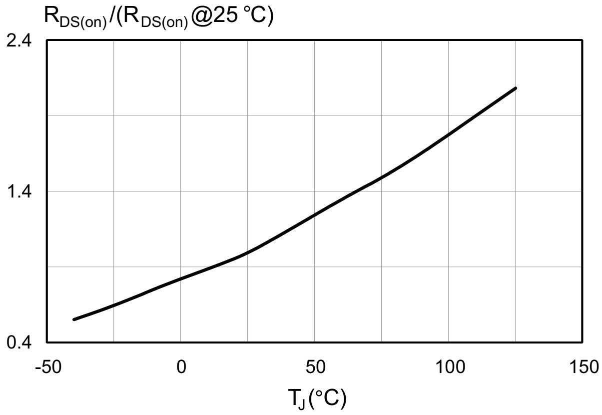


Figure 17. V_{BVDSS} vs T_J

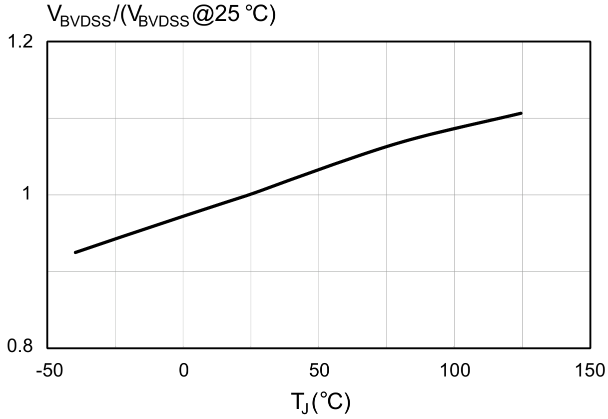


Figure 18. I_{DDch1} vs T_J

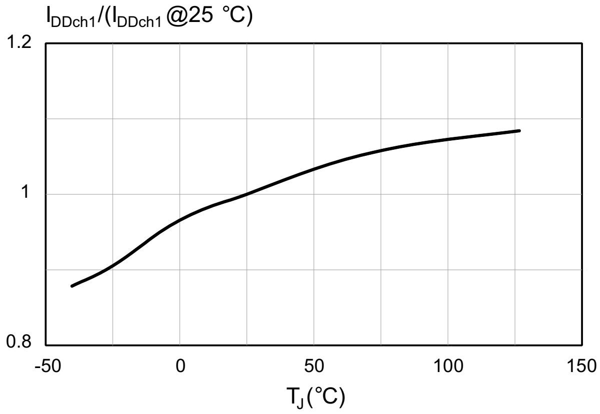


Figure 19. I_{DDch2} vs T_J

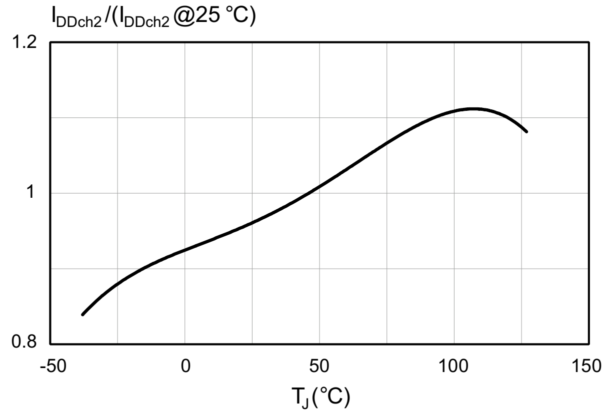


Figure 20. F_{OSClim_L} vs T_J

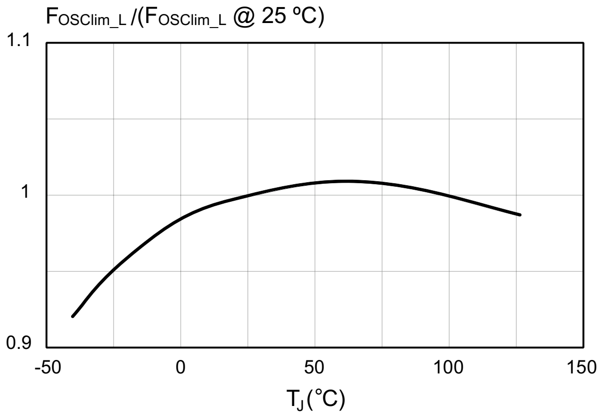


Figure 21. F_{OSClim_H} vs T_J

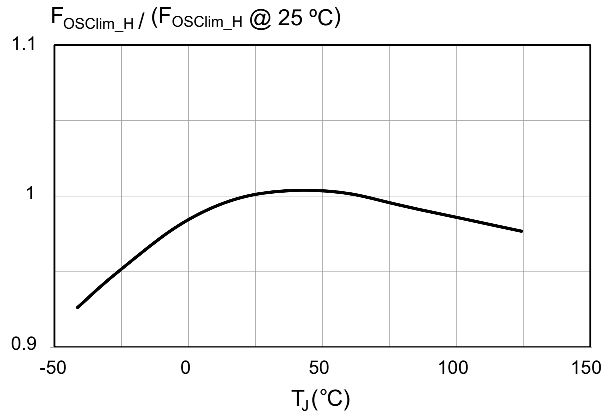
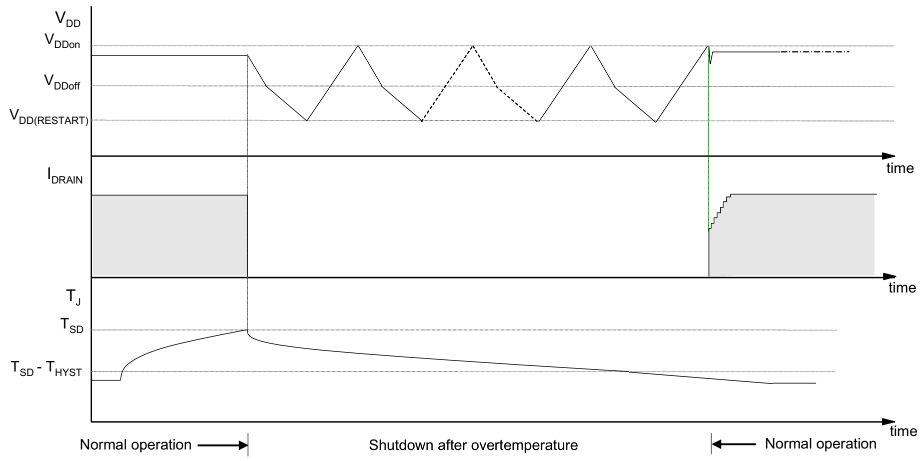


Figure 22. Thermal shutdown timing diagram



6 Typical circuits

Figure 23. Min-feature quasi-resonant flyback (isolated)

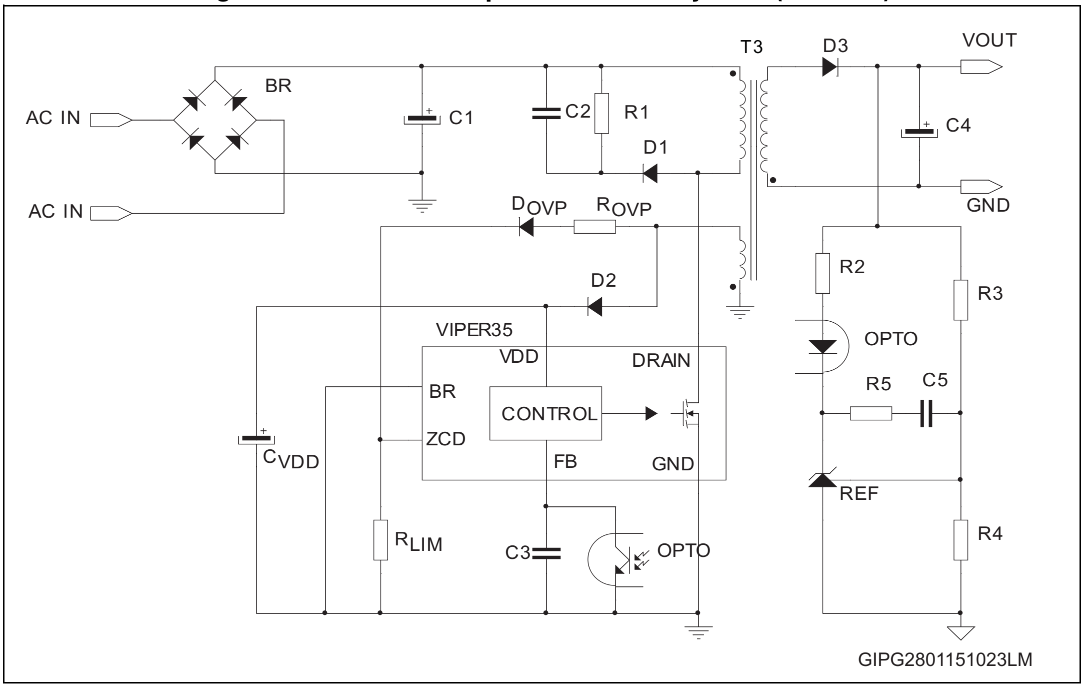
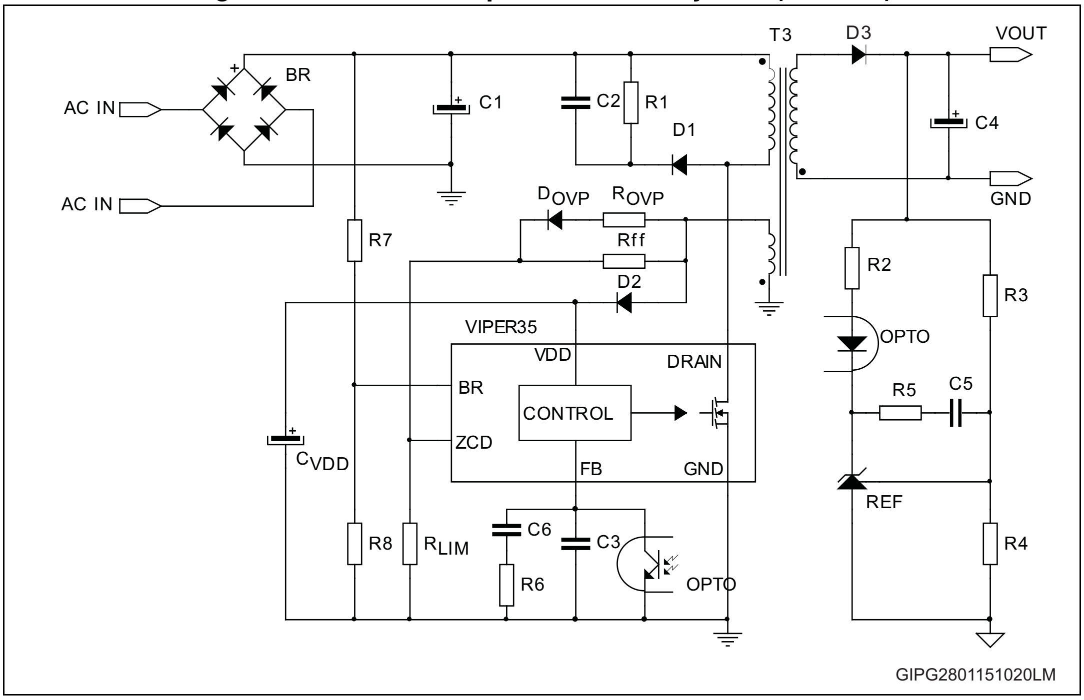


Figure 24. Full-feature quasi-resonant flyback (isolated)



7 Efficiency performance for a typical flyback converter

The efficiency of the converter has been measured in different load and line voltage conditions. In accordance with the Energy Star average active mode testing efficiency method, the efficiency measurements have been performed at 25%, 50% and 75% and 100% of the rated output power, both at 115 V_{AC} and 230 V_{AC}.

Table 8. Power supply efficiency, V_{OUT} = 12 V, V_{IN} = 115 V_{AC}

%load	I_{OUT} [A]	V_{OUT} [V]	P_{OUT} [W]	P_{IN}[W]	Efficiency [%]
25%	0.31	12.1	3.78	4.53	83.47
50%	0.63	12.1	7.56	8.98	84.21
75%	0.94	12.1	11.34	13.4	84.65
100%	1.25	12.1	15.12	17.93	84.36
Average efficiency					84.17

Table 9. Power supply efficiency, V_{OUT} = 12 V, V_{IN} = 230 V_{AC}

%load	I_{OUT} [A]	V_{OUT} [V]	P_{OUT} [W]	P_{IN}[W]	Efficiency [%]
25%	0.31	12.1	3.78	4.71	80.28
50%	0.63	12.1	7.56	9.22	82.02
75%	0.94	12.1	11.34	13.53	83.84
100%	1.25	12.1	15.12	17.77	85.12
Average efficiency					82.82

Figure 25. Power supply consumption at light output loads, V_{OUT} = 12 V

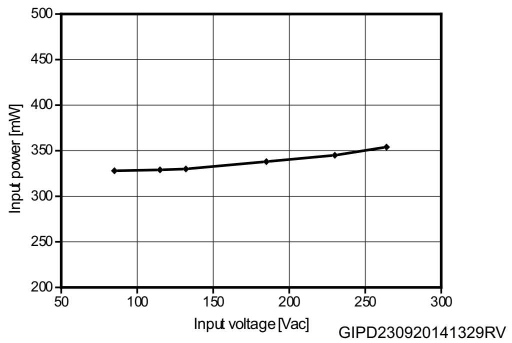
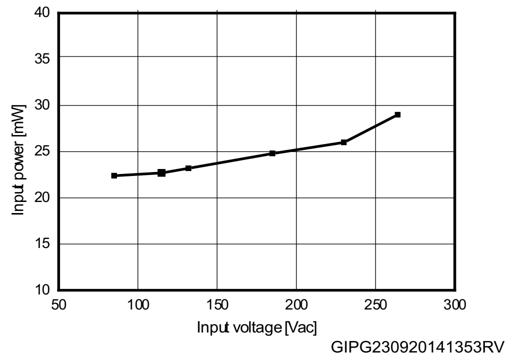


Figure 26. Power supply consumption at no output load, V_{OUT} = 12 V



8 Operation description

The device is a high performance low voltage PWM controller chip with an 800 V, avalanche-rugged power section.

The controller includes the PWM logic, ZCD logic for quasi-resonant operation, oscillator, start-up circuit with soft-start, current limiting circuit with adjustable set-point, burst mode management, brown-out circuit, UVLO circuit, auto-restart circuit and thermal protection circuit.

The current limit set-point can be reduced by ZCD pin. Burst mode operation guarantees high performance in standby mode and meets energy-saving standards.

All fault protections are built-in auto-restart mode with very low repetition rate to prevent the IC overheating.

8.1 Power section and gate driver

The power section is given by an avalanche-rugged N-channel MOSFET, which guarantees safe operation within the specified energy rating as well as high dv/dt capability. The power MOSFET has a B_{VDSS} of 800 V min. and a typical $R_{DS(on)}$ of 4.5 Ω at 25 °C. The integrated senseFET structure allows a virtual loss-less current sensing.

The gate driver is designed to supply a controlled gate current during both turn-on and turn-off in order to minimize common-mode EMI. Under UVLO conditions an internal pull-down circuit holds the gate low in order to ensure that the power section cannot be turned on accidentally.

8.2 High voltage start-up generator

The HV current generator is supplied through the DRAIN pin and it is enabled only if the input bulk capacitor voltage is higher than V_{DRAIN_START} threshold, 80 V DC typically.

When HV current generator is on, I_{DDch1} current (3 mA typical value) is delivered to the capacitor on VDD pin. During auto-restart mode after a fault event, the current is reduced to I_{DDch2} (0.6 mA, typ.) in order to have a slow duty cycle during the restart phase.

8.3 Power-up and soft-start

When the input voltage reaches the device start threshold, $V_{DRAIN\_START,}$ the VDD voltage begins growing due to I_{DDch1} current (see *Table 7*) coming from the internal high voltage start-up circuit. If the VDD voltage reaches V_{DDon} threshold, the power MOSFET starts switching and the HV current generator turns off.

The IC is powered by the energy stored in the capacitor on V_{DD} pin, C_{VDD}, until the self-supply circuit (typically an auxiliary winding of the transformer and a steering diode) develops a voltage so high to sustain the operation.

C_{VDD} capacitor must be correctly sized to avoid fast discharge and keep the required voltage higher than V_{DDoff} threshold. In fact, an insufficient capacitance value could terminate the switching operation before the controller receives any energy from the auxiliary winding.

The following formula can be used to calculate C_{VDD} capacitor:

Equation 1

$$C_{VDD} = \frac{I_{DDch} \times t_{SSaux}}{V_{DDon} - V_{DDoff}}$$

t_{SSaux} is the time needed for the steady-state of the auxiliary voltage. It represents an estimate of the user's application according to the output stage configurations (transformer, output capacitances, etc.).

During the normal operation, the power MOSFET switches on after the transformer demagnetization, detected through the voltage V_{ZCD} sensed on ZCD pin.

At power-up, the initial output voltage is zero and the voltage V_{ZCD} is not so high to correctly arm the internal ZCD circuit. In this case, the power MOSFET turns on with the fixed frequency $F_{STARTER}$, reported in *Table 7*. After the start-up, as soon as the voltage on ZCD logic is enabled to work, the turn-on of the power MOSFET is driven by this circuit and it is not related to the internal oscillator (except for the frequency foldback function) any longer.

The start-up phase is managed by a dedicated internal logic and is activated by every attempt of the start-up converter or after a fault.

An internal clock counter defines the start-up time, t_{SU}, since during quasi-resonant operation, the switching frequency and the duration of the start-up time depend on the load, t_{SU} range is indicated in *Table 7*. At the beginning of the start-up time, the drain current limitation progressively rises to the maximum value. In this way a soft-start occurs and the stress on the secondary diode is considerably reduced. It also prevents transformer saturation.

The soft-start time lasts 3.5 ms (VIPER35L) or 4.2 ms (VIPER35H), (see t_{SS} in *Table 7*).

At the start-up, until the output voltage reaches its regulated value, the feedback loop is open and an improper activation of the overload protection could occur. In order to avoid this, OLP logic is disabled and it is active at the end of the start-up phase, $t > t_{SU}$. *Figure 29* and *Figure 30* show two possible start-up cases.

As soon as the output voltage reaches the regulated value, the regulation loop takes over and the drain current is regulated below its limit, I_{Dlim}, by the feedback voltage, which is at a value lower than the V_{FBlin} threshold.

Figure 27. I_{DD} current during start-up and burst mode

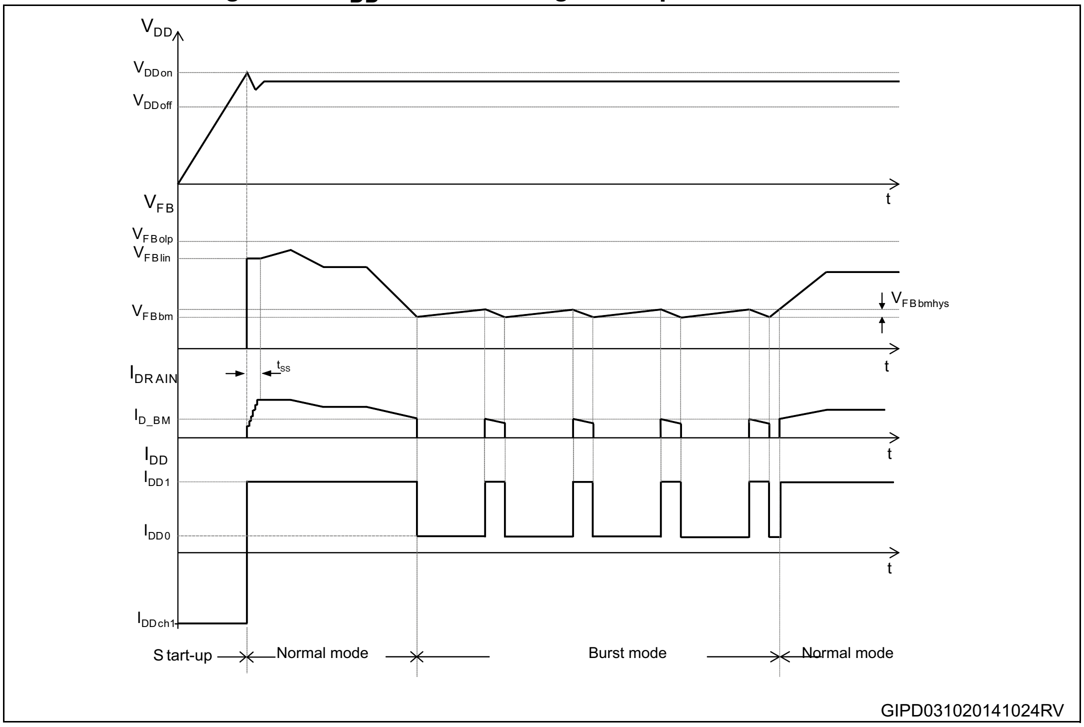


Figure 28. Timing diagram: normal power-up and power-down sequence

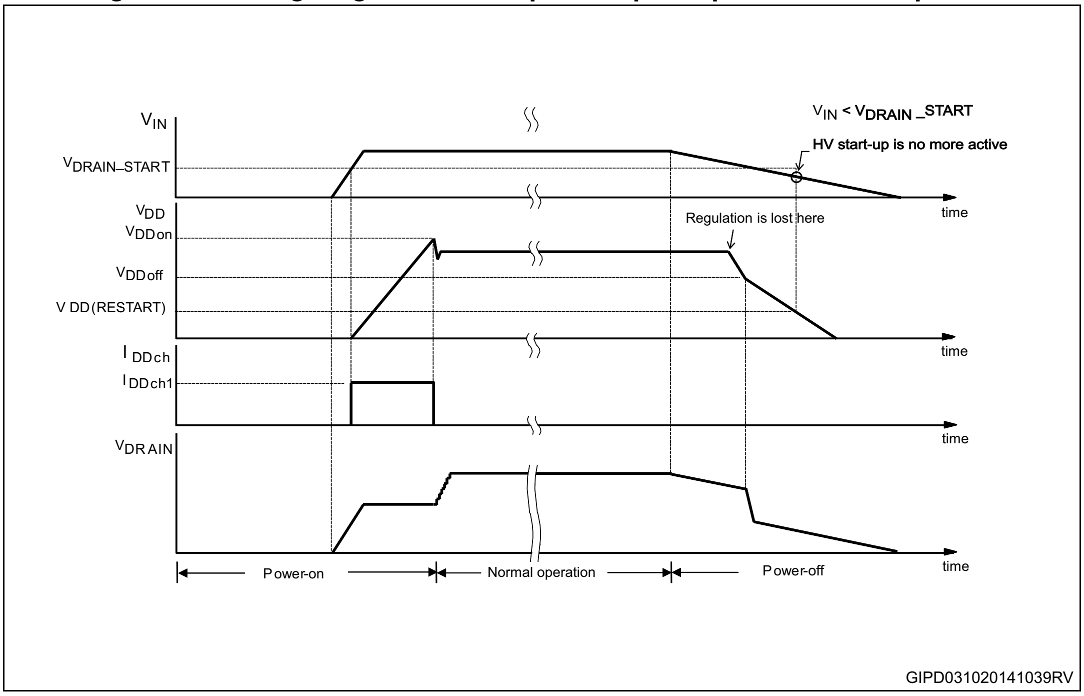


Figure 29. Timing diagram: start-up phase and soft-start (case 1)

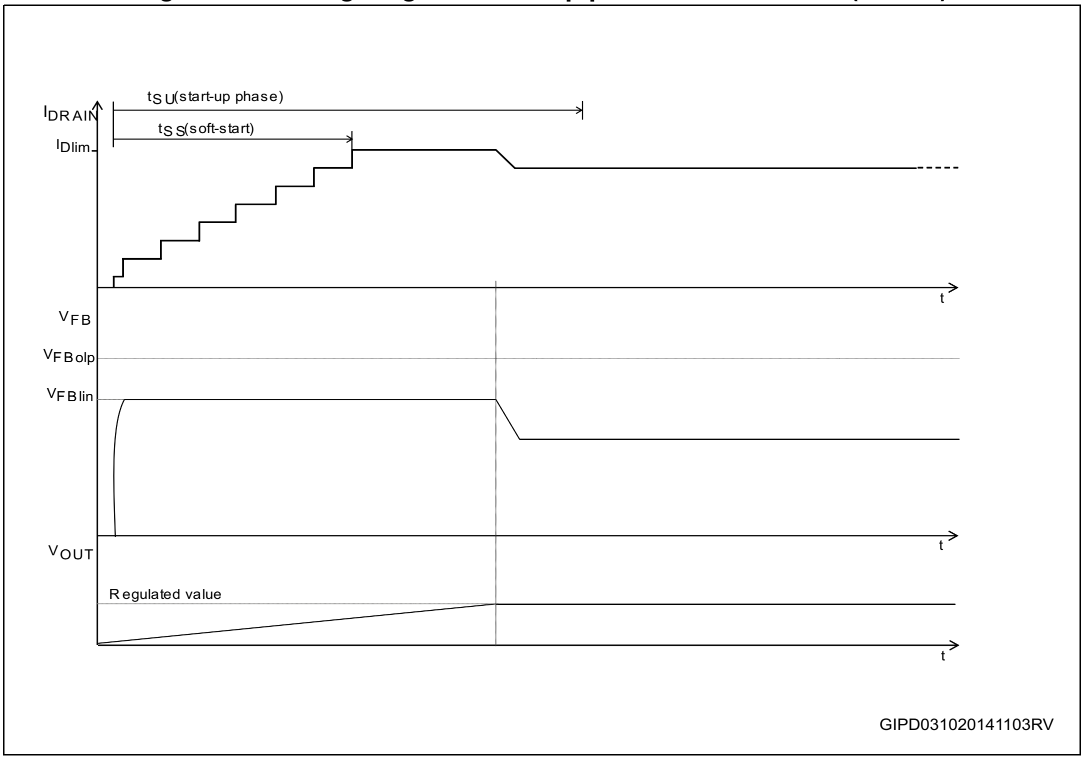
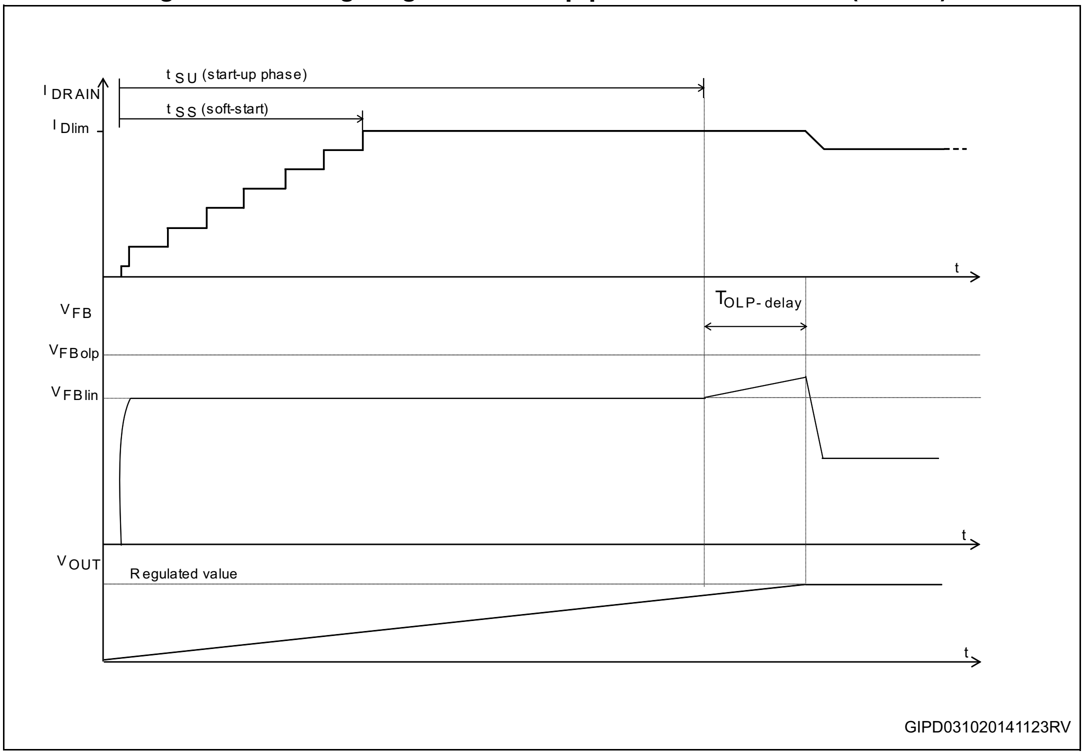


Figure 30. Timing diagram: start-up phase and soft-start (case 2)



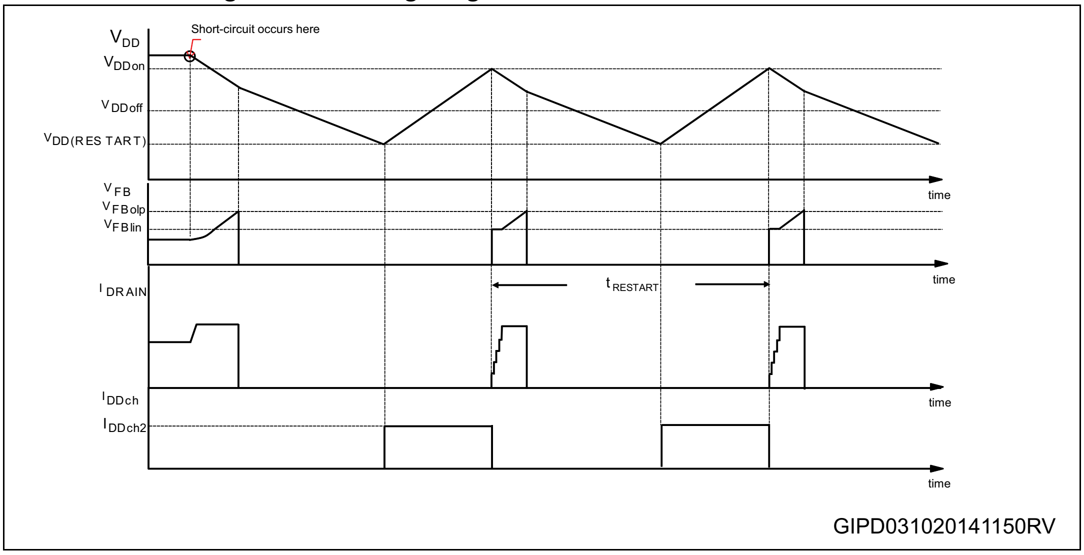
8.4 Power-down description

At converter power-down, the system loses its ability to regulate as soon as the decreasing input voltage is so low to reach the peak current limitation. V_{DD} voltage drops and when it falls below V_{DDoff} threshold (see *Table 7*) the power MOSFET switches off, the energy is interrupted, V_{DD} voltage decreases, the start-up sequence is inhibited and the power-down is completed. This feature prevents any restart attempt and ensures a monotonic output voltage decay during the system power-down.

8.5 Auto-restart description

Every time a protection is tripped, the IC automatically restarts after a duration depending on the discharge and recharge of C_{VDD} capacitor. As shown in *Figure 31*, after a fault, the IC stops and V_{DD} voltage decreases because of IC consumption. As soon as V_{DD} voltage falls below $V_{DD(RESTART)}$ threshold and if the DC input voltage is higher than V_{DRAIN_START} threshold, the internal HV current source turns on and it starts to charge C_{VDD} capacitor with the current I_{DDch2} (0.6 mA, typ.). As soon as V_{DD} voltage reaches $V_{DD(ON)}$ threshold, the IC restarts.

Figure 31. Timing diagram: behavior after short-circuit



8.6 Quasi-resonant operation (QR)

The control core of the VIPER35 is a current mode PWM controller with a zero-current detect circuit designed for quasi-resonant (QR) operation, a technique whose benefits are: minimum turn-on losses, low EMI emission and safe behavior in case of short-circuit. At heavy load the converter operates in quasi-resonant mode; operation synchronizes MOSFET turn-on to the transformer demagnetization by detecting the resulting negative-going edge of the voltage across any winding of the transformer. The system works close to the boundary between discontinuous (DCM) and continuous conduction (CCM) of the transformer and as a result, the switching frequency is different according to different line/load conditions. See the hyperbolic-like portion reported in *Figure 32*.

At medium/ light load, depending on the converter input voltage as well, the device enters valley-skipping mode. An internal oscillator, synchronized to MOSFET turn-on, defines the maximum operating frequency of the converter, F_{OSClim}.

The VIPER35 is available as type 'L' or type 'H', depending on F_{OSClim} value, see *Table 7*. During the normal operation the converter works with a frequency below F_{OSClim}, so the 'L' type is suitable for applications where the priority is on the EMI filter minimization. The 'H' type is suitable when an extended QR operation range or the transformer size reduction are priorities.

As the load is reduced, and the switching frequency tends to exceed the oscillator’s one, MOSFET turn-on doesn’t occur on the first valley but on the second one, the third one and so on. In this way a “frequency clamp” effect is achieved, piecewise linear portion is showed in *Figure 32*.

When the load is extremely light or disconnected, the converter enters burst mode operation. By decreasing the load, the frequency is reduced even few hundred hertz, so to comply with energy saving regulations or recommendations. As the peak current is low, no audible noise occurs.

The above mentioned operation is based on ZCD pin. This pin is the input of the integrated ZCD circuit which allows the power section turn-on at the end of the transformer demagnetization. The input signal for the ZCD is obtained as a partition of the auxiliary voltage used to supply the device, see *Figure 33*.

When the triggering circuit senses a negative-going edge below V_{ZCDTth} threshold (see *Table 7*), after an internal delay that helps to achieve minimum drain-source voltage switch-on (“valley switching”), the power MOSFET turns on. However, to enable power MOSFET turn-on, the triggering circuit has to be previously armed by a positive-going edge exceeding V_{ZCDAth} threshold (see *Table 7*) on the same ZCD pin.

After the MOSFET turn-off, the blanking time, t_{BLANK}, is generated to avoid an erroneous arming and triggering due to the noise, generated by the leakage inductance resonance of the transformer which rings and couples with ZCD pin.

Figure 32. Switching frequency vs power

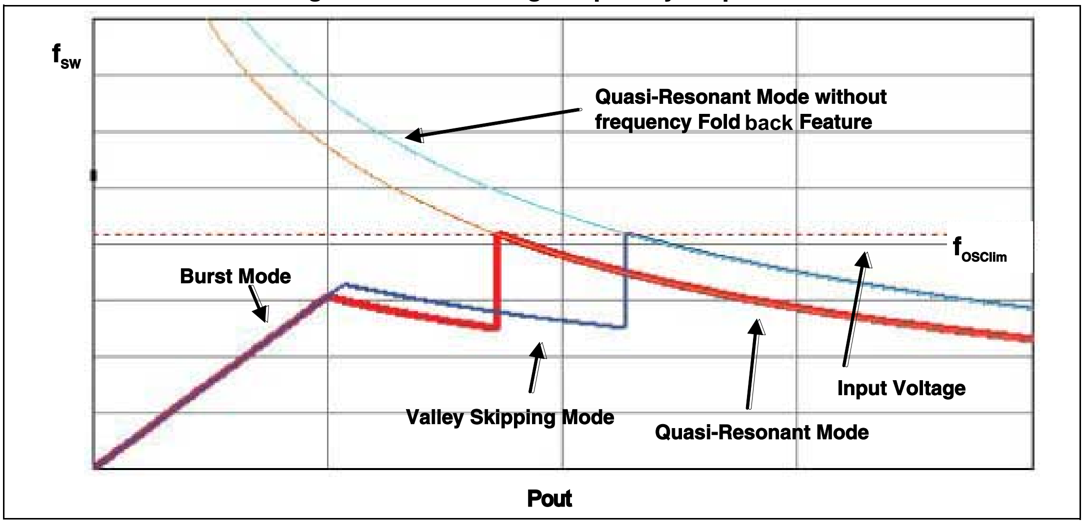
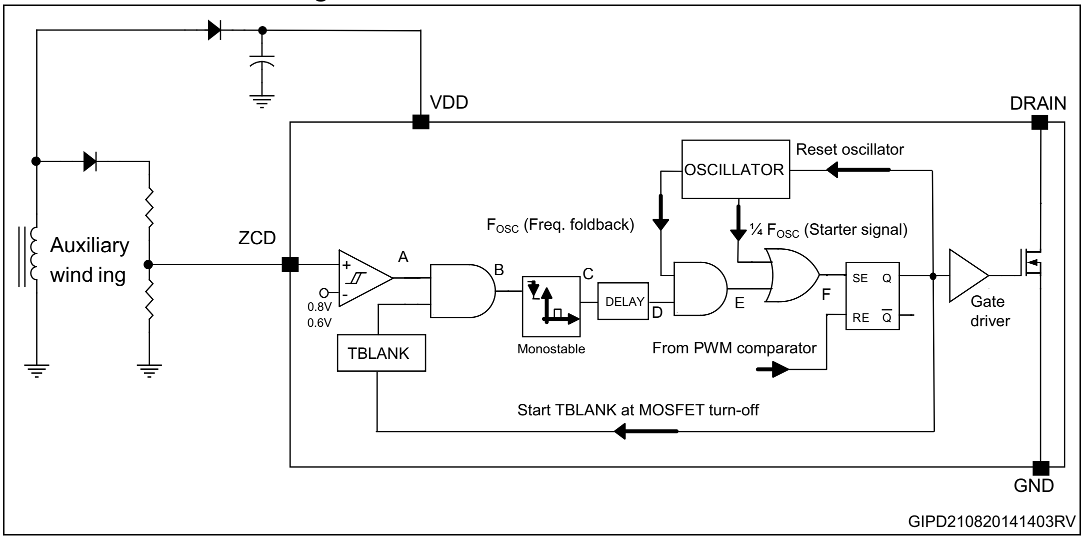


Figure 33. Zero-current detection circuit



8.7 Frequency foldback function and valley-skipping mode

The switching frequency, in quasi-resonant mode, is not fixed and it depends on both the load and the converter input voltage. The switching frequency increases when the load decreases, or when the mains voltage increases, and vice versa. To avoid that, the VIPER35 taps the maximum switching frequency of the application thanks to its control logic.

The frequency limit is given by an internal oscillator switching at 136 kHz for the VIPER35L or at 225 kHz for the VIPER35H, (see parameter F_{OSClim} in *Table 7*). This oscillator is synchronized with the power MOSFET turn-on. When the power MOSFET is off, if the first negative-going edge voltage of the ZCD pin, resulting from transformer demagnetization, appears after at least one oscillator cycle has been completed, the MOSFET turns on and the oscillator is synchronized again.

Otherwise, if the first negative-going edge voltage appears before completing one oscillator cycle, the signal is ignored. Due to the ringing of the drain voltage, the ZCD pin experiences another positive-going edge voltage that arms the circuit and a negative-going edge voltage. Again, if this appears before the oscillator cycle is completed, it is ignored, otherwise the MOSFET turns on and the oscillator is synchronized. In this manner, one or more drain ringing cycles are skipped (*Figure 34* shows the so called “valley-skipping mode”) and the switching frequency doesn’t exceed F_{OSClim} limit.

Figure 34. Drain ringing cycle skipping as the load progressively reduces