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Reference Manual

VL-1260

12-Bit Analog Input Card
for the STD Bus

STD

VERSALOGIC CORPORATION

VL-1260

12-Bit Analog Input Card
for the STD Bus

Model VL-1260

12-Bit Analog Input Card for the STD Bus

REFERENCE MANUAL

VL-1260 Rev. 2.01
Doc. Rev. 09/29/94

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M1260

Table of Contents

Overview

This manual details the installation and operation of VersaLogic's VL-1260 analog input card. This card interfaces directly with external analog voltages and provides digital readings to the STD Bus with 12-bit accuracy.

Introduction

In its standard configuration the VL-1260 provides 16 single-ended, or 8 differential analog input channels. An optional expansion kit increases the number of input channels to 32 single-ended, or 16 differential inputs. It features 12-bit resolution, 25 µs conversion time, and an on-board DC to DC converter (requires +5 volt supply only). The board operates with an input range 0 to +10, or ±10 volts with an adjustable gain of 1 to 1000. It can accommodate input signals in a single-ended, differential, or pseudo-differential configuration.

Each input channel can be read as desired by the system CPU. The board is capable of 25,000 samples per second throughput at a gain of 1 to 150.

The VL-1260 is plug-in compatible with the Analog Devices RTI-1260 card.

Features

- 16 single-ended or 8 differential input channels (expandable to 32 s.e./16 Diff.).
- 12-bit (4096 counts) resolution.
- 25 µs input conversion time.
- 25,000 samples per send throughput.
- 0 to +10, or ±10 volt input ranges.
- Input gain of 1 to 1000.
- 16-bit memory or I/O addressing.
- MEMEX and IOEXP supported.
- +5 volt single supply operation.
- Plug-in replacement for Analog Devices RTI-1260.

Specifications

Specifications are typical at 25°C with 5.0V supply unless otherwise noted.

Number of Channels: 16 single-ended or 8 differential
Range: 0 to +10V, ±10V
Resolution: 12 bits (4096 counts)
Conversion Time: 25 µs + settling time
Throughput:
- 25,000 channels/sec (gain < 150)
- 20,000 channels/sec (gain = 150 to 300)
- 11,000 channels/sec (gain = 1000)

Overvoltage Protection:
- ±35V with power on
- ±20V with power off

Impedance: .6 x 10^8 Ω min.
Data Format: Binary, offset binary, or two's complement
Common Mode Voltage (CMV): ±10V min
Common Mode Rejection (CMR): 78 dB
Linearity: ±½ LSB
Differential Nonlinearity: ±½ LSB
Temperature Coefficient:
- Gain ±30 ppm/°C of FSR (gain = 1)
- Gain ±100 ppm/°C of FSR (gain = 1000)
- Offset ±10 ppm/°C of FSR (gain = 1)
- Offset ±100 ppm/°C of FSR (gain = 1000)

Addressing: 16 bits + MEMEX or IOEXP
Mapping: 8-byte memory or I/O block on any 8-byte boundary
Size: Meets all STD 32 Bus mechanical specifications
Storage Temperature: –40° to +75 °C
Free Air Operating Temperature: 0° to +65 °C
Power Requirements:
- 5V ±5% @ 225 ma typ.

Bus Compatibility:
- STD 80: Full compliance, all bus speeds
- STD Z80: Full compliance, all bus speeds
- STD 32: I/O Slave, SA8

Configuration

Jumper Options

Various options available on the VL-1260 cards are selected using removable jumper blocks (shorting plugs). Features are selected or deselected by installing or removing the jumpers as noted. The terms "In" or "Jumpered" are used to indicate an installed plug: "Out" or "Open" are used to indicate a removed plug.

Figure 2-1 shows the jumper block locations on the VL-1260 card. The figures indicate the position of the jumpers as shipped from the factory.

VL-1260 Jumper Block Locations

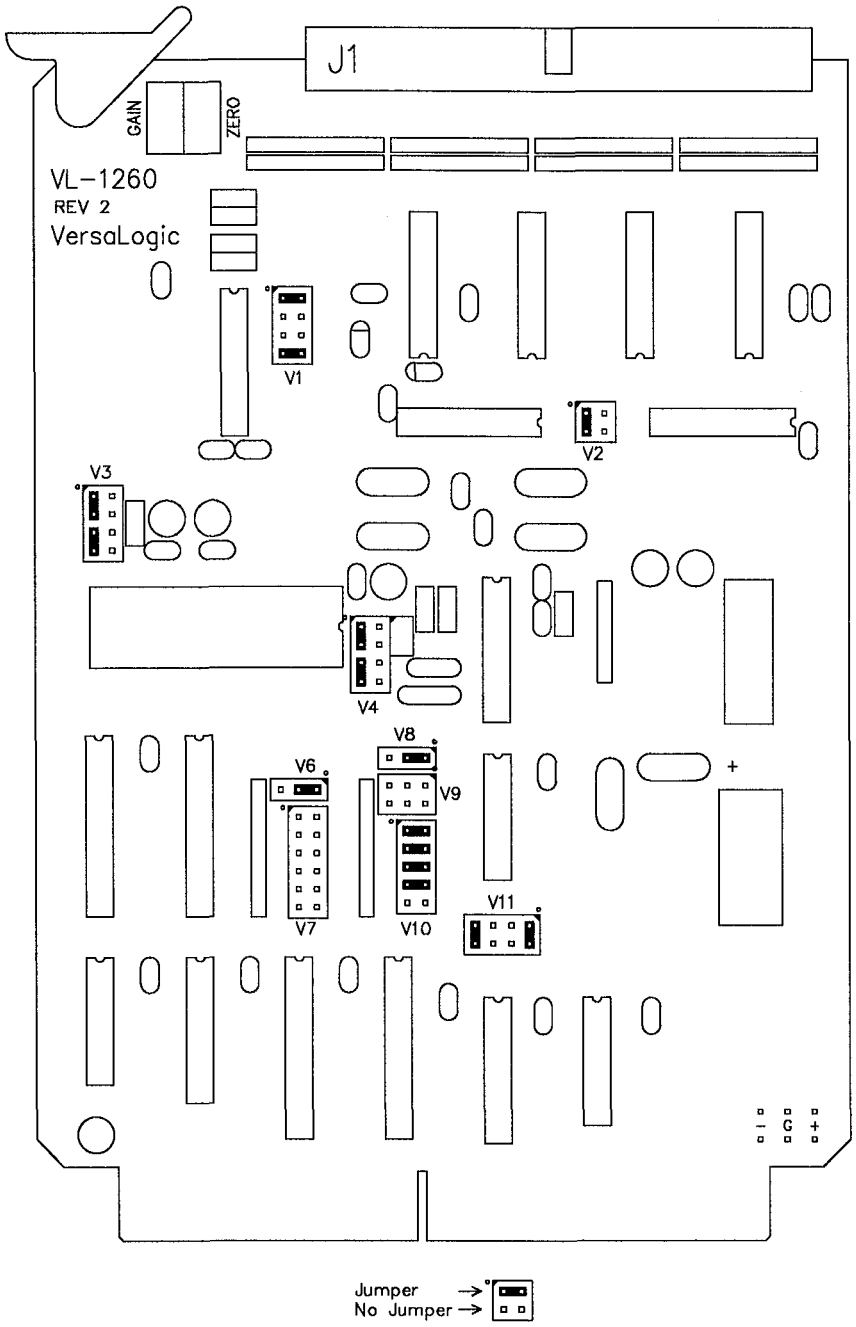


Figure 2-1. Jumper Block Locations for VL-1260

VL-1260 Jumper Options

Jumper Block	Description	As Shipped	Page
V1 & V2	Input Mode	S.E.	2-11
	$V1_{1-2}$ = In, $V1_{3-4}$ = Out, $V1_{5-6}$ = Out, $V1_{7-8}$ = In, $V2_{1-3}$ = In, $V2_{2-4}$ = Out – Single Ended		
	$V1_{1-2}$ = Out, $V1_{3-4}$ = In, $V1_{5-6}$ = Out, $V1_{7-8}$ = In, $V2_{1-3}$ = In, $V2_{2-4}$ = Out – Pseudo-Differential		
	$V1_{1-2}$ = Out, $V1_{3-4}$ = Out, $V1_{5-6}$ = In, $V1_{7-8}$ = Out, $V2_{1-3}$ = Out, $V2_{2-4}$ = In – Differential		
V3	Input Voltage Range Select	±10V	2-14
	$V3_{1-3}$ = In, $V3_{2-4}$ = Out, $V3_{5-7}$ = In, $V3_{6-8}$ = Out – ±10V		
	$V3_{1-3}$ = Out, $V3_{2-4}$ = In, $V3_{5-7}$ = Out, $V3_{6-8}$ = In – 0 to 10V		
V4	Input Data Format	2's Comp.	2-15
	$V4_{1-3}$ = In, $V4_{2-4}$ = Out $V4_{5-7}$ = In, $V4_{6-8}$ = Out – Two's Complement		
	$V4_{1-3}$ = Out, $V4_{2-4}$ = In $V4_{5-7}$ = Out, $V4_{6-8}$ = In – Binary / Offset Binary		
V5	External Trigger – Contact Factory		
V6	MEMEX Select	Ignore	2-5
	$V6_{1-2}$ = In, $V6_{2-3}$ = Out – Ignore MEMEX		
	$V6_{1-2}$ = Out, $V6_{2-3}$ = Out – Enable on MEMEX high		
	$V6_{1-2}$ = Out, $V6_{2-3}$ = In – Enable on MEMEX low		
V7	Board Address (A10 – A15)	FF08H	2-5
	$V7_{1-2}$ = In – A15 decoded Low $V7_{1-2}$ = Out – A15 decoded High		
	$V7_{3-4}$ = In – A14 decoded Low $V7_{3-4}$ = Out – A14 decoded High		
	$V7_{5-6}$ = In – A13 decoded Low $V7_{5-6}$ = Out – A13 decoded High		
	$V7_{7-8}$ = In – A12 decoded Low $V7_{7-8}$ = Out – A12 decoded High		
	$V7_{9-10}$ = In – A11 decoded Low $V7_{9-10}$ = Out – A11 decoded High		
	$V7_{11-12}$ = In – A10 decoded Low $V7_{11-12}$ = Out – A10 decoded High		
V8	IOEXP Select	Ignore	2-5
	$V8_{1-2}$ = In, $V8_{2-3}$ = Out – Ignore IOEXP		
	$V8_{1-2}$ = Out, $V8_{2-3}$ = Out – Enable on IOEXP high		
	$V8_{1-2}$ = Out, $V8_{2-3}$ = In – Enable on IOEXP low		
V9	Board Address (A8, A9) / 8-Bit Mode Selector	FF08H	2-5
	$V9_{1-3}$ = In, $V9_{2-4}$ = In, $V9_{3-5}$ = Out, $V9_{4-6}$ = Out – 8-Bit Mode (ignore A8 & A9)		
	$V9_{1-3}$ = Out, $V9_{2-4}$ = Out, $V9_{3-5}$ = Out, $V9_{4-6}$ = Out – 10- or 16-Bit Decoding (A8 = High, A9 = High)		
	$V9_{1-3}$ = Out, $V9_{2-4}$ = Out, $V9_{3-5}$ = In, $V9_{4-6}$ = Out – 10- or 16-Bit Decoding (A8 = High, A9 = Low)		
	$V9_{1-3}$ = Out, $V9_{2-4}$ = Out, $V9_{3-5}$ = Out, $V9_{4-6}$ = In – 10- or 16-Bit Decoding (A8 = Low, A9 = High)		
	$V9_{1-3}$ = Out, $V9_{2-4}$ = Out, $V9_{3-5}$ = In, $V9_{4-6}$ = In – 10- or 16-Bit Decoding (A8 = Low, A9 = Low)		
V10	Board Address (A3 – A7)	FF08H	2-5
	$V10_{1-2}$ = In – A7 decoded Low $V10_{1-2}$ = Out – A7 decoded High		
	$V10_{3-4}$ = In – A6 decoded Low $V10_{3-4}$ = Out – A6 decoded High		
	$V10_{5-6}$ = In – A5 decoded Low $V10_{5-6}$ = Out – A5 decoded High		
	$V10_{7-8}$ = In – A4 decoded Low $V10_{7-8}$ = Out – A4 decoded High		
	$V10_{9-10}$ = In – A3 decoded Low $V10_{9-10}$ = Out – A3 decoded High		
V11	Address Type Select	Memory	2-5
	$V11_{1-2}$ = In, $V11_{3-4}$ = Out, $V11_{5-6}$ = Out, $V11_{7-8}$ = In – 16-Bit Memory Mapped		
	$V11_{1-2}$ = In, $V11_{3-4}$ = Out, $V11_{5-6}$ = In, $V11_{7-8}$ = Out – 8- or 10-Bit I/O Mapped		
	$V11_{1-2}$ = Out, $V11_{3-4}$ = In, $V11_{5-6}$ = Out, $V11_{7-8}$ = In – 16-Bit I/O Mapped		

Figure 2-2. VL-1260 Jumper Functions

Board Addressing

The VL-1260 supports 8-, 10-, and 16-bit I/O addressing, and 16-bit memory addressing. 8-bit I/O addressing is used with most 8-bit processors (Z80, 8085, 6809, etc.) which provide 256 I/O addresses. 10- or 16-bit addressing can be used with 16-bit processors (8088, 80188, 80186, etc.) to decode 1024 or 65536 I/O port addresses. 16-bit memory addressing can be used with most 8-bit processors (Z80, 8085, 6809, etc.) if desired.

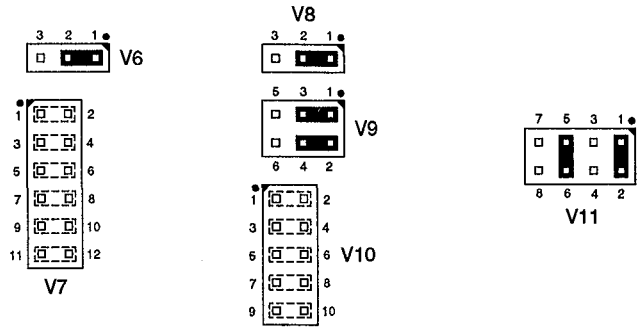
I/O addressing can be extended (capacity doubled) using the IOEXP signal which is decoded by the VL-1260. Memory addressing can be extended (capacity doubled) using the MEMEX signal which is decoded by the VL-1260.

As shipped the board is configured for 16-bit memory addressing with a board address of hex FF08. The card occupies eight consecutive addresses (i.e. FF08H to FF0FH). The VL-1260 uses three of these addresses as control, data, and status registers, the remaining five are inaccessible. See the Register Mapping section on page 4-1 for further information.

8-Bit I/O Addressing

To configure the board for an 8-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate upper and lower halves of the desired starting address (i.e., "3" and "0" = hex address 30).

This jumper configuration ignores the state of the IOEXP signal in addressing the board. To use the IOEXP signal refer to page 2-8.



$V10_{1-2}$	$V10_{3-4}$	$V10_{5-6}$	$V10_{7-8}$	Upper Digit	$V10_{9-10}$	Lower Digit
X	X	X	X	0	X	0
X	X	X	–	1	–	8
X	X	–	X	2		
X	X	–	–	3		
X	–	X	X	4		
X	–	X	–	5		
X	–	–	X	6		
X	–	–	–	7		
–	X	X	X	8		
–	X	X	–	9		
–	X	–	X	A		
–	X	–	–	B		
–	–	X	X	C		
–	–	X	–	D		
–	–	–	X	E		
–	–	–	–	F		

X = Jumper installed
– = Jumper removed

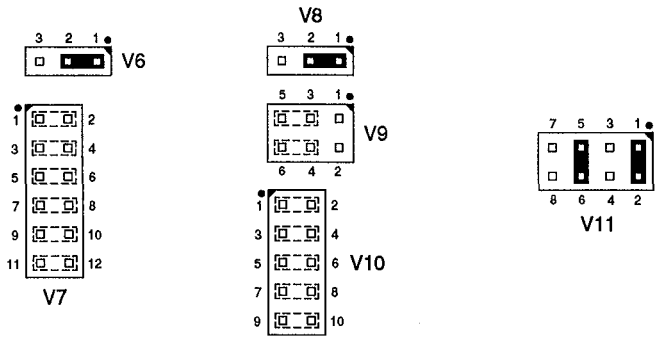
Jumper Block	Description	As Shipped
V6	MEMEX Select	Ignore
V7	Board Address (A10 – A15)	FF08H
V8	IOEXP Select	Ignore
V9	Board Address (A8, A9) / 8-Bit Mode Selector	FF08H
V10	Board Address (A3 – A7)	FF08H
V11	Address Type Select	Memory

Figure 2-3. 8-Bit I/O Address Jumpers

10-Bit I/O Addressing

To configure the board for a 10-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate upper, middle, and lower hex digits of the desired starting address (i.e., "1" and "3" and "0" = hex address 130).

This jumper configuration ignores the state of the IOEXP signal in addressing the board. To use the IOEXP signal refer to page 2-8.



$V9_{3-5}$	$V9_{4-6}$	Upper Digit	$V10_{1-2}$	$V10_{3-4}$	$V10_{5-6}$	$V10_{7-8}$	Middle Digit	$V10_{9-10}$	Lower Digit
X	X	0	X	X	X	X	0	X	0
X	–	1	X	X	X	–	1	–	8
–	X	2	X	X	–	X	2		
–	–	3	X	X	–	–	3		
			X	–	X	X	4		
			X	–	X	–	5		
			X	–	–	X	6		
			X	–	–	–	7		
			–	X	X	X	8		
			–	X	X	–	9		
			–	X	–	X	A		
			–	X	–	–	B		
			–	–	X	X	C		
			–	–	X	–	D		
			–	–	–	X	E		
			–	–	–	–	F		

X = Jumper installed
– = Jumper removed

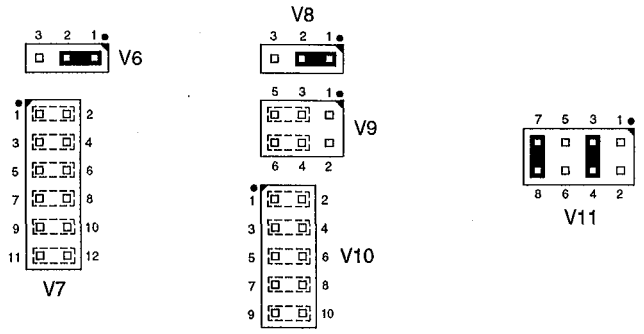
Jumper Block	Description	As Shipped
V6	MEMEX Select	Ignore
V7	Board Address (A10 – A15)	FF08H
V8	IOEXP Select	Ignore
V9	Board Address (A8, A9) / 8-Bit Mode Selector	FF08H
V10	Board Address (A3 – A7)	FF08H
V11	Address Type Select	Memory

Figure 2-4. 10-Bit I/O Address Jumpers

16-Bit I/O Addressing

To configure the board for a 16-bit I/O address refer to the figure below. See the table to select the jumpering for the appropriate four hex digits of the desired starting address (i.e., "6" and "1" and "3" and "0" = hex address 6130).

This jumper configuration ignores the state of the IOEXP signal in addressing the board. To use the IOEXP signal refer to page 2-8.



$V7_{1-2}$	$V7_{3-4}$	$V7_{5-6}$	$V7_{7-8}$	Upper Digit	$V7_{9-10}$	$V7_{11-12}$	$V9_{3-5}$	$V9_{4-6}$	Second Digit	$V10_{1-2}$	$V10_{3-4}$	$V10_{5-6}$	$V10_{7-8}$	Third Digit	$V10_{9-10}$	Lower Digit
X	X	X	X	0	X	X	X	X	0	X	X	X	X	0	X	0
X	X	X	–	1	X	X	X	–	1	X	X	X	–	1	–	8
X	X	–	X	2	X	X	–	X	2	X	X	–	X	2		
X	X	–	–	3	X	X	–	–	3	X	X	–	–	3		
X	–	X	X	4	X	–	X	X	4	X	–	X	X	4		
X	–	X	–	5	X	–	X	–	5	X	–	X	–	5		
X	–	–	X	6	X	–	–	X	6	X	–	–	X	6		
X	–	–	–	7	X	–	–	–	7	X	–	–	–	7		
–	X	X	X	8	–	X	X	X	8	–	X	X	X	8		
–	X	X	–	9	–	X	X	–	9	–	X	X	–	9		
–	X	–	X	A	–	X	–	X	A	–	X	–	X	A		
–	X	–	–	B	–	X	–	–	B	–	X	–	–	B		
–	–	X	X	C	–	–	X	X	C	–	–	X	X	C		
–	–	X	–	D	–	–	X	–	D	–	–	X	–	D		
–	–	–	X	E	–	–	–	X	E	–	–	–	X	E		
–	–	–	–	F	–	–	–	–	F	–	–	–	–	F		

X = Jumper installed
– = Jumper removed

Jumper Block	Description	As Shipped
V6	MEMEX Select	Ignore
V7	Board Address (A10 – A15)	FF08H
V8	IOEXP Select	Ignore
V9	Board Address (A8, A9) / 8-Bit Mode Selector	FF08H
V10	Board Address (A3 – A7)	FF08H
V11	Address Type Select	Memory

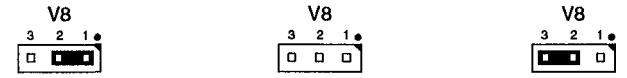
Figure 2-5. 16-Bit I/O Address Jumpers

IOEXP Signal

The IOEXP (I/O expansion) signal on the STD Bus is normally used to select between two different I/O banks or maps. It can be used to double the number of available I/O addresses in the system (by selecting between two banks of I/O boards). The IOEXP signal is usually controlled by (or jumpered to ground on) the system CPU card.

A low IOEXP signal usually selects the standard or normal I/O map. A high IOEXP signal usually selects the secondary or alternate I/O map. Boards that ignore (or do not decode) IOEXP will appear in both I/O maps.

As shipped the IOEXP jumper is configured to ignore the IOEXP signal. The board will be addressed whether the IOEXP signal is high or low. It can be jumpered for two other modes as shown below.



Ignore IOEXP* | Decode on IOEXP* High | Decode on IOEXP* Low

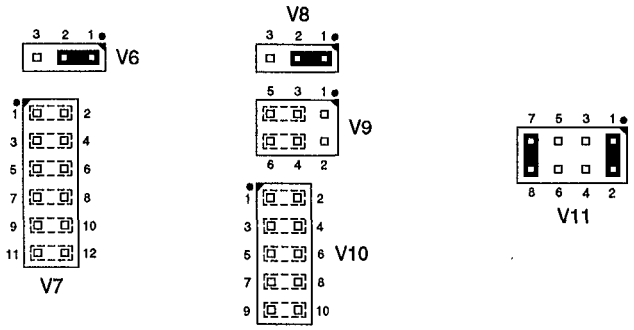
Jumper Block	Description			As Shipped
V8	IOEXP Select			Ignore
	$V8_{1-2}$ = In,	$V8_{2-3}$ = Out	– Ignore IOEXP	
	$V8_{1-2}$ = Out,	$V8_{2-3}$ = Out	– Enable on IOEXP high	
	$V8_{1-2}$ = Out,	$V8_{2-3}$ = In	– Enable on IOEXP low	

Figure 2-6. IOEXP Options

16-Bit Memory Addressing

To configure the board for a 16-bit memory address refer to the figure below. Use the table to select the jumpering for the appropriate four hex digits of the desired starting address (i.e., "6" and "1" and "3" and "0" = hex address 6130).

This jumper configuration ignores the state of the MEMEX signal in addressing the board. To use the MEMEX signal refer to the MEMEX Signal heading in this section.



$V7_{1-2}$	$V7_{3-4}$	$V7_{5-6}$	$V7_{7-8}$	Upper Digit	$V7_{9-10}$	$V7_{11-12}$	$V9_{3-5}$	$V9_{4-6}$	Second Digit	$V10_{1-2}$	$V10_{3-4}$	$V10_{5-6}$	$V10_{7-8}$	Third Digit	$V10_{9-10}$	Lower Digit
X	X	X	X	0	X	X	X	X	0	X	X	X	X	0	X	0
X	X	X	–	1	X	X	X	–	1	X	X	X	–	1	–	8
X	X	–	X	2	X	X	–	X	2	X	X	–	X	2		
X	X	–	–	3	X	X	–	–	3	X	X	–	–	3		
X	–	X	X	4	X	–	X	X	4	X	–	X	X	4		
X	–	X	–	5	X	–	X	–	5	X	–	X	–	5		
X	–	–	X	6	X	–	–	X	6	X	–	–	X	6		
X	–	–	–	7	X	–	–	–	7	X	–	–	–	7		
–	X	X	X	8	–	X	X	X	8	–	X	X	X	8		
–	X	X	–	9	–	X	X	–	9	–	X	X	–	9		
–	X	–	X	A	–	X	–	X	A	–	X	–	X	A		
–	X	–	–	B	–	X	–	–	B	–	X	–	–	B		
–	–	X	X	C	–	–	X	X	C	–	–	X	X	C		
–	–	X	–	D	–	–	X	–	D	–	–	X	–	D		
–	–	–	X	E	–	–	–	X	E	–	–	–	X	E		
–	–	–	–	F	–	–	–	–	F	–	–	–	–	F		

X = Jumper installed
– = Jumper removed

Jumper Block	Description	As Shipped
V6	MEMEX Select	Ignore
V7	Board Address (A10 – A15)	FF08H
V8	IOEXP Select	Ignore
V9	Board Address (A8, A9) / 8-Bit Mode Selector	FF08H
V10	Board Address (A3 – A7)	FF08H
V11	Address Type Select	Memory

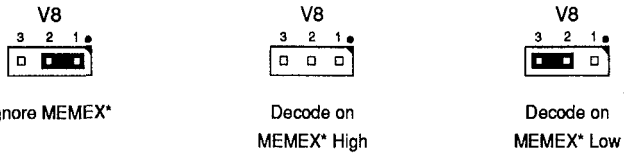
Figure 2-7. 16-Bit Memory Address Jumpers

MEMEX Signal

The MEMEX (memory expansion) signal on the STD Bus is normally used to select between two different memory banks or maps. It can be used to double the number of available memory addresses in the system (by selecting between the two memory banks). The MEMEX signal is usually controlled by (or jumpered to ground on) the system CPU card.

A low MEMEX signal usually selects the standard or normal memory map. A high MEMEX signal usually selects the secondary or alternate memory map. Boards that ignore (or do not decode) MEMEX will appear in both memory maps.

As shipped the MEMEX jumper is configured to ignore the MEMEX signal. The board will be addressed whether the MEMEX signal is high or low. It can be jumpered for two other modes as shown below.



Jumper Block	Description	As Shipped
V6	MEMEX Select	Ignore
	$V6_{1-2}$ = In, $V6_{2-3}$ = Out – Ignore MEMEX	
	$V6_{1-2}$ = Out, $V6_{2-3}$ = Out – Enable on MEMEX high	
	$V6_{1-2}$ = Out, $V6_{2-3}$ = In – Enable on MEMEX low	

Figure 2-8. MEMEX Options

Analog Input Configuration

The VL-1260 board accommodates 16 single-ended or 8 differential channels. An option kit for the VL-1260 (Part #9672), expands the board to accommodate 32 single-ended or 16 differential channels.

Input Mode

The VL-1260 board can be configured for three types of voltage inputs: differential, single-ended, and pseudo-differential. In addition, by adding an external user-supplied 500 Ω resistor, the VL-1260 can be hooked up to a 4-20 ma current loop. All inputs connected to the boards must be of the same type.

Typical connections for the three input modes are shown in the figures below. Since ground loops (current flowing between various equipment ground lines) affect analog measurements made with reference to ground, careful attention should be paid to the ground connections shown. In particular, the STD Bus power supply logic ground line should never be connected to earth ground when operating in the differential or pseudo-differential modes.

Single Ended Mode

The single-ended mode is used for signals that are referenced to a common ground. It is normally used only for higher level signals on short distance runs (less than 10 feet). In this mode up to 16 input channels can be accommodated.

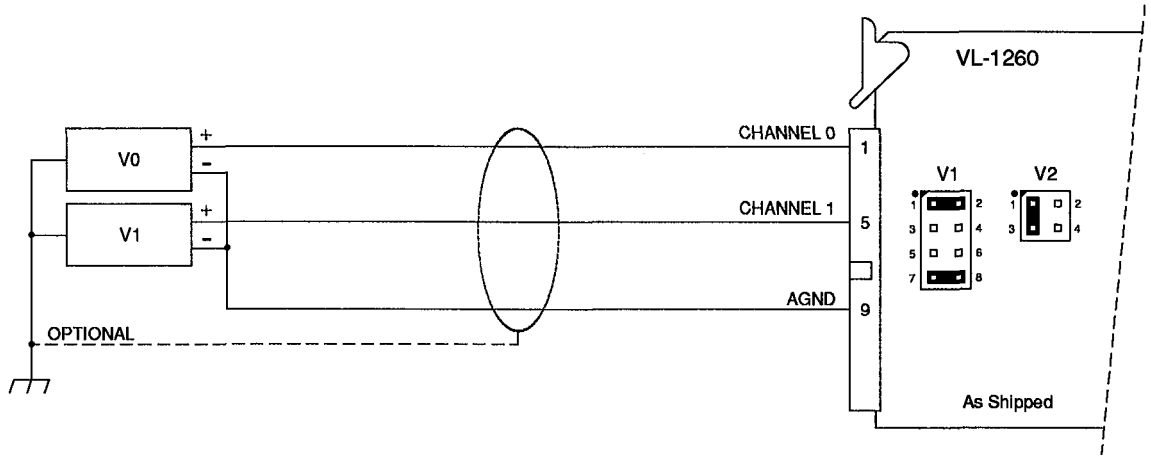


Figure 2-9. Single Ended Input Mode

Pseudo-Differential Mode

The pseudo-differential mode is used for signals that are not referenced to ground, but are all connected to a single common return line. This mode can provide most of the advantages of full differential input while requiring fewer total wires. In the pseudo-differential mode, 16 input channels can be accommodated.

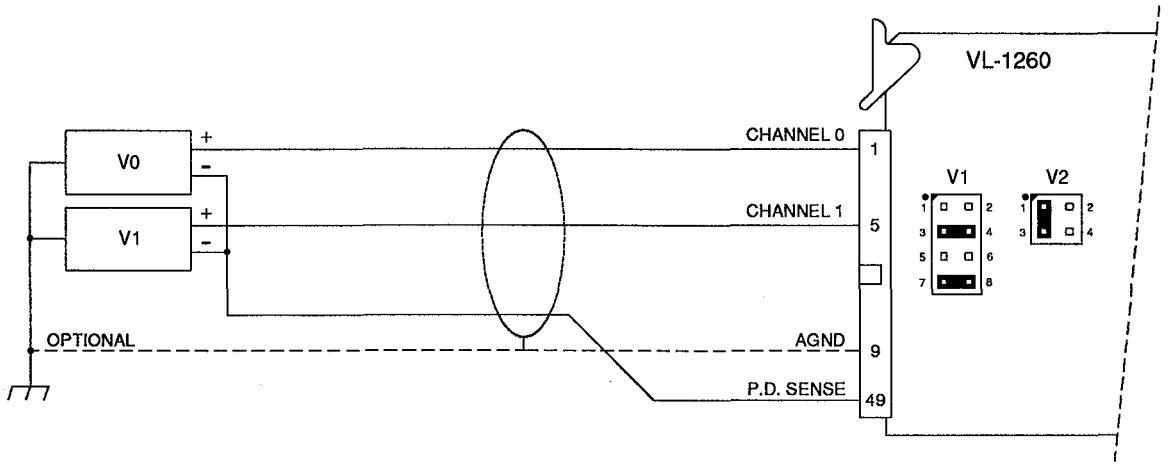


Figure 2-10. Pseudo-Differential Input Mode

Differential Mode

The differential mode is used for signals that are not referenced to a common or ground point, but simply have a voltage difference between the two input wires (usually a twisted pair). It is desirable to use the differential mode in electrically noisy environments since it reduces the effects of electromagnetically induced noise and ground currents. It is especially useful in eliminating the effects of common mode noise generated on input lines over longer distances. In the differential mode, only eight input channels are available.

Note that in full differential operation a return path must be provided for the bias currents of the input amplifier. This can be accomplished by grounding the voltage source power supply(s) to the VL-1260 board, or by installing a 10K to 100K Ω resistor as shown for each channel. These resistors should be located in close proximity to the voltage source.

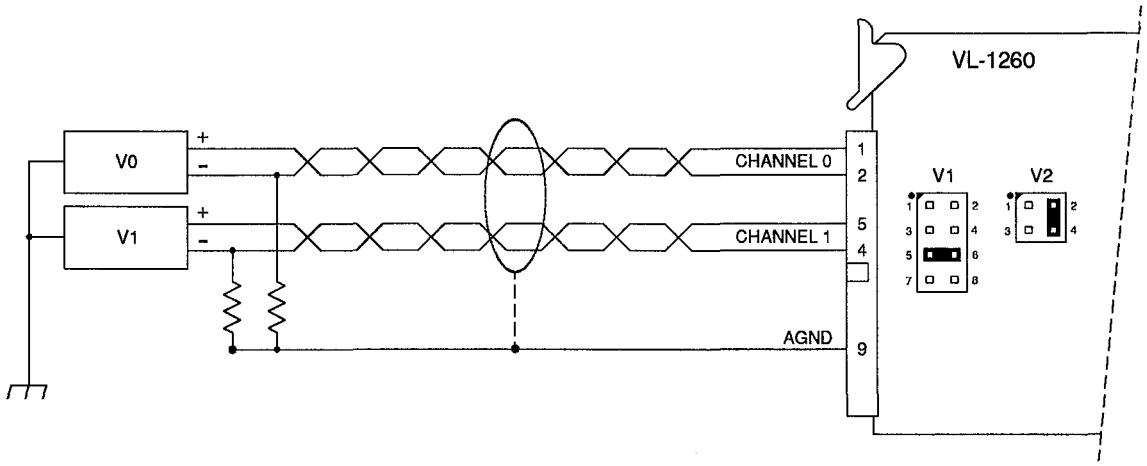


Figure 2-11. Differential Input Mode

Current Loop Mode

While the VL-1260 cannot directly hook up to a 4-20 ma current loop, the addition of an external user-supplied 500 Ω precision dropping resistor can be used to develop a 2-10 volt signal proportional to the 4-20 ma current. This voltage is applied to the VL-1260 as a differential-mode signal. The input range should be jumpered for unipolar 0 to 10V operation. The circuit below can be repeated for all 8 differential input channels.

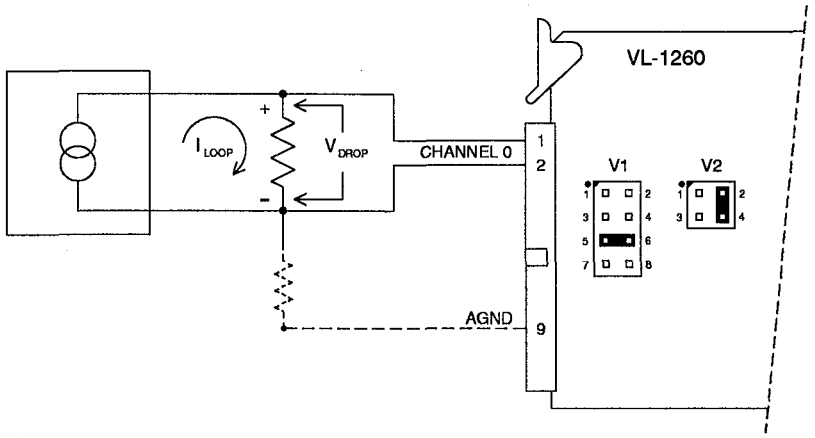
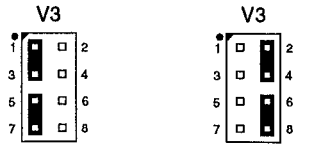


Figure 2-12. Current Loop Input Mode

Input Voltage Range

The board may be operated with an input range of 0 to +10 volts, or ±10 volts. The 0 to +10 volt range is preferred for signals which do not go negative, since the per volt resolution is twice that of the ±10 volt range. Input voltage range selection applies to all input channels.



Jumper Block	Description	As Shipped
V3	Input Voltage Range Select	±10V
	$V3_{1-3}$ = In, $V3_{2-4}$ = Out, $V3_{5-7}$ = In, $V3_{6-8}$ = Out	– ±10V
	$V3_{1-3}$ = Out, $V3_{2-4}$ = In, $V3_{5-7}$ = Out, $V3_{6-8}$ = In	– 0 to 10V

Figure 2-13. Input Range Selection

Input Gain

The on-board instrumentation amplifier allows low level input signals to be amplified to the full scale input range of the board so that they can be read with the full resolution available (one part in 4096).

The amplifier gain is determined by parallel resistors R1 and R2. The resulting gain applies to all channels on the board.

As shipped, the gain of the amplifier is set to one. Other gains may be selected using the following formula:

$$Rg = \left[\frac{20K\,\Omega}{(gain - 1)} \right]$$

To change the gain, use one of the resistors for coarse adjustment (use the largest standard resistor value above Rg). Use the second resistor to fine tune the total resistance. The resistor(s) used should be a high-stability metal film type (RN55 style, ±25ppm/°C typ.).

Settling Time

The VL-1260 board includes a delay between the time a channel is selected for reading (by a software command), and the start of the actual A/D conversion. This delay allows the multiplexer and sample/hold circuitry to properly settle for a more accurate reading.

With an input gain of 1, the standard 15 microsecond delay (as shipped) is appropriate. For higher gains, an additional capacitor should be installed in position CT as shown in the table below.

Use of settling times less than those shown will decrease the accuracy of readings beyond ±1 LSB.

Gain	Value for CT	Settling Time
1–150	(Open)	15 µs
151–300	680 pf	20 µs
301–500	1500 pf	30 µs
501–700	3300 pf	40 µs
701–1000	6200 pf	85 µs

Figure 2-14. Settling Time

Input Data Format

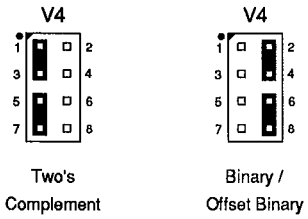
The digital data format for the analog input channels can be jumpered for binary, offset binary, or two's complement. The configuration affects all channels.

The selection is dependent upon the input voltage range selected with jumper V3. Unipolar voltages should use the binary data format. Bipolar voltages can use two's complement or offset binary formats, however, two's complement is is the best choice since it "maps" the positive and negative voltages into positive and negative digital values.

See the Input Data Representation section starting on page 4-4 for further information on the various analog input data formats.

Input Range	Valid Input Data Formats
0 to +10V	Binary
±10V	Offset Binary or Two's Complement

Figure 2-15. Valid Input Data Formats



Jumper Block	Description	As Shipped
V4	Input Data Format	2's Complement
	$V4_{1-3}$ = In, $V4_{2-4}$ = Out, $V4_{5-7}$ = In, $V4_{6-8}$ = Out	– Two's Complement
	$V4_{1-3}$ = Out, $V4_{2-4}$ = In, $V4_{5-7}$ = Out, $V4_{6-8}$ = In	– Binary / Offset Binary

Figure 2-16. Input Data Format Options