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Reference Manual

VL-7614

64-Line TTL Interface Card
for the STD Bus

VERSALOGIC
CORPORATION

VL-7614
VL-76CT14

64-Line TTL Interface Card
for the STD Bus

Model VL-7614

64-Line TTL Interface Card for the STD Bus

REFERENCE MANUAL

VL-7614 Rev. 2.00
Doc. Rev. 01/04/94

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M7614

Model VL-7614
64-Line TTL Interface Card

REFERENCE MANUAL

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VL-7614 Parts Placement Diagram
VL-7614 Schematic
VL-7614 Parts List
VL-76CT14 Parts List

STD Bus Pinout
ASCII Table

VersaLogic Corporation
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Section 1
OVERVIEW

INTRODUCTION

This manual details the installation and operation of VersaLogic's VL-7614 interface card. This card provides 64 TTL type I/O lines for general purpose interfacing requirements.

The VL-7614 is available in standard (VL-7614) and extended temperature (VL-76CT14) versions. Throughout this manual "VL-7614" will be used to refer to both versions of these boards, unless specifically noted otherwise.

OVERVIEW

The VL-7614 card provides 64 TTL type input/output lines. Grouped as 8 ports of 8 lines, each port can be configured as 8 inputs, 8 outputs, or 8 outputs with readback.

I/O configuration is accomplished by physically removing or inserting selected chips from the board (one input and output chip per 8-bit port). This allows the board to be configured in any combination of input and output ports desired.

Each 8-bit port of non-inverting input lines can be read at any time by the system processor. Pull-up resistors are included to assure that unconnected lines do not have an undetermined state. Input ports can also be used in conjunction with output ports to "read back" the output data. LS244 type chips with .4V hysteresis (ACT244 in the extended temperature version) are used for the data input buffers.

The output lines are non-inverting and can drive 17 LS TTL loads (6.8 ma sink, 3.5 ma CT version). When a port is used for output, it can optionally be configured with the corresponding input buffer left in place. This allows the state of the output lines for that port to be read by the processor. This function, usually called port readback, can be used to simplify programming and assure correct program operation in many applications. LS273 type chips (HCT273 in the extended temperature version) are used for the data output latches.

External connections are made through four 34-pin latching connectors. Each connector interfaces sixteen I/O lines (two 8-bit ports) to external devices. Alternating ground lines, paired with each signal line, improve noise immunity and reduce cross talk.

The VL-7614 features 8 and 10-bit addressing, and is compatible with all common STD Bus processor types. The IOEXP line is also supported.

The VL-7614 normally occupies eight consecutive I/O addresses. It can alternately be mapped into only four I/O addresses when it is configured as four input ports and four output ports.

The board is fully compatible with the Pro-Log 7614 card.

FEATURES

- Eight 8-bit I/O Ports.
- 6.8 ma output drive (3.5 ma CT version).
- 8 or 10-bit I/O addressing.
- IOEXP supported.
- Latching I/O connectors.
- Extended temperature version available.
- Universal STD Bus processor compatible.
- Plug-in replacement for Pro-Log 7614.

SPECIFICATIONS

Size: Meets all STD Bus mechanical specifications

Storage Temperature:
- VL-7614: -40· to +75· C
- VL-76CT14: -40· to +85· C

Free Air Operating Temperature:
- VL-7614: 0· to +65· C
- VL-76CT14: -40· to +85· C

Power Requirements:
- VL-7614: 5V ±5% @ 450 ma typ. (all outputs high)
  5V ±5% @ 540 ma typ. (all outputs low)

- VL-76CT14: 5V ±10% @ 5.5 ma typ. (all outputs high)
  5V ±10% @ 38.5 ma typ. (all outputs low)

I/O Port Interface:
- VL-7614: Low level output drive: 6.8 ma @ .35V
  High level output drive: .9 ma @ 2.7V
  Input load: 1.2 ma @ .35V (4.7K ohm pull-up)

- VL-76CT14: Low level output drive: 3.5 ma @ .1V
  High level output drive: 4.0 ma @ 4.9V
  Input load .5 ma @ .1V (10K ohm pull-up)

Section 2
CONFIGURATION

JUMPER SUMMARY

Various options available on the VL-7614 card are selected using removable jumper plugs (shorting plugs). Features are selected or deselected by installing or removing the jumper plugs as noted. The terms "IN" or "JUMPED" are used to indicate an installed plug. "OUT" or "OPEN" indicates the absence of a jumper plug.

The function of each jumper block is detailed in Figure 2-1. Figure 2-2 shows the jumper block locations on the VL-7614 board. It indicates the position of the jumper plugs as shipped from the factory.

Jumper Block	Description	As Shipped
V1	10-bit address control. See Board Address. a - A9 control. b - A8 control.	 a - ignore A9 b - ignore A8
V2	Board address. See Board Address.	Hex 00
V3	Addressing control. See Board Address. a - A2 control (4-port mode only). b - IOEXP control.	 Ignore A2 Ignore IOEXP
V4	4 or 8-port mapping. See Mapping Mode.	8-port mode

Figure 2-1. Jumper Functions

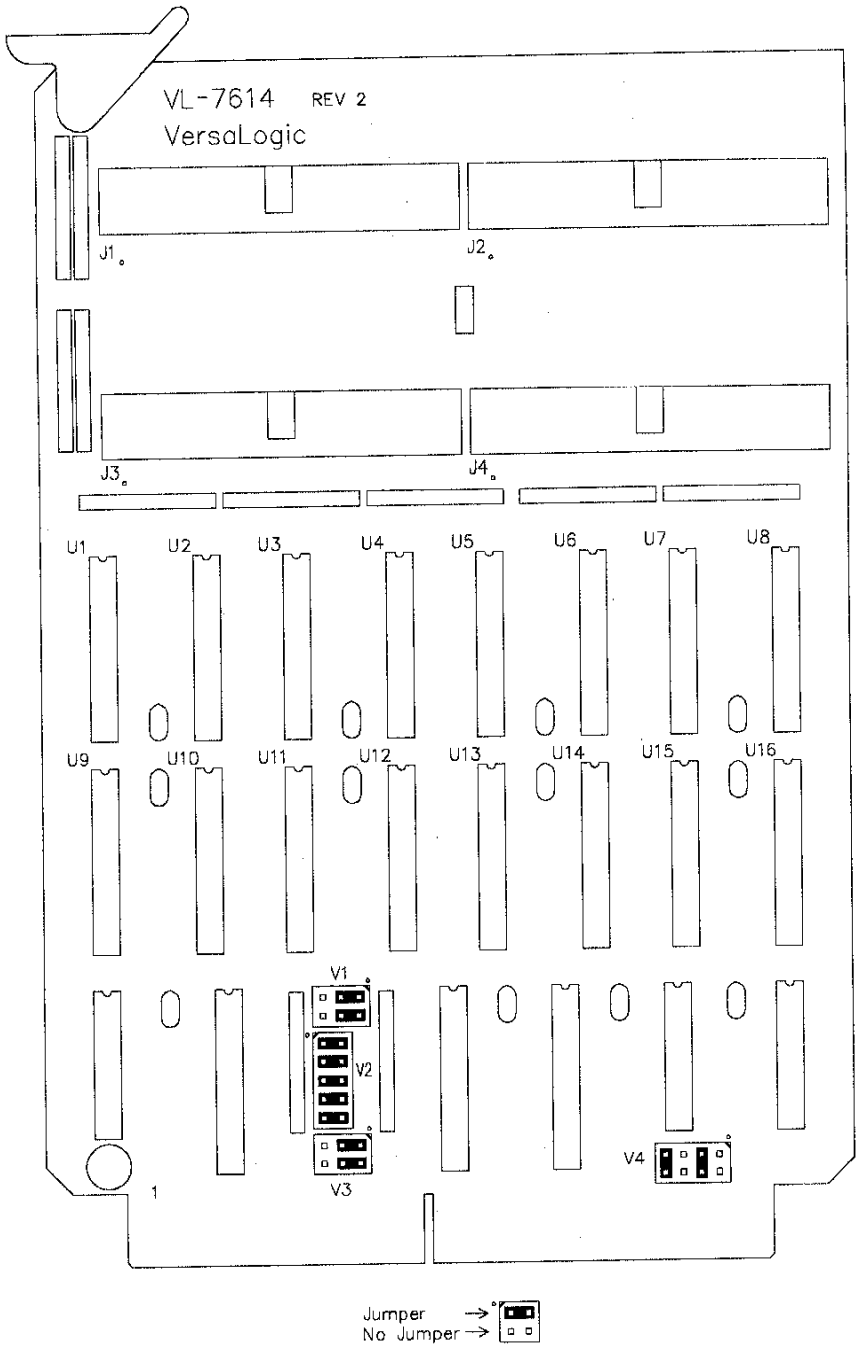


Figure 2-2. Jumper Block Locations

BOARD ADDRESS

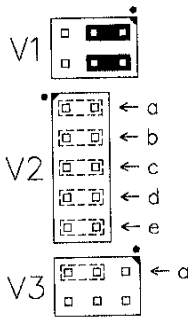
The VL-7614 supports both 8 and 10-bit I/O addressing. 8-bit addressing is used with most 8-bit processors (Z80, 8085, 6809, etc.) which provide 256 I/O addresses. 10-bit addressing can be used with 16-bit processors (i.e. 8088) to decode up to 1024 I/O port addresses.

Both 8 and 10-bit addressing can be extended (capacity doubled) using the IOEXP signal which is decoded by the VL-7614.

As shipped the board is configured for 8-bit addressing with a board address of hex 00. The VL-7614 normally occupies eight consecutive I/O addresses (i.e. 00-07). If it is configured as four input ports and four output ports it can optionally be mapped into only four I/O ports.

8-Bit Addressing

To configure the board for an 8-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate upper and lower halves of the desired starting address (i.e. "3" and "0" = hex address 30).



V2				Upper
a	b	c	d	Digit
X	X	X	X	0
X	X	X	-	1
X	X	-	X	2
X	X	-	-	3
X	-	X	X	4
X	-	X	-	5
X	-	-	X	6
X	-	-	-	7
-	X	X	X	8
-	X	X	-	9
-	X	-	X	A
-	X	-	-	B
-	-	X	X	C
-	-	X	-	D
-	-	-	X	E
-	-	-	-	F

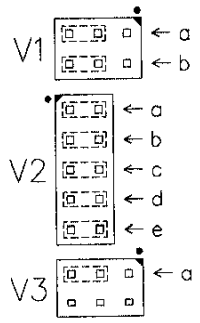
V2	V3	Lower
e	a*	Digit
X	X	0
X	-	4
-	X	8
-	-	C

X = Jumper installed.
- = Jumper removed.
* Jumper V3a is used only with optional 4-port mapping. Otherwise the lower hex digit will be 0 or 8 (per the position of V2e).

Figure 2-3. 8-Bit Address Jumpers

10-Bit Addressing

To configure the board for a 10-bit I/O address refer to the figure below. Use the table to select the jumpering for the appropriate upper, middle, and lower hex digits of the desired address (i.e. "1" and "3" and "0" = hex address 130).



V1 a	V1 b	Upper Digit
X	X	0
X	-	1
-	X	2
-	-	3

V2 a	V2 b	V2 c	V2 d	Middle Digit
X	X	X	X	0
X	X	X	-	1
X	X	-	X	2
X	X	-	-	3
X	-	X	X	4
X	-	X	-	5
X	-	-	X	6
X	-	-	-	7
-	X	X	X	8
-	X	X	-	9
-	X	-	X	A
-	X	-	-	B
-	-	X	X	C
-	-	X	-	D
-	-	-	X	E
-	-	-	-	F

V2 e	V3 a*	Lower Digit
X	X	0
X	-	4
-	X	8
-	-	C

X = Jumper installed.
- = Jumper removed.
* Jumper V3a is used only with optional 4-port mapping. Otherwise the lower hex digit will be 0 or 8 (per the position of V2e).

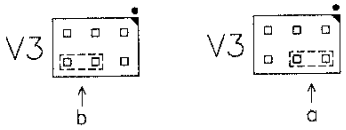
Figure 2-4. 10-Bit Address Jumpers

IOEXP Signal

The IOEXP (I/O expansion) signal on the STD Bus is normally used to select between two different I/O banks or maps. It can be used to double the number of available I/O addresses in the system (by selecting between two banks of I/O boards). The IOEXP signal is usually controlled by (or jumpered to ground on) the system CPU card.

A low IOEXP signal usually selects the standard or normal I/O map. A high IOEXP signal usually selects the secondary or alternate I/O map. Boards that ignore (or do not decode) IOEXP will appear in both I/O maps.

As shipped the IOEXP jumper is configured to ignore the IOEXP signal. The board will be addressed whether the IOEXP signal is high or low. It can be jumpered for two other modes as shown in Figure 2-5.



Jumper Block	Description	As Shipped
V3	a - Ignore IOEXP (enable high or low).	a - IN
	b - Enable on IOEXP low.	b - out
	None - Enable on IOEXP high (no jumpers).	

Figure 2-5. IOEXP Options

MAPPING MODE

The VL-7614 normally occupies eight I/O port addresses. In this mode the I/O ports can be configured in any way desired (all inputs, all outputs or any mix).

Optionally the board can be configured to occupy only four I/O port addresses. In this mode the I/O ports must be configured as four input channels and four output channels. This mode is advantageous only when there are many I/O boards in the system and the I/O map is becoming full.

Unless system I/O addresses are very scarce (all 256 or more being used), the board should be used in the 8-port mode.

8-Port Mapping

To configure the board for 8-port mapping, jumper the board as shown below. In this mode jumper V3a is ignored when selecting the starting address for the board and should be located as shown below.

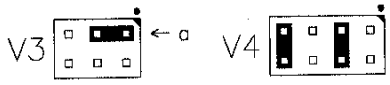


Figure 2-6. 8-Port Mapping

4-Port Mapping

To configure the board for 4-port mapping, jumper the board as shown below. In this mode jumper V3a is used for addressing the board and should be inserted or removed from the position shown according to the addressing tables in the preceding sections.

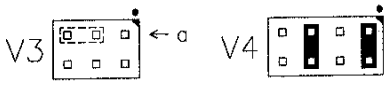


Figure 2-7. 4-Port Mapping

I/O PORTS

The I/O ports are configured for input or output by removing selected chips from the board. The board is arranged as 8 channels of 8 lines each (64 lines total). Each group of 8 lines can be configured as either input or output lines.

As shipped, with all the chips on the board, the VL-7614 is configured as 8 output channels. To configure any of the channels for input the output chip (for that channel) is removed from the board.

Normally it is desirable to leave the input chip installed on channels used for output. This allows the current state of the output lines to be read if desired. If this feature is not needed, the input chips can be removed to save a small amount of power.

In the standard 8-port mode, any of the eight channels (0-7) can be configured as inputs or outputs as desired. The figure below shows an example of a typical configuration. It shows the location of the input and output chips for each channel, and how the channels would appear on the I/O connectors.

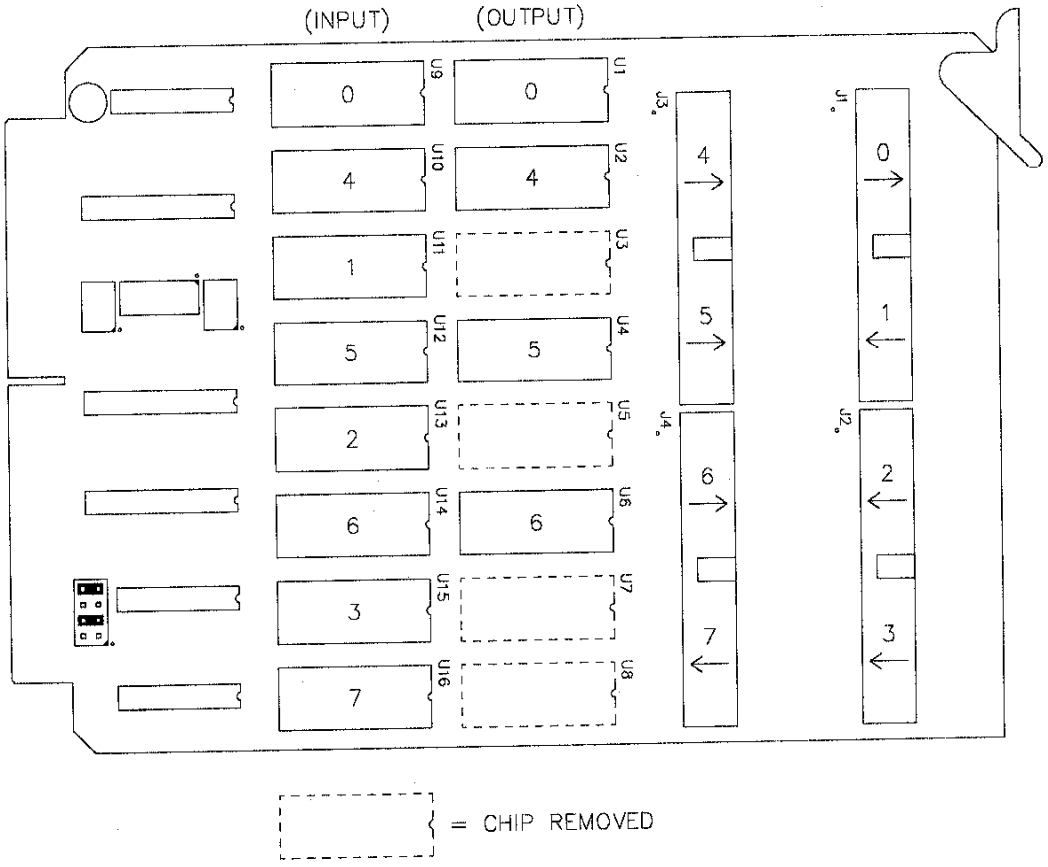


Figure 2-8. Typical I/O Configuration

Alternately the board can be configured as four ports (I/O addresses) with an input and an output channel at each location. This configuration is not recommended for most applications.

When this mode is used the the board must be configured only as shown below. Writing to channels 0 - 3 will output data on connectors J1 and J2. Reading channels 0 - 3 will input data from connectors J3 and J4.

This configuration does not allow for readback of output channel data.

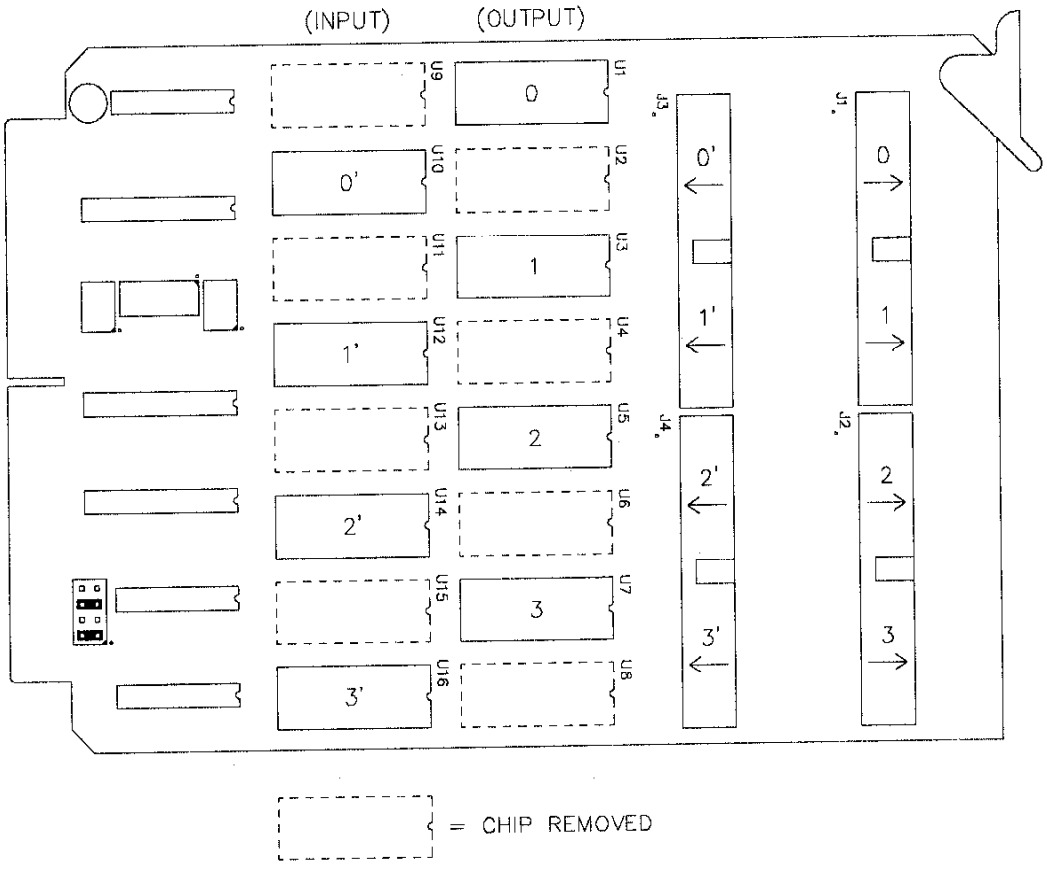


Figure 2-9. Special 4-Port Mode Configuration

Section 3
INSTALLATION

HANDLING

** CAUTION ** The VL-7614 card uses chips which are sensitive to static electricity discharges. Normal precautions, such as discharging yourself, work stations, and tools to ground before touching the board should be taken whenever the board is handled.

The board should also be protected during shipment or storage by placing it in a conductive bag (such as the one it was received in) or by wrapping it in metal foil.

INSTALLATION

The VL-7614 card can be installed in any slot of an STD Bus card cage.

The VL-7614 does not use the STD Bus priority interrupt chain. However, the priority IN and OUT pins on this board are connected together so that the priority chain will not be broken. This board may be inserted between other boards that are using the priority chain.

** CAUTION ** When cards are installed in an STD Bus card cage they must be oriented correctly (usually with the card ejector toward the top of the cage). Refer to the card cage documentation for the correct way to insert the STD Bus cards.

** CAUTION ** Cards should be inserted or removed from the STD Bus card cage only when the system power is off.

EXTERNAL CONNECTIONS

Connection to the VL-7614 can be made as noted below. Pinout listings for these connectors appear on the following pages. A pinout of the STD Bus connector appears in Section 5.

Connectors J1 - J4

Connectors J1 - J4 are 34-pin latching header type connectors (on .1" centers). They may each be connected to external equipment using mating connectors such as Ansley #609-3441, AMP #499506-0, and 3M #3414-6034. The mating connectors should include a strain relief in order to use the built-in latch bars.

Connector J1

Pin	Channel - Bit
1	0 - 0
3	0 - 1
5	0 - 2
7	0 - 3
9	0 - 4
11	0 - 5
13	0 - 6
15	0 - 7
17	1 - 0
19	1 - 1
21	1 - 2
23	1 - 3
25	1 - 4
27	1 - 5
29	1 - 6
31	1 - 7
33	Ground

2-34 even numbered pins ground.

Connector J2

Pin	Channel - Bit
1	2 - 0
3	2 - 1
5	2 - 2
7	2 - 3
9	2 - 4
11	2 - 5
13	2 - 6
15	2 - 7
17	3 - 0
19	3 - 1
21	3 - 2
23	3 - 3
25	3 - 4
27	3 - 5
29	3 - 6
31	3 - 7
33	Ground

2-34 even numbered pins ground.

Figure 3-1. Connectors J1 and J2 Pinouts

Connector J3

Pin	Channel - Bit
1	4 - 0
3	4 - 1
5	4 - 2
7	4 - 3
9	4 - 4
11	4 - 5
13	4 - 6
15	4 - 7
17	5 - 0
19	5 - 1
21	5 - 2
23	5 - 3
25	5 - 4
27	5 - 5
29	5 - 6
31	5 - 7
33	Ground

2-34 even numbered pins ground.

Connector J4

Pin	Channel - Bit
1	6 - 0
3	6 - 1
5	6 - 2
7	6 - 3
9	6 - 4
11	6 - 5
13	6 - 6
15	6 - 7
17	7 - 0
19	7 - 1
21	7 - 2
23	7 - 3
25	7 - 4
27	7 - 5
29	7 - 6
31	7 - 7
33	Ground

2-34 even numbered pins ground.

Figure 3-2. Connectors J3 and J4 Pinouts

Section 4
OPERATION

INTRODUCTION

This section includes general information about the use and operation of the VL-7614 card. It focuses primarily on the software commands necessary to operate the card and includes examples to assist you in constructing your own software routines.

I/O PORT MAPPING

The VL-7614 normally occupies eight I/O port addresses. Each I/O address corresponds to one 8-bit channel of inputs or outputs.

An alternate mapping may also be used which provides four ports that each access one input and one output channel. This mapping is not recommended for most applications and will not be covered in this section.

The locations of the eight ports is determined by the board address, which is jumper selectable. As shipped, the board is jumpered for hex address 00.

Once the board's I/O address has been determined, the addresses of the eight I/O ports can be determined as shown in Figure 4-1. Each I/O module port can be both read (for inputting data or reading the current output data) and written (for outputting data) depending on the physical configuration of the channel.

For applications that use byte-oriented data, each port can be read/written directly as needed. For applications that use bit-oriented data (i.e. many single status/control lines) the board is much easier to use with subroutines that treat it as 64 single addressable lines. Subroutines with this purpose are included later in this section.

Figure 4-2 details the way in which the bit numbering corresponds to each connector and port number (shown as shipped addressed at hex 00).