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Product Specifications

PART NO.:

VL470T2863A-E6S

REV: 1.0

General Information

1GB 128Mx64 DDR2 SDRAM NON-ECC UNBUFFERED SODIMM 200-PIN

Description

The VL470T2863A is a 128Mx64 DDR2 SDRAM high density SODIMM. This single rank memory module consists of eight CMOS 128Mx8 bits with 8 banks DDR2 synchronous DRAMs in BGA packages and a 2K EEPROM in an 8-pin TSSOP package. This module is a 200-pin small-outline dual in-line memory module and is intended for mounting into an edge connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR2 SDRAM.

Features

- 200-pin, small-outline dual in-line memory module (SODIMM)
- JEDEC pin out
- Fast data transfer rate: PC2-5300
- VDD = VDDQ = 1.8V +/-0.1V
- JEDEC standard 1.8V (SSTL_18 compatible)
- VDDSPD = 1.7V to 3.6V
- Differential data strobe (DQS, DQS#) option
- Differential clock inputs (CK, CK#)
- Four-bit pre-fetch architecture
- DLL aligns DQ and DQS transition with CK
- Nominal and dynamic on-die termination (ODT)
- Programmable CAS# latency: 5 (DDR2-667)
- Write latency = Read latency - 1 tCK
- Eight internal component banks for concurrent operation
- Programmable burst; length (4, 8)
- Adjustable data-output drive strength
- Auto & self refresh, (8K/64ms refresh)
- Serial presence detect (SPD) with EEPROM
- Gold edge contacts
- Lead-free, RoHS compliant
- PCB: Height 30.00mm (1.181"), double sided component
- Operating temperature (TOPER): - Commercial (0°C <= Tc <= 95°C)
- Industrial (-40°C <= Tc <= 95°C)

Notes: Double refresh rate is required when 85°C < TOPER <= 95°C.
TOPER is DRAM case temperature.

Pin Description

| Pin Name | Function |
|-------------------------|------------------------------|
| A0~A13 | Address Inputs |
| A10/AP | Address Input/ Autoprecharge |
| BA0~BA2 | Bank Address Inputs |
| DQ0~DQ63 | Data Input/Output |
| DQS0~DQS7 | Data Strobes |
| DQS0#~DQS7# | Data Strobes Complement |
| DM0~DM7 | Data Masks |
| CK0, CK0#, CK1, CK1# | Clock Inputs |
| ODT0 | On-die Termination Control |
| CKE0 | Clock Enables |
| CS0# | Chip Selects |
| RAS# | Row Address Strobes |
| CAS# | Column Address Strobes |
| WE# | Write Enable |
| VDD | Voltage Supply |
| VSS | Ground |
| SA0~SA1 | SPD Address |
| SDA | SPD Data Input/Output |
| SCL | SPD Clock Input |
| VDDSPD | SPD Voltage Supply |
| VREF | SSTL_18 Reference Voltage |
| NC | No Connect |

Order Information:

VL470T2863A - E6 S X - X

OPERATING TEMPERATURE

Blank: Commercial
S1: Industrial screening

DRAM DIE
(Option)

DRAM MANUFACTURER
S - SAMSUNG

MODULE SPEED
E6: PC2-5300 @ CL5

VL: Lead-free/RoHS



Product Specifications

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Pin Configuration

| 200-PIN DDR2 SODIMM FRONT | | | | | | | | 200-PIN DDR2 SODIMM BACK | | | | | | | |
|---------------------------|-------|-----|------|-----|--------|-----|--------|--------------------------|------|-----|-------|-----|-------|-----|-------|
| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | | |
| 1 | VREF | 51 | DQS2 | 101 | A1 | 151 | DQ42 | 2 | VSS | 52 | DM2 | 102 | A0 | 152 | DQ46 |
| 3 | VSS | 53 | VSS | 103 | VDD | 153 | DQ43 | 4 | DQ4 | 54 | VSS | 104 | VDD | 154 | DQ47 |
| 5 | DQ0 | 55 | DQ18 | 105 | A10/AP | 155 | VSS | 6 | DQ5 | 56 | DQ22 | 106 | BA1 | 156 | VSS |
| 7 | DQ1 | 57 | DQ19 | 107 | BA0 | 157 | DQ48 | 8 | VSS | 58 | DQ23 | 108 | RAS# | 158 | DQ52 |
| 9 | VSS | 59 | VSS | 109 | WE# | 159 | DQ49 | 10 | DM0 | 60 | VSS | 110 | CS0# | 160 | DQ53 |
| 11 | DQS0# | 61 | DQ24 | 111 | VDD | 161 | VSS | 12 | VSS | 62 | DQ28 | 112 | VDD | 162 | VSS |
| 13 | DQS0 | 63 | DQ25 | 113 | CAS# | 163 | NC | 14 | DQ6 | 64 | DQ29 | 114 | OTD0 | 164 | CK1 |
| 15 | VSS | 65 | VSS | 115 | CS1#* | 165 | VSS | 16 | DQ7 | 66 | VSS | 116 | A13 | 166 | CK1# |
| 17 | DQ2 | 67 | DM3 | 117 | VDD | 167 | DQS6# | 18 | VSS | 68 | DQS3# | 118 | VDD | 168 | VSS |
| 19 | DQ3 | 69 | NC | 119 | ODT1* | 169 | DQS6 | 20 | DQ12 | 70 | DQS3 | 120 | NC | 170 | DM6 |
| 21 | VSS | 71 | VSS | 121 | VSS | 171 | VSS | 22 | DQ13 | 72 | VSS | 122 | VSS | 172 | VSS |
| 23 | DQ8 | 73 | DQ26 | 123 | DQ32 | 173 | DQ50 | 24 | VSS | 74 | DQ30 | 124 | DQ36 | 174 | DQ54 |
| 25 | DQ9 | 75 | DQ27 | 125 | DQ33 | 175 | DQ51 | 26 | DM1 | 76 | DQ31 | 126 | DQ37 | 176 | DQ55 |
| 27 | VSS | 77 | VSS | 127 | VSS | 177 | VSS | 28 | VSS | 78 | VSS | 128 | VSS | 178 | VSS |
| 29 | DQS1# | 79 | CKE0 | 129 | DQS4# | 179 | DQ56 | 30 | CK0 | 80 | CKE1* | 130 | DM4 | 180 | DQ60 |
| 31 | DQS1 | 81 | VDD | 131 | DQS4 | 181 | DQ57 | 32 | CK0# | 82 | VDD | 132 | VSS | 182 | DQ61 |
| 33 | VSS | 83 | NC | 133 | VSS | 183 | VSS | 34 | VSS | 84 | NC | 134 | DQ38 | 184 | VSS |
| 35 | DQ10 | 85 | BA2 | 135 | DQ34 | 185 | DM7 | 36 | DQ14 | 86 | A14 * | 136 | DQ39 | 186 | DQS7# |
| 37 | DQ11 | 87 | VDD | 137 | DQ35 | 187 | VSS | 38 | DQ15 | 88 | VDD | 138 | VSS | 188 | DQS7 |
| 39 | VSS | 89 | A12 | 139 | VSS | 189 | DQ58 | 40 | VSS | 90 | A11 | 140 | DQ44 | 190 | VSS |
| 41 | VSS | 91 | A9 | 141 | DQ40 | 191 | DQ59 | 42 | VSS | 92 | A7 | 142 | DQ45 | 192 | DQ62 |
| 43 | DQ16 | 93 | A8 | 143 | DQ41 | 193 | VSS | 44 | DQ20 | 94 | A6 | 144 | VSS | 194 | DQ63 |
| 45 | DQ17 | 95 | VDD | 145 | VSS | 195 | SDA | 46 | DQ21 | 96 | VDD | 146 | DQS5# | 196 | VSS |
| 47 | VSS | 97 | A5 | 147 | DM5 | 197 | SCL | 48 | VSS | 98 | A4 | 148 | DQS5 | 198 | SA0 |
| 49 | DQS2# | 99 | A3 | 149 | VSS | 199 | VDDSPD | 50 | NC | 100 | A2 | 150 | VSS | 200 | SA1 |

(*): These pins are not used on this module.



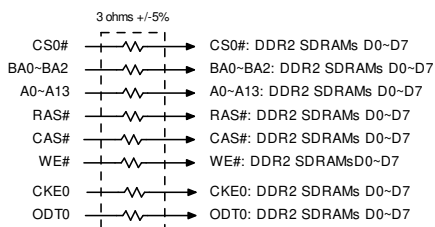
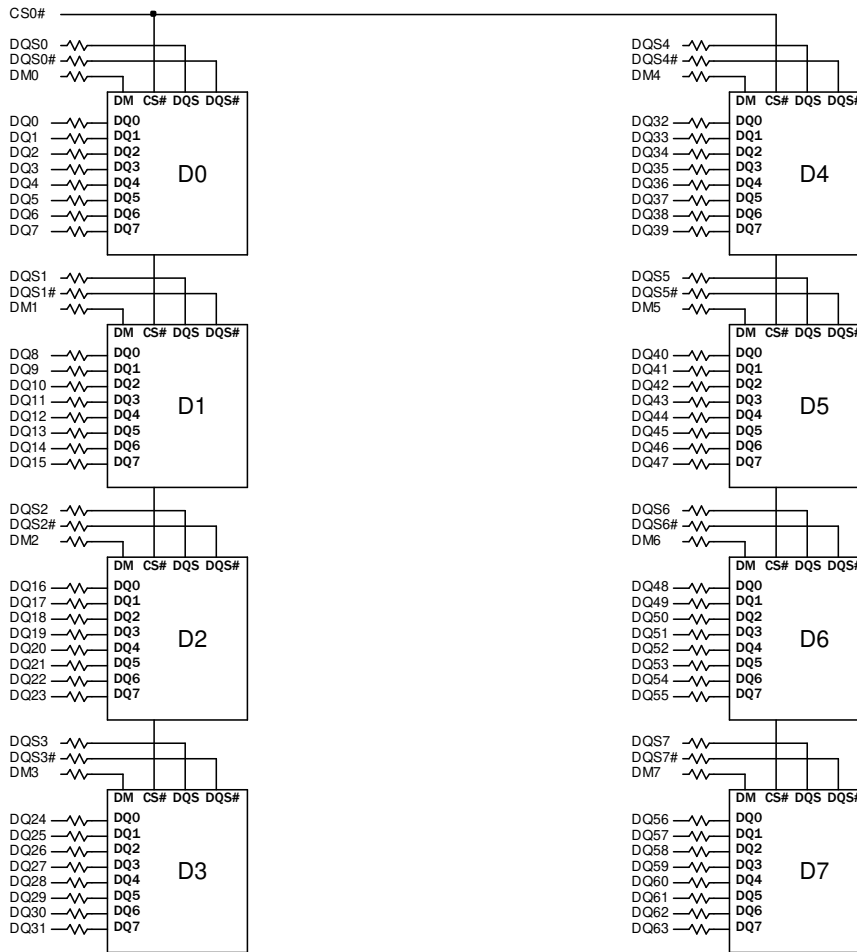
Product Specifications

PART NO.:

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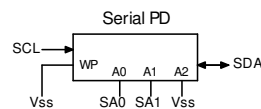
REV: 1.0

Function Block Diagram



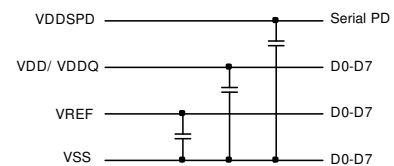
Notes:

1. Unless otherwise noted, resistor values are 22 ohms +/-5%



| * Clock Wiring | |
|----------------|-------------|
| Clock Input | DDR2 SDRAMs |
| *CK0, CK0# | 4 SDRAMs |
| *CK1, CK1# | 4 SDRAMs |

* Wire per Clock Loading Table/Wiring Diagrams





Product Specifications

PART NO.:

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REV: 1.0

Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Unit | |
|-----------|--|------------------------------|-----|------|----|
| VDD | Voltage on VDD pin relative to VSS | -1.0 | 2.3 | V | |
| VDDQ | Voltage on VDDQ pin relative to VSS | -0.5 | 2.3 | V | |
| VDDL | Voltage on VDDL pin relative to VSS | -0.5 | 2.3 | V | |
| VIN, VOUT | Voltage on any pin relative to VSS | -0.5 | 2.3 | V | |
| TSTG | Storage temperature | -55 | 100 | °C | |
| IL | Input leakage current; Any input $0V < VIN < VDD$; VREF input $0V < VIN < 0.95V$; Other pins not under test = 0V | Address, BA, RAS#, CAS#, WE# | -40 | 40 | µA |
| | | CS#, CKE, ODT | -40 | 40 | µA |
| | | CK, CK# | -40 | 40 | µA |
| | | DM | -5 | 5 | µA |
| IOZ | Output leakage current; $0V < VOUT < VDDQ$; DQs and ODT are disabled | DQ, DQS, DQS# | -5 | 5 | µA |
| IVREF | VREF supply leakage current; VREF = Valid VREF level | -16 | 16 | µA | |

DC Operating Conditions

| Symbol | Parameter | Min | Typical | Max | Unit | Notes |
|--------|-------------------------|--------------------|--------------------|--------------------|------|-------|
| VDD | Supply voltage | 1.7 | 1.8 | 1.9 | V | 1 |
| VDDQ | I/O supply voltage | 1.7 | 1.8 | 1.9 | V | 4 |
| VDDL | VDDL supply voltage | 1.7 | 1.8 | 1.9 | V | 4 |
| VREF | I/O reference voltage | $0.49 \times VDDQ$ | $0.50 \times VDDQ$ | $0.51 \times VDDQ$ | V | 2 |
| VTT | I/O termination voltage | $VREF - 0.04$ | VREF | $VREF + 0.04$ | V | 3 |

Notes:

1. VDD, VDDQ must track each other. VDDQ must be less than or equal to VDD.
2. VREF is expected to equal $VDDQ/2$ of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed +/-1percent of the DC value. Peak-to-peak AC noise on VREF may not exceed +/-2 percent of VREF. This measurement is to be taken at the nearest VREF bypass capacitor.
3. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the DC level of VREF.
4. VDDQ tracks with VDD; VDDL tracks with VDD.



| Product Specifications | | |
|------------------------|-----------------|----------|
| PART NO.: | VL470T2863A-E6S | REV: 1.0 |

| Operating Temperature Condition | | | | | |
|---------------------------------|-----------------------|------------|------------|-------|-------|
| Symbol | Parameter | | Rating | Units | Notes |
| TOPER | Operating temperature | Commercial | 0 to +95 | °C | 1,2 |
| | | Industrial | -40 to +85 | | |

Notes:

- Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51-2.
- At -40 to +85°C, operation temperature range, all DRAM specifications will be supported. The refresh rate is required to double when 85°C < TOPER <= 95°C.

| Input DC Logic Level | | | | |
|--------------------------------|------------------------------|--------------|--------------|------|
| All voltages referenced to VSS | | | | |
| Symbol | Parameter | Min | Max | Unit |
| VIH(DC) | Input High (Logic 1) Voltage | VREF + 0.125 | VDDQ + 0.300 | V |
| VIL(DC) | Input Low (Logic 0) Voltage | -0.300 | VREF - 0.125 | V |

| Input AC Logic Level | | | | |
|--------------------------------|------------------------------|--------------|--------------|------|
| All voltages referenced to VSS | | | | |
| Symbol | Parameter | Min | Max | Unit |
| VIH(AC) | Input High (Logic 1) Voltage | VREF + 0.200 | - | V |
| VIL(AC) | Input Low (Logic 0) Voltage | - | VREF - 0.200 | V |

| Input/Output Capacitance | | | | |
|--|--------|------------------|-----|------|
| TA=25°C, f=100MHz | | | | |
| Parameter | Symbol | E6 (DDR2-667) | | Unit |
| | | Min | Max | |
| Input capacitance (A0~A13, BA0~BA2, RAS#, CAS#, WE#) | CIN1 | 12 | 18 | pF |
| Input capacitance (CKE0, ODT0, CS0#) | CIN2 | 12 | 18 | pF |
| Input capacitance (CK0, CK0#), (CK1, CK1#) | CIN3 | 8 | 12 | pF |
| Input/Output capacitance (DQ, DQS, DQS#, DM) | CIO | 6.5 | 7.5 | pF |



Product Specifications

PART NO.:

VL470T2863A-E6S

REV: 1.0

IDD Specification

| Condition | Symbol | E6 (DDR2-667) | Unit |
|---|---------------------------|------------------|------|
| Operating one bank active-pre-charge current; $t_{CK} = t_{CK(IDD)}$; $t_{RC} = t_{RC(IDD)}$; $t_{RAS} = t_{RAS\ MIN(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING | IDD0* | 344 | mA |
| Operating one bank active-read-pre-charge current; IOUT = 0mA; BL = 4; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$; $t_{RC} = t_{RC(IDD)}$; $t_{RAS} = t_{RAS\ MIN(IDD)}$; $t_{RCD} = t_{RCD(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W | IDD1* | 384 | mA |
| Pre-charge power-down current; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | IDD2P** | 80 | mA |
| Pre-charge quiet standby current; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | IDD2Q** | 160 | mA |
| Pre-charge standby current; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are SWITCHING | IDD2N** | 192 | mA |
| Active power-down current; All banks open; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING. | Fast PDN Exit MRS(12) = 0 | 176 | mA |
| | Slow PDN Exit MRS(12) = 1 | 120 | mA |
| Active standby current; All banks open; $t_{CK} = t_{CK(IDD)}$; $t_{RP} = t_{RP(IDD)}$; $t_{RAS} = t_{RAS\ MAX(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING. | IDD3N** | 240 | mA |
| Operating burst write current; All banks open; Continuous burst writes; BL = 8; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS\ MAX(IDD)}$; $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING | IDD4W* | 480 | mA |
| Operating burst read current; All banks open; Continuous burst reads; IOUT = 0mA; BL = 4; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS\ MAX(IDD)}$; $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W. | IDD4R* | 560 | mA |
| Burst refresh current; $t_{CK} = t_{CK(IDD)}$; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING. | IDD5** | 800 | mA |
| Self refresh current; CK and CK# at 0V; CKE < 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING. | Normal | 80 | mA |
| Operating bank interleave read current; All bank interleaving reads; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = $t_{RCD(IDD)} - 1 * t_{CK(IDD)}$; $t_{CK} = t_{CK(IDD)}$; $t_{RC} = t_{RC(IDD)}$; $t_{RRD} = t_{RRD(IDD)}$; $t_{RCD} = 1 * t_{CK(IDD)}$; CKE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING. | IDD7* | 1160 | mA |

Notes:

IDD specification is based on Samsung F-die components.

*: Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.

** : Value calculated reflects all module ranks in this operating condition.



Product Specifications

PART NO.:

VL470T2863A-E6S

REV: 1.0

AC TIMING PARAMETERS & SPECIFICATIONS

| Parameter | Symbol | E7 (DDR2-800) | | E6 (DDR2-667) | | D5 (DDR2-533) | | Unit | |
|--|--------|------------------|-------------------|------------------|-------------------|------------------|-------------------|-----------|-----|
| | | Min | Max | Min | Max | Min | Max | | |
| Clock Timing | | | | | | | | | |
| Clock Cycle Time | CL6 | tCK(6) | 2,500 | 8,000 | - | - | - | - | ps |
| | CL5 | tCK(5) | 3,000 | 8,000 | 3,000 | 8,000 | - | - | ps |
| | CL4 | tCK(4) | 3,750 | 8,000 | 3,750 | 8,000 | 3,750 | 8,000 | ps |
| CK high-level width | | tCH(avg) | 0.48 | 0.52 | 0.48 | 0.52 | 0.48 | 0.52 | tCK |
| CK low-level width | | tCL(avg) | 0.48 | 0.52 | 0.48 | 0.52 | 0.48 | 0.52 | tCK |
| Half clock period | | tHP | MIN (tCH, tCL) | - | MIN (tCH, tCL) | - | MIN (tCH, tCL) | - | ps |
| Clock jitter | | tJIT | -100 | 100 | -125 | 125 | -125 | 125 | ps |
| Data Timing | | | | | | | | | |
| DQ output access time from CK/CK# | | tAC | -400 | 400 | -450 | +450 | -500 | 500 | ps |
| Data-out high impedance window from CK/CK# | | tHZ | - | tAC(MAX) | - | tAC(MAX) | - | tAC(MAX) | ps |
| Data-out low impedance window from CK/CK# | | tLZ (DQ) | 2 x tAC(MIN) | tAC(MAX) | 2 x tAC(MIN) | tAC(MAX) | 2 x tAC(MIN) | tAC(MAX) | ps |
| DQ and DM input setup time relative to DQS | | tDS | 50 | - | 100 | - | 100 | - | ps |
| DQ and DM input hold time relative to DQS | | tDH | 125 | - | 175 | - | 225 | - | ps |
| DQ and DM input pulse width (for each input) | | tDIPW | 0.35 | - | 0.35 | - | 0.35 | - | tCK |
| Data hold skew factor | | tQHS | - | 300 | - | 340 | - | 400 | ps |
| DQ-DQS hold, DQS to first DQ to go non-valid, per access | | tQH | tHP - tQHS | - | tHP - tQHS | - | tHP - tQHS | - | ps |
| Data valid output window (DVW) | | tDVW | tQH - tDQSQ | - | tQH - tDQSQ | - | tQH - tDQSQ | - | ns |
| Data Strobe Timing | | | | | | | | | |
| DQS input high pulse width | | tDQSH | 0.35 | - | 0.35 | - | 0.35 | - | tCK |
| DQS input low pulse width | | tDQSL | 0.35 | - | 0.35 | - | 0.35 | - | tCK |
| DQS output access time from CK/CK# | | tDQSCK | -350 | +350 | -400 | +400 | -450 | +450 | ps |
| DQS failing edge to CK rising-setup time | | tDSS | 0.2 | - | 0.2 | - | 0.2 | - | tCK |
| DQS failing edge from CK rising-hold time | | tDSH | 0.2 | - | 0.2 | - | 0.2 | - | tCK |
| DQS-DQ skew, DQS to last DQ valid, per group, per access | | tDQSQ | - | 200 | - | 240 | - | 300 | ps |
| DQS read preamble | | tRPRE | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | tCK |
| DQS read preamble | | tRPST | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK |
| DQS read preamble setup time | | tWPRES | 0 | - | 0 | - | 0 | - | ps |
| DQS read preamble | | tWPRE | 0.35 | - | 0.35 | - | 0.35 | - | tCK |
| DQS read preamble | | tWPST | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK |
| First DQS latching transition to associated clock edge | | tDQSS | -0.25 | 0.25 | -0.25 | 0.25 | -0.25 | 0.25 | tCK |
| Write command to first DQS latching transition | | - | WL - tDQSS | WL+ tDQSS | WL - tDQSS | WL+ tDQSS | WL - tDQSS | WL+ tDQSS | tCK |
| Command and Address Timing | | | | | | | | | |
| Address and control input pulse width for each input | | tIPW | 0.6 | - | 0.6 | - | 0.6 | - | tCK |
| Address and control input setup time | | tIS | 175 | - | 200 | - | 250 | - | ps |
| Address and control input hold time | | tIH | 250 | - | 275 | - | 375 | - | ps |
| CAS# to CAS# command delay | | tCCD | 2 | - | 2 | - | 2 | - | tCK |
| ACTIVE to ACTIVE (same bank) command | | tRC | 60 | - | 60 | - | 60 | - | ns |
| Active to active command period for 1KB page size products | | tRRD | 7.5 | - | 7.5 | - | 7.5 | - | ns |
| Active to active command period for 2KB page size products | | tRRD | 10 | - | 10 | - | 10 | - | ns |



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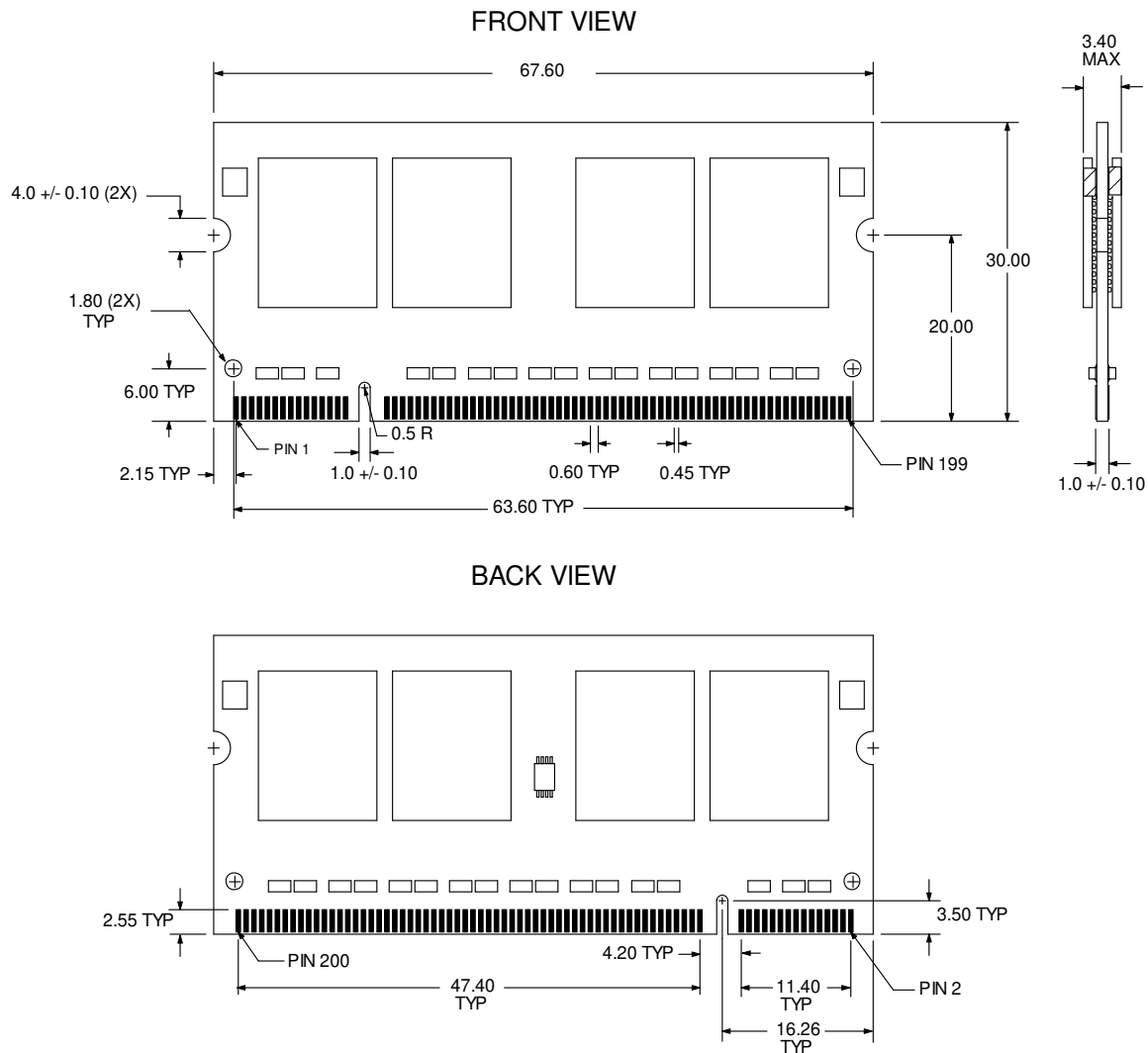
REV: 1.0

AC TIMING PARAMETERS & SPECIFICATIONS

| Parameter | Symbol | E7 (DDR2-800) | | E6 (DDR2-667) | | D5 (DDR2-533) | | Unit | |
|--|--------|---------------------|-----------------------------------|--------------------|-----------------------------------|--------------------|-----------------------------------|------|----|
| | | Min | Max | Min | Max | Min | Max | | |
| ACTIVE to READ or WRITE delay | tRCD | 15 | - | 15 | - | 15 | - | ns | |
| Four Activate Window for 1KB page size products | tFAW | 35 | - | 37.5 | - | 37.5 | - | ns | |
| Four Activate Window for 2KB page size products | tFAW | 45 | - | 50 | - | 50 | - | ns | |
| ACTIVE to PRECHARGE command | tRAS | 45 | 70,000 | 45 | 70,000 | 45 | 70,000 | ns | |
| Internal READ to precharge Command delay | tRTP | 7.5 | - | 7.5 | - | 7.5 | - | ns | |
| Write recovery time | tWR | 15 | - | 15 | - | 15 | - | ns | |
| Auto precharge write recovery + precharge time | tDAL | tWR + tRP | - | tWR + tRP | - | tWR + tRP | - | tCK | |
| Internal WRITE to READ Command delay | tWTR | 7.5 | - | 7.5 | - | 7.5 | - | ns | |
| PRECHARGE command period | tRP | 15 | - | 15 | - | 15 | - | ns | |
| PRECHARGE ALL command period | tRPA | <1Gb | 15 | - | 15 | - | 15 | - | ns |
| | | ≥1Gb | 17.5 | - | 18 | - | 18.75 | - | ns |
| LOAD MODE command cycle time | tMRD | 2 | - | 2 | - | 2 | - | tCK | |
| CKE low to CK, CK# uncertainty | tDELAY | tIS+tCK +tIH | - | tIS+tCK +tIH | - | tIS+tCK +tIH | - | ns | |
| Refresh, Self-Refresh | | | | | | | | | |
| Refresh to Active or Refresh to Refresh command interval | tRFC | 127.5 | - | 127.5 | - | 127.5 | - | ns | |
| Average periodic Refresh interval | tREFI | 0°C ≤ tCASE ≤ 85°C | - | 7.8 | - | 7.8 | - | 7.8 | us |
| | | 85°C ≤ tCASE ≤ 95°C | - | 3.9 | - | 3.9 | - | 3.9 | us |
| Exit Self Refresh to non-READ command | tXSNR | tRFC(MIN) +10 | - | tRFC(MIN) +10 | - | tRFC(MIN) +10 | - | ns | |
| Exit Self Refresh to READ | tXSRD | 200 | - | 200 | - | 200 | - | tCK | |
| Exit Self Refresh timing reference | tISXR | tIS | - | tIS | - | tIS | - | ps | |
| ODT | | | | | | | | | |
| ODT turn-on delay | tAOND | 2 | 2 | 2 | 2 | 2 | 2 | tCK | |
| ODT turn-on | tAON | tAC(MIN) | tAC(MAX)+ 700 | tAC(MIN) | tAC(MAX)+ 700 | tAC(MIN) | tAC(MAX)+ 1,000 | ps | |
| ODT turn-off delay | tAOFD | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | tCK | |
| ODT turn-off | tAOF | tAC(MIN) | tAC(MAX)+ 600 | tAC(MIN) | tAC(MAX)+ 600 | tAC(MIN) | tAC(MAX)+ 600 | ps | |
| ODT turn-on(power-down mode) | tAONPD | tAC(MIN)+ 2,000 | 2 x tCK + tAC(MAX)+ 1,000 | tAC(MIN)+ 2,000 | 2 x tCK + tAC(MAX)+ 1,000 | tAC(MIN)+ 2,000 | 2 x tCK + tAC(MAX)+ 1,000 | ps | |
| ODT turn-off (power-down mode) | tAOFPD | tAC(MIN)+ 2,000 | 2.5 x tCK + tAC(MAX)+ 1,000 | tAC(MIN)+ 2,000 | 2.5 x tCK + tAC(MAX)+ 1,000 | tAC(MIN)+ 2,000 | 2.5 x tCK + tAC(MAX)+ 1,000 | ps | |
| ODT to power-down entry latency | tANPD | 3 | - | 3 | - | 3 | - | tCK | |
| ODT power-down exit latency | tAXPD | 8 | - | 8 | - | 8 | - | tCK | |
| Power Down | | | | | | | | | |
| Exit active power-down to READ command, MR[bit12=0] | tXARD | 2 | - | 2 | - | 2 | - | tCK | |
| Exit active power-down to READ command, MR[bit12=1] | tXARDS | 8-AL | - | 7-AL | - | 6-AL | - | tCK | |
| Exit precharge power-down to any non-READ command | tXP | 2 | - | 2 | - | 2 | - | tCK | |
| CKE minimum high/low time | tCKE | 3 | - | 3 | - | 3 | - | tCK | |

| Product Specifications | | |
|------------------------|-----------------|----------|
| PART NO.: | VL470T2863A-E6S | REV: 1.0 |

Package Dimensions



Note: 1. All dimensions are in millimeters with tolerance +/- 0.15mm unless otherwise specified.
 2. The dimensional diagram is for reference only.



| Product Specifications | | |
|-------------------------------|------------------------|-----------------|
| PART NO.: | VL470T2863A-E6S | REV: 1.0 |

Revision History:

| Date | Rev. | Page | Changes |
|-------------|-------------|-------------|----------------|
| 10/24/2012 | 1.0 | All | Spec release |
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