Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

N-Channel Enhancement-Mode Vertical DMOS FET

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral source-drain diode
- High input impedance and high gain

Applications

- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

General Description

This enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven, silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

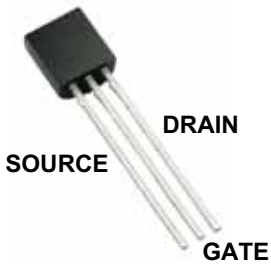
Part Number	Package Option	Packing
VN0550N3-G	TO-92	1000/Bag
VN0550N3-G P002	TO-92	2000/Reel
VN0550N3-G P003		
VN0550N3-G P005		
VN0550N3-G P013		
VN0550N3-G P014		

-G denotes a lead (Pb)-free / RoHS compliant package.
Contact factory for Wafer / Die availablity.
Devices in Wafer / Die form are lead (Pb)-free / RoHS compliant.

Product Summary

BV_{DSS}/BV_{DGS}	$R_{DS(ON)}$ (max)	I_{DSS} (min)
500V	60Ω	150mA

Pin Configuration



TO-92

Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Product Marking

YY = Year Sealed
WW = Week Sealed
_____ = "Green" Packaging

Package may or may not include the following marks: Si or 

TO-92

Typical Thermal Resistance

Package	θ_{ja}
TO-92	132°C/W

Thermal Characteristics

Package	I_D (continuous)†	I_D (pulsed)	Power Dissipation @T_C = 25°C	I_{DR}†	I_{DRM}
TO-92	50mA	250mA	1.0W	50mA	250mA

Notes:

† I_D *(continuous) is limited by max rated* T_j .

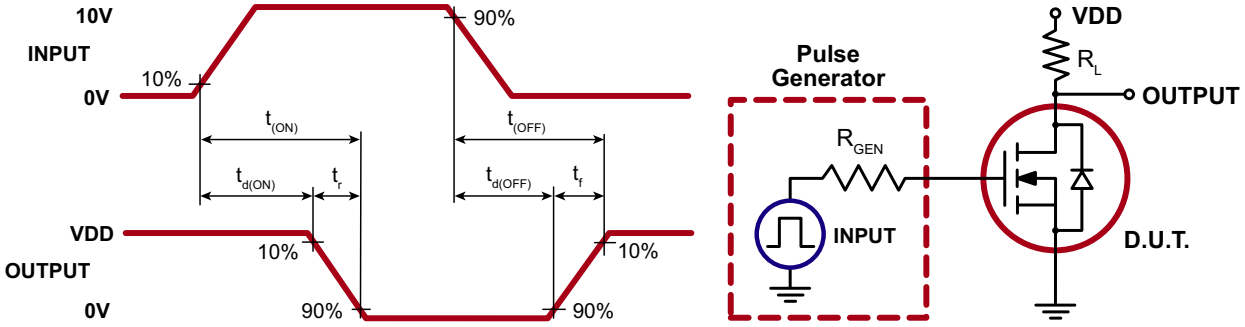
Electrical Characteristics *(T_A = 25°C unless otherwise specified)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	500	-	-	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate threshold voltage	2.0	-	4.0	V	V_{GS} = V_{DS}, I_D = 1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-3.8	-5.0	mV/°C	V_{GS} = V_{DS}, I_D = 1.0mA
I_{GSS}	Gate body leakage current	-	-	100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero gate voltage drain current	-	-	10	µA	V_{GS} = 0V, V_{DS} = Max Rating
		-	-	1.0	mA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	On-state drain current	-	100	-	mA	V_{GS} = 5.0V, V_{DS} = 25V
		150	350	-		V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	45	-	Ω	V_{GS} = 5.0V, I_D = 50mA
		-	40	60		V_{GS} = 10V, I_D = 50mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	1.0	1.7	%/°C	V_{GS} = 10V, I_D = 50mA
G_{FS}	Forward transconductance	50	100	-	mmho	V_{DS} = 25V, I_D = 50mA
C_{ISS}	Input capacitance	-	45	55	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-	8.0	10		
C_{RSS}	Reverse transfer capacitance	-	2.0	5.0		
$t_{d(ON)}$	Turn-on time	-	-	10	ns	V_{DD} = 25V, I_D = 150mA, R_{GEN} = 25Ω
t_r	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-off time	-	-	10		
t_f	Fall time	-		10		
V_{SD}	Diode forward voltage drop	-	0.8	-	V	V_{GS} = 0V, I_{SD} = 500mA
t_{rr}	Reverse recovery time	-	300	-	ns	V_{GS} = 0V, I_{SD} = 500mA

Notes:

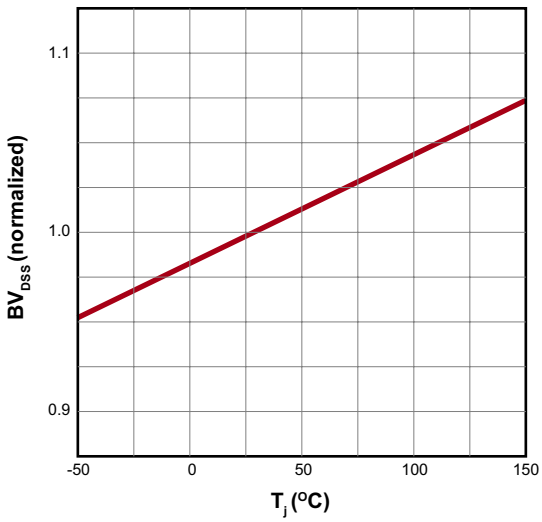
1. *All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)*
2. *All A.C. parameters sample tested.*

Switching Waveforms and Test Circuit

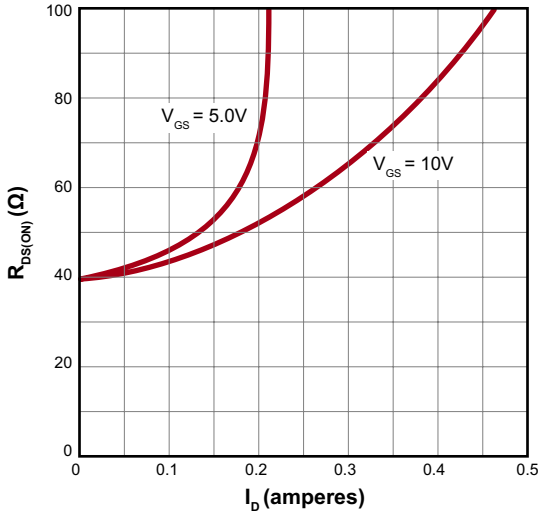


Typical Performance Curves

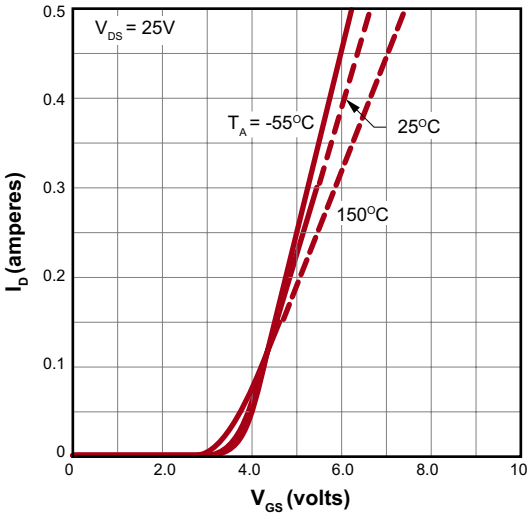
BV_{DSS} Variation with Temperature



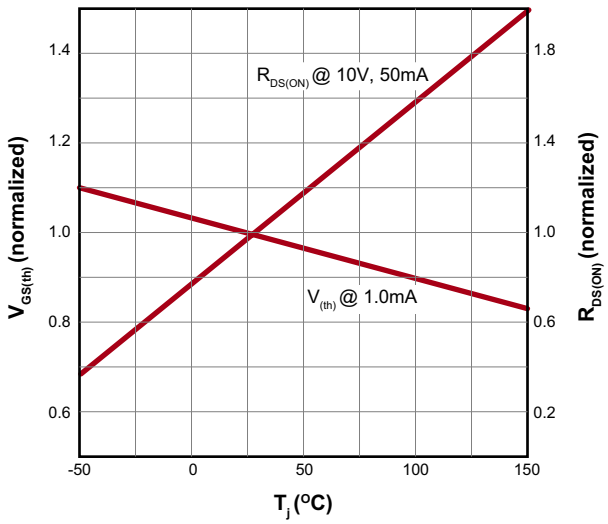
On-Resistance vs. Drain Current



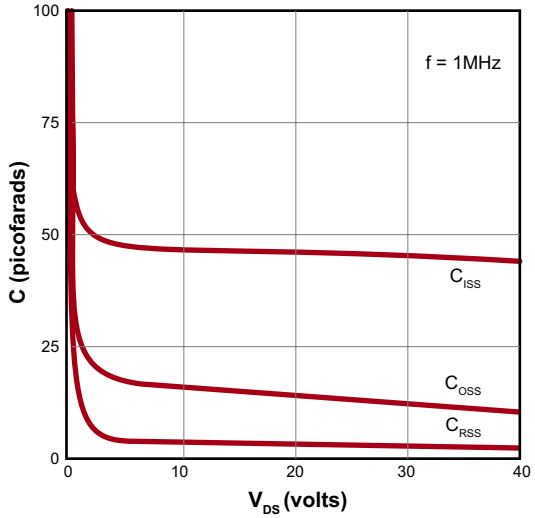
Transfer Characteristics



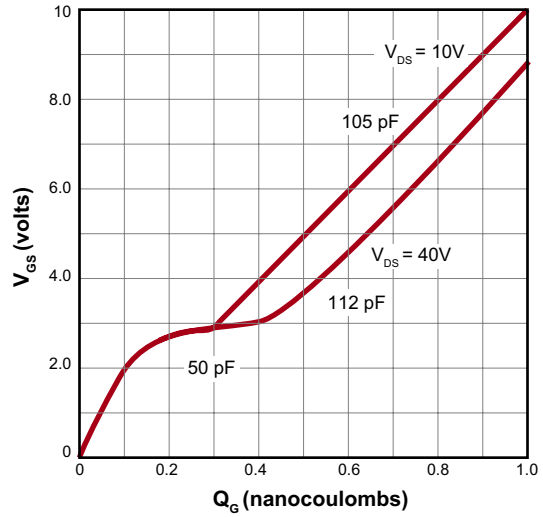
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage

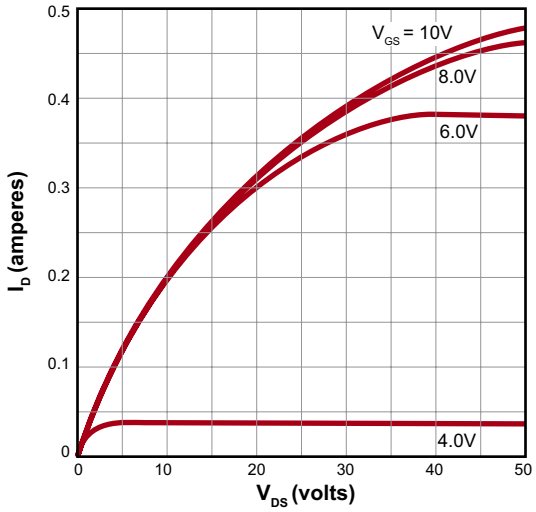


Gate Drive Dynamic Characteristics

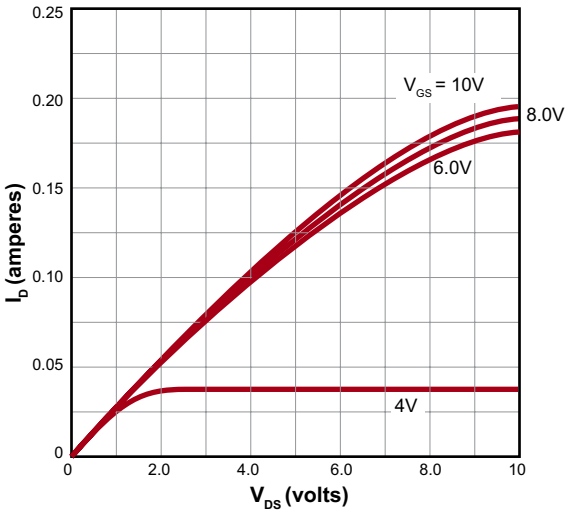


Typical Performance Curves *(cont.)*

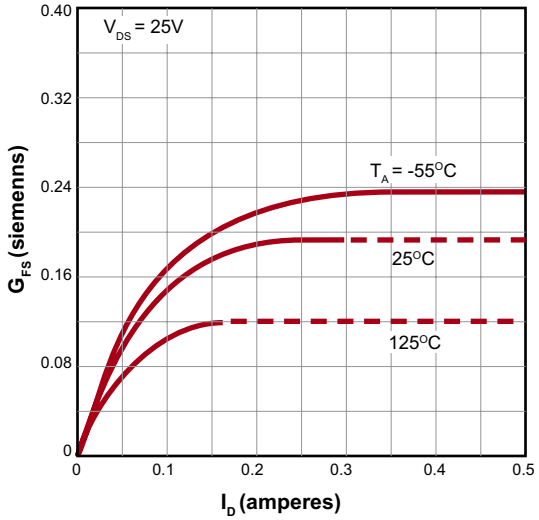
Output Characteristics



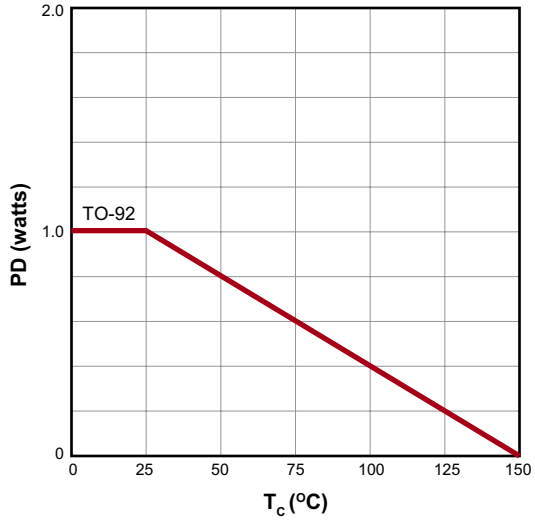
Saturation Characteristics



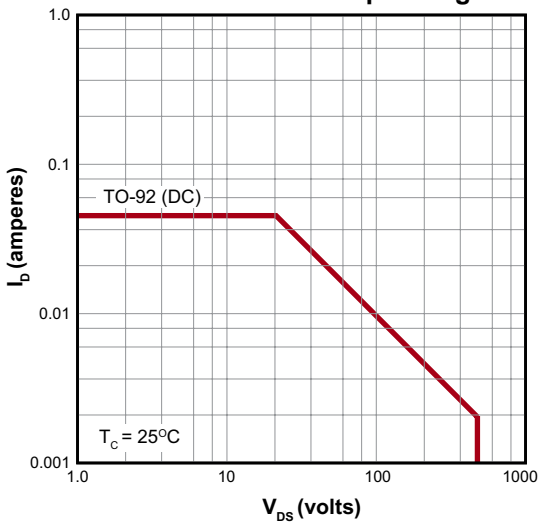
Transconductance vs. Drain Current



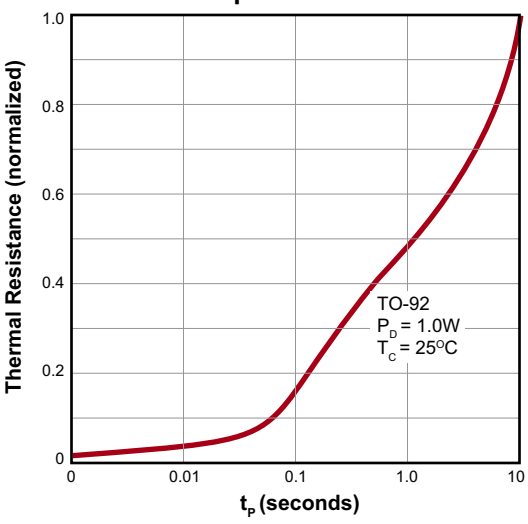
Power Dissipation vs. Case Temperature



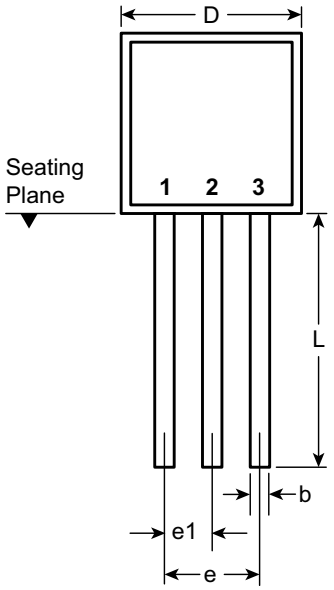
Maximum Rated Safe Operating Area



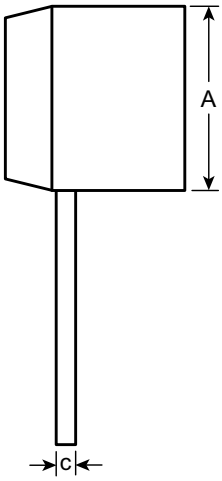
Thermal Response Characteristics



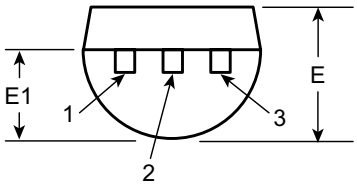
3-Lead TO-92 Package Outline (N3)



Front View



Side View



Bottom View

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014†	.014†	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022†	.022†	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
***Supertex Doc.#:** DSPD-3TO92N3, Version E041009.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

Supertex inc. does not recommend the use of its products in life support applications, and will not knowingly sell them for use in such applications unless it receives an adequate "product liability indemnification insurance agreement." **Supertex inc.** does not assume responsibility for use of devices described, and limits its liability to the replacement of the devices determined defective due to workmanship. No responsibility is assumed for possible omissions and inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications refer to the **Supertex inc.** (website: http//www.supertex.com)

©2013 **Supertex inc.** All rights reserved. Unauthorized use or reproduction is prohibited.

Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
Tel: 408-222-8888
www.supertex.com