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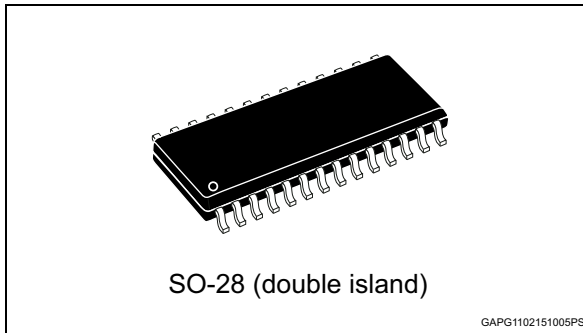
Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# Quad smart power solid state relay for complete H-bridge configurations

Datasheet - production data



- Thermal shutdown indication on both the high and low-side switches

## Applications

- DC motor driving in full or half bridge configuration
- All types of resistive, inductive and capacitive loads

## Description

The VN5770AKP-E is a device formed by three monolithic chips housed in a standard SO-28 package: a double high-side and two low-side switches. The double high-side is made using STMicroelectronics® VIPower® M0-5 technology, while the low-side switches are fully protected VIPower M0-3 OMNIFET II. This device is suitable to drive a DC motor in a bridge configuration as well as to be used as a quad switch for any low voltage application.

The dual high-side switches integrate built in non latching thermal shutdown with thermal hysteresis. An output current limiter protects the device in overload condition. In case of long overload duration, the device limits the dissipated power to a safe level up to thermal shutdown intervention. An analog current sense pin delivers a current proportional to the load current (according to a known ratio) and indicates overtemperature shutdown of the relevant high-side switch through a voltage flag.

The low-side switches have built in non latching thermal shutdown with thermal hysteresis, linear current limitation and overvoltage clamping.

Fault feedback for overtemperature shutdown of the low-side switch is indicated by the relevant input pin current consumption going up to the fault sink current flag.

## Features

Type	R <sub>DS(on)</sub>	I <sub>OUT</sub> (typ)	V <sub>CC</sub>
VN5770AKP-E	280 mΩ <sup>(1)</sup>	8.5 A	36 V

1. Total resistance of one side in bridge configuration

- ECOPACK®: lead free and RoHS compliant
- Automotive Grade: compliance with AEC guidelines
- General features
  - Inrush current management by active power limitation on the high-side switches
  - Very low standby current
  - Very low electromagnetic susceptibility
  - Compliance with European directive 2002/95/EC
- Protection
  - High-side drivers undervoltage shutdown
  - Overvoltage clamp
  - Output current limitation
  - High and low-side overtemperature shutdown
  - Short circuit protection
  - ESD protection
- Diagnostic functions
  - Proportional load current sense

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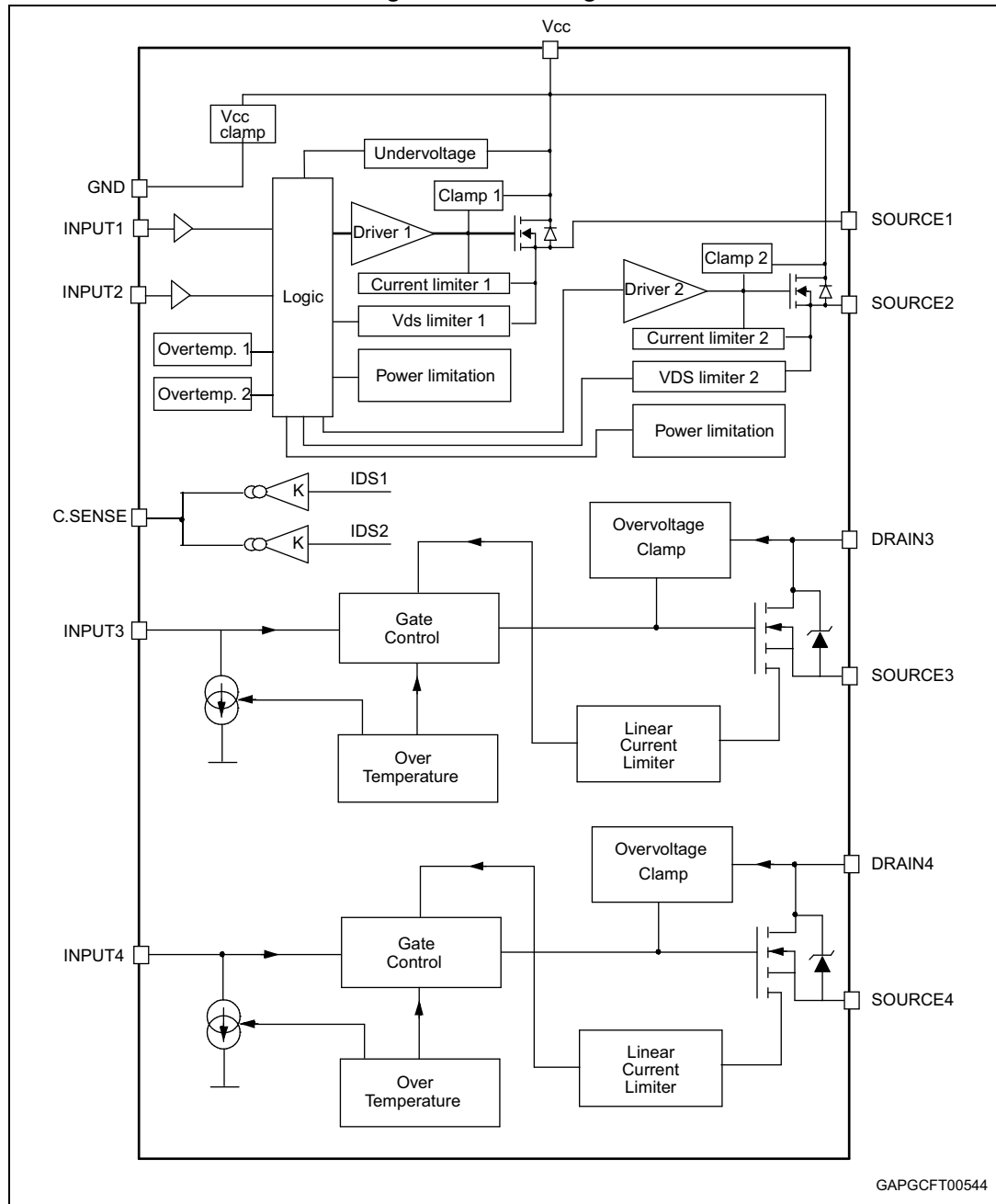


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# 1 Block diagram and pin descriptions

Figure 1. Block diagram



**Table 1. Pin descriptions**

No	Name	Function
1, 3, 25, 28	DRAIN 3	Drain of switch 3 (low-side switch)
2	INPUT 3	Input of switch 3 (low-side switch)
4, 11	N.C.	Not connected
5, 10, 19, 24	V <sub>CC</sub>	Drain of switches 1 and 2 (high-side switches) and power supply voltage
6	GND	Ground of switches 1 and 2 (high-side switches)
7	INPUT 1	Input of switch 1 (high-side switches)
8	INPUT 2	Input of switch 2 (high-side switch)
9	CURRENT SENSE	Analog current sense pin, it delivers a current proportional to the load current
12, 14, 15, 18	DRAIN 4	Drain of switch 4 (low-side switch)
13	INPUT 4	Input of switch 4 (low-side switch)
16, 17	SOURCE 4	Source of switch 4 (low-side switch)
20, 21	SOURCE 2	Source of switch 2 (high-side switch)
22, 23	SOURCE 1	Source of switch 1 (high-side switch)
26, 27	SOURCE 3	Source of switch 3 (low-side switch)

**Figure 2. Configuration diagram (top view)**

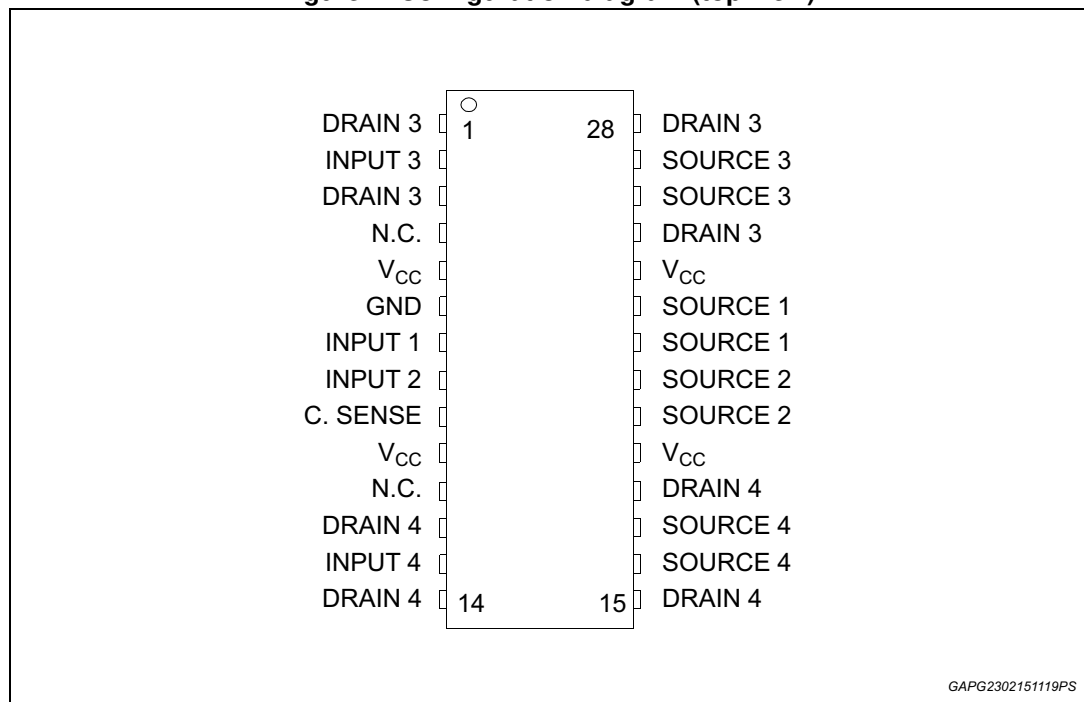


Table 2. Thermal data

Symbol	Parameter	Max value	Unit
$R_{thj-case}$	Thermal resistance junction-lead (high-side switch)	10	°C/W
$R_{thj-case}$	Thermal resistance junction-lead (low-side switch)	7	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	See <a href="#">Figure 39</a>	°C/W



## 2 Absolute maximum ratings

Stressing the device above the rating listed in [Table 3](#) and [Table 4](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in [Section 2.1: Absolute maximum ratings](#) for extended periods may affect device reliability.

### 2.1 Absolute maximum ratings

Table 3. Dual high-side switch

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
$I_{OUT}$	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-12	A
$I_{IN}$	DC input current	-1 to 10	mA
$I_{CSD}$	DC current sense disable input current	-1 to 10	mA
$V_{CSENSE}$	Current sense maximum voltage	$V_{CC}-41$ $+V_{CC}$	V V
$E_{MAX}$	Maximum switching energy (single pulse) ( $L = 3.7\text{ mH}$ ; $R_L = 0\ \Omega$ ; $V_{bat} = 13.5\text{ V}$ ; $T_{jstart} = 150\text{ }^\circ\text{C}$ ; $I_{OUT} = I_{limL}(Typ.)$ )	32	mJ
$V_{ESD}$	Electrostatic discharge (Human Body Model: $R = 1.5\text{ K}\Omega$ ; $C = 100\text{ pF}$ ) – INPUT – CURRENT SENSE – OUTPUT – $V_{CC}$	4000 2000 5000 5000	V V V V
$V_{ESD}$	Charge device model (CDM-AEC-Q100-011)	750	V
$T_j$	Junction operating temperature	-40 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$

Table 4. Low-side switch

Symbol	Parameter	Value	Unit
$V_{DSn}$	Drain-source voltage ( $V_{INn} = 0$ V)	Internally clamped	V
$V_{INn}$	Input voltage	Internally clamped	V
$I_{INn}$	Input current	+/-20	mA
$R_{IN\ MINn}$	Minimum input series impedance	220	$\Omega$
$I_{Dn}$	Drain current	Internally limited	A
$I_{Rn}$	Reverse DC output current	-12	A
$V_{ESD1}$	Electrostatic discharge ( $R = 1.5$ K $\Omega$ , $C = 100$ pF)	4000	V
$V_{ESD2}$	Electrostatic discharge on output pins only ( $R = 330$ $\Omega$ , $C = 150$ pF)	16500	V
$P_{tot}$	Total dissipation at $T_c = 25$ °C	4	W
$T_j$	Operating junction temperature	Internally limited	°C
$T_c$	Case operating temperature	Internally limited	°C
$T_{stg}$	Storage temperature	-55 to 150	°C

### 3 Electrical characteristics

#### 3.1 Electrical characteristics for dual high-side switch

Values specified in this section are for  $8\text{ V} < V_{CC} < 36\text{ V}$ ;  $-40\text{ °C} < T_j < 150\text{ °C}$ , unless otherwise specified (for each channel).

**Table 5. Power section**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC}$	Operating supply voltage		4.5	13	36	V
$V_{USD}$	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
$R_{ON}$	On-state resistance	$I_{OUT} = 3\text{ A}$ ; $T_j = 25\text{ °C}$		160		m $\Omega$
		$I_{OUT} = 3\text{ A}$ ; $T_j = 150\text{ °C}$			320	m $\Omega$
		$I_{OUT} = 3\text{ A}$ ; $V_{CC} = 5\text{ V}$ ; $T_j = 25\text{ °C}$			210	m $\Omega$
$V_{clamp}$	Clamp Voltage	$I_S = 20\text{ mA}$	41	46	52	V
$I_S$	Supply current	Off-state; $V_{CC} = 13\text{ V}$ ; $T_j = 25\text{ °C}$ ; $V_{IN} = V_{OUT} = V_{SENSE} = 0\text{ V}$		2 <sup>(1)</sup>	5 <sup>(1)</sup>	$\mu\text{A}$
		On-state; $V_{CC} = 13\text{ V}$ ; $V_{IN} = 5\text{ V}$ ; $I_{OUT} = 0\text{ A}$		3	6	mA
$I_{L(off)}$	Off-state output current <sup>(2)</sup>	$V_{IN} = V_{OUT} = 0\text{ V}$ ; $V_{CC} = 13\text{ V}$ ; $T_j = 25\text{ °C}$	0		3	$\mu\text{A}$
		$V_{IN} = V_{OUT} = 0\text{ V}$ ; $V_{CC} = 13\text{ V}$ ; $T_j = 125\text{ °C}$	0		5	$\mu\text{A}$
$V_F$	Output - $V_{CC}$ diode voltage <sup>(2)</sup>	$-I_{OUT} = 3\text{ A}$ ; $T_j = 150\text{ °C}$			0.7	V

1. PowerMOS leakage included

2. For each channel

**Table 6. Switching ( $V_{CC} = 13\text{ V}$ )**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 4.3\ \Omega$ (see <a href="#">Figure 3</a> )	—	15	—	$\mu\text{s}$
$t_{d(off)}$	Turn-off delay time	$R_L = 4.3\ \Omega$ (see <a href="#">Figure 3</a> )	—	10	—	$\mu\text{s}$
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	$R_L = 4.3\ \Omega$	—	See <a href="#">Figure 15</a>	—	V/ $\mu\text{s}$
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	$R_L = 4.3\ \Omega$	—	See <a href="#">Figure 17</a>	—	V/ $\mu\text{s}$
$W_{ON}$	Switching energy losses during $t_{won}$	$R_L = 4.3\ \Omega$ (see <a href="#">Figure 3</a> )	—	0.16	—	mJ
$W_{OFF}$	Switching energy losses during $t_{woff}$	$R_L = 4.3\ \Omega$ (see <a href="#">Figure 3</a> )	—	0.08	—	mJ

Table 7. Logic input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Input low level voltage				0.9	V
$I_{IL}$	Low level input current	$V_{IN} = 0.9\text{ V}$	1			$\mu\text{A}$
$V_{IH}$	Input high level voltage		2.1			V
$I_{IH}$	High level input current	$V_{IN} = 2.1\text{ V}$			10	$\mu\text{A}$
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
$V_{ICL}$	Input clamp voltage	$I_{IN} = 1\text{ mA}$	5.5		7	V
		$I_{IN} = -1\text{ mA}$		-0.7		V

Table 8. Protection and diagnostics<sup>(1)</sup>

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{limH}$	DC Short circuit current	$V_{CC} = 13\text{ V}$	6	8.5	12	A
		$5\text{ V} < V_{CC} < 36\text{ V}$			12	A
$I_{limL}$	Short circuit current during thermal cycling	$V_{CC} = 13\text{ V}; T_R < T_j < T_{TSD}$		3.5		A
$T_{TSD}$	Shutdown temperature		150	175	200	$^{\circ}\text{C}$
$T_R$	Reset temperature		$T_{RS} + 1$	$T_{RS} + 5$		$^{\circ}\text{C}$
$T_{RS}$	Thermal reset of STATUS		135			$^{\circ}\text{C}$
$T_{HYST}$	Thermal hysteresis ( $T_{TSD} - T_R$ )			7		$^{\circ}\text{C}$
$V_{DEMAG}$	Turn-off output voltage clamp	$I_{OUT} = 1\text{ A}; V_{IN} = 0;$ $L = 20\text{ mH}$	$V_{CC} - 41$	$V_{CC} - 46$	$V_{CC} - 52$	V
$V_{ON}$	Output voltage drop limitation	$I_{OUT} = 0.03\text{ A};$ $T_j = -40\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$ (see <a href="#">Figure 4</a> )		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles

Table 9. Current sense (8V<V<sub>CC</sub><16V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K <sub>0</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 0.08 A; V <sub>SENSE</sub> = 0.5 V; T <sub>j</sub> = -40°C to 50°C	850	1450	2120	
K <sub>1</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 0.35 A; V <sub>SENSE</sub> = 0.5V; T <sub>j</sub> = -40°C to 150°C T <sub>j</sub> = 25°C to 150°C	840 980	1360 1360	2000 1740	
K <sub>2</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 3A; V <sub>SENSE</sub> = 4V; T <sub>j</sub> = -40°C to 150°C	1200	1270	1350	
K <sub>3</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 4A; V <sub>SENSE</sub> = 4V; T <sub>j</sub> = -40°C to 150°C	1200	1270	1350	
I <sub>SENSE0</sub>	Analog sense current	I <sub>OUT</sub> = 0A; V <sub>SENSE</sub> = 0V; V <sub>IN</sub> = 0V; T <sub>j</sub> = -40°C to 150°C	0		1	μA
		I <sub>OUT</sub> = 0A; V <sub>SENSE</sub> = 0V; V <sub>IN</sub> = 5V; T <sub>j</sub> = -40°C to 150°C	0		2	μA
V <sub>SENSE</sub>	Max analog sense output voltage	I <sub>OUT</sub> = 5A; R <sub>SENSE</sub> = 3.9 KΩ	5			V
V <sub>SENSEH</sub>	Analog sense output voltage in overtemperature condition	V <sub>CC</sub> = 13V; R <sub>SENSE</sub> = 3.9 KΩ		9		V
I <sub>SENSEH</sub>	Analog sense output current in overtemperature condition	V <sub>CC</sub> = 13V		8		mA
t <sub>DSSENSE2H</sub>	Delay response time from rising edge of INPUT pin	V <sub>SENSE</sub> <4 V; 0.35 A<I <sub>out</sub> <5 A; I <sub>SENSE</sub> = 90% of I <sub>SENSE</sub> max (see Figure 5)		70	300	μs
t <sub>DSSENSE2L</sub>	Delay response time from falling edge of INPUT pin	V <sub>SENSE</sub> <4 V; 0.35 A<I <sub>out</sub> <5 A; I <sub>SENSE</sub> = 10% of I <sub>SENSE</sub> max (see Figure 5)		100	250	μs

Figure 3. Switching time waveforms

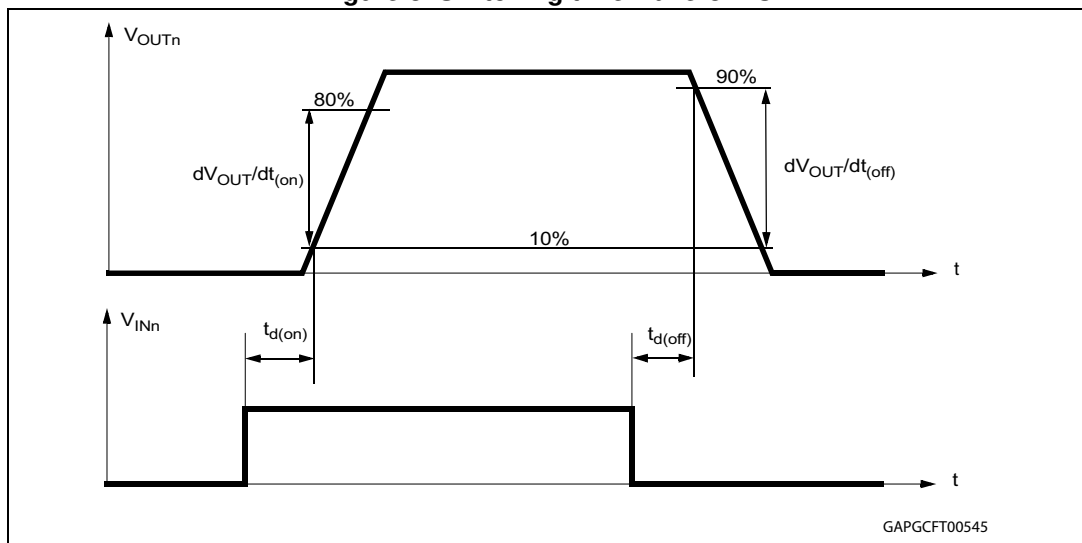


Figure 4. Output voltage drop limitation

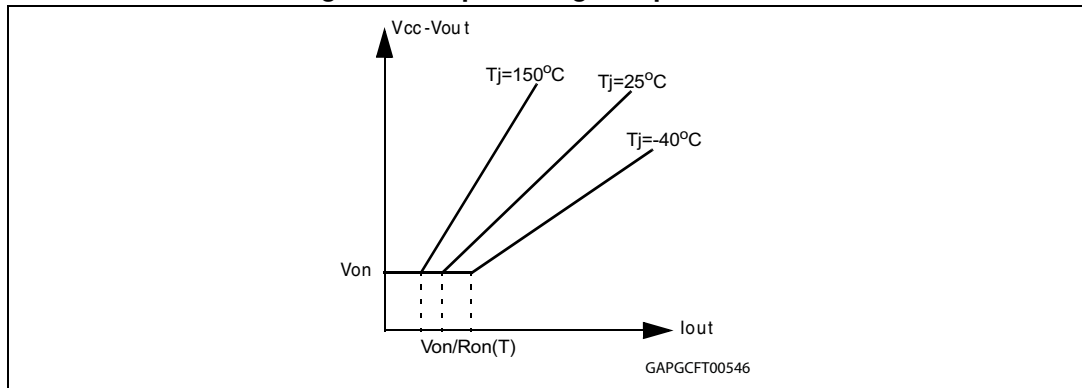
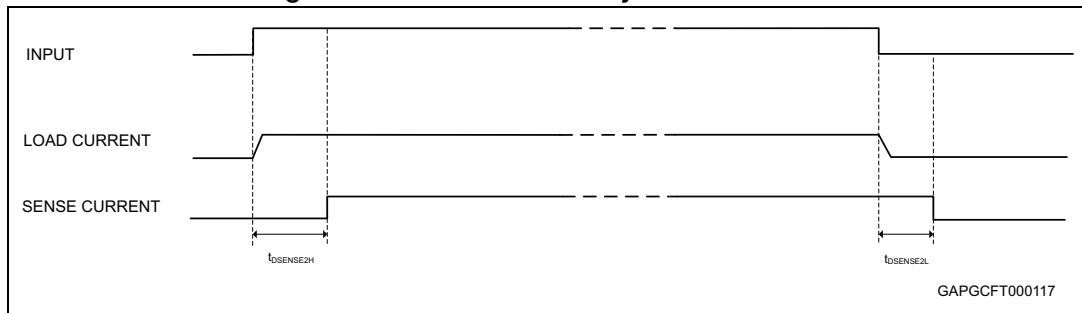


Table 10. Truth table

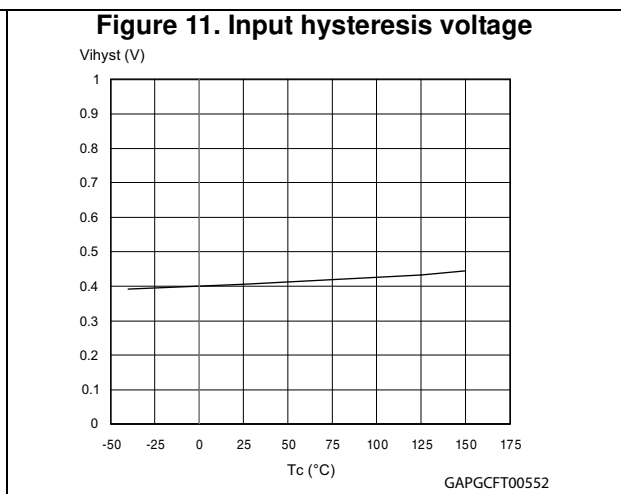
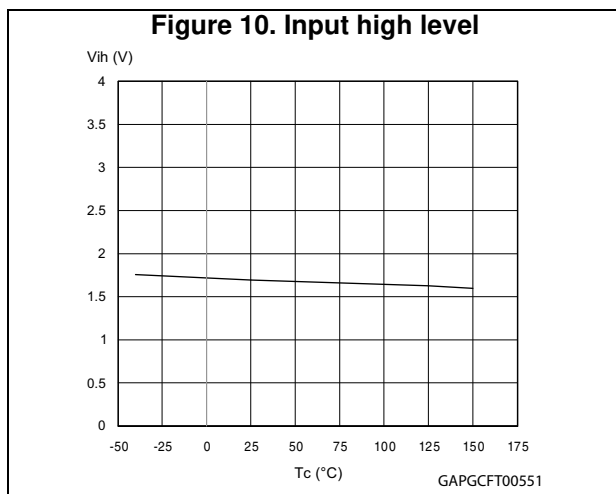
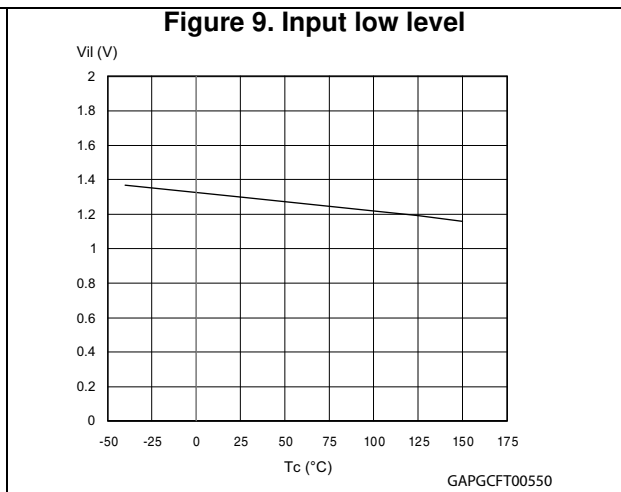
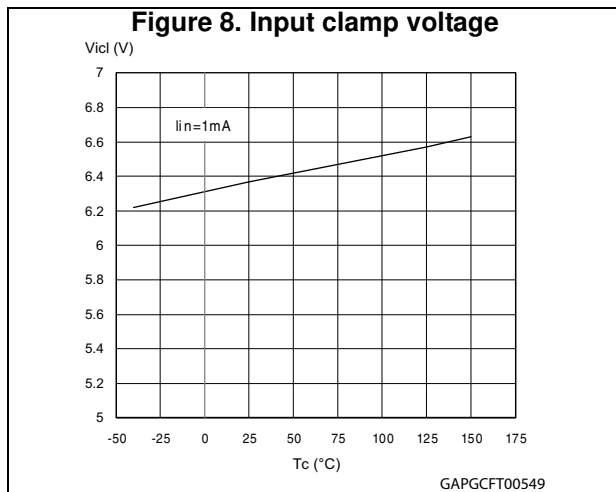
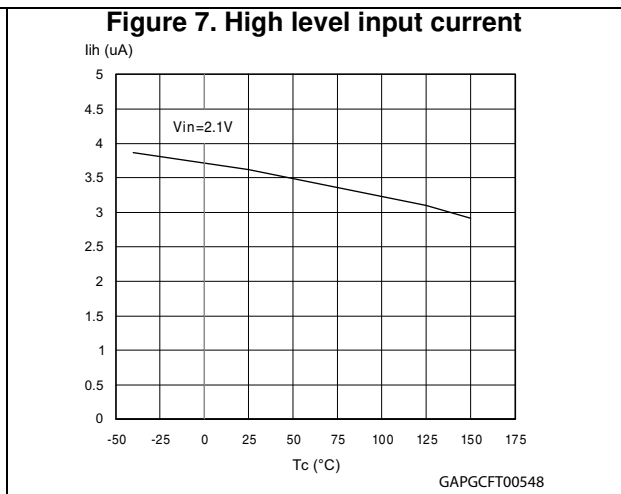
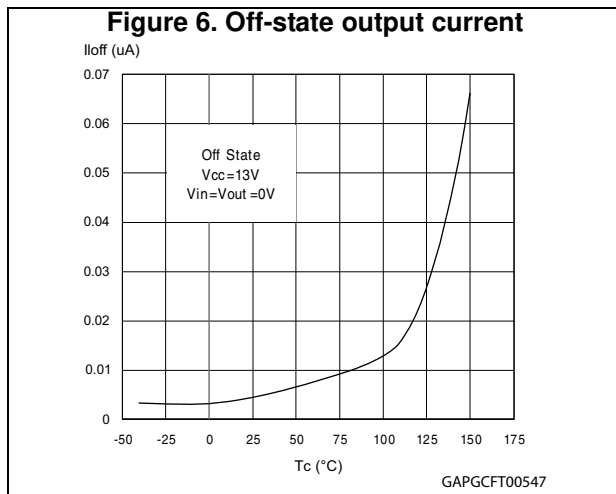
Conditions	Input	Output	Sense
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	$V_{SENSEH}$
Undervoltage	L	L	0
	H	L	0
Short circuit to GND	L	L	0
	H	L	0
Short circuit to $V_{CC}$	L	H	0
	H	H	< Nominal
Negative output voltage clamp	L	L	0

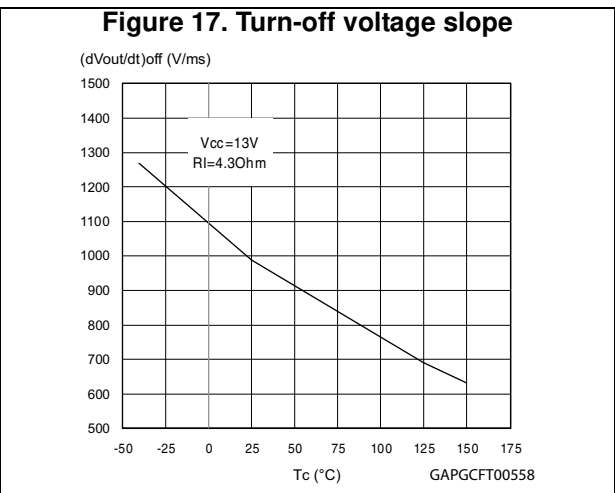
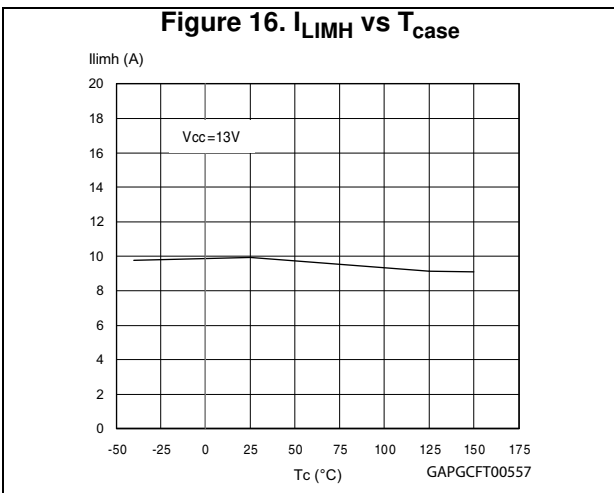
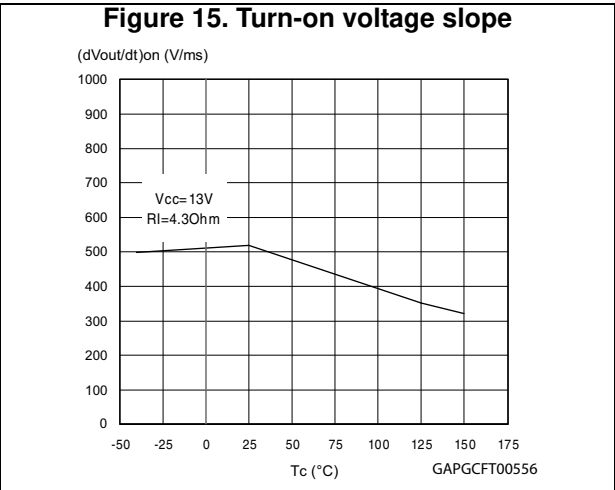
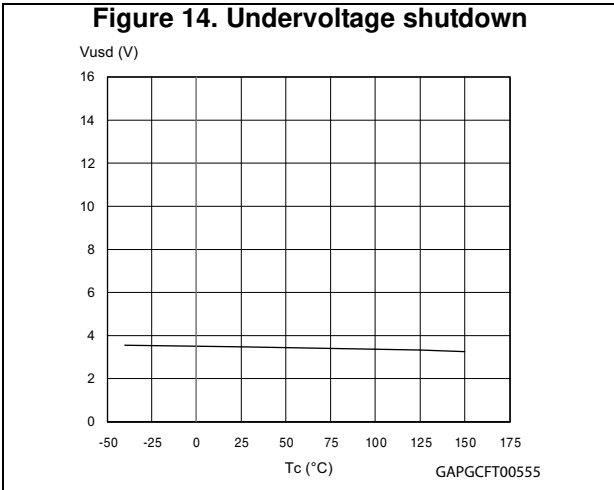
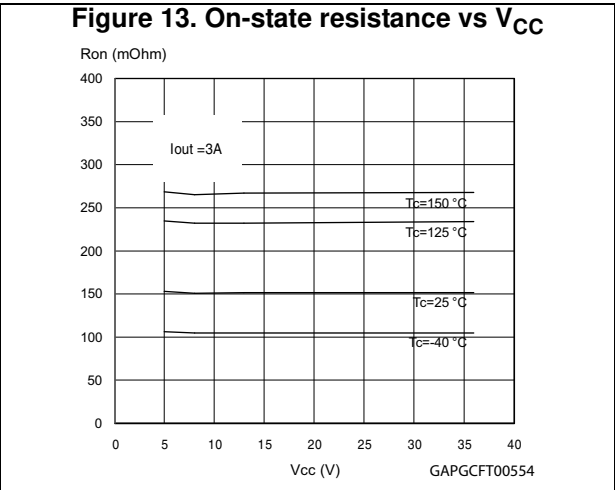
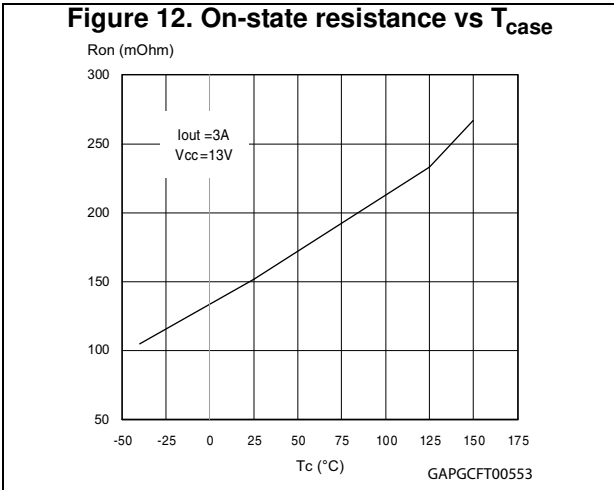
Figure 5. Current sense delay characteristics





# 4 Electrical characteristics curves for dual high-side switch





### 4.1 Electrical characteristics for low-side switches

Values specified in this section are for  $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$ , unless otherwise specified

**Table 11. Off**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{CLAMP}$	Drain-source clamp voltage	$V_{IN} = 0\text{ V}; I_D = 1.5\text{ A}$	40	45	55	V
$V_{CLTH}$	Drain-source clamp threshold voltage	$V_{IN} = 0\text{ V}; I_D = 2\text{ mA}$	36			V
$V_{INTH}$	Input threshold voltage	$V_{DS} = V_{IN}; I_D = 1\text{ mA}$	0.5		2.5	V
$I_{ISS}$	Supply current from input pin	$V_{DS} = 0\text{ V}; V_{IN} = 5\text{ V}$		100	150	$\mu\text{A}$
$V_{INCL}$	Input-source clamp voltage	$I_{IN} = 1\text{ mA}$	6	6.8	8	V
		$I_{IN} = -1\text{ mA}$	-1.0		-0.3	V
$I_{DSS}$	Zero input voltage drain current ( $V_{IN} = 0\text{V}$ )	$V_{DS} = 13\text{ V}; V_{IN} = 0\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$			30	$\mu\text{A}$
		$V_{DS} = 25\text{ V}; V_{IN} = 0\text{ V}$			75	$\mu\text{A}$

**Table 12. On**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$R_{DS(on)}$	Static drain-source on resistance	$V_{IN} = 5\text{ V}; I_D = 3\text{ A}; T_j = 25\text{ }^{\circ}\text{C}$	—	—	120	$\text{m}\Omega$
		$V_{IN} = 5\text{ V}; I_D = 3\text{ A}$	—	—	240	$\text{m}\Omega$

**Table 13. Dynamic ( $T_j = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$g_{fs}$	Forward transconductance	$V_{DD} = 13\text{ V}; I_D = 1.5\text{ A}$	—	2.5	—	S
$C_{OSS}$	Output capacitance	$V_{DS} = 13\text{ V}; f = 1\text{ MHz}; V_{IN} = 0\text{ V}$	—	150	—	$\text{pF}$

**Table 14. Switching ( $T_j = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}; I_D = 3\text{ A}; V_{gen} = 5\text{ V}; R_{gen} = R_{IN\text{ MIN}n} = 220\text{ }\Omega$	—	200	400	ns
$t_r$	Rise time		—	1.2	2.5	$\mu\text{s}$
$t_{d(off)}$	Turn-off delay time		—	600	1350	ns
$t_f$	Fall time		—	400	1000	ns
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}; I_D = 3\text{ A}; V_{gen} = 5\text{ V}; R_{gen} = 2.2\text{ K}\Omega$	—	0.80	2.5	$\mu\text{s}$
$t_r$	Rise time		—	3.7	7.5	$\mu\text{s}$
$t_{d(off)}$	Turn-off delay time		—	2.6	7.5	$\mu\text{s}$
$t_f$	Fall time		—	2.3	7.0	$\mu\text{s}$

Table 14. Switching ( $T_j = 25\text{ °C}$ , unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$(di/dt)_{on}$	Turn-on current slope	$V_{DD} = 15\text{ V}$ ; $I_D = 3\text{ A}$ ; $V_{gen} = 5\text{ V}$ ; $R_{gen} = R_{IN\ MINn} = 220\ \Omega$	—	3.0		A/ $\mu$ s
$Q_i$	Total input charge	$V_{DD} = 12\text{ V}$ ; $I_D = 3\text{ A}$ ; $V_{IN} = 5\text{ V}$ ; $I_{gen} = 2.13\text{ mA}$	—	9.0		nC

Table 15. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 1.5\text{ A}$ ; $V_{IN} = 0\text{ V}$	—	0.8	—	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 1.5\text{ A}$ ; $di/dt = 12\text{ A/ms}$ ; $V_{DD} = 30\text{ V}$ ; $L = 200\ \mu\text{H}$	—	400	—	ns
$Q_{rr}$	Reverse recovery charge		—	200	—	nC
$I_{RRM}$	Reverse recovery current		—	1.0	—	A

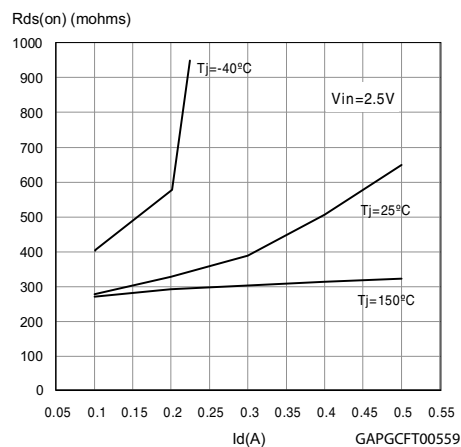
1. Pulsed: pulse duration = 300 $\mu$ s, duty cycle 1.5%

Table 16. Protection and diagnostics ( $-40\text{ °C} < T_j < 150\text{ °C}$ , unless otherwise specified)

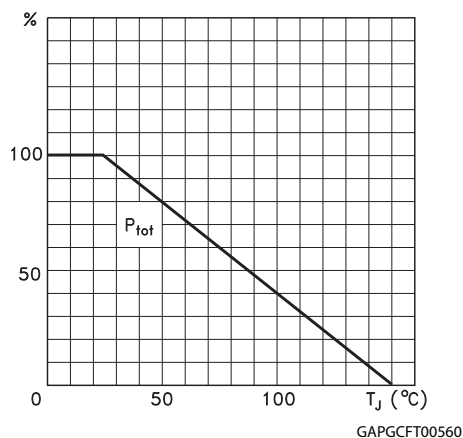
Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$I_{lim}$	Drain current limit	$V_{IN} = 5\text{ V}$ ; $V_{DS} = 13\text{ V}$	6	8.5	12	A
$t_{dlim}$	Step response current limit	$V_{IN} = 5\text{ V}$ ; $V_{DS} = 13\text{ V}$		10		$\mu$ s
$T_{jsh}$	Overtemperature shutdown		150	175	200	$^{\circ}\text{C}$
$T_{jrs}$	Overtemperature reset		135			$^{\circ}\text{C}$
$I_{gf}$	Fault sink current	$V_{IN} = 5\text{ V}$ ; $V_{DS} = 13\text{ V}$ ; $T_j = T_{jsh}$	10	15	20	mA
$E_{as}$	Single pulse avalanche energy	Starting $T_j = 25\text{ °C}$ ; $V_{DD} = 24\text{ V}$ ; $V_{IN} = 5\text{ V}$ ; $R_{gen} = R_{IN\ MINn} = 220\ \Omega$ ; $L = 24\text{ mH}$	100			mJ

## 4.2 Electrical characteristics curves for low-side switches

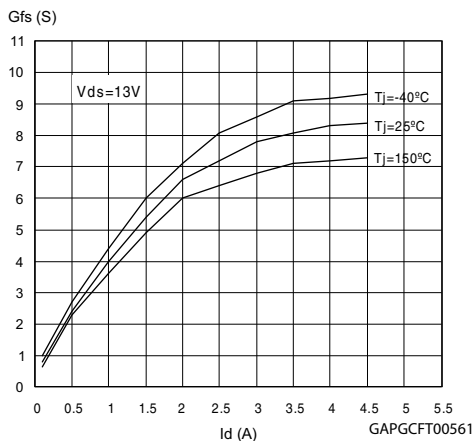
**Figure 18. Static drain source on resistance**



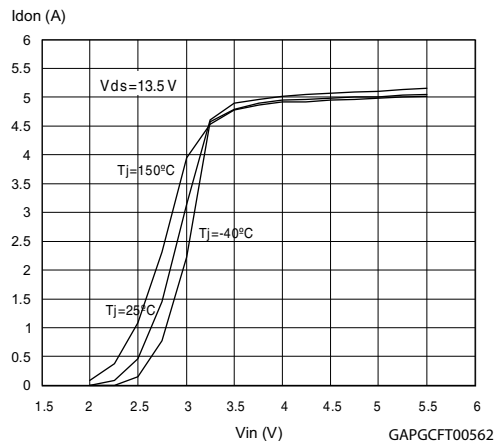
**Figure 19. Derating curve**



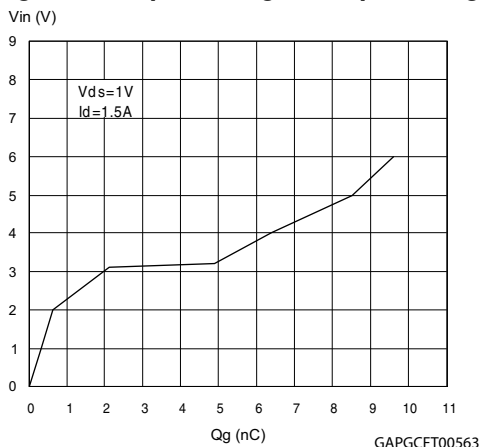
**Figure 20. Transconductance**



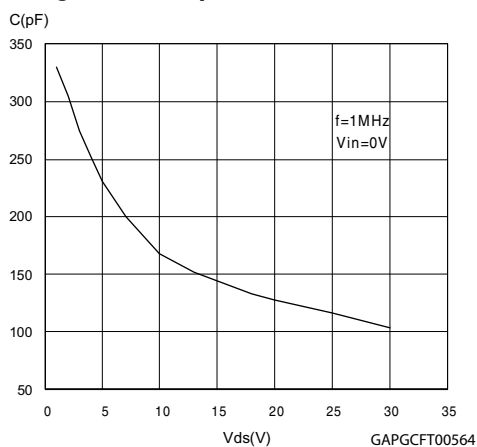
**Figure 21. Transfer characteristics**

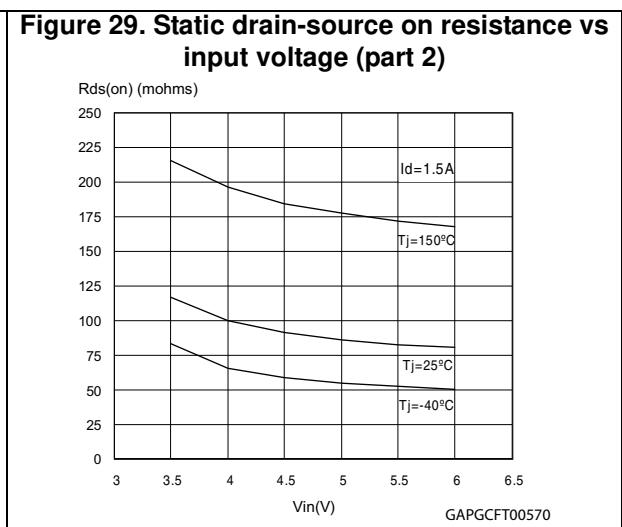
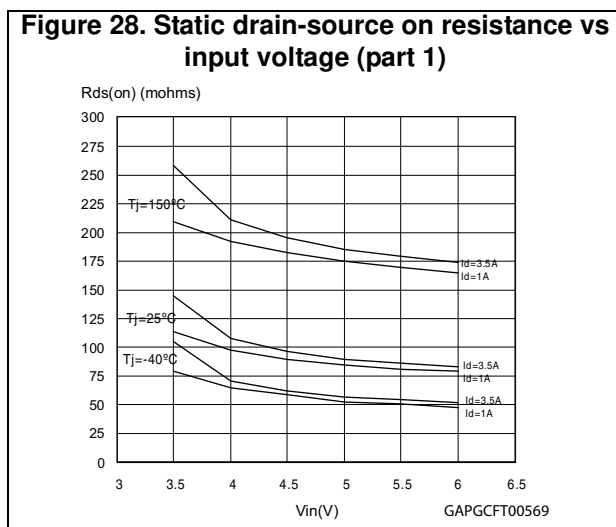
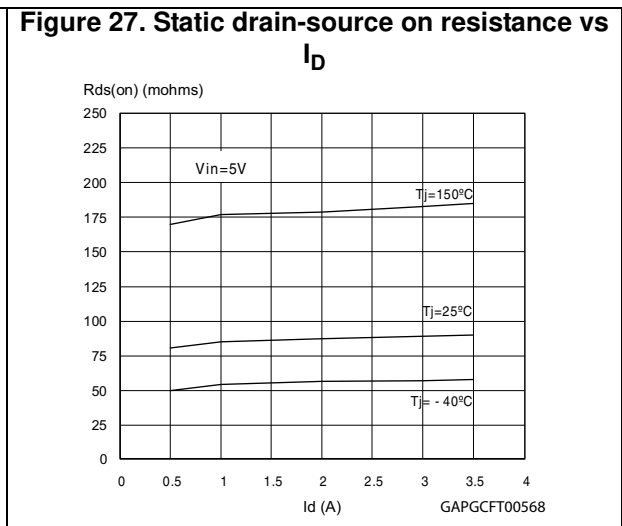
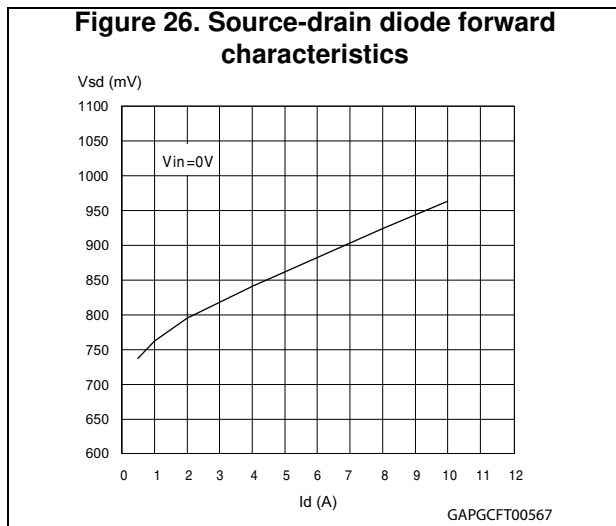
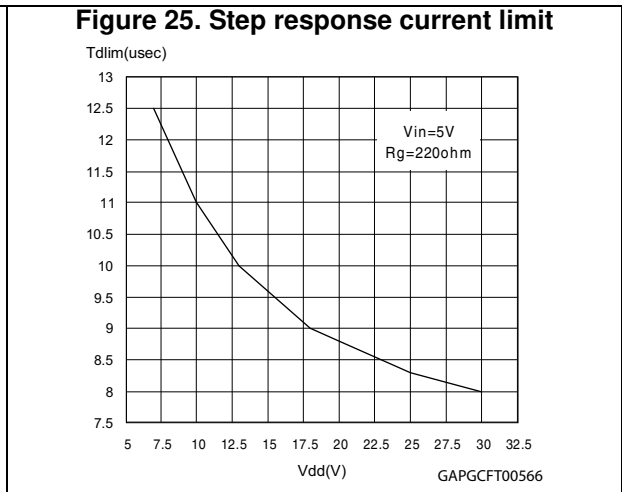
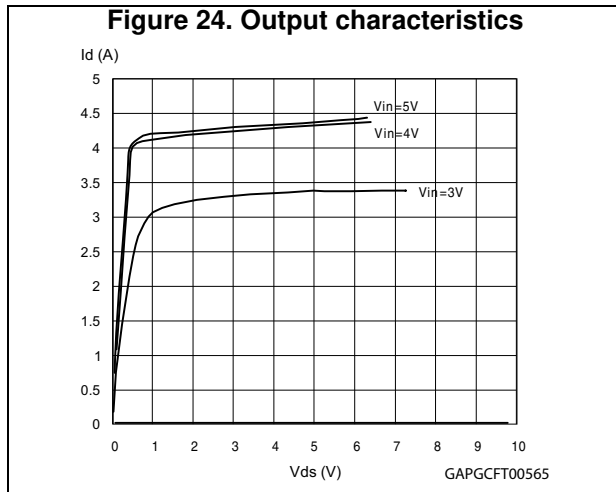


**Figure 22. Input voltage vs input charge**



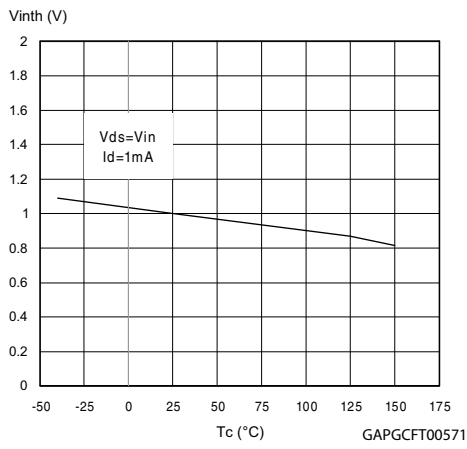
**Figure 23. Capacitance variations**



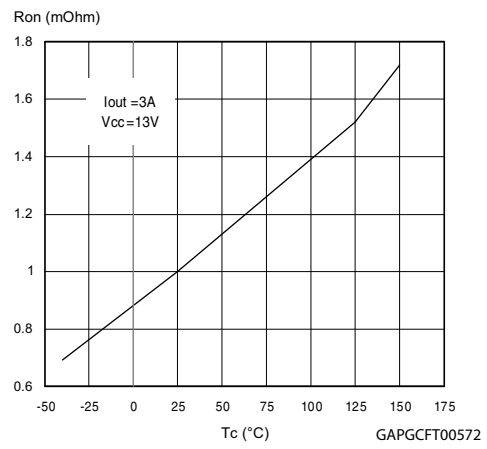




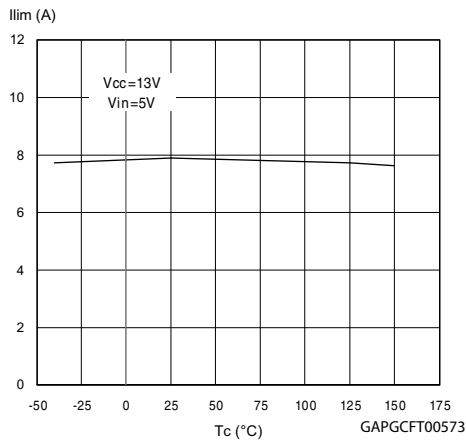
**Figure 30. Normalized input threshold voltage vs temperature**



**Figure 31. Normalized on resistance vs temperature**

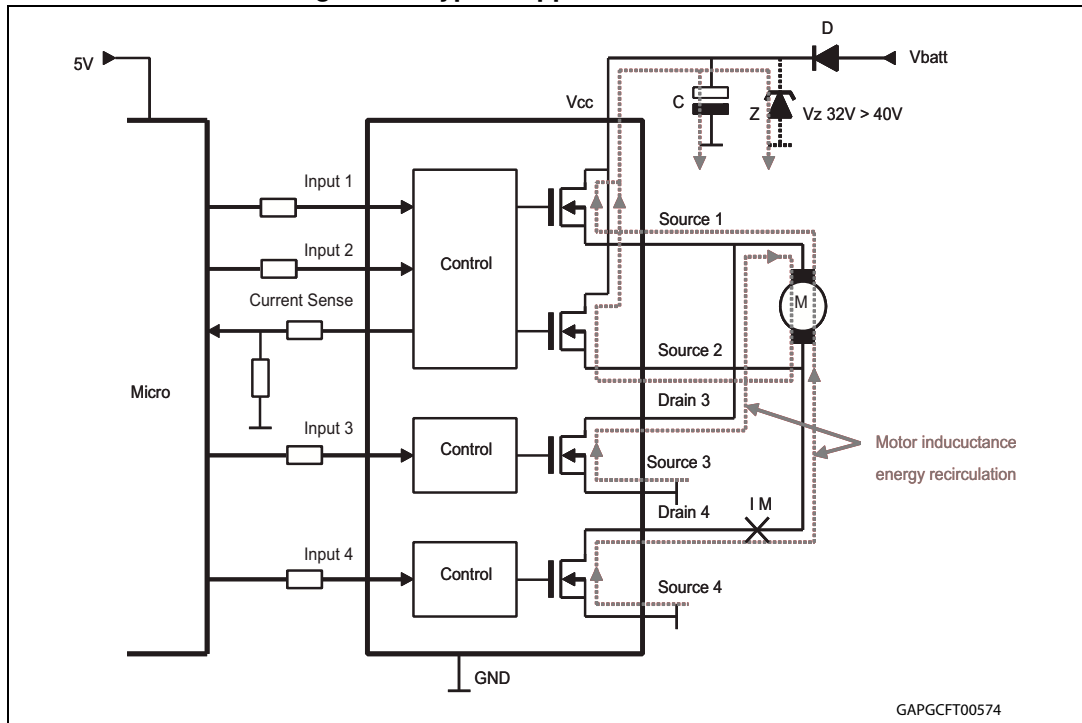


**Figure 32. Current limit vs junction temperature**



## 5 Application information

Figure 33. Typical application schematic



**Note:** *Mostly motor bridge drivers use a reverse battery protection diode (D) inside supply rail. This diode prevents a reverse current flow back to Vbatt in case the bridge gets disabled via the logic inputs while motor inductance still carries energy. In order to prevent a hazardous overvoltage at circuit supply terminal (Vcc), a blocking capacitor (C) is needed to limit the voltage overshoot. As basic orientation, 50  $\mu$ F per 1 A load current is recommended. In alternative, also a Zener protection (Z) is suitable. Even if a reverse polarity diode is not present, it is recommended to use a capacitor or zener at Vcc because a similar problem appears in case supply terminal of the module has intermittent electrical contact to the battery or gets disconnected while motor is operating.*

Figure 34. Recommended motor operation

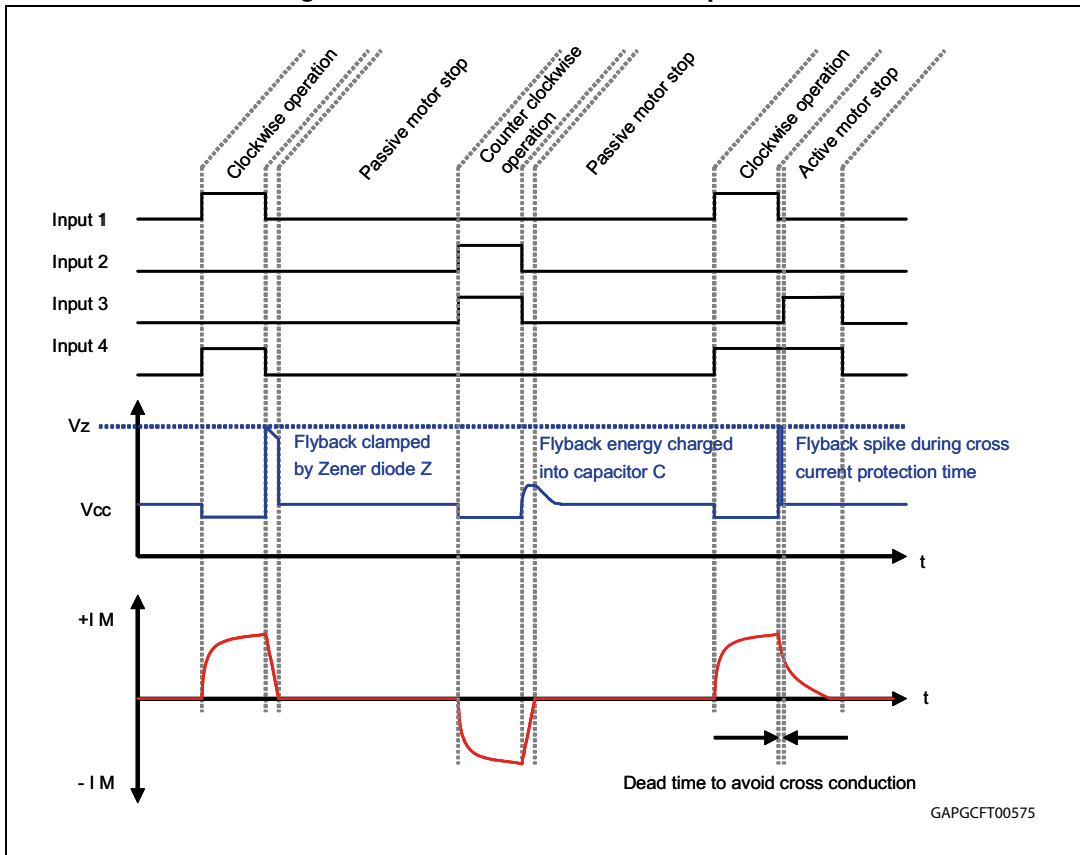
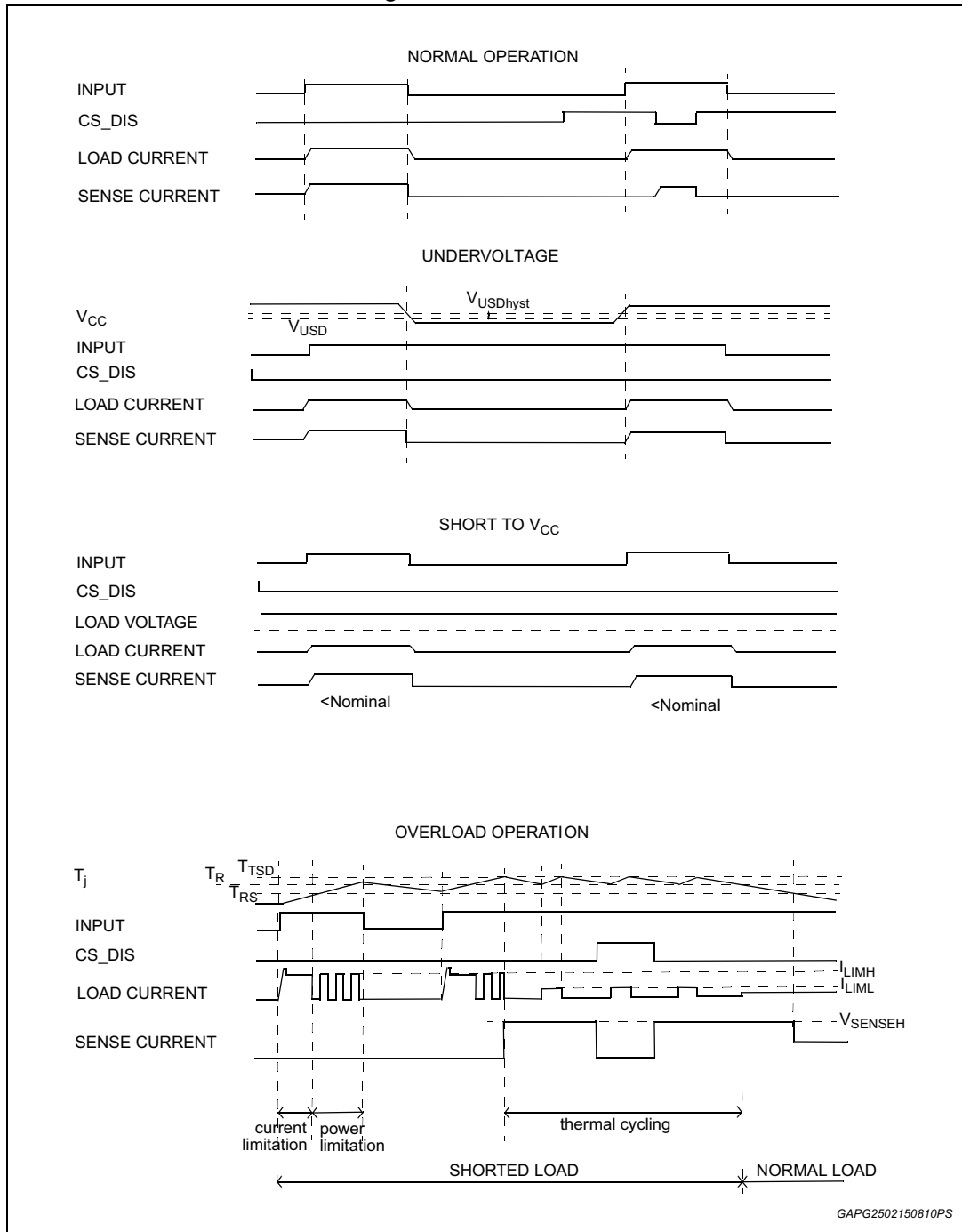
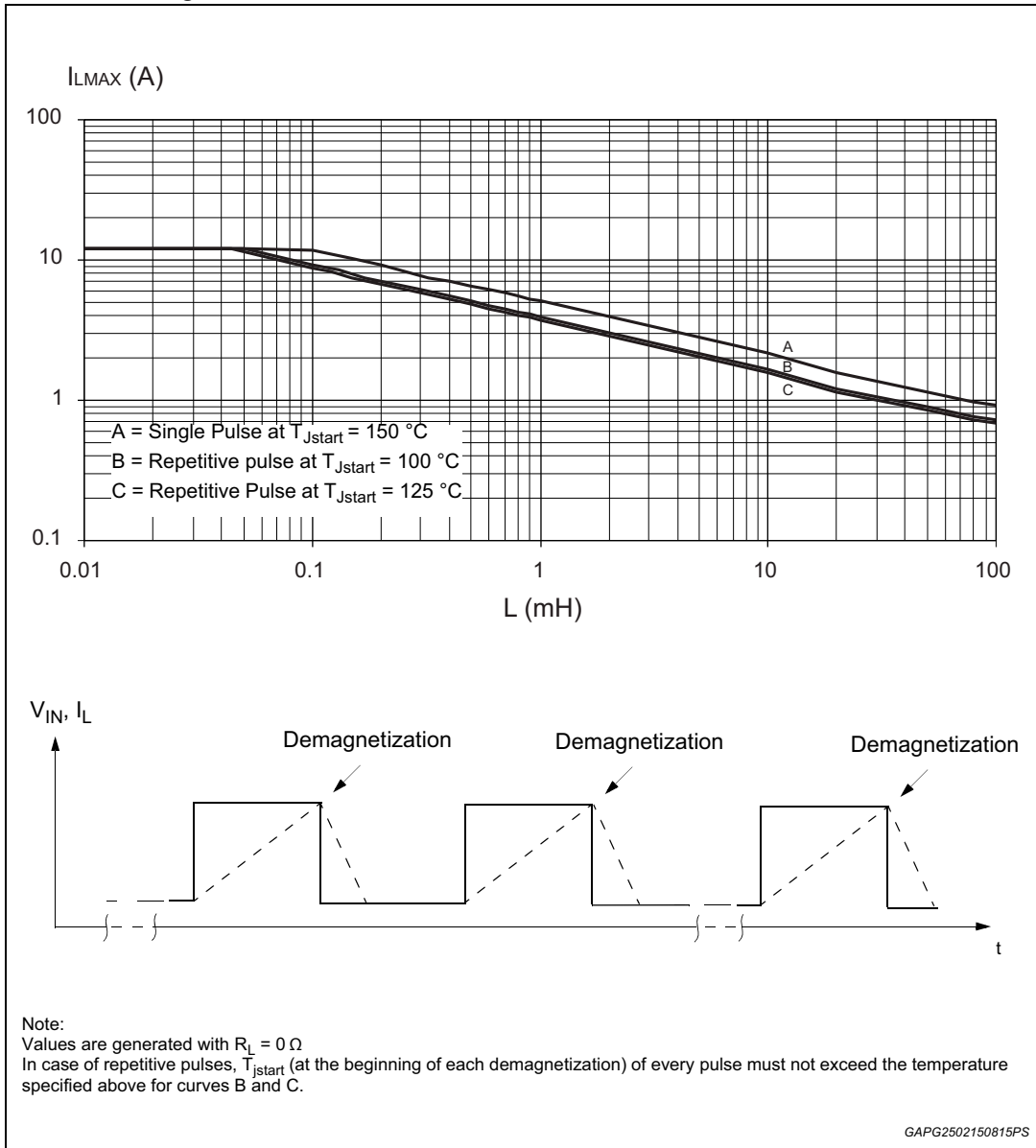


Figure 35. Waveforms



### 5.1 Maximum demagnetization energy ( $V_{CC} = 13.5\text{ V}$ )

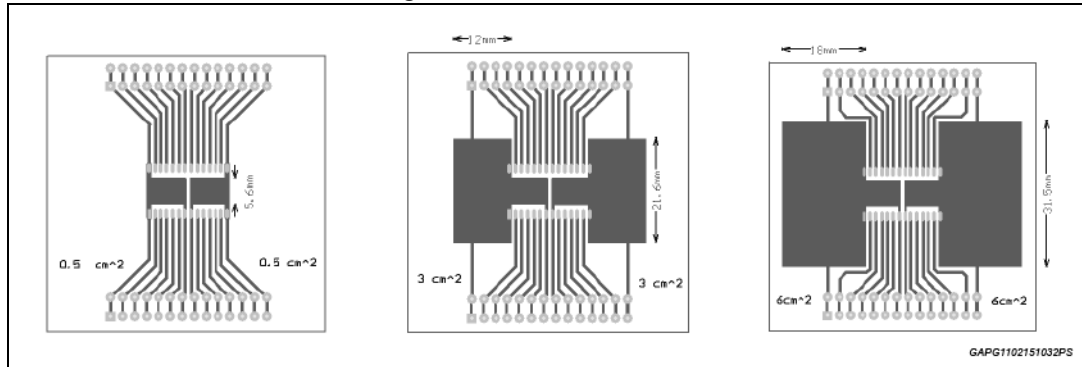
Figure 36. Maximum turn off current versus load inductance



## 6 Package and thermal data

### 6.1 SO-28 thermal data

Figure 37. SO-28 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area= 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 mm, Copper areas: from minimum pad layout to 16 cm<sup>2</sup>).

Figure 38. Chipset configuration

