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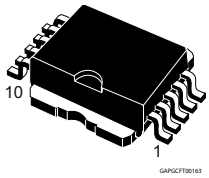
VN5E006ASP-E

Single channel high-side driver with analog current sense for automotive applications

Datasheet - production data



PowerSO-10

Features

Max transient supply voltage	V_{CC}	41 V
Operating voltage range	V_{CC}	4.5 to 28 V
Max on-state resistance (per ch.)	R_{ON}	6 mΩ
Current limitation (typ)	I_{LIMH}	90 A
Off-state supply current	I_S	2 µA(1)

1. Typical value with all loads connected.

- General
  - Very low standby current
  - 3.0 V CMOS compatible inputs
  - Optimized electromagnetic emissions
  - Very low electromagnetic susceptibility
  - Compliance with European directive 2002/95/EC
  - Very low current sense leakage
- Diagnostic functions
  - Proportional load current sense
  - High current sense precision for wide currents range
  - Diagnostic enable pin
  - Off-state open-load detection
  - Output short to V_{CC} detection
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
- Protection
  - Inrush current active management by power limitation
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of V_{CC}
  - Overtemperature shutdown with auto restart (thermal shutdown)
  - Reverse battery protected with self switch of the Power MOSFET
  - Electrostatic discharge protection

Applications

- All types of resistive, inductive and capacitive loads

Description

The VN5E006ASP-E is a single channel high-side driver manufactured using ST proprietary VIPower® M0-5 technology and housed in PowerSO-10 package. The device is designed to drive 12 V automotive grounded loads delivering protection, diagnostics. It also implements a 3 V and 5 V CMOS-compatible interface for use with any microcontroller.

The device integrates advanced protective functions such as load current limitation, inrush and overload active management by power limitation, overtemperature shut-off with auto-restart and overvoltage active clamp. A dedicated analog current sense pin is associated with every output channel providing enhanced diagnostic functions including fast detection of overload and short-circuit to ground through power limitation indication, over-temperature indication, short-circuit to V_{CC} diagnosis and on-state and off-state open-load detection. The current sensing and diagnostic feedback of the whole device can be disabled by pulling the DE pin low to share the external sense resistor with similar devices.

Contents

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1 Block diagram and pin description

Figure 1. Block diagram

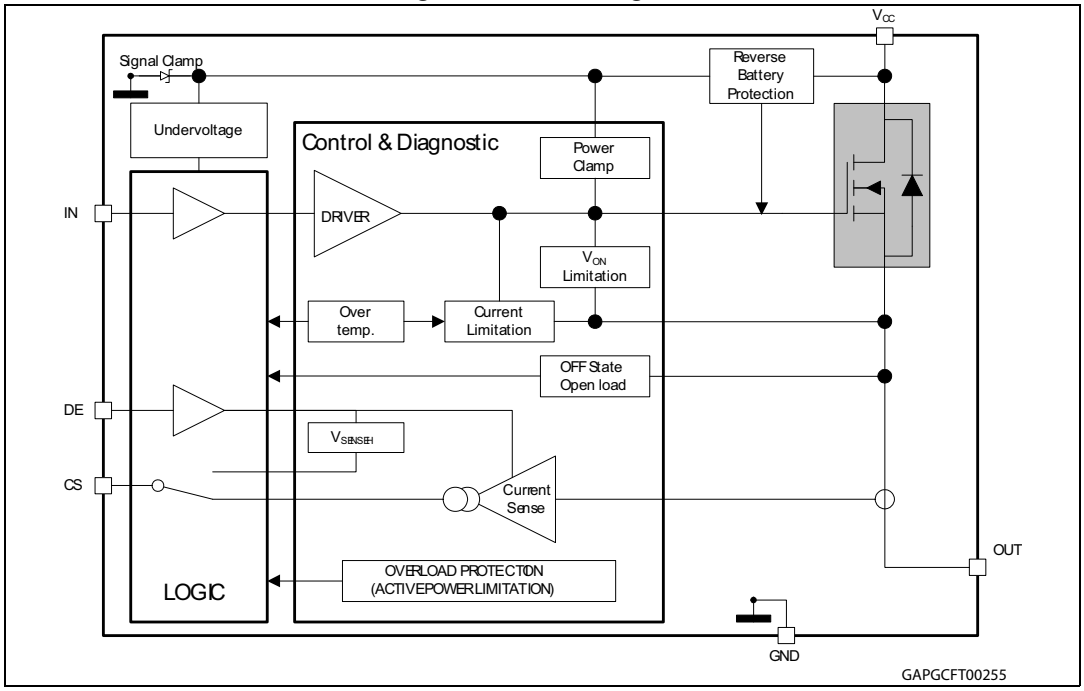


Table 1. Pin function

Name	Function
V_{CC}	Battery connection.
OUTPUT	Power output.
GND	Ground connection.
INPUT	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state.
CURRENT SENSE	Analog current sense pin, delivers a current proportional to the load current.
DE	Active high diagnostic enable pin.

Figure 2. Configuration diagram (top view)

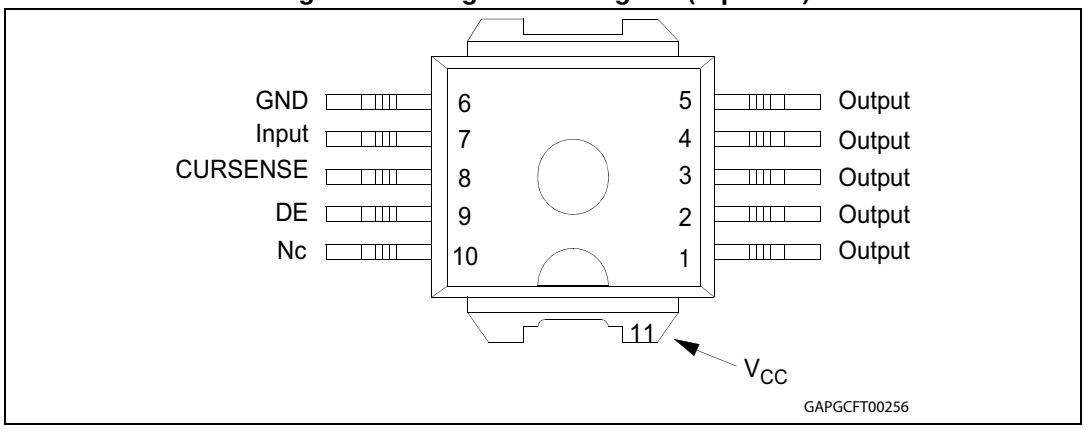
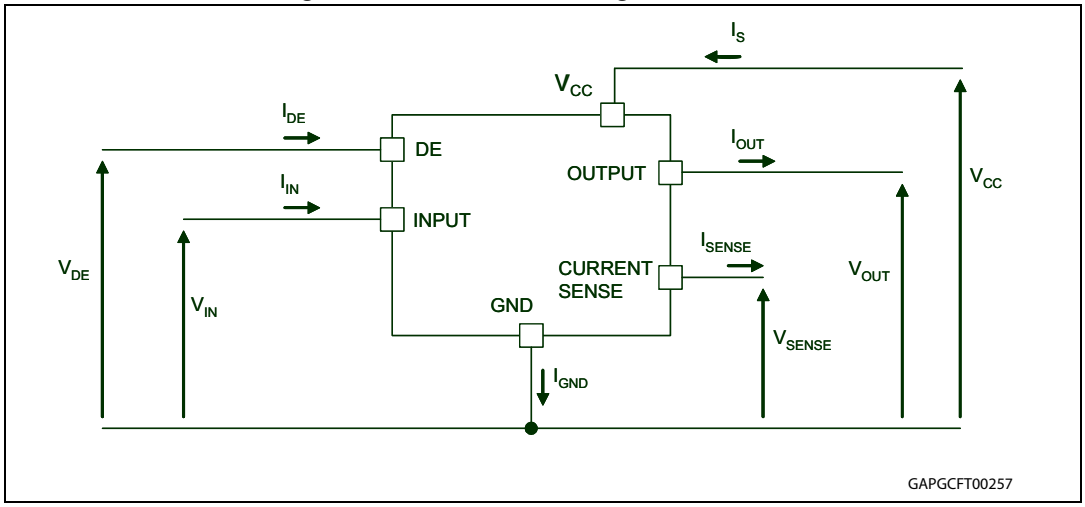


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input	DE
Floating	Not allowed	X	X	X	X
To ground	Through 1KΩ resistor	X	Not allowed	Through 10KΩ resistor	Through 10KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the ratings listed in *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in this section for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	28	V
V_{CCPK}	Transient supply voltage (T < 400 ms, R_{LOAD} > 0.5 Ω)	41	V
$-V_{CC}$	Reverse DC supply voltage	16	V
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	60	A
I_{IN}	DC input current	-1 to 10	mA
I_{DE}	DC diagnostic enable input current	-1 to 10	mA
V_{CSENSE}	Current sense maximum voltage	V_{CC}-41 +V_{CC}	V V
E_{MAX}	Maximum switching energy (single pulse) (L = 1.4 mH; R_L = 0 Ω; V_{bat} = 13.5 V; T_{jstart} = 150 °C; I_{OUT} = I_{limL}(*Typ.*))	600	mJ
V_{ESD}	Electrostatic discharge (Human Body Model: R = 1.5 KΩ; C = 100 pF)	2000	V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
T_j	Junction operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Maximum value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case (one channel ON)	0.45	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	See *Figure 36* in the thermal section	°C/W

2.3 Electrical characteristics

8 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	ON state resistance	I_{OUT} = 10 A; T_j = 25 °C		4.5		mΩ
		I_{OUT} = 10 A; T_j = 150 °C			9	
		I_{OUT} = 10 A; V_{CC} = 5 V; T_j = 25 °C			6	
$R_{ON\ REV}$	Reverse battery on state resistance	V_{CC} = -13 V; I_{OUT} = -10 A; T_j = 25 °C			6	mΩ
V_{clamp}	Clamp voltage	I_S = 20 mA	41	46	52	V
I_S	Supply current	Disable V_{DE} = 0 V; V_{CC} = 13 V; T_j = 25 °C; V_{IN}=x; V_{OUT} = V_{SENSE} = 0 V		2	5	µA
		Off state; V_{CC} = 13 V; V_{DE} = 5 V; T_j = 25 °C; V_{IN} = V_{OUT} = V_{SENSE} = 0 V		10(1)	15(1)	
		On state; V_{CC} = 13 V; V_{DE} = 5 V; V_{IN} = 5 V; I_{OUT} = 0 A		2	4	mA
$I_{L(off1)}$	Off state output current (2)	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 25 °C	0	0.01	3	µA
		V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 125 °C	0		5	

1. PowerMOS leakage included.
2. For each channel.

Table 6. Switching (V_{CC} = 13 V; T_j = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 1.3 Ω (see *Figure 6*)	—	30	—	µs
$t_{d(off)}$	Turn-off delay time	R_L = 1.3 Ω (see *Figure 6*)	—	30	—	µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	R_L = 1.3 Ω	—	See *Figure 27*	—	V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	R_L = 1.3 Ω	—	See *Figure 28*	—	V/µs
W_{ON}	Switching energy losses during t_{won}	R_L = 1.3 Ω (see *Figure 6*)	—	3	—	mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L = 1.3 Ω (see *Figure 6*)	—	1.5	—	mJ

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.5		7	V
		I_{IN} = -1 mA		-0.7		
V_{DEL}	DE low level voltage				0.9	V
I_{DEL}	DE low level current	V_{IN} = 0.9 V	1			µA
V_{DEH}	DE high level voltage		2.1			V
I_{DEH}	DE high level current	V_{IN} = 2.1 V			10	µA
$V_{DE(hyst)}$	DE hysteresis voltage		0.25			V
V_{DECL}	DE clamp voltage	I_{DE} = 1 mA	5.5		7	V
		I_{DE} = -1 mA		-0.7		

Table 8. Protections and diagnostic(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	Short circuit current	V_{CC} = 13 V	63.5	90	127	A
		5 V < V_{CC} < 24 V			127	
I_{limL}	Short circuit current during thermal cycling	V_{CC} = 13 V; $T_R < T_j < T_{TSD}$		25		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of status		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD}-T_R)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 2 A; V_{IN} = 0; L = 6 mH	V_{CC}-28	V_{CC}-31	V_{CC}-35	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 1.2 A; T_j = -40 °C...150 °C (see *Figure 8*)		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 9. Current sense (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 5 A; V_{SENSE} = 0.5 V; V_{DE} = 5 V; T_j = -40 °C...150 °C	7350	10700	14590	
dK_0/K_0(1)	Current sense ratio drift	I_{OUT} = 5 A; V_{SENSE} = 0.5 V; V_{DE} = 5 V; T_j = -40 °C to 150 °C	-12		12	%
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 10 A; V_{SENSE} = 4 V V_{DE} = 5 V T_j = -40 °C...150 °C T_j = 25 °C...150 °C	7490 8240	10500 10500	13930 12815	
dK_1/K_1(1)	Current sense ratio drift	I_{OUT} = 10 A; V_{SENSE} = 4 V; V_{DE} = 5 V; T_j = -40 °C to 150 °C	-12		12	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} =15 A; V_{SENSE} = 4 V V_{DE} = 5 V T_j = -40 °C...150 °C T_j = 25 °C...150 °C	8340 8680	10400 10400	12760 12070	
dK_2/K_2(1)	Current sense ratio drift	I_{OUT} = 15 A; V_{SENSE} = 4 V; V_{DE} = 5 V; T_j = -40°C to 150°C	-8		8	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 25 A; V_{SENSE} = 4 V V_{DE} = 5 V T_j = -40 °C...150 °C T_j = 25 °C...150 °C	8785 8965	10300 10300	11950 11545	
dK_3/K_3(1)	Current sense ratio drift	I_{OUT} = 25 A; V_{SENSE} = 4 V; V_{DE} = 5 V; T_j = -40 °C to 150 °C	-6		6	%
I_{SENSE0}	Analog sense leakage current	I_{OUT} = 0 A; V_{SENSE} = 0 V; V_{DE} = 0 V; V_{IN} = 0 V; T_j = -40 °C...150 °C	0		1	µA
		I_{OUT} = 0 A; V_{DE} = 5 V; V_{IN} = 5 V; V_{SENSE} = 0 V T_j = -40 °C...150 °C	0		2	
		I_{OUT} = 10 A; V_{DE} = 0 V; V_{SENSE} = 0 V; V_{IN} = 5 V;	0		1	
I_{OL}	Open-load on state current detection threshold	V_{IN} = 0 V, 8 V< V_{CC} < 18 V; I_{SENSE} = 5 µA	10		100	mA
V_{SENSE}	Max analog sense output voltage	I_{OUT} = 25 A; V_{DE} = 5 V; R_{SENSE} = 3.9 KΩ	5			V
V_{SENSEH}(2)	Analog sense output voltage in fault conditions	V_{CC} = 13 V; R_{SENSE} = 10 KΩ		8		V
I_{SENSEH}(1)	Analog sense output current in fault conditions	V_{CC} = 13 V; V_{SENSE} = 5 V		9		mA

Table 9. Current sense (8 V < V_{CC} < 18 V) (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{DSENSE1H}$	Delay response time from falling edge of DE pin	V_{SENSE} < 4 V, 5 A < I_{out} < 25 A I_{SENSE} = 90 % of $I_{SENSE\ max}$ (see *Figure 4*)		50	100	µs
$t_{DSENSE1L}$	Delay response time from rising edge of DE pin	V_{SENSE} < 4 V, 5 A < I_{out} < 25 A I_{SENSE} = 10 % of $I_{SENSE\ max}$ (see *Figure 4*)		5	20	µs
$t_{DSENSE2H}$	Delay response time from rising edge of INPUT pin	V_{SENSE} < 4 V, 5 A < I_{out} < 25 A I_{SENSE} = 90 % of $I_{SENSE\ max}$ (see *Figure 4*)		200	600	µs
$\Delta t_{DSENSE2H}$	Delay response time between rising edge of output current and rising edge of current sense	V_{SENSE} < 4 V, I_{SENSE} = 90 % of $I_{SENSEMAX}$, I_{OUT} = 90 % of I_{OUTMAX} I_{OUTMAX} = 25 A (see *Figure 7*)			200	µs
$t_{DSENSE2L}$	Delay response time from falling edge of INPUT pin	V_{SENSE} < 4 V, 5 A < I_{out} < 25 A I_{SENSE} = 10 % of $I_{SENSE\ max}$ (see *Figure 4*)		100	250	µs

1. Parameter guaranteed by design; it is not tested.
2. Fault conditions include: power limitation, overtemperature and open load OFF state detection.

Table 10. Open-load detection (8 V < V_{CC} < 18 V, V_{DE} = 5 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Open-load off state voltage detection threshold	V_{IN} = 0 V; V_{DE} = 5 V; See *Figure 5*	2	—	4	V
t_{DSTKON}	Output short circuit to V_{CC} detection delay at turn off	V_{DE} = 5 V; See *Figure 5*	180	—	1200	µs
$I_{L(off2)r}$	Off-state output current at V_{OUT} = 4V	V_{IN} = 0 V; V_{SENSE} = 0 V V_{DE}= 5 V; V_{OUT} rising from 0V to 4 V	-120	—	90	µA
$I_{L(off2)f}$	Off-state output current at V_{OUT} = 2V	V_{IN} = 0 V; V_{SENSE} = V_{SENSEH} V_{DE}= 5 V; V_{OUT} falling from V_{CC} to 2 V	-50	—	90	µA
td_vol	Delay response from output rising edge to V_{SENSE} rising edge in open load	V_{OUT} = 4 V; V_{IN} = 0 V V_{DE} = 5 V; V_{SENSE} = 90 % of V_{SENSEH}		—	20	µs
td_voh	Delay response from output falling edge to V_{SENSE} falling edge in open-load	V_{OUT} = 2 V; V_{IN} = 0 V V_{DE}= 5 V; V_{SENSE} = 10 % of V_{SENSEH}		—	20	µs

Figure 4. Current sense delay characteristics

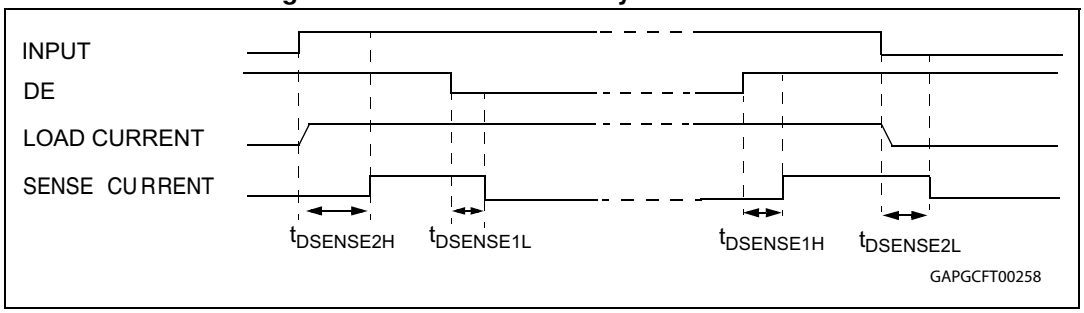


Figure 5. Open load Off-state delay timing

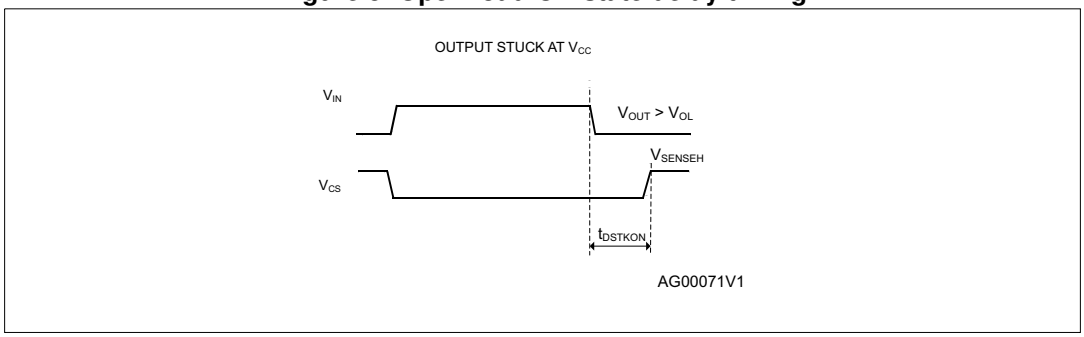


Figure 6. Switching characteristics

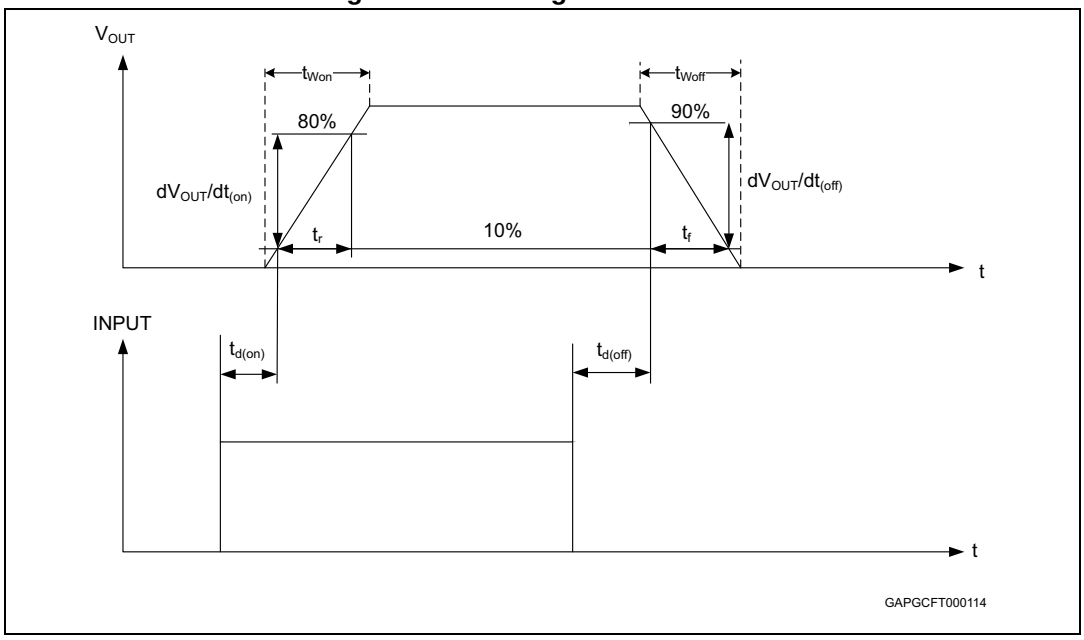


Figure 7. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

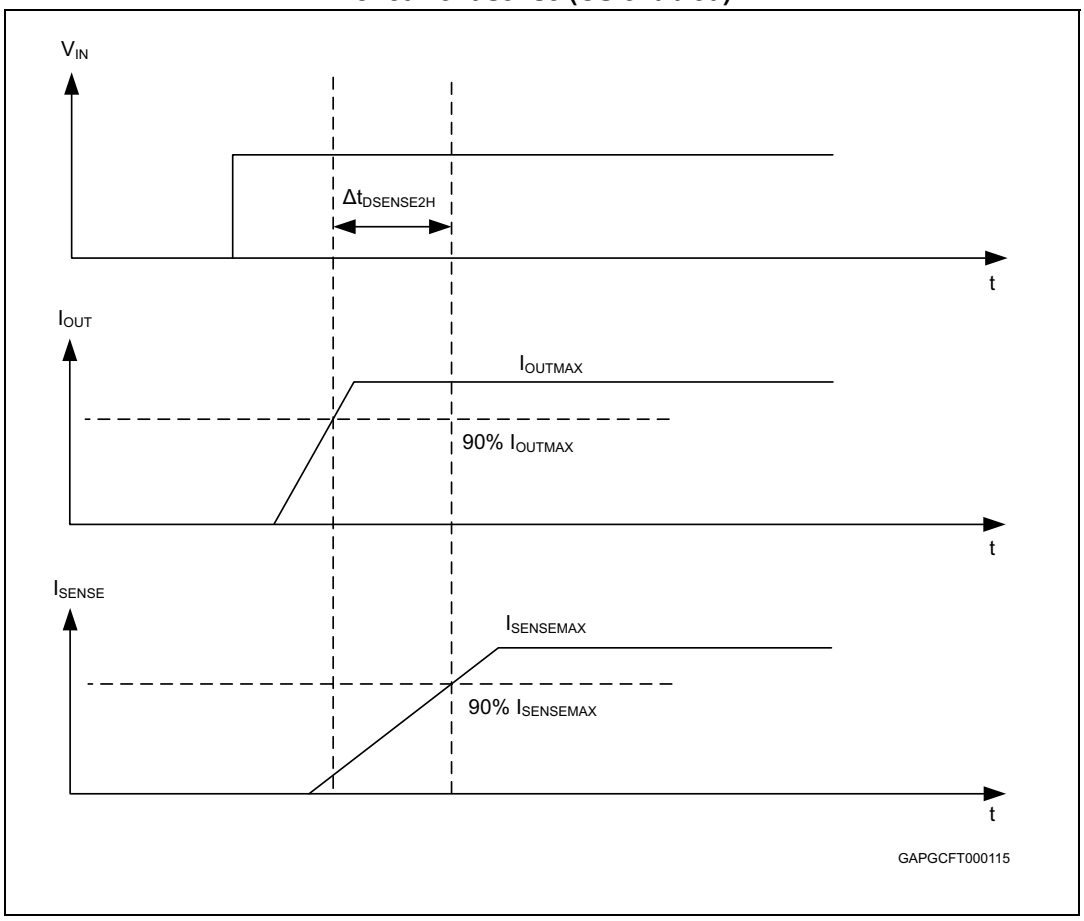


Figure 8. Output voltage drop limitation

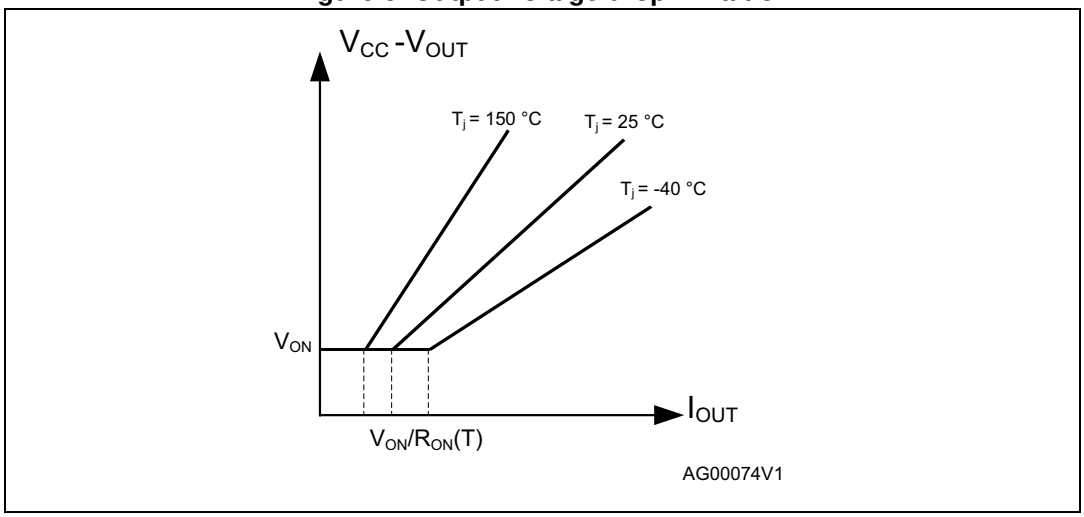
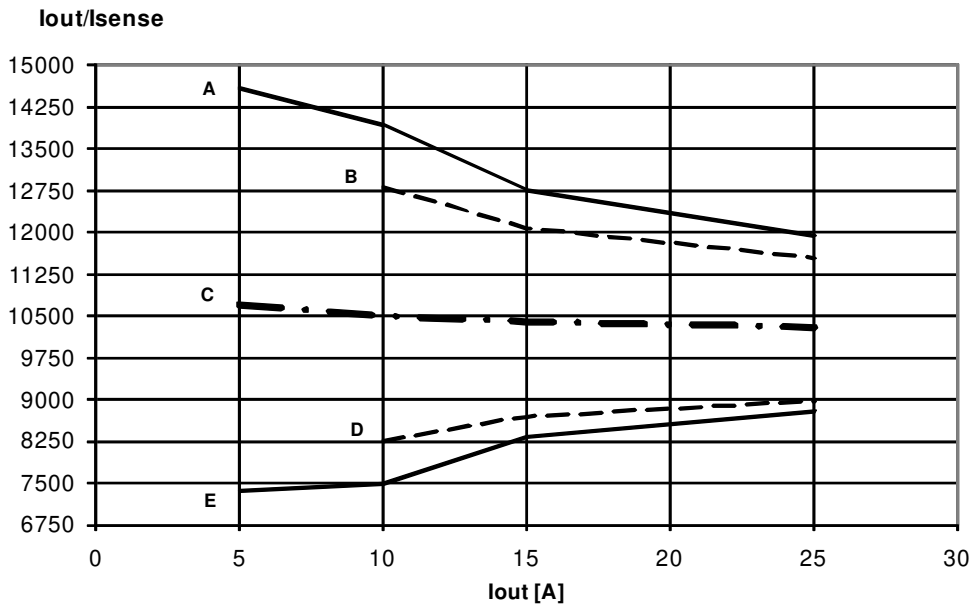
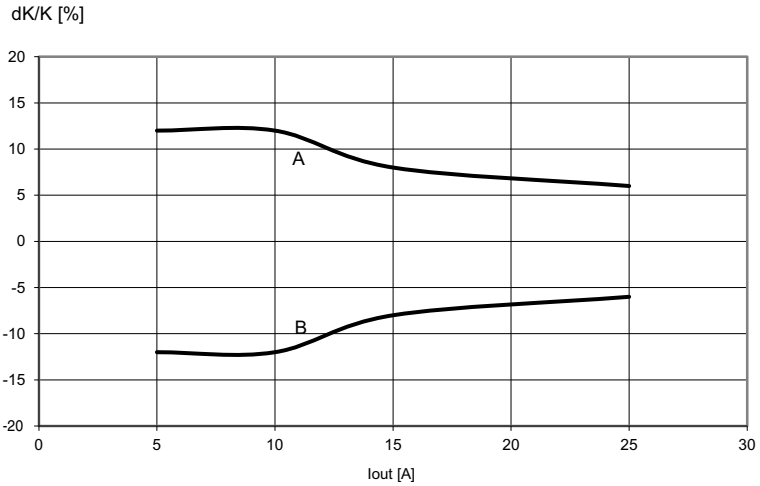


Figure 9. I_{OUT}/I_{SENSE} vs I_{OUT}



A: Max, Tj = -40 C to 150 C
B: Max, Tj = 25 C to 150 C
C: Typical, Tj = -40 C to 150 C
D: Min, Tj = 25 C to 150 C
E: Min, Tj = -40 C to 150 C

Figure 10. Maximum current sense ratio drift vs load current



A: Max, Tj = -40 C to 150 C
B: Min, Tj = -40 C to 150 C
GAPGCFT00770

Table 11. Truth table

Conditions	Enable	Input	Output	Sense (V_{DE} = 5 V)(1)
Normal operation	H H	L H	L H	0 Nominal
Overtemperature	H H	L H	L L	0 V_{SENSEH}
Undervoltage	H H	L H	L L	0 0
Overload	H H	H H	X (no power limitation) Cycling (power limitation)	Nominal V_{SENSEH}
Short circuit to GND (Power limitation)	H H	L H	L L	0 V_{SENSEH}
Open load OFF State (with external pull up)	H	L	H	V_{SENSEH}
Short circuit to V_{CC} (external pull up disconnected)	H H	L H	H H	V_{SENSEH} < Nominal
Negative output voltage clamp	H	L	L	0

1. If the V_{DE} is low, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Table 12. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test Pulse	Test levels(1)		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01 Ω
5b(2)	+65 V	+87 V	1 pulse			400 ms, 2 Ω

1. The above test levels must be considered referred to V_{CC} = 13.5V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.

Table 13. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) test pulse	Test level results(1)	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b (2) (3)	C	C

1. The above test levels must be considered referred to V_{CC} = 13.5V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.
3. Suppressed load dump (pulse 5b) is withstood with a minimum load connected as specified in *Table 3.: Absolute maximum ratings*.

Table 14. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the

2.4 Waveforms

Figure 11. Normal operation

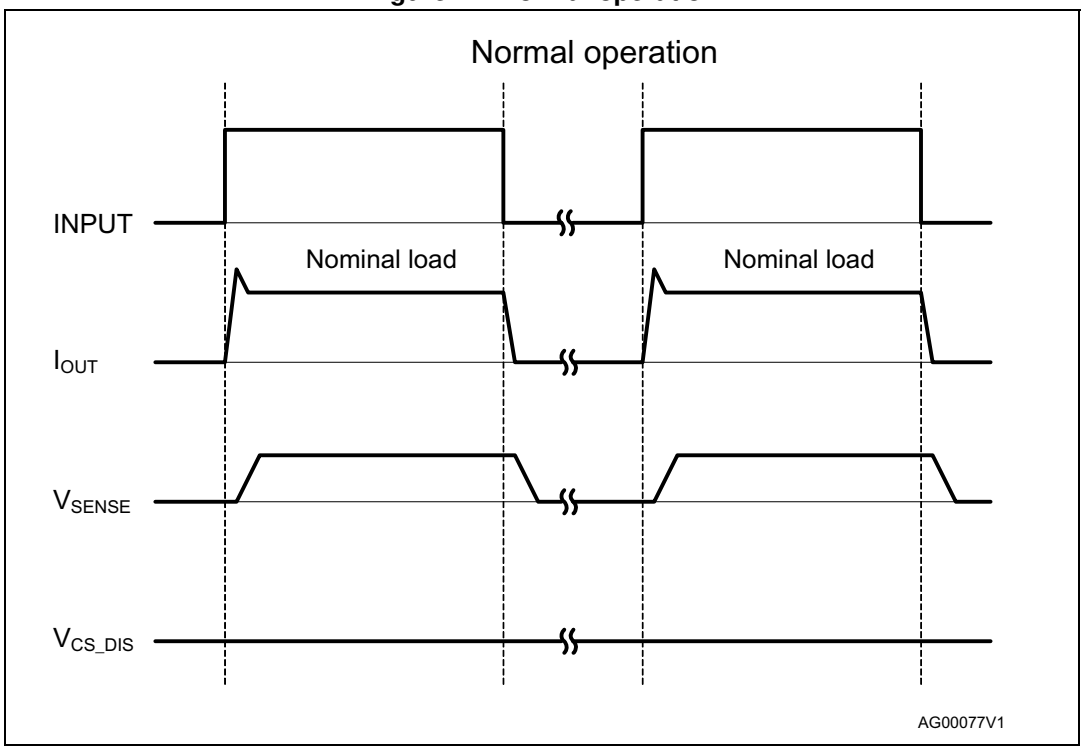


Figure 12. Overload or short to GND

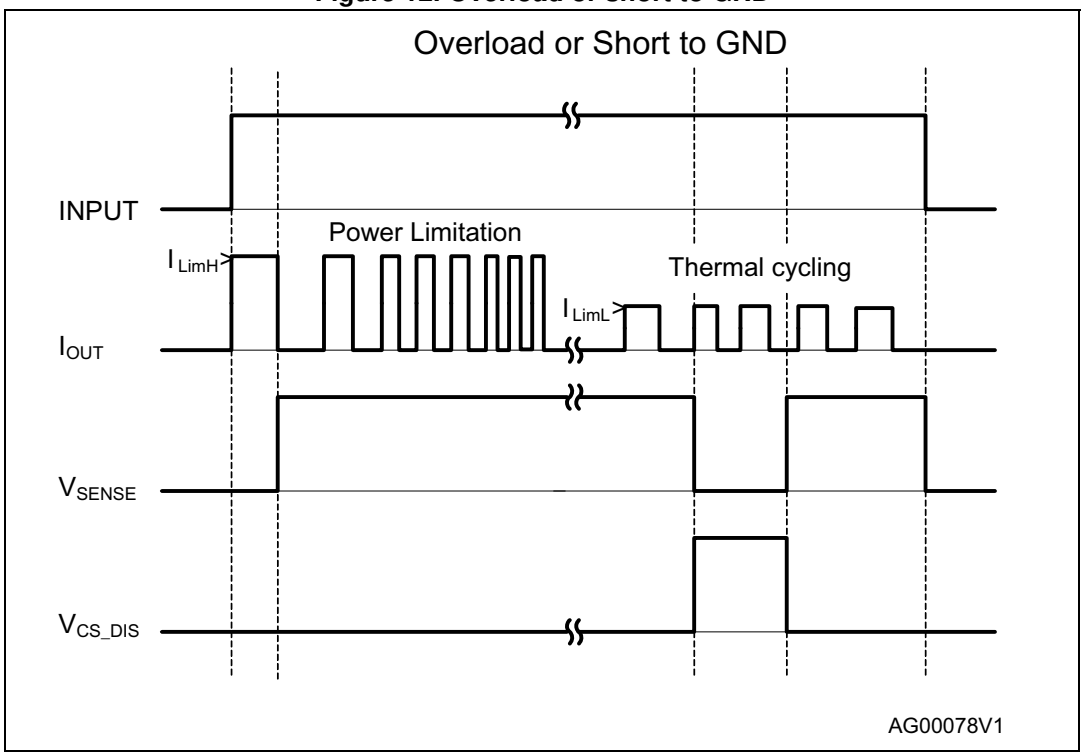


Figure 13. Intermittent overload

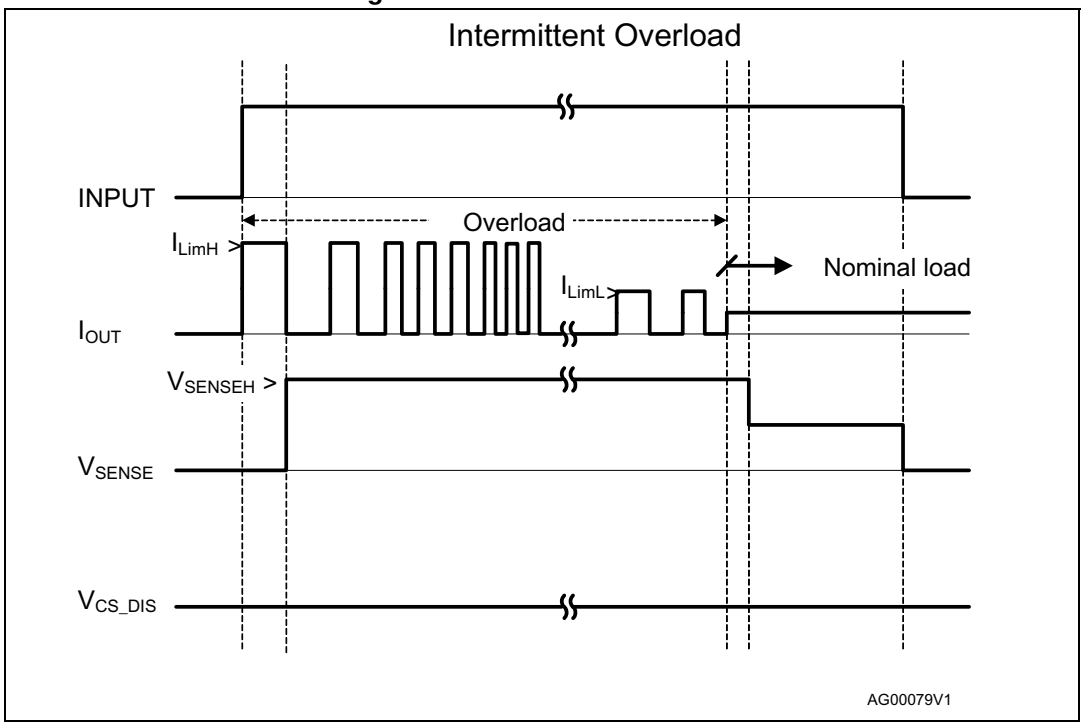


Figure 14. OFF-state open load with external circuitry

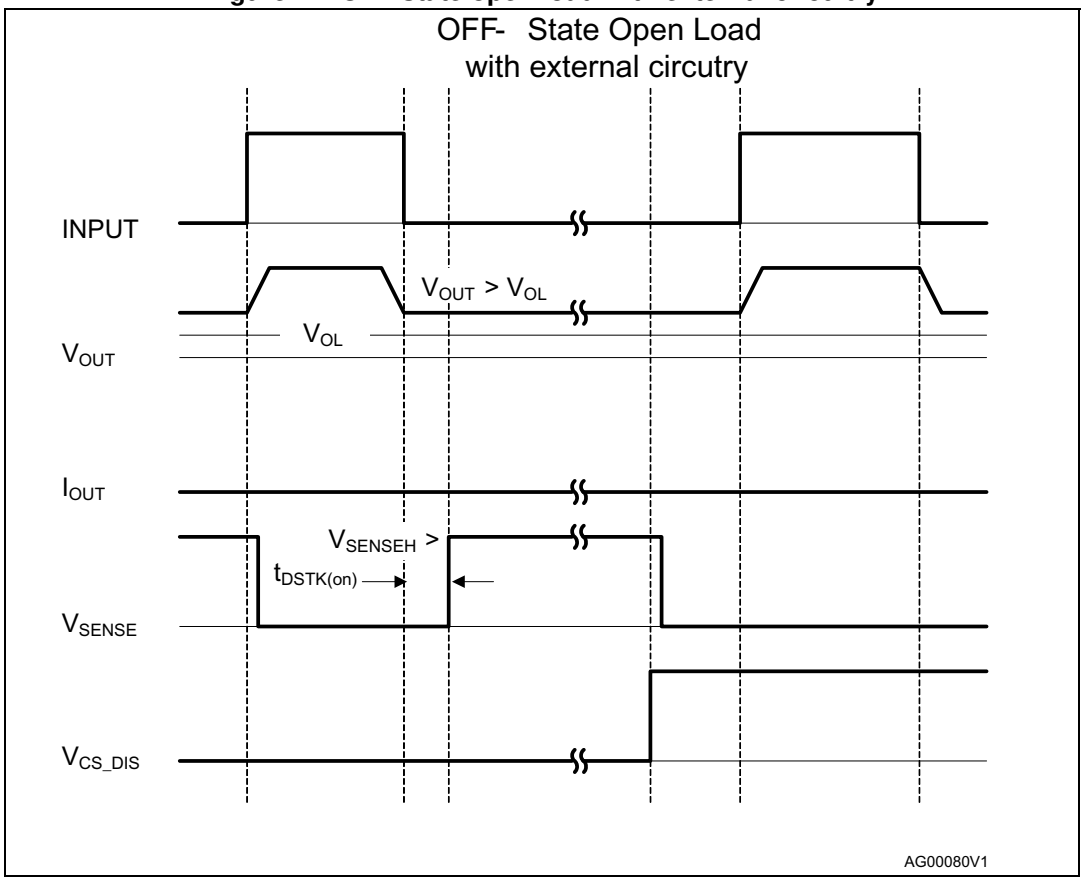


Figure 15. Short to V_{CC}

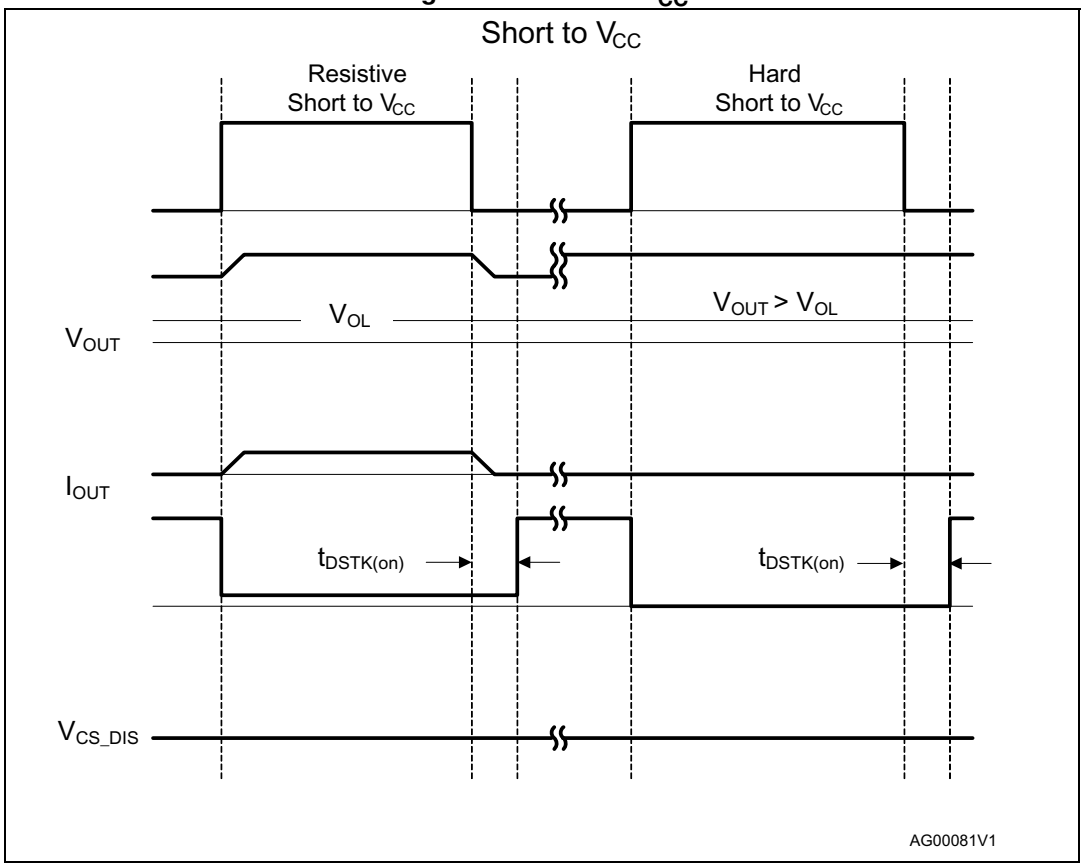
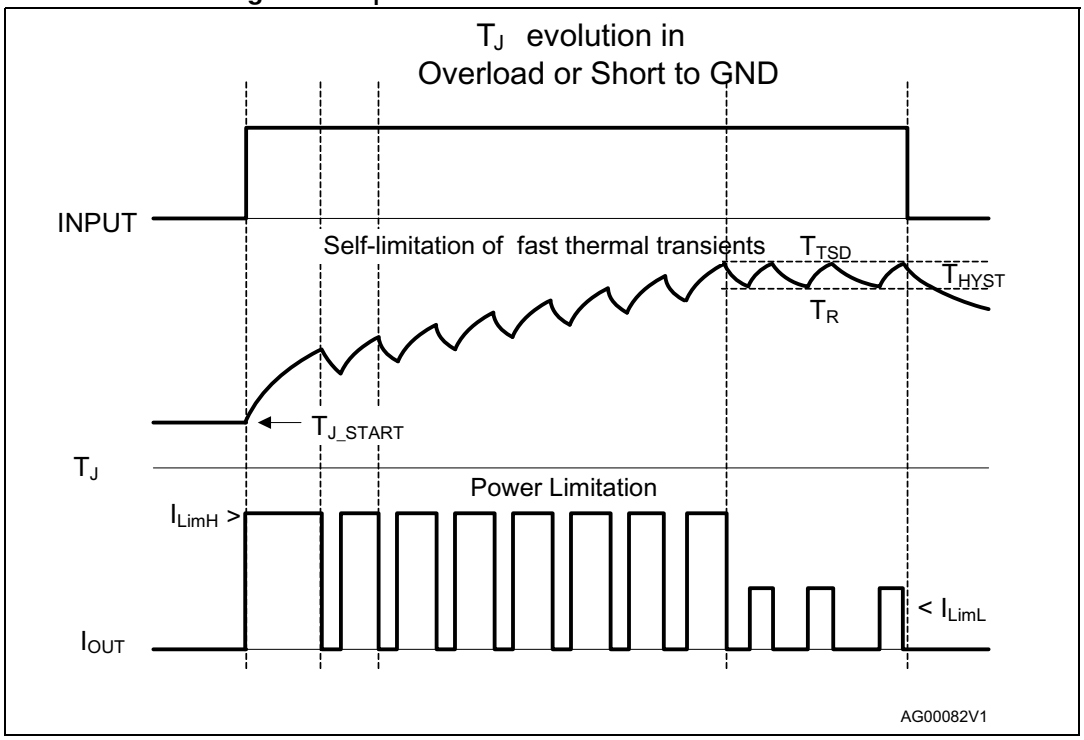


Figure 16. T_i evolution in overload or short to GND



2.5 Electrical characteristics curves

Figure 17. Off-state output current

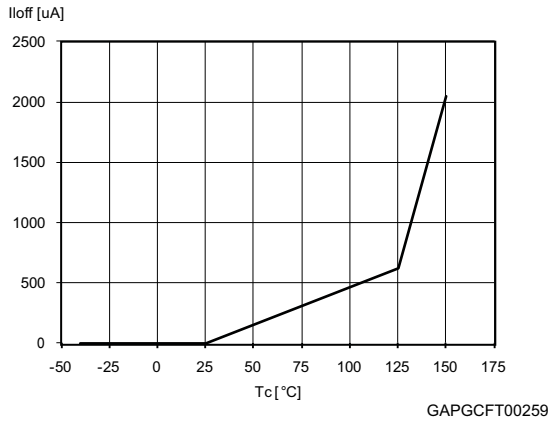


Figure 18. High level input current

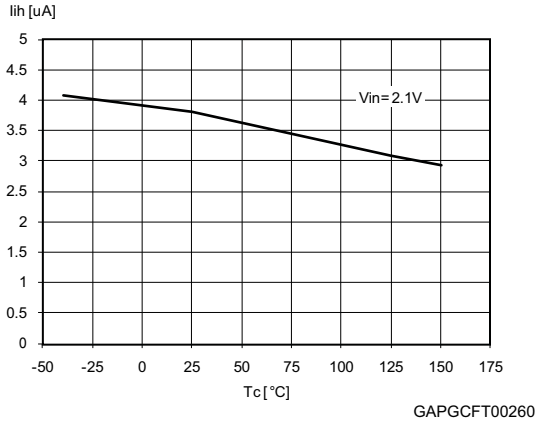


Figure 19. Input clamp voltage

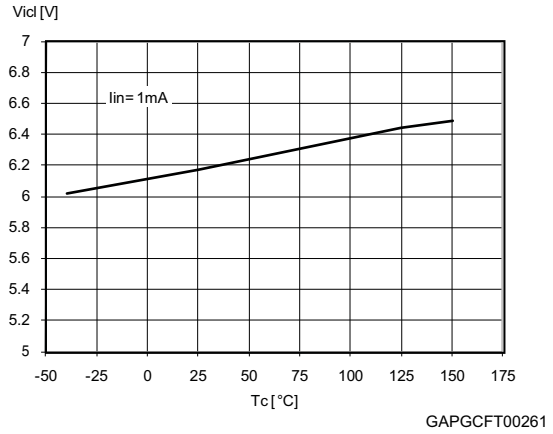


Figure 20. Input high level

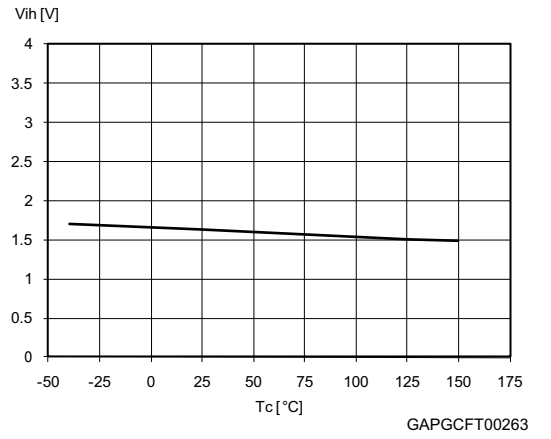


Figure 21. Input low level

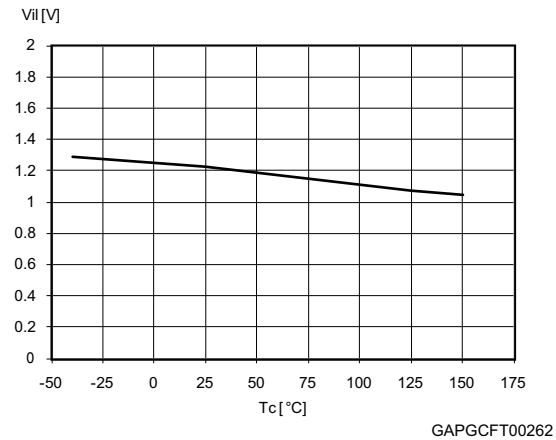


Figure 22. Input hysteresis voltage

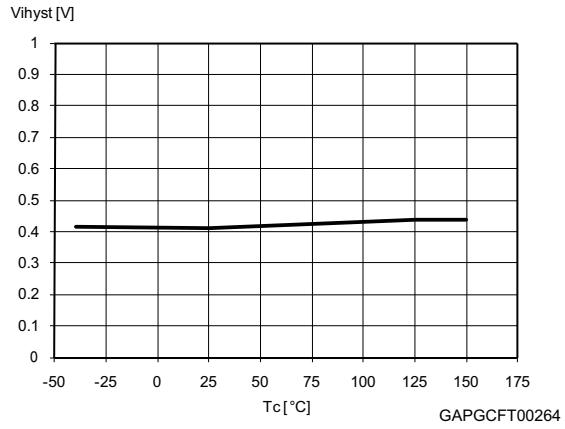


Figure 23. On-state resistance vs T_{case}

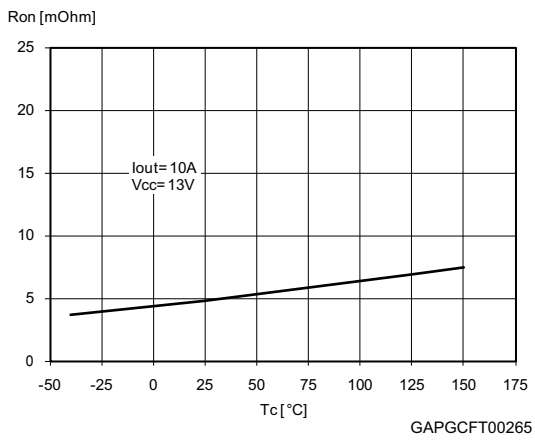


Figure 24. On state resistance vs V_{CC}

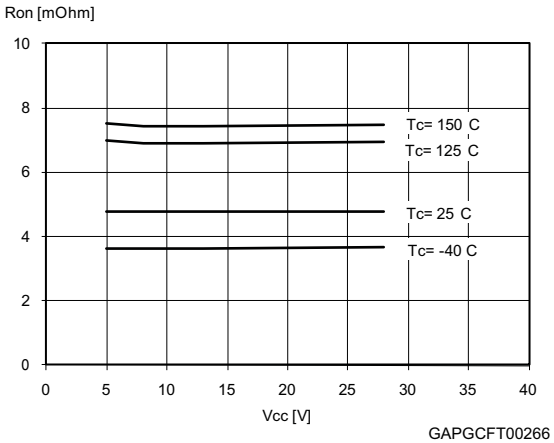


Figure 25. Undervoltage shutdown

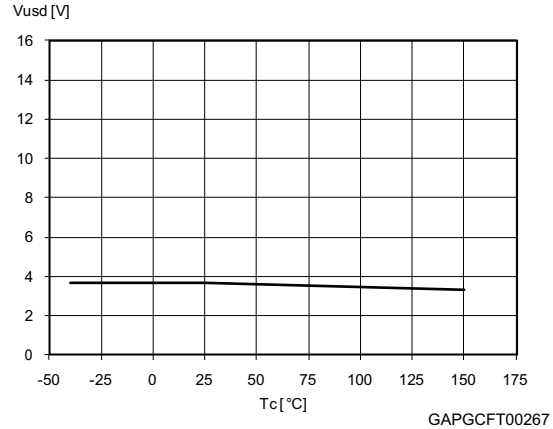


Figure 26. I_{LIMH} vs T_{case}

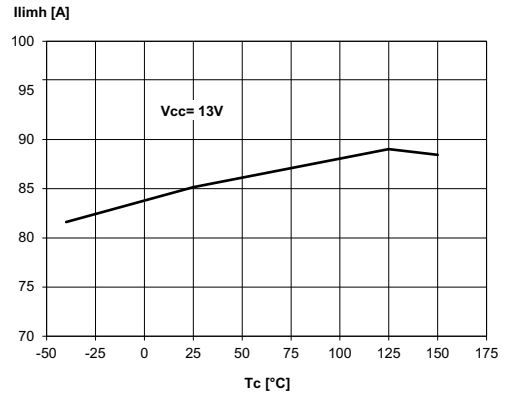


Figure 27. Turn-on voltage slope

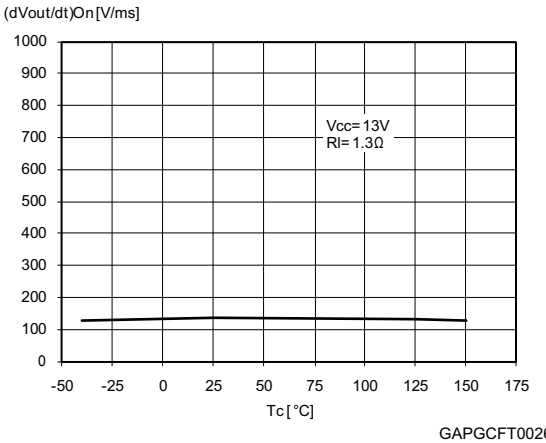


Figure 28. Turn-off voltage slope

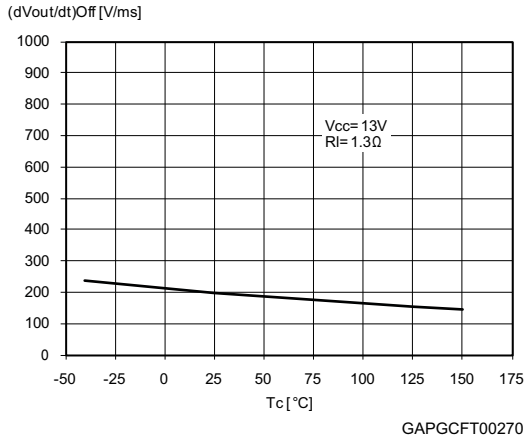


Figure 29. DE clamp voltage

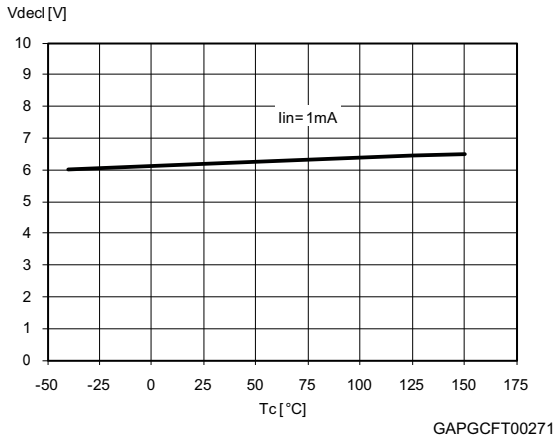


Figure 30. Low level DE voltage

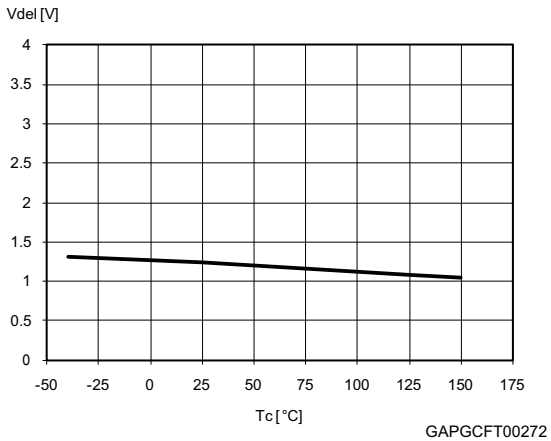
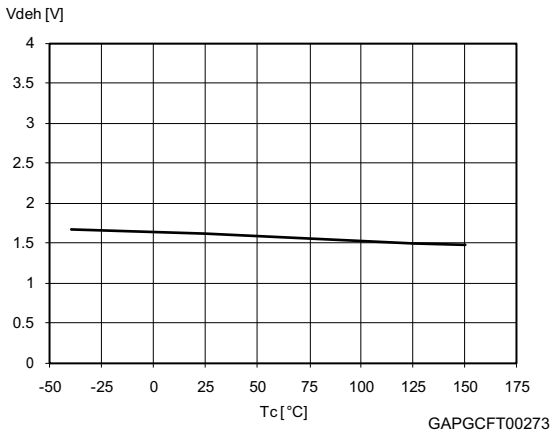
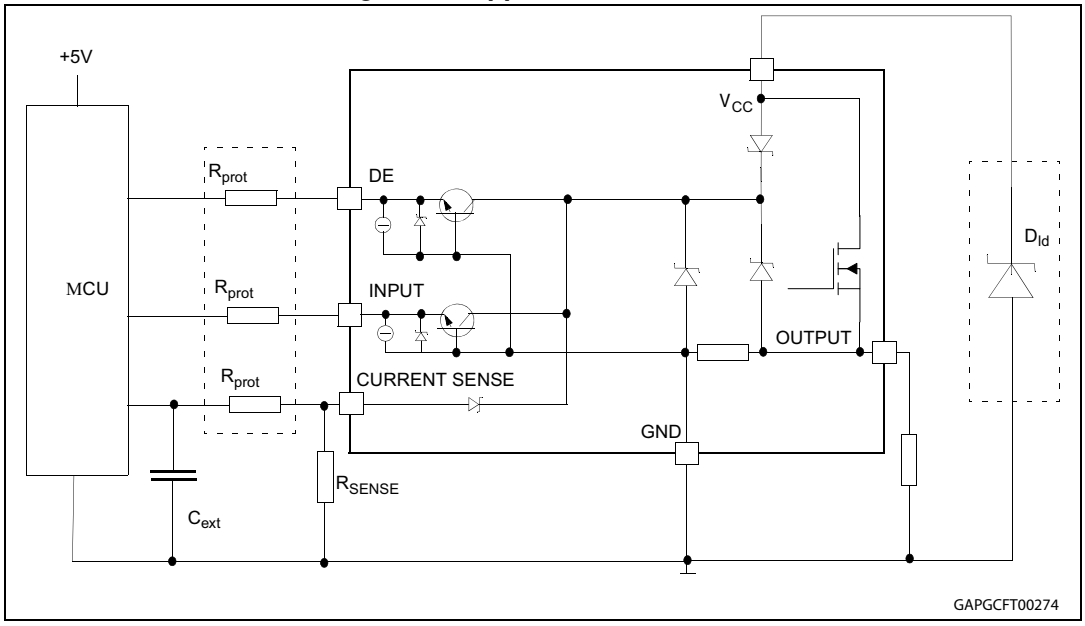


Figure 31. High level DE voltage



3 Application information

Figure 32. Application schematic



3.1 MCU I/Os protection

When negative transients are present on the V_{CC} line, the control pins are pulled negative to approximately -1.5V.

ST suggests the insertion of resistors (R_{prot}) in the lines to prevent the microcontroller I/O pins from latching up.

The values of these resistors provide a compromise between the leakage current of the microcontroller, the current required by the HSD I/Os (input levels compatibility) and the latch-up limit of the microcontroller I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}) / I_{IHmax}$

Calculation example:

For V_{CCpeak}= -1.5 V and $I_{latchup} \geq$ 20 mA; $V_{OH\mu C} \geq$ 4.5 V

75 Ω ≤ R_{prot} ≤ 240 kΩ.

Recommended values: R_{prot} = 10 kΩ, C_{EXT} = 10 nF

3.2 Load dump protection

D_{ld} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CCPK} max rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 Current sense and diagnostic

The current sense pin performs a double function (see *Figure 33: Current sense and diagnostics*):

- **Current mirror of the load current in normal operation,** delivering a current proportional to the load one according to a known ratio $\mathbf{K_X}$.
  The current I_{SENSE} can be easily converted to a voltage V_{SENSE} by means of an external resistor R_{SENSE}. Linearity between I_{OUT} and V_{SENSE} is ensured up to 5V minimum (see parameter V_{SENSE} in *Table 9: Current sense (8 V < V_{CC} < 18 V)*). The current sense accuracy depends on the output current (refer to current sense electrical characteristics *Table 9: Current sense (8 V < V_{CC} < 18 V)*).
- **Diagnostic flag in fault conditions**, delivering a fixed voltage V_{SENSEH} up to a maximum current I_{SENSEH} in case of the following fault conditions (refer to *Truth table*):
  - Power limitation activation
  - Overtemperature
  - Short to V_{CC} in OFF-state
  - Open-load in OFF-state with additional external components.

A logic level low on DE pin sets at the same time all the current sense pins of the device in a high impedance state, thus disabling the current monitoring and diagnostic detection. This feature allows multiplexing of the microcontroller analog inputs by sharing of sense resistance and ADC line among different devices.

Figure 33. Current sense and diagnostics