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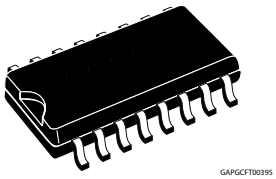
VN5MB02-E

Smart Power driver for motorbike blinker

Datasheet - production data



SO-16 narrow

Features

Type	$R_{DS(on)}$	I_{lsd} (Typ)	V_{CC}
VN5MB02-E	0.08 Ω	30 A	41 V

- Complete direction indicator in a SMD package
- Double frequency flashing in low load conditions
- High accuracy in setting operating frequency and low load detection
- Maximum current protection with latch
- Reverse battery protected
- Cycle by cycle thermal limitation
- Suitable for load configuration up to 2 x 10 W + 3.4 W
- Open-load detection for FAST lane change (patent pending)

Description

The VN5MB02-E is a Smart Power driver for motorbike blinker; it is connected between the battery positive terminal (V_{CC} pin) and a mechanical switch to the right or left side. As soon as the series switch connects the OUT pin to the bulbs, the device begins to turn on/off with a 50% duty cycle.

External low voltage capacitors are needed for supplying the device (C_{EXT}), for stabilizing the internal voltage regulator output (C_{REG}) and for setting the oscillating frequency (C_{FREQ}).

When a low load is detected, output current lower than I_{df}, flashing frequency is automatically doubled.

The internal current shutdown latches the VN5MB02-E when a heavy overload occurs; thermal limitation reduces the stress on the device if the junction temperature raises (for instance when a soft over current event, not triggering the current latch protection, happens). If the overload condition lasts more than a time t_{fault}, the VN5MB02-E is latched.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
SO-16 narrow	VN5MB02-E	VN5MB02TR-E

This is information on a product in full production. www.st.com

Contents

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1 Block diagram and pin descriptions

Figure 1. Block diagram

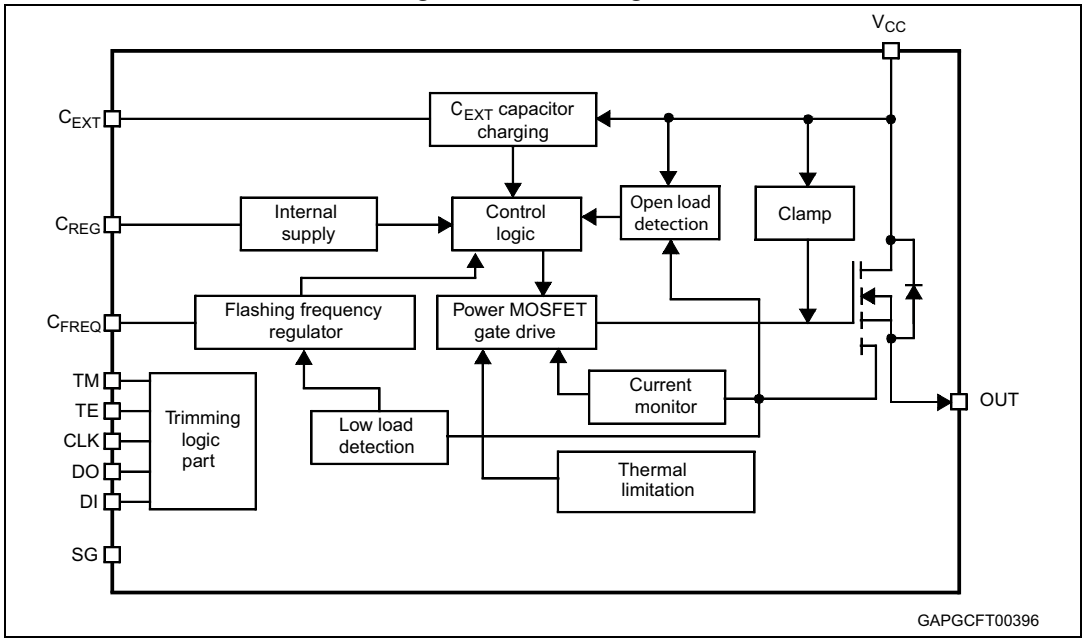


Figure 2. Configuration diagram (top view)

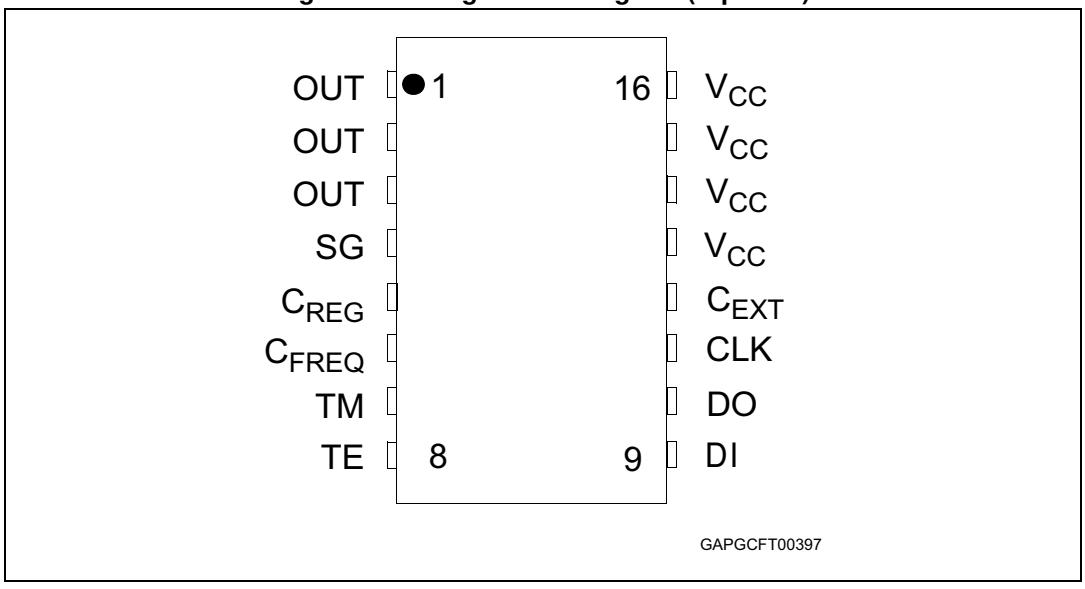
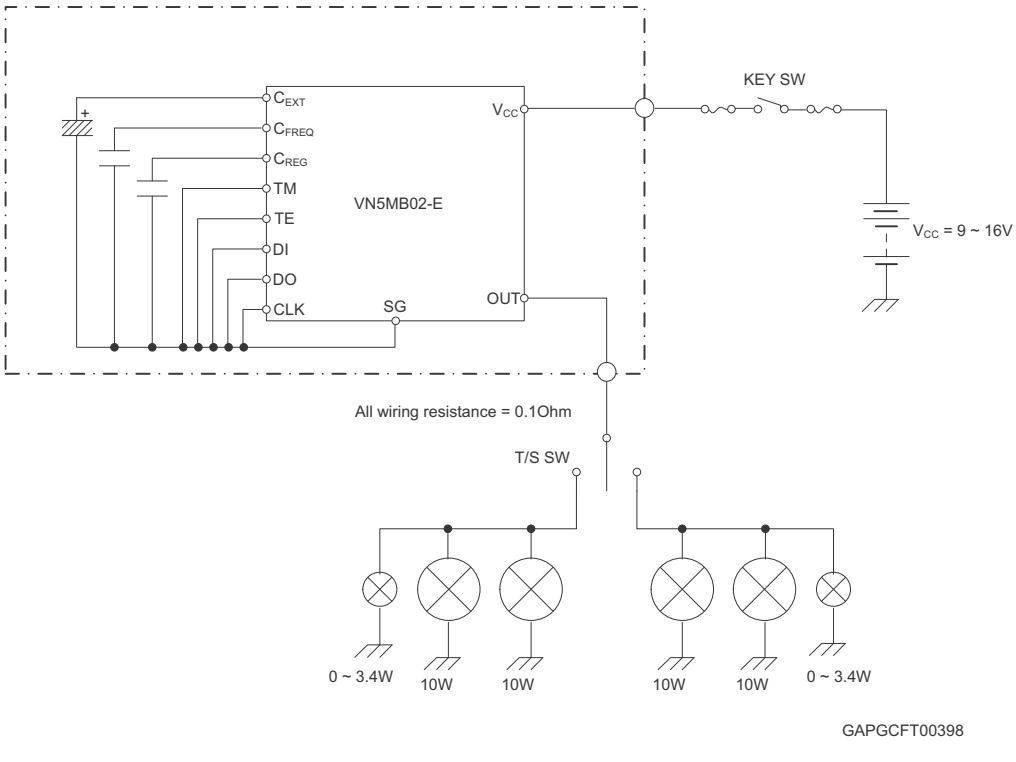


Table 2. Pin functions

Name	Pin number	Function
OUT	1, 2, 3	Power output
SG	4	Control stage signal ground.
C_{REG}	5	Internal voltage regulator output, it needs a stability capacitor C > 220 nF
C_{FREQ}	6	Needed for generating the internal sawtooth signal It is connected to an external capacitor C = 1.5 nF
TM	7	Test mode pin. Must be connected to SG.
TE	8	Test mode enable. Must be connected to SG.
DI	9	SPI data input. Must be connected to SG.
DO	10	SPI data output. Must be connected to SG.
CLK	11	SPI clock. Must be connected to SG.
C_{EXT}	12	Device supply, connected to an electrolytic capacitor C > 220 µF
V_{CC}	13, 14, 15, 16	Battery connection

Figure 3. Application diagram



2 Electrical specifications

2.1 Absolute maximum rating

Stressing the device above the rating listed in *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	37	V
V_{CCPK}	Transient supply voltage (t < 400 ms, T_j = 25°C)	41	V
C_{EXT}	C_{EXT} voltage	-0.3 to 20	V
C_{REG}	C_{REG} voltage	-0.3 to 3.6	V
C_{FREQ}	C_{FREQ} voltage	-0.3 to 3.6	V
TM	Test mode voltage	-0.3 to 3.6	V
I_D	Maximum DC drain current	Internally limited	A
$-I_D$	Reverse DC output current	5	A
V_{ESD}	Electrostatic discharge (human body model: R = 1.5 KΩ; C = 100 pF) – OUTPUT – V_{CC} – C_{EXT} – C_{FREQ} – C_{REG} – TM	 4000 4000 2000 2000 2000 2000	 V V V V V V
V_{esd}	Electrostatic discharge CDM	750	V
T_j	Junction operating temperature	Internally limited	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (max)	See *Figure 14*	°C/W

2.3 Electrical characteristics

Values specified in this section are for 9 V < V_{CC} < 16 V; -40°C < T_j < 150°C, unless otherwise specified.

Table 5. Features

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{clamp}	V_{DS} clamp voltage	I_{OUT} = 2 A	41			V
R_{ON}	On-state resistance	I_{OUT} = 2 A; T_j = 25°C			80	mΩ
		I_{OUT} = 2 A; T_j = 150°C			160	mΩ
I_{freq}	Oscillating frequency current		-3%	10	3%	µA
Duty	Duty cycle		47		53	%
K_{freq}	Fault frequency vs normal frequency ratio		2.15		2.3	
V_{ch} - V_{cl}	Internal sawtooth delta limit		-2%	1.1	2%	V
C_{ext_clamp}	Cext voltage charging limit	V_{CC} = 20 V; -40 °C < T_j < 85°C	14	16	18	V
del_{ON}	Delay at first ON	V_{CC} = 9 V; C_{EXT} = 220 µF; -40 °C < T_j < 85°C		85	100	ms
$t_{firstON}$	Minimum first t_{ON}	V_{CC} = 13.5 V; C_{EXT} = 220 µF; -40°C < T_j < 85°C	200			ms
$I_{\_cext\_Charge}$	C_{ext} voltage charging current	V_{CC} = 9 V; V_{CEXT} = 0 V; -40°C < T_j < 85°C	50	80		mA
I_{s_ON}	Current consumption in ON state	V_{CC} = 9 V; -40°C < T_j < 85°C		2	2.1	mA
$I_{\_OL}$	Max open load current	-40°C < T_j < 85°C		250	740	mA
$V_{\_OL}$	Max open load voltage	-40°C < T_j < 85°C		5.7	6.5	V

Table 6. Protection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{lsd}	Current shutdown	-40°C < T_j < 25°C	27	30		A
		T_j = 85°C	25			A
T_{jsh}	Overtemperature shutdown			175		°C
ΔT_h	Temperature hysteresis			14		°C
t_{fault}	Fault time			10		ms
I_{df1_9V}	Double frequency flashing threshold	V_{CC} = 9 V; -40°C < T_j < 85°C	0.911	0.987	1.063	A
I_{df1_13V}	Double frequency flashing threshold	V_{CC} = 13 V; -40°C < T_j < 85°C	1.112	1.210	1.308	A
I_{df1_16V}	Double frequency flashing threshold	V_{CC} = 16 V; -40°C < T_j < 85°C	1.245	1.358	1.470	A

Table 7. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test pulse	Test levels(1)		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100 V	-150 V	1 h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75 V	+100 V	1 h	90 ms	100 ms	0.1 µs, 50 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01 Ω
5b(2)	+65 V	+87 V	1 pulse			400 ms, 2 Ω

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b
2. Valid in case of external load dump clamp: 40V maximum referred to OUT.

Table 8. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) Test pulse	Test level results(1)	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b(2)	C	C

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b
2. Valid in case of external load dump clamp: 40 V maximum referred to OUT.

Table 9. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Waveforms

Figure 4. First turn-on

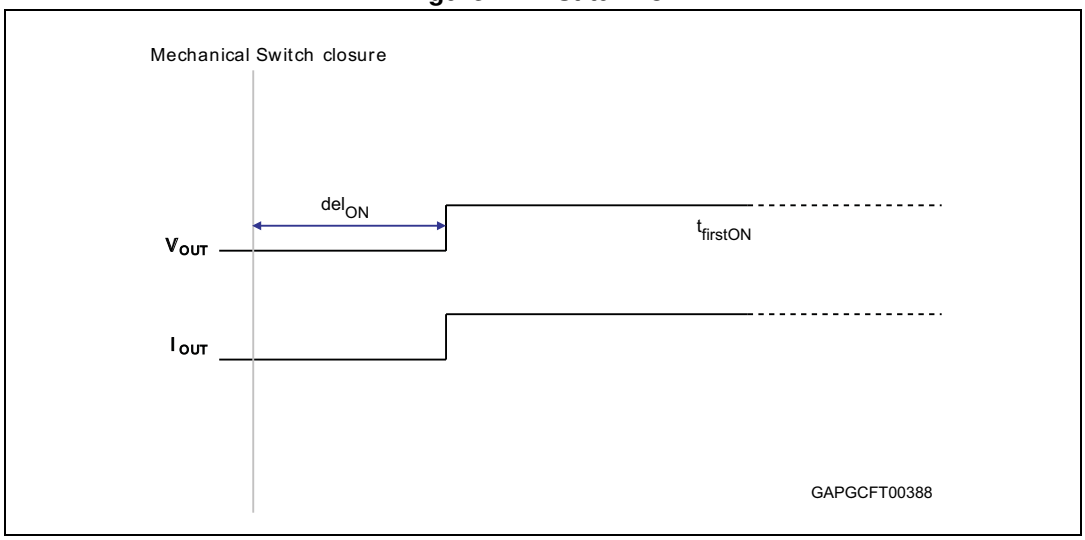


Figure 5. Normal operation

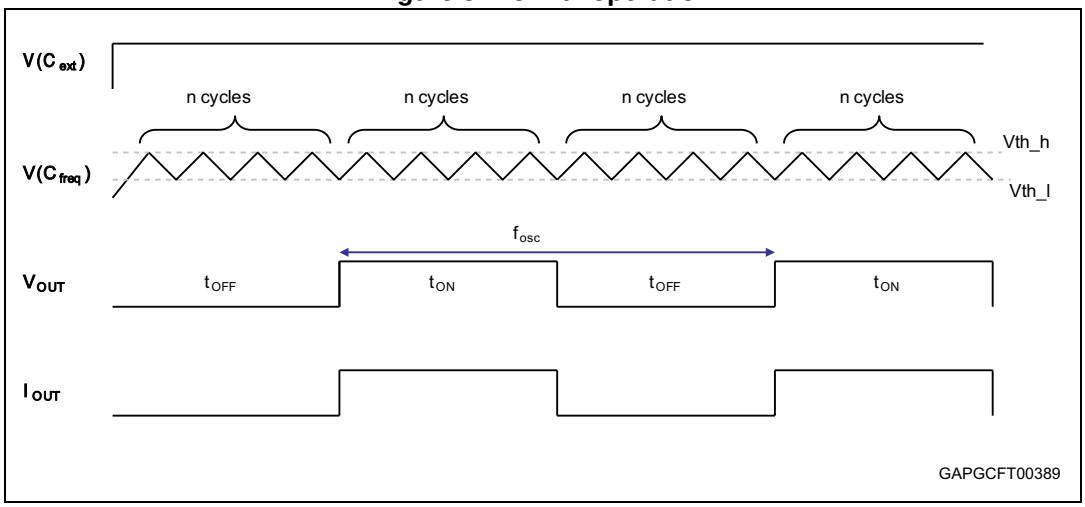


Figure 6. Low load condition

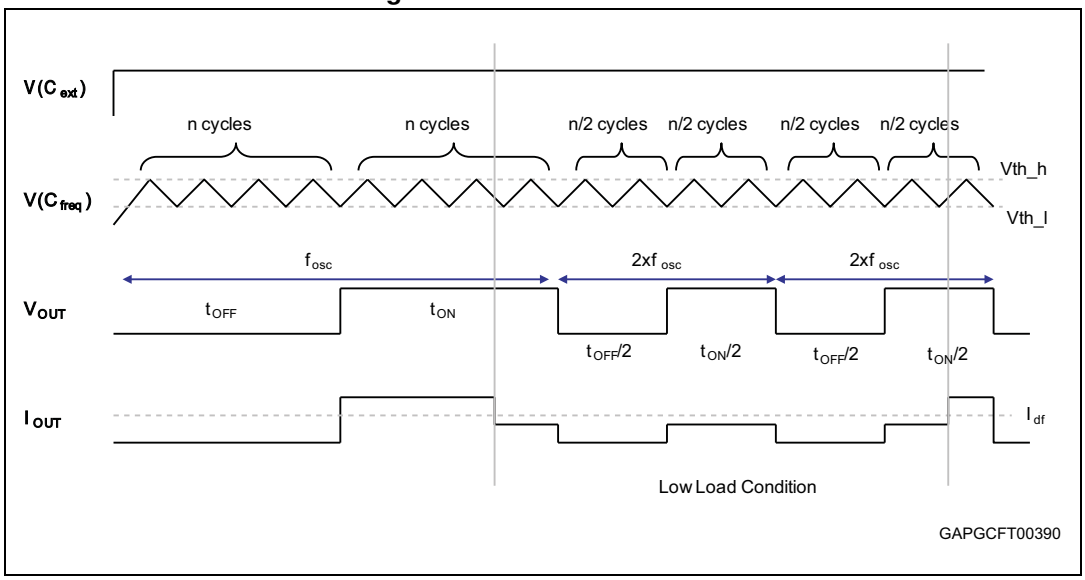


Figure 7. I_{SD} shutdown

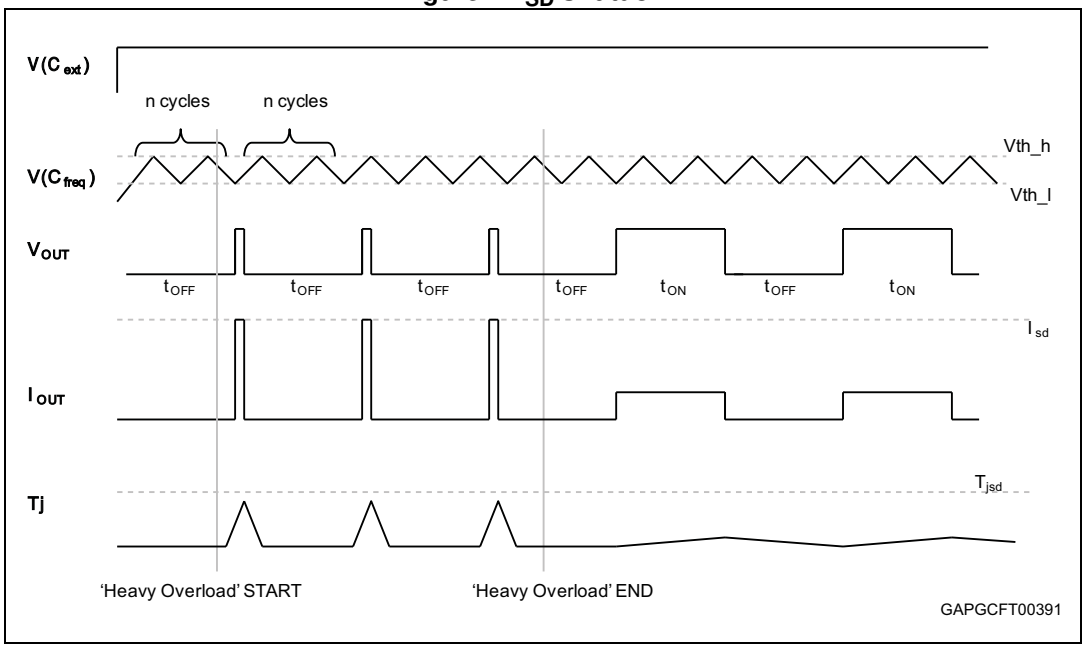


Figure 8. Thermal limitation event duration > t_{FAULT}

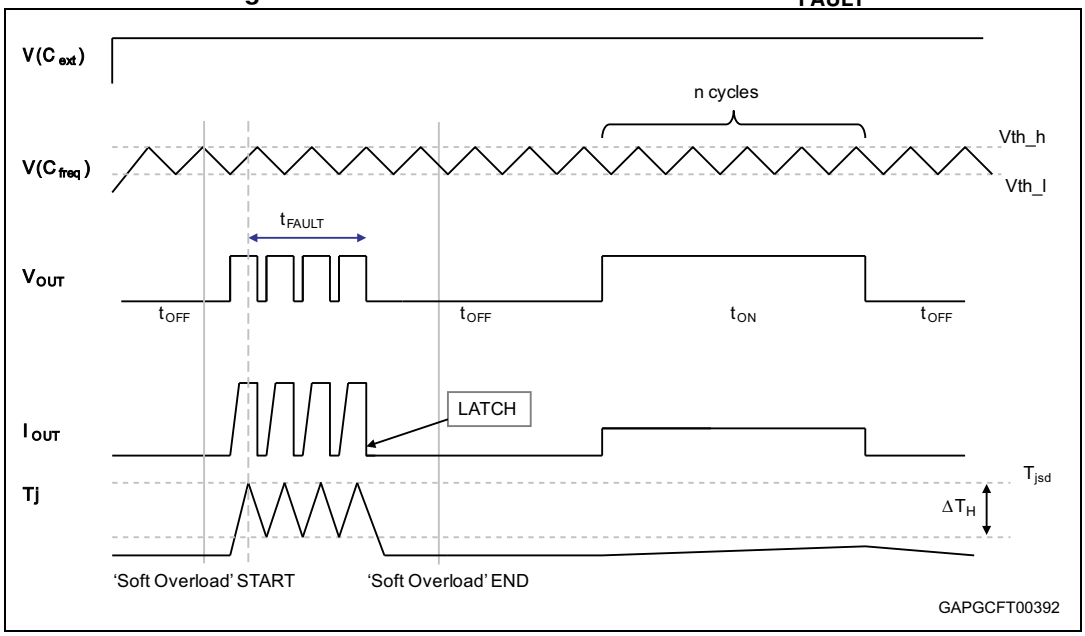


Figure 9. Thermal limitation with duration < t_{FAULT}

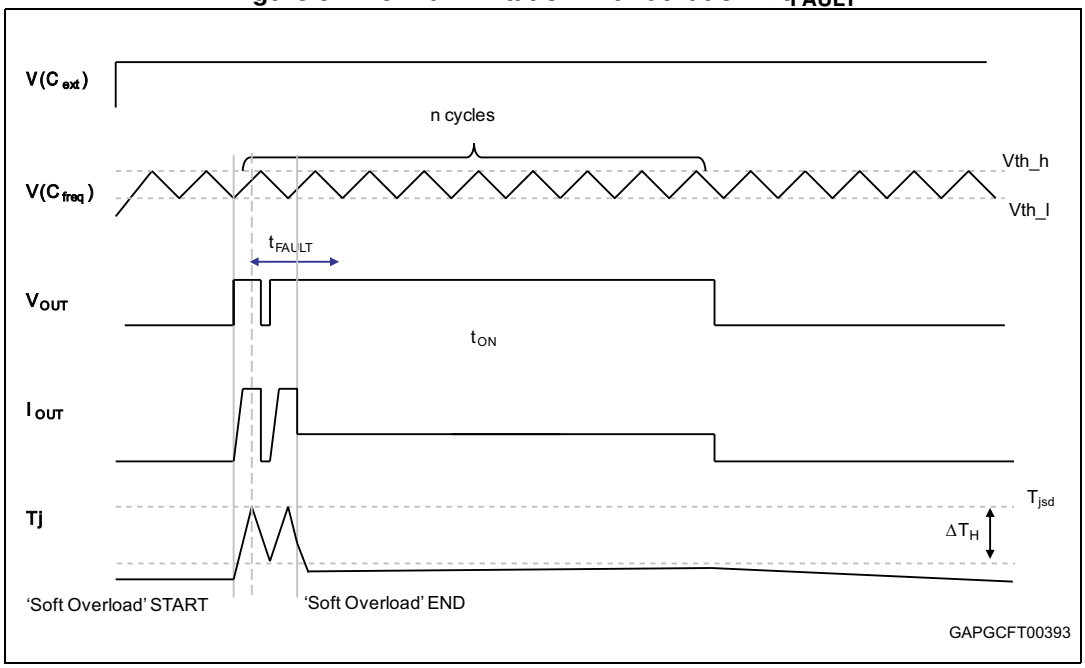


Figure 10. Open-load detection for FAST lane change (OFF)

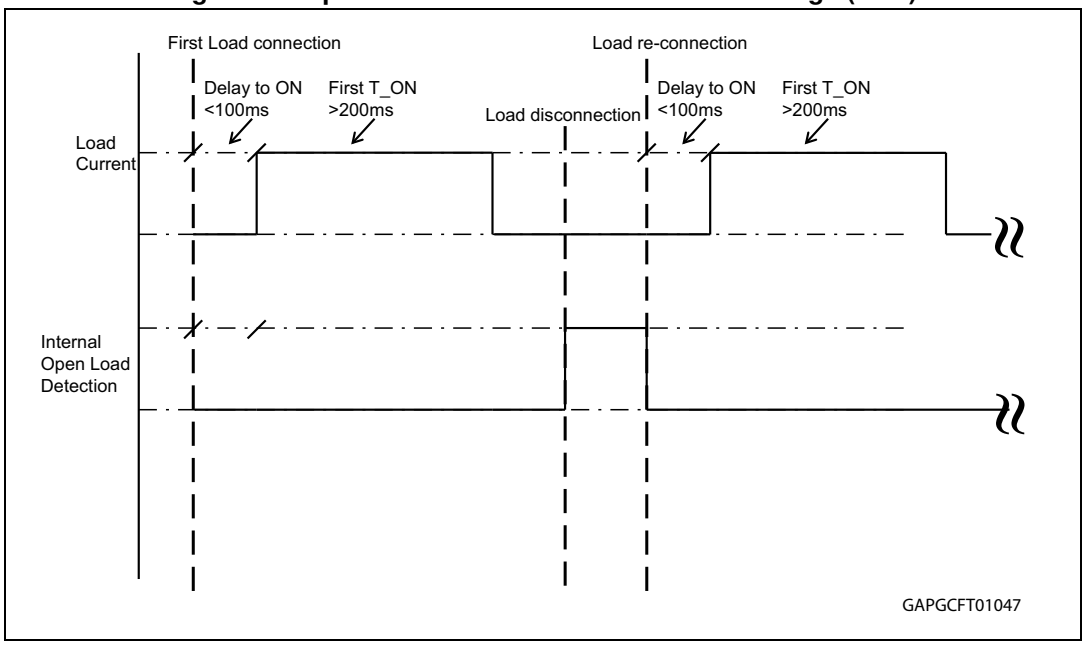
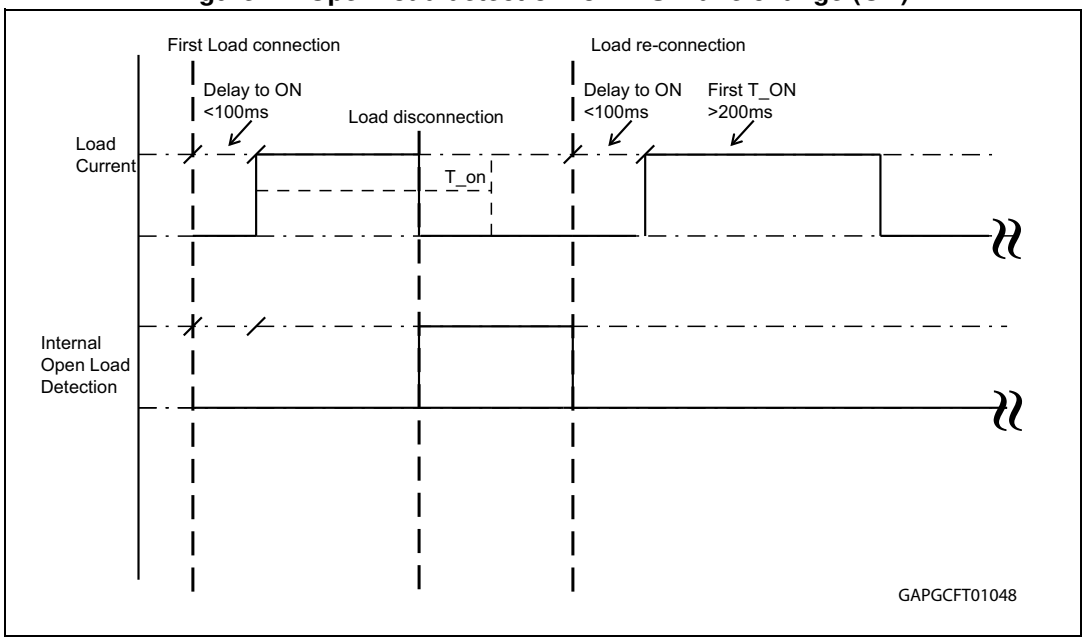


Figure 11. Open-load detection for FAST lane change (ON)



3 Functional description

3.1 Normal operation

When a nominal load is connected to the OUT pin, the device oscillates by charging the C_{EXT} capacitor up to the threshold voltage V_{ch} quickly, and then slowly discharging C_{EXT} to the threshold voltage V_{cl} by a constant current I_{CEXT}.

The self oscillating frequency of the device is determined by the relation:

$$f_{OSC} = \frac{I_{freq}}{4 \times n \times C_{freq} \times (V_{ch} - V_{cl})}$$

n is the internal digital counter (equal to 1066).

3.2 Low load condition

If the load current is lower than I_{df}, the device will detect the low load at the end of the ON phase, and will double the oscillating frequency.

$$F(fault) = f_{OSC} \times Kfreq$$

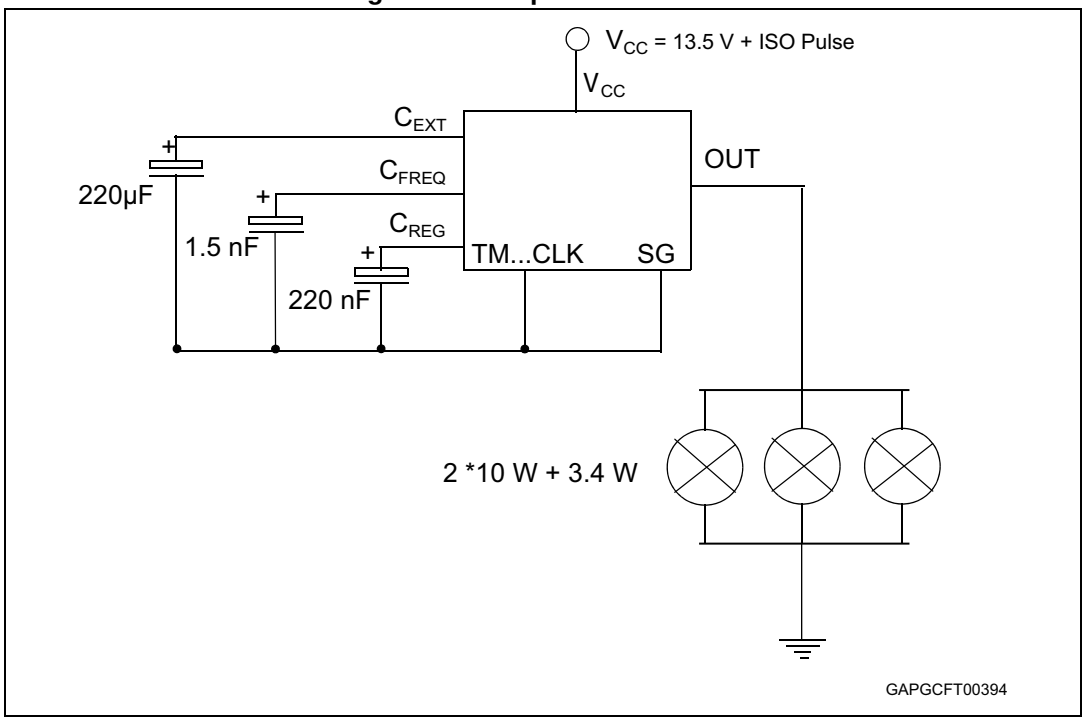
3.3 Current protection and thermal limitation

The internal current shutdown latches the VN5MB02-E when a heavy overload occurs and, if the overload even is removed, the device may be turned on at the following on time.

The thermal limitation reduces the stress on the device if the junction temperature rises (for instance when a soft over current event, not triggering the current latch protection, happens).

If the overload condition lasts more than a time t_{fault}, the VN5MB02-E is latched; when the overload condition is not anymore present, device can be turned on at the following on time.

Figure 12. ISO pulse test circuit

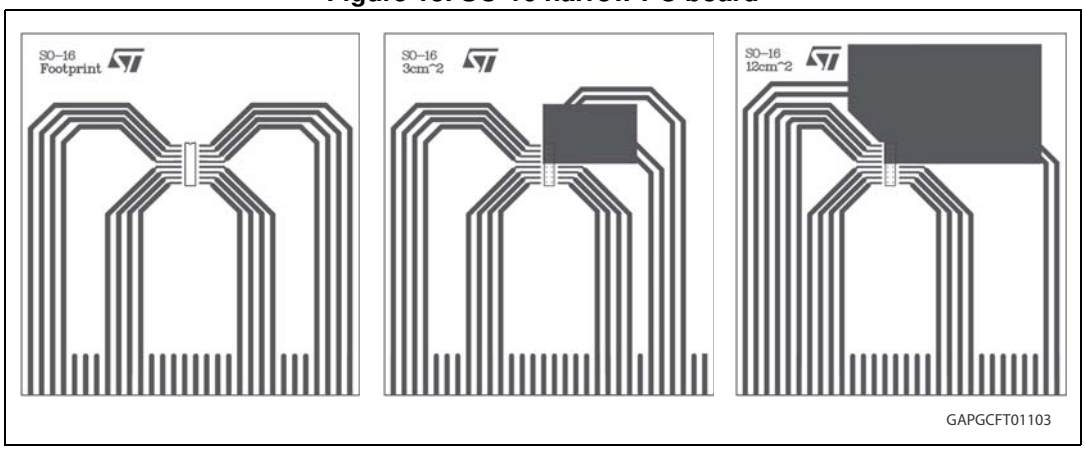


1. For pulse 5b an external protection is needed: see *Table 7*.

4 Package and PCB thermal data

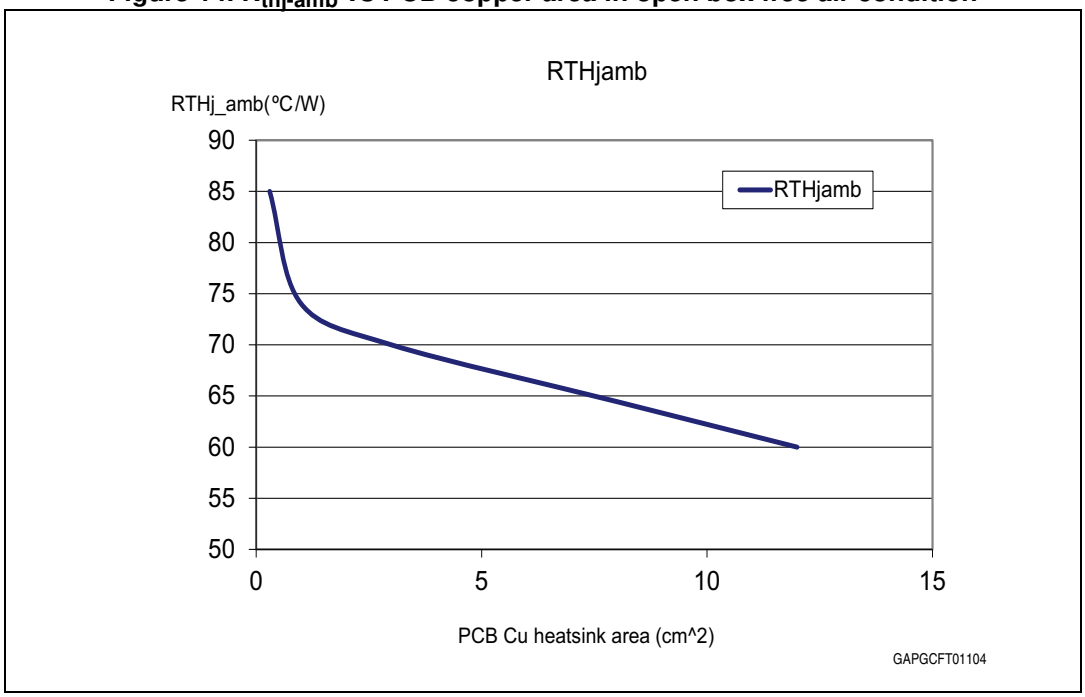
4.1 SO-16 narrow thermal data

Figure 13. SO-16 narrow PC board



1. Board finish thickness 1.6 mm +/- 10%; Board double layer; Board dimension 129 mm x 60 mm; Board Material FR4; Cu thickness 0.070 mm (front and back side); Thermal vias separation 1.2 mm; Thermal via diameter 0.3 mm +/- 0.08 mm; Cu thickness on vias 0.025 mm

Figure 14. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition



5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

Figure 15. SO-16 narrow package dimensions

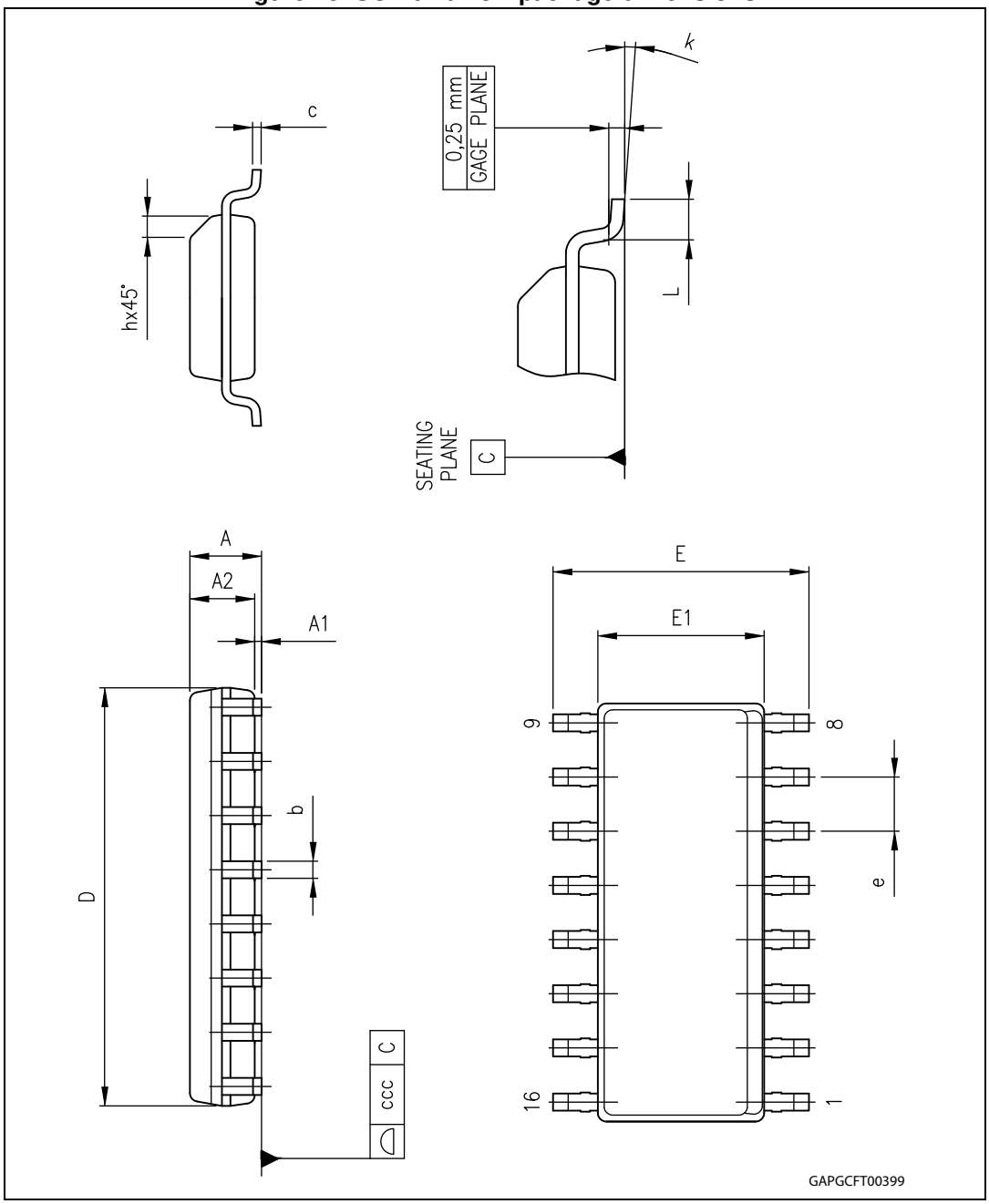


Table 10. SO-16 narrow mechanical data

DIM.	mm.		
	Min.	Typ.	Max.
A			1.75
A1	0.1		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.8	9.9	10
E	5.8	6	6.2
E1	3.8	3.9	4
e		1.27	
h	0.25		0.5
L	0.4		1.27
k	0		8
ccc			0.1

6 Revision history

Table 11. Document revision history

Date	Revision	Changes
17-Oct-2012	1	Initial release.
06-Dec-2012	2	*Table 3: Absolute maximum ratings*: – $-I_D$: updated value *Table 4: Thermal data*: – $R_{thj\text{-}case}$: removed row *Table 5: Features*: – I_{freq}: updated minimum and maximum values – V_{ch}, V_{cl}: removed rows – V_{ch} - V_{cl}, $I_{\_OL}$, $V_{\_OL}$: added row Added *Chapter 4: Package and PCB thermal data*
12-Dec-2012	3	*Table 5: Features*: – V_{ch} - V_{cl}: added typical value
09-Jan-2014	4	Updated *Figure 14: Rthj-amb vs PCB copper area in open box free air condition* Updated *Section 3.1: Normal operation*
28-Jul-2014	5	Changed document status from “Preliminary data” to “Production data”

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