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VN7010AJ

High-side driver with MultiSense analog feedback for automotive applications

Datasheet - production data

PowerSSO-16

GAPGCFT00327

Features

Max transient supply voltage	V_{CC}	40 V
Operating voltage range	V_{CC}	4 to 28 V
Typ. on-state resistance (per Ch)	R_{ON}	10 mΩ
Current limitation (typ)	I_{LIMH}	91 A
Standby current (max)	I_{STBY}	0.5 µA

- Automotive qualified
- General
  - Single channel smart high-side driver with MultiSense analog feedback
  - Very low standby current
  - Compatible with 3 V and 5 V CMOS outputs
- MultiSense diagnostic functions
  - Multiplexed analog feedback of: load current with high precision proportional current mirror, V_{CC} supply voltage and T_{CHIP} device temperature
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
  - OFF-state open-load detection
  - Output short to V_{CC} detection
  - Sense enable/disable
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Configurable latch-off on overtemperature or power limitation with dedicated fault reset pin
  - Loss of ground and loss of V_{CC}
  - Reverse battery with external components
  - Electrostatic discharge protection

Applications

- All types of Automotive resistive, inductive and capacitive loads
- Specially intended for Automotive Headlamps

Description

The device is a single channel high-side driver manufactured using ST proprietary VIPower® M0-7 technology and housed in PowerSSO-16 package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, providing protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off.

A $\overline{\text{FaultRST}}$ pin unlatches the output in case of fault or disables the latch-off functionality.

A dedicated multifunction multiplexed analog output pin delivers sophisticated diagnostic functions including high precision proportional load current sense, supply voltage feedback and chip temperature sense, in addition to the detection of overload and short circuit to ground, short to V_{CC} and OFF-state open-load.

A sense enable pin allows OFF-state diagnosis to be disabled during the module low-power mode as well as external sense resistor sharing among similar devices.

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1 Block diagram and pin description

Figure 1: Block diagram

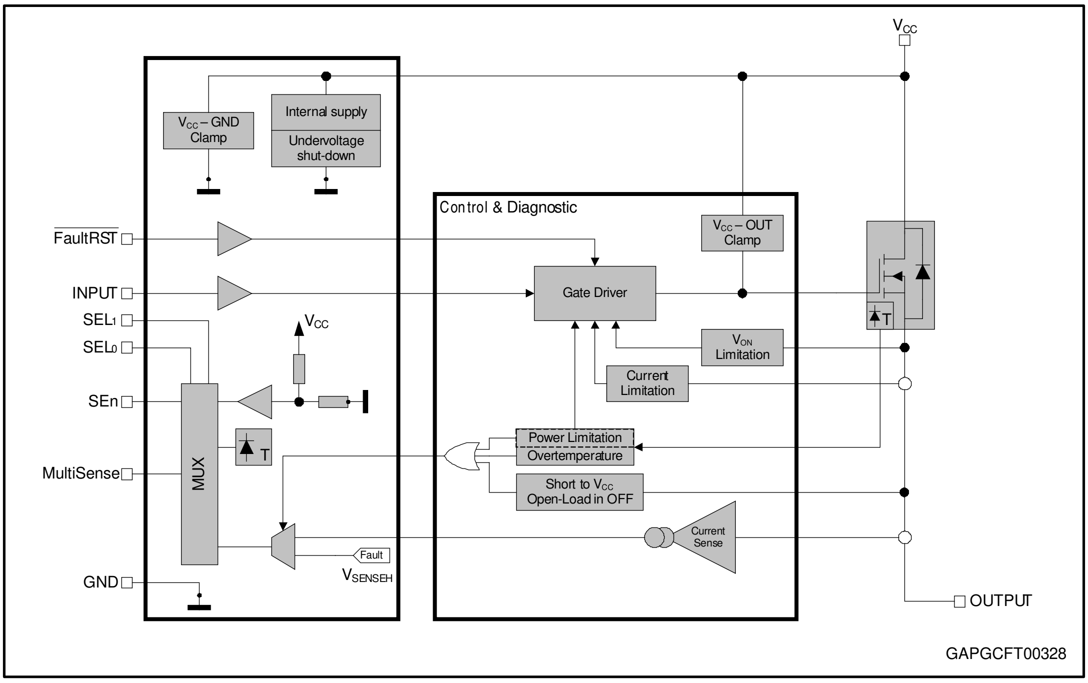
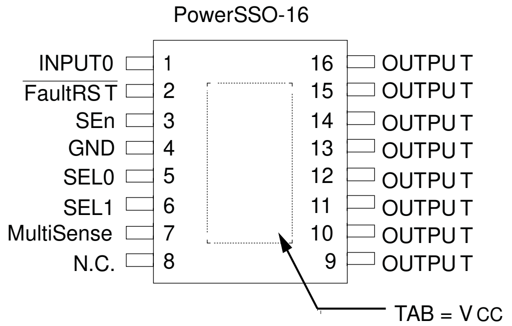


Table 1: Pin functions

Name	Function
V_{CC}	Battery connection.
OUTPUT	Power outputs. All the pins must be connected together.
GND	Ground connection. Must be reverse battery protected by an external diode / resistor network.
INPUT	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. It controls output switch state.
MultiSense	Multiplexed analog sense output pin; it delivers a current proportional to the selected diagnostic: load current, supply voltage or chip temperature.
SEn	Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the MultiSense diagnostic pin.
$SEL_{0,1}$	Active high compatible with 3 V and 5 V CMOS outputs pin; they address the MultiSense multiplexer.
FaultRST	Active low compatible with 3 V and 5 V CMOS outputs pin; it unlatches the output in case of fault; If kept low, sets the outputs in auto-restart. mode

Figure 2: Configuration diagram (top view)



Pins 9, 10, 11 and 12 are internally connected; Pins 13, 14, 15 and 16 are internally connected; All output pins must be connected together on PCB.

Table 2: Suggested connections for unused and not connected pins

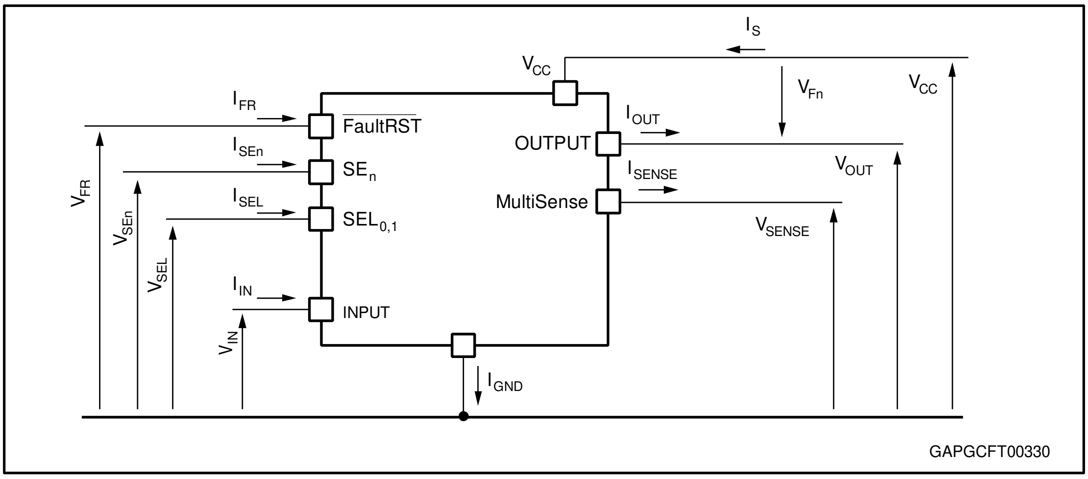
Connection / pin	MultiSense	N.C.	Output	Input	SEn, SELx, $\overline{\text{FaultRST}}$
Floating	Not allowed	X [1]	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 15 kΩ resistor	Through 15 kΩ resistor

Notes:

[1]X: do not care.

2 Electrical specification

Figure 3: Current and voltage conventions



$V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 3: "Absolute maximum ratings"* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	38	V
$-V_{CC}$	Reverse DC supply voltage	0.3	
V_{CCPK}	Maximum transient supply voltage (ISO 16750-2:2010 Test B clamped to 40 V; R_L = 4 Ω)	40	V
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	OUTPUT DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	35	
I_{IN}	INPUT DC input current	-1 to 10	mA
I_{SEn}	SEn DC input current		
I_{SEL}	$SEL_{0,1}$ DC input current		
I_{FR}	FaultRST DC input current		
V_{FR}	FaultRST DC input voltage	7.5	V

Symbol	Parameter	Value	Unit
I_{SENSE}	MultiSense pin DC output current (V_{GND} = V_{CC} and V_{SENSE} < 0 V)	10	mA
	MultiSense pin DC output current in reverse (V_{CC} < 0 V)	-20	
E_{MAX}	Maximum switching energy (single pulse) (T_{DEMAG} = 0.4 ms; T_{jstart} = 150 °C)	168	mJ
V_{ESD}	Electrostatic discharge (JEDEC 22A-114F) • INPUT • MultiSense • SEn, $SEL_{0,1}$, FaultRST • OUTPUT • V_{CC}	 4000 2000 4000 4000 4000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	

2.2 Thermal data

Table 4: Thermal data

Symbol	Parameter	Typ. value	Unit
$R_{thj\text{-}board}$	Thermal resistance junction-board (JEDEC JESD 51-5 / 51-8) (1)	3.9	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-5)(2)	55	
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-7)(1)	21.2	

Notes:

(1)Device mounted on four-layers 2s2p PCB

(2)Device mounted on two-layers 2s0p PCB with 2 cm^2 heatsink copper trace

2.3 Main electrical characteristics

7 V < V_{CC} < 18 V; -40°C < T_j < 150°C, unless otherwise specified.

All typical values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.

Table 5: Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4	13	28	V
V_{USD}	Undervoltage shutdown				4	V
$V_{USDReset}$	Undervoltage shutdown reset				5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.3		V
R_{ON}	On-state resistance	I_{OUT} = 5 A; T_j = 25°C		10		mΩ
		I_{OUT} = 5 A; T_j = 150°C			20	
		I_{OUT} = 5 A; V_{CC} = 4 V; T_j = 25°C			15	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{clamp}	Clamp voltage	I_S = 20 mA; 25°C < T_j < 150°C	41	46	52	V
		I_S = 20 mA; T_j = -40°C	38			V
I_{STBY}	Supply current in standby at V_{CC} = 13 V [(1)]	V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{FR} = V_{SEn} = 0 V; $V_{SEL0,1}$ = 0 V; T_j = 25°C			0.5	µA
		V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{FR} = V_{SEn} = 0 V; $V_{SEL0,1}$ = 0 V; T_j = 85°C [(2)]			0.5	
		V_{CC} = 13 V; V_{IN} = V_{OUT} = V_{FR} = V_{SEn} = 0 V; $V_{SEL0,1}$ = 0 V; T_j = 125°C			3	
t_{D_STBY}	Standby mode blanking time	V_{CC} = 13 V; V_{IN} = 5 V; V_{SEn} = V_{FR} = $V_{SEL0,1}$ = 0 V; I_{OUT} = 0 V	60	300	550	µs
$I_{S(ON)}$	Supply current	V_{CC} = 13 V; V_{SEn} = V_{FR} = $V_{SEL0,1}$ = 0 V; V_{IN} = 5 V; I_{OUT} = 0 A		3	5	mA
$I_{GND(ON)}$	Control stage current consumption in ON state. All channels active.	V_{CC} = 13 V; V_{SEn} = 5 V; V_{FR} = $V_{SEL0,1}$ = 0 V; V_{IN} = 5 V; I_{OUT} = 5 A			6	mA
$I_{L(off)}$	Off-state output current at V_{CC} = 13 V	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 25°C	0	0.01	0.5	µA
		V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 125°C	0		3	
V_F	Output - V_{CC} diode voltage	I_{OUT} = -5 A; T_j = 150°C			0.7	V

Notes:

(1)PowerMOS leakage included.

(2)Parameter specified by design; not subject to production test.

Table 6: Switching

V_{CC} = 13 V; -40°C < T_j < 150°C, unless otherwise specified						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
$t_{d(on)}$ [(1)]	Turn-on delay time at T_j = 25 °C	R_L = 2.6 Ω	10	70	120	µs
$t_{d(off)}$ [(1)]	Turn-off delay time at T_j = 25 °C		10	40	100	
$(dV_{OUT}/dt)_{on}$ [(1)]	Turn-on voltage slope at T_j = 25 °C	R_L = 2.6 Ω	0.1	0.2	0.7	V/µs
$(dV_{OUT}/dt)_{off}$ [(1)]	Turn-off voltage slope at T_j = 25 °C		0.1	0.3	0.7	
W_{ON}	Switching energy losses at turn-on (t_{won})	R_L = 2.6 Ω	—	0.9	1.2 [(2)]	mJ
W_{OFF}	Switching energy losses at turn-off (t_{woff})	R_L = 2.6 Ω	—	0.6	0.8 [(2)]	mJ
t_{SKEW} [(1)]	Differential Pulse skew (t_{PHL} - t_{PLH})	R_L = 2.6 Ω	-90	-40	10	µs

Notes:

(1)See *Figure 6: "Switching time and Pulse skew"*.

(2)Parameter guaranteed by design and characterization; not subject to production test.

Table 7: Logic inputs

7 V < V_{CC} < 28 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
INPUT characteristics						
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.2			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
$\overline{\text{FaultRST}}$ characteristics						
V_{FRL}	Input low level voltage				0.9	V
I_{FRL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{FRH}	Input high level voltage		2.1			V
I_{FRH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{FR(hyst)}$	Input hysteresis voltage		0.2			V
V_{FRCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.5	V
		I_{IN} = -1 mA		-0.7		
$SEL_{0,1}$ characteristics (7 V < V_{CC} < 18 V)						
V_{SELL}	Input low level voltage				0.9	V
I_{SELL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SELH}	Input high level voltage		2.1			V
I_{SELH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEL(hyst)}$	Input hysteresis voltage		0.2			V
V_{SELCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
SEn characteristics (7 V < V_{CC} < 18 V)						
V_{SEnL}	Input low level voltage				0.9	V
I_{SEnL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SEnH}	Input high level voltage		2.1			V
I_{SEnH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEn(hyst)}$	Input hysteresis voltage		0.2			V
V_{SEnCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		

Table 8: Protections

7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
I_{LIMH}	DC short circuit current	V_{CC} = 13 V	65	91	130	A
		4 V < V_{CC} < 18 V (1)				
I_{LIML}	Short circuit current during thermal cycling	V_{CC} = 13 V; T_R < T_j < T_{TSD}		30		
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature(1)		T_{RS} + 1	T_{RS} + 7		
T_{RS}	Thermal reset of fault diagnostic indication	V_{FR} = 0 V; V_{SEn} = 5 V	135			
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)(1)			7		
ΔT_{J_SD}	Dynamic temperature	T_j = -40°C; V_{CC} = 13 V		60		K
t_{LATCH_RST}	Fault reset time for output unlatch(1)	V_{FR} = 5 V to 0 V; V_{SEn} = 5 V; V_{IN} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V	3	10	20	µs
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 2 A; L = 6 mH; T_j = -40°C	V_{CC} - 38			V
		I_{OUT} = 2 A; L = 6 mH; T_j = 25°C to 150°C	V_{CC} - 41	V_{CC} - 46	V_{CC} - 52	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 0.2 A		20		mV

Notes:

(1)Parameter guaranteed by design and characterization; not subject to production test.

Table 9: MultiSense

7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{SENSE_CL}	MultiSense clamp voltage	V_{SEn} = 0 V; I_{SENSE} = 1 mA	-17		-12	V
		V_{SEn} = 0 V; I_{SENSE} = -1 mA		7		
CurrentSense characteristics						
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.9 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	3190	5210	7450	
dK_0/K_0(1)(2)	Current sense ratio drift	I_{OUT} = 0.9 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-20		20	%
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 1.5 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	3530	4950	6560	
dK_1/K_1(1)(2)	Current sense ratio drift	I_{OUT} = 1.5 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-15		15	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 6 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	3840	4720	5640	

7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
dK_2/K_2 (1)(2)	Current sense ratio drift	I_{OUT} = 6 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-10		10	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 18 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	4260	4710	5140	
dK_3/K_3 (1)(2)	Current sense ratio drift	I_{OUT} = 18 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-5		5	%
I_{SENSE0}	MultiSense leakage current	MultiSense disabled: V_{SEn} = 0 V	0		0.5	µA
		MultiSense disabled: -1 V < V_{SENSE} < 5 V (1)	-0.5		0.5	
		MultiSense enabled: V_{SEn} = 5 V; Channel ON; I_{OUT} = 0 A; Diagnostic selected; V_{IN} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT} = 0 A	0		2	
		MultiSense enabled: V_{SEn} = 5 V; Channel OFF; Diagnostic selected: V_{IN} = 0 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V	0		2	
V_{OUT_MSD} (1)	Output Voltage for MultiSense shutdown	V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; R_{SENSE} = 2.7 kΩ; I_{OUT} = 5 A		5		V
V_{SENSE_SAT}	Multisense saturation voltage	V_{CC} = 7 V; R_{SENSE} = 2.7 kΩ; V_{SEn} = 5 V; V_{IN} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT} = 18 A; T_j = 150°C	5			V
I_{SENSE_SAT} (1)	CS saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; T_j = 150°C	4			mA
I_{OUT_SAT} (1)	Output saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; T_j = 150°C	24			A
OFF-state diagnostic						
V_{OL}	OFF-state open-load voltage detection threshold	V_{IN} = 0 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V	2	3	4	V
$I_{L(off2)}$	OFF-state output sink current	V_{IN} = 0 V; V_{OUT} = V_{OL}; T_j = -40°C to 125°C	-100		-15	µA
t_{DSTKON}	OFF-state diagnostic delay time from falling edge of INPUT (see *Figure 9: "TDSTKON"*)	V_{IN} = 5 V to 0 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT} = 0 A; V_{OUT} = 4 V	100	350	700	µs
$t_{D\_OL\_V}$	Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn	V_{IN} = 0 V; V_{FR} = 0 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; V_{OUT} = 4 V; V_{SEn} = 0 V to 5 V			60	µs
t_{D_VOL}	OFF-state diagnostic delay time from rising edge of V_{OUT}	V_{IN} = 0 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; V_{OUT} = 0 V to 4 V		5	30	µs

7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Chip temperature analog feedback						
V_{SENSE_TC}	MultiSense output voltage proportional to chip temperature	V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; V_{IN} = 0 V; R_{SENSE} = 1 kΩ; T_j = -40°C	2.325	2.41	2.495	V
		V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; V_{IN} = 0 V; R_{SENSE} = 1 kΩ; T_j = 25°C	1.985	2.07	2.155	V
		V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; V_{IN} = 0 V; R_{SENSE} = 1 kΩ; T_j = 125°C	1.435	1.52	1.605	V
dV_{SENSE_TC}/dT	Temperature coefficient	T_j = -40°C to 150°C		-5.5		mV/K
Transfer function		$V_{SENSE\_TC}(T) = V_{SENSE\_TC}(T_0) + dV_{SENSE\_TC} / dT * (T - T_0)$				
V_{CC} supply voltage analog feedback						
V_{SENSE_VCC}	MultiSense output voltage proportional to V_{CC} supply voltage	V_{CC} = 13 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; V_{IN} = 0 V; R_{SENSE} = 1 kΩ	3.16	3.23	3.3	V
Transfer function (3)		$V_{SENSE\_VCC} = V_{CC} / 4$				
Fault diagnostic feedback (see *Table 10: "Truth table"*)						
V_{SENSEH}	MultiSense output voltage in fault condition	V_{CC} = 13 V; V_{IN} = 0 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT} = 0 A; V_{OUT} = 4 V; R_{SENSE} = 1 kΩ;	5		6.6	V
I_{SENSEH}	MultiSense output current in fault condition	V_{CC} = 13 V; V_{SENSE} = 5 V	7	20	30	mA
MultiSense timings (current sense mode - see *Figure 7: "MultiSense timings (current sense mode)"*)(4)						
$t_{DSENSE1H}$	Current sense settling time from rising edge of SEn	V_{IN} = 5 V; V_{SEn} = 0 V to 5 V; R_{SENSE} = 1 kΩ; R_L = 2.6 Ω			60	µs
$t_{DSENSE1L}$	Current sense disable delay time from falling edge of SEn	V_{IN} = 5 V; V_{SEn} = 5 V to 0 V; R_{SENSE} = 1 kΩ; R_L = 2.6 Ω		5	20	µs
$t_{DSENSE2H}$	Current sense settling time from rising edge of INPUT	V_{IN} = 0 V to 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 2.6 Ω		100	250	µs
$\Delta t_{DSENSE2H}$	Current sense settling time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	V_{IN} = 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; I_{SENSE} = 90 % of $I_{SENSEMAX}$; R_L = 2.6 Ω			100	µs
$t_{DSENSE2L}$	Current sense turn-off delay time from falling edge of INPUT	V_{IN} = 5 V to 0 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 2.6 Ω		50	250	µs

7 V < V_{CC} < 18 V; -40°C < T_j < 150°C						
Symbol	**Parameter**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
MultiSense timings (chip temperature sense mode - see *Figure 8: "Multisense timings (chip temperature and VCC sense mode)"*)[(4)]						
$t_{DSENSE3H}$	V_{SENSE_TC} settling time from rising edge of SEn	V_{SEn} = 0 V to 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			60	µs
$t_{DSENSE3L}$	V_{SENSE_TC} disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
MultiSense timings (V_{CC} voltage sense mode - see *Figure 8: "Multisense timings (chip temperature and VCC sense mode)"*)[(4)]						
$t_{DSENSE4H}$	V_{SENSE_VCC} settling time from rising edge of SEn	V_{SEn} = 0 V to 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			60	µs
$t_{DSENSE4L}$	V_{SENSE_VCC} disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
MultiSense timings (Multiplexer transition times)[(4)]						
t_{D_CStoTC}	MultiSense transition delay from current sense to T_C sense	V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V to 5 V; I_{OUT} = 2.5 A; R_{SENSE} = 1 kΩ			60	µs
t_{D_TCtoCS}	MultiSense transition delay from T_C sense to current sense	V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V to 0 V; I_{OUT} = 2.5 A; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_CStoVCC}$	MultiSense transition delay from current sense to V_{CC} sense	V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 0 V to 5 V; I_{OUT} = 2.5A; R_{SENSE} = 1 kΩ			60	µs
$t_{D\_VCCtoCS}$	MultiSense transition delay from V_{CC} sense to current sense	V_{IN} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V to 0 V; I_{OUT} = 2.5 A; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_TCtoVCC}$	MultiSense transition delay from T_C sense to V_{CC} sense	V_{CC} = 13 V; T_j = 125°C; V_{SEn} = 5 V; V_{SEL0} = 0 V to 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_VCCtoTC}$	MultiSense transition delay from V_{CC} sense to T_C sense	V_{CC} = 13 V; T_j = 125°C; V_{SEn} = 5 V; V_{SEL0} = 5 V to 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs

Notes:

(1)Parameter specified by design; not subject to production test.

(2)All values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.

(3)V_{CC} sensing and T_C are referred to GND potential.

(4)Transition delay are measured up to +/- 10% of final conditions.

Figure 4: IOUT/ISENSE versus IOUT

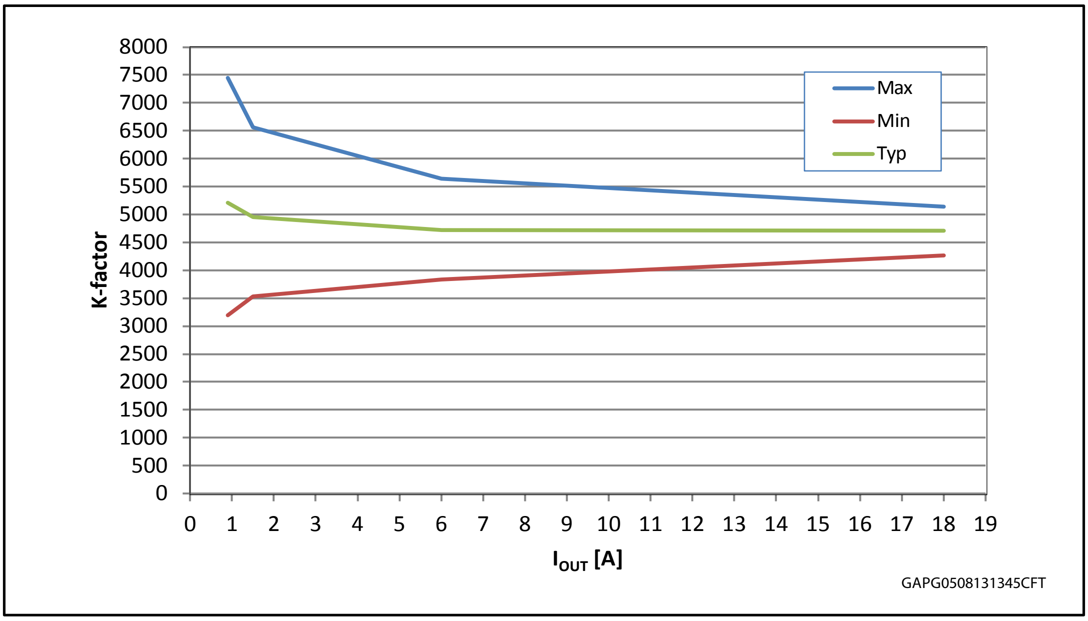


Figure 5: Current sense accuracy versus IOUT

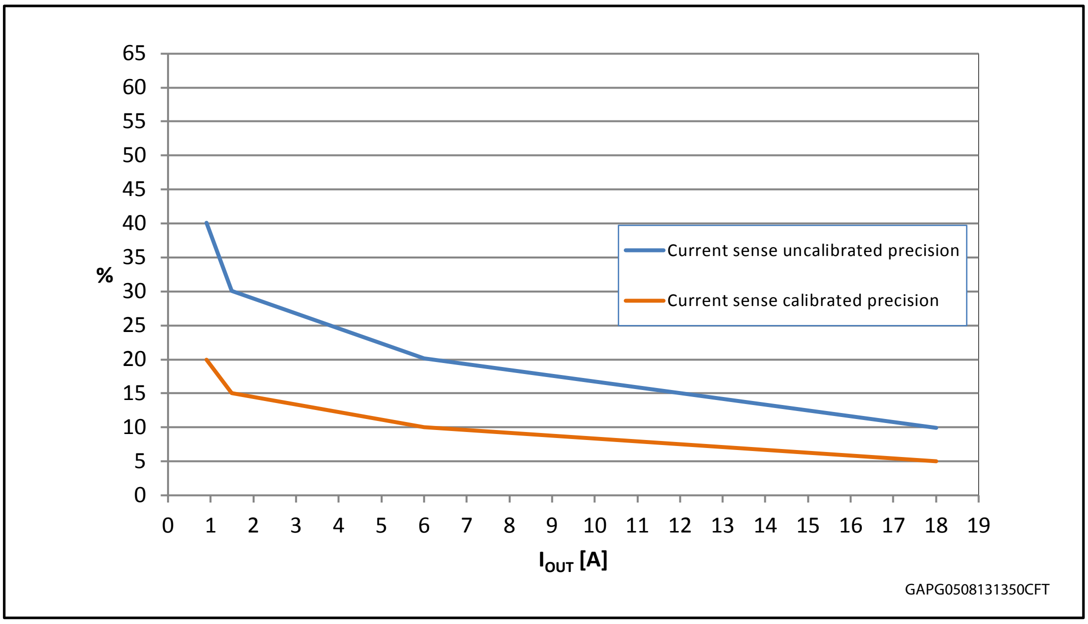


Figure 6: Switching time and Pulse skew

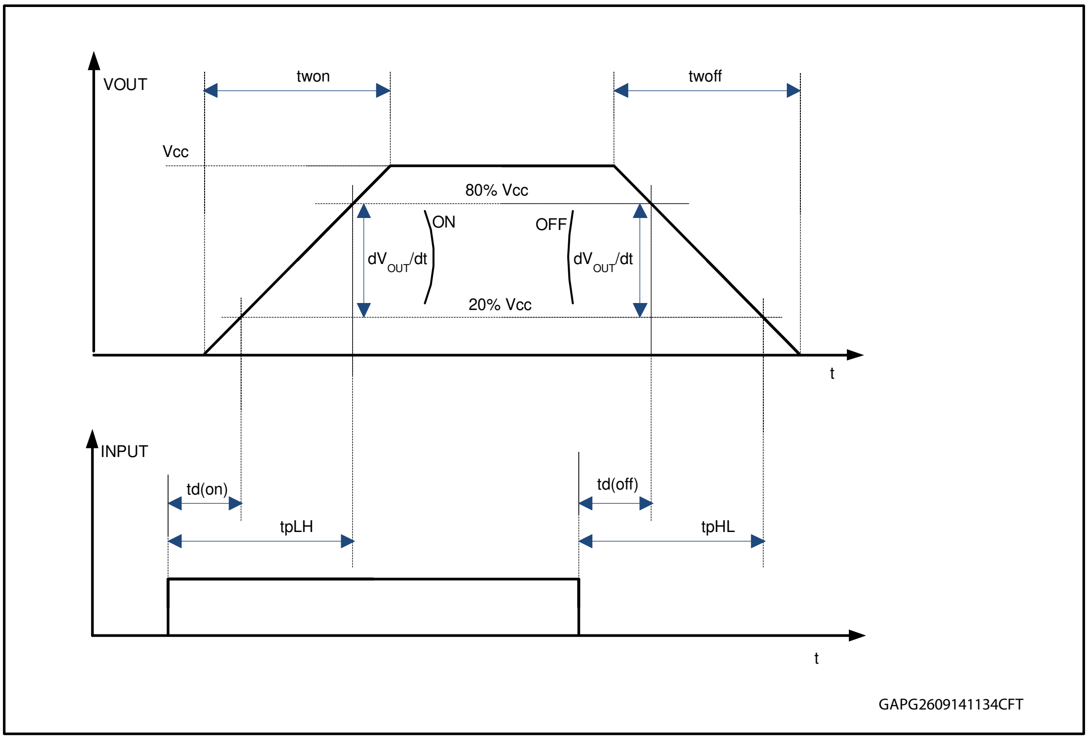


Figure 7: MultiSense timings (current sense mode)

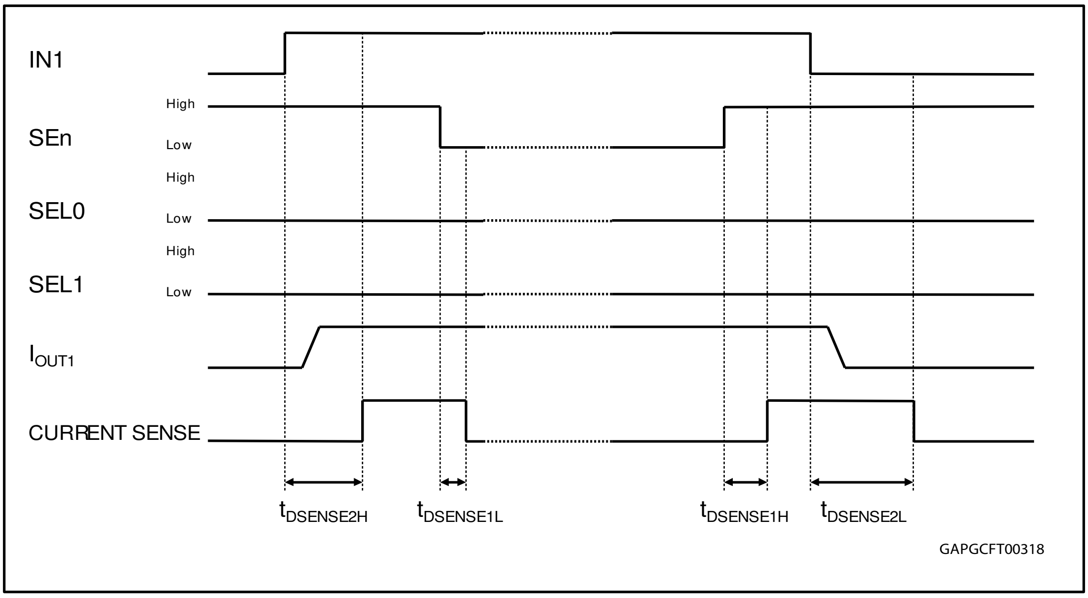


Figure 8: Multisense timings (chip temperature and VCC sense mode)

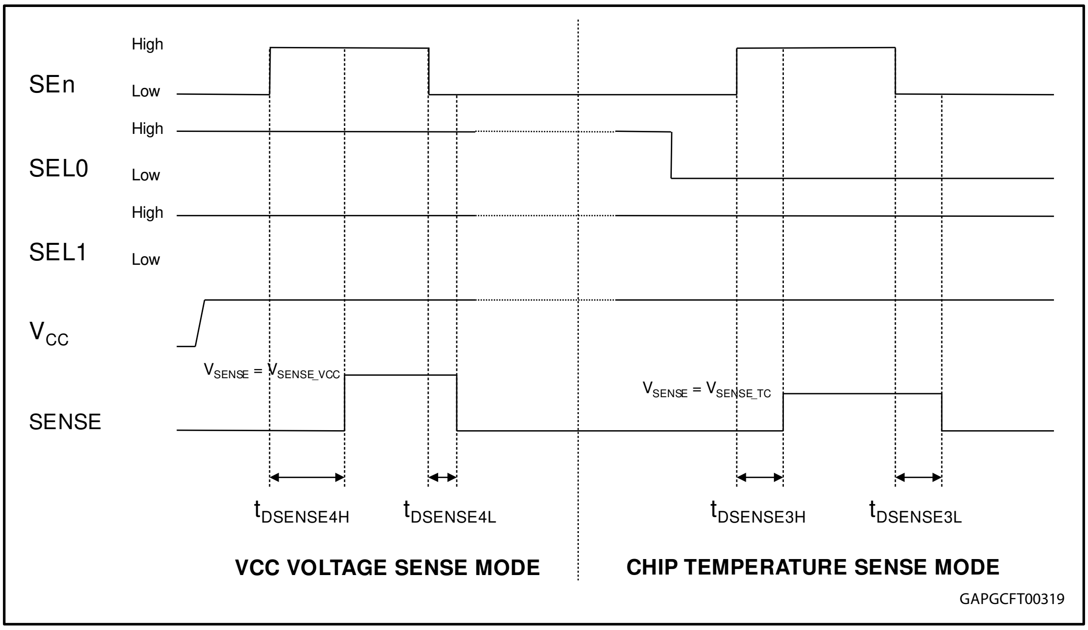


Figure 9: TDSTKON

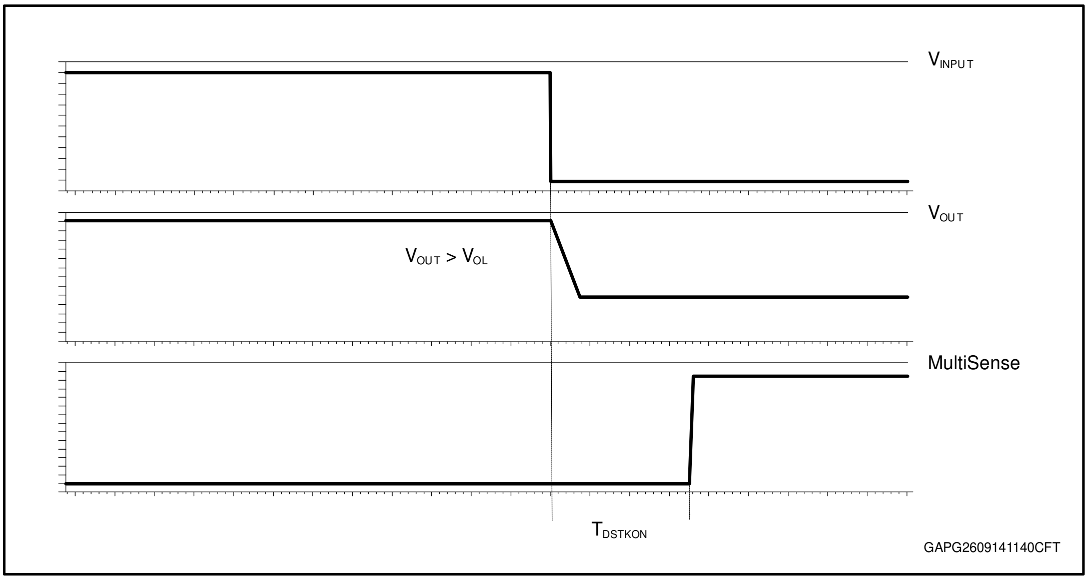


Table 10: Truth table

Mode	Conditions	IN_X	FR	SEn	SEL_X	OUT_X	MultiSense	Comments
Standby	All logic inputs low	L	L	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; $T_j < 150$ °C	L	X	See (1)		L	See (1)	
		H	L			H	See (1)	Outputs configured for auto-restart
		H	H			H	See (1)	Outputs configured for Latch-off
Overload	Overload or short to GND causing: $T_j > T_{TSD}$ or $\Delta T_j > \Delta T_{j\_SD}$	L	X	See (1)		L	See (1)	
		H	L			H	See (1)	Output cycles with temperature hysteresis
		H	H			L	See (1)	Output latches-off
Undervoltage	$V_{CC} < V_{USD}$ (falling)	X	X	X	X	L L	Hi-Z Hi-Z	Re-start when $V_{CC} > V_{USD} + V_{USDhyst}$ (rising)
OFF-state diagnostics	Short to V_{CC}	L	X	See (1)		H	See (1)	
	Open-load	L	X			H	See (1)	External pull-up
Negative output voltage	Inductive loads turn-off	L	X	See (1)		< 0 V	See (1)	

Notes:

(1)Refer to *Table 11: "MultiSense multiplexer addressing"*

Table 11: MultiSense multiplexer addressing

SEn	SEL_1	SEL_0	MUX channel	MultiSense output			
				Normal mode	Overload	OFF-state diag. (1)	Negative output
L	X	X		Hi-Z			
H	L	L	Output diagnostic	$I_{SENSE} = 1/K * I_{OUT}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	Hi-Z
H	L	H					
H	H	L	T_{CHIP} Sense	$V_{SENSE} = V_{SENSE\_TC}$			
H	H	H	V_{CC} Sense	$V_{SENSE} = V_{SENSE\_VCC}$			

Notes:

(1)In case the output channel corresponding to the selected MUX channel is latched off while the relevant input is low, Multisense pin delivers feedback according to OFF-State diagnostic. Example 1: FR = 1; IN = 0; OUT = L (latched); MUX channel = channel 0 diagnostic; Mutisense = 0. Example 2: FR = 1; IN = 0; OUT = latched, $V_{OUT} > V_{OL}$; MUX channel = channel 0 diagnostic; Mutisense = V_{SENSEH}

2.4 Waveforms

Figure 10: Latch functionality - behavior in hard short circuit condition (TAMB << TTSD)

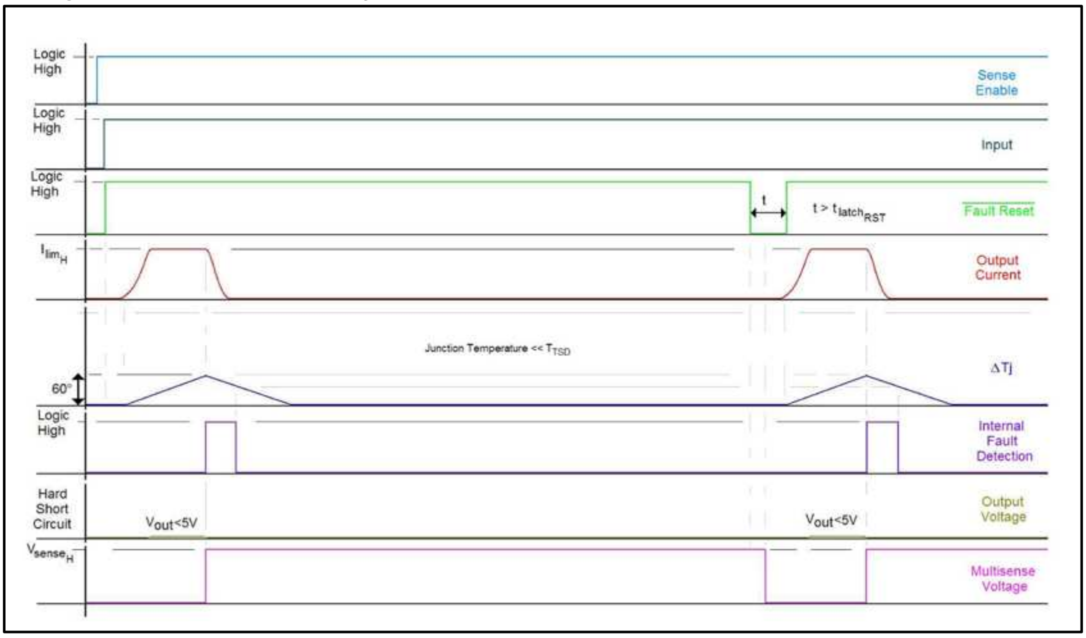


Figure 11: Latch functionality - behavior in hard short circuit condition

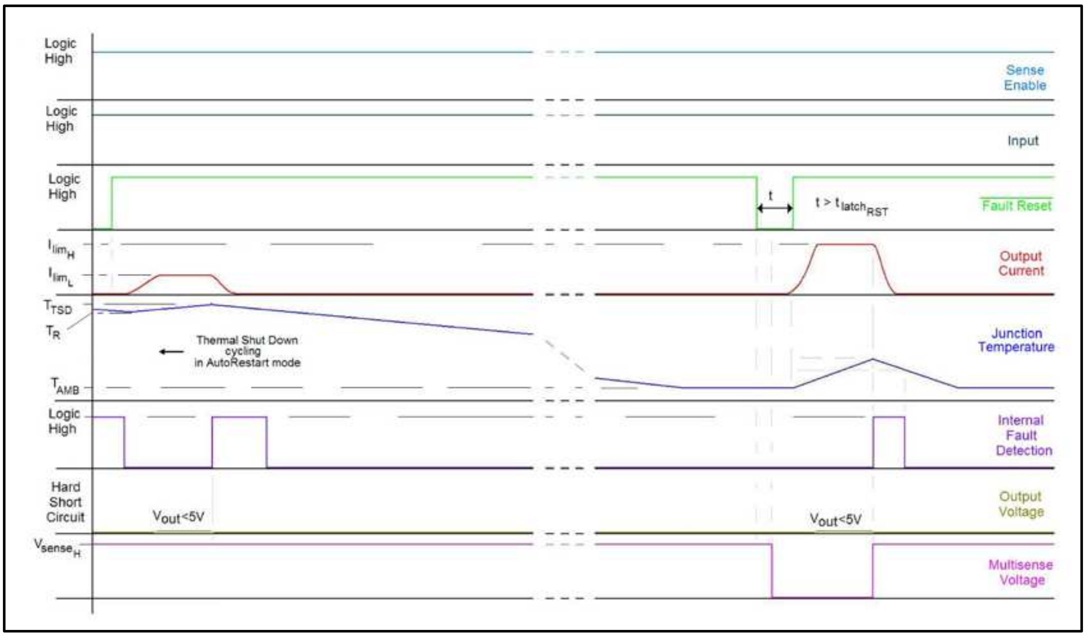


Figure 12: Latch functionality - behavior in hard short circuit condition (autorestart mode + latch off)

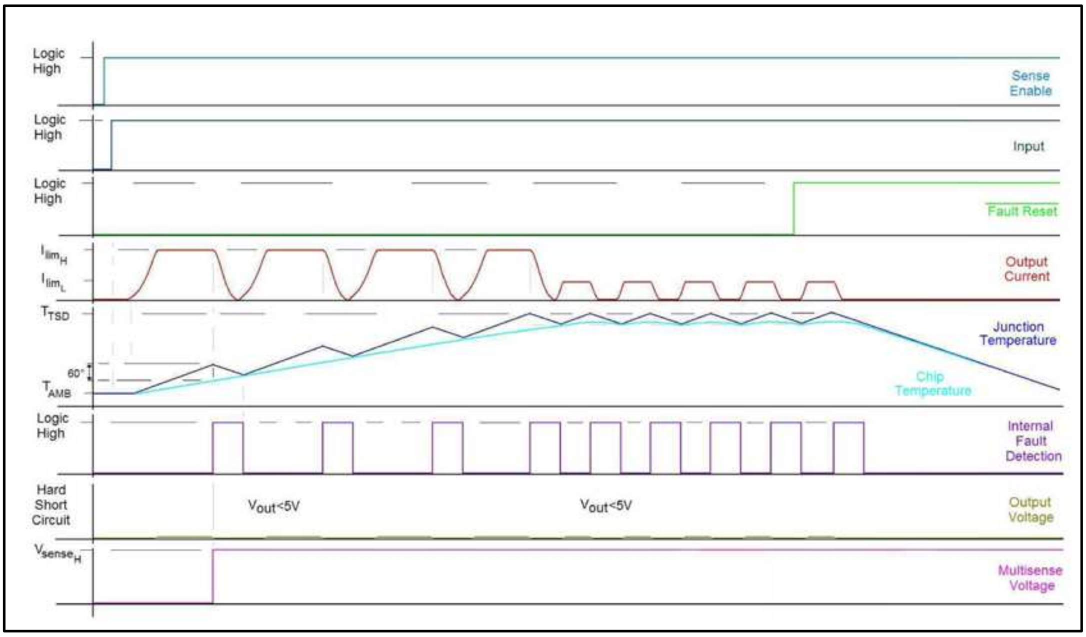


Figure 13: Standby mode activation

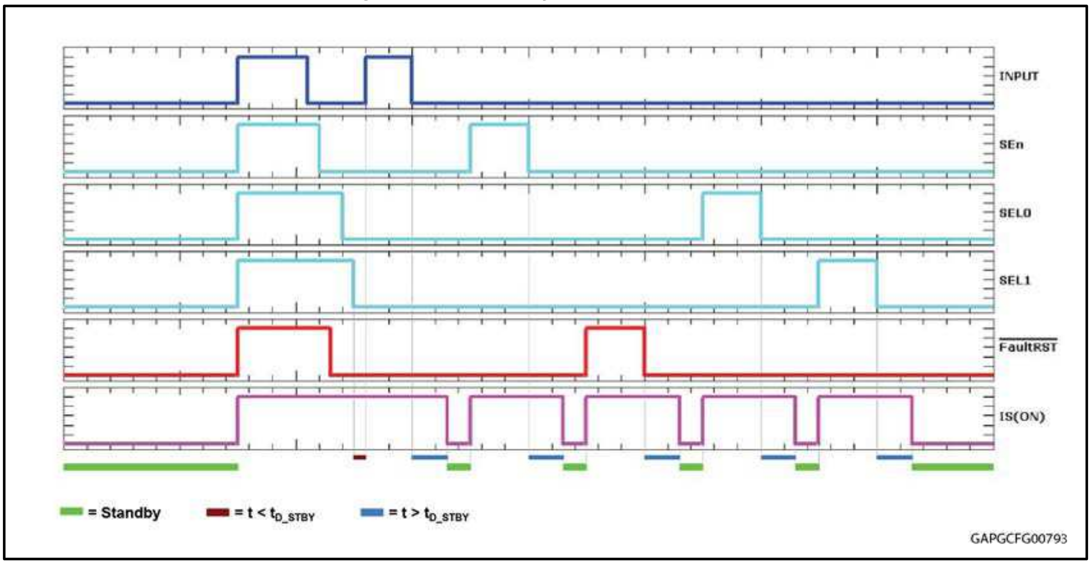
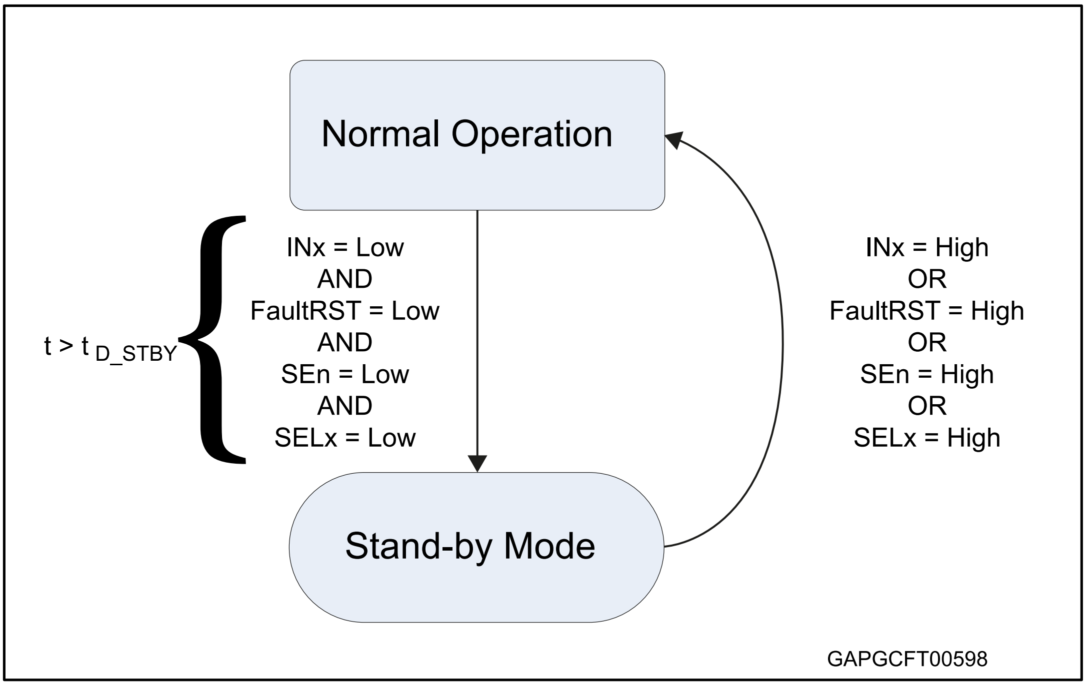


Figure 14: Standby state diagram



2.5 Electrical characteristics curves

Figure 15: OFF-state output current

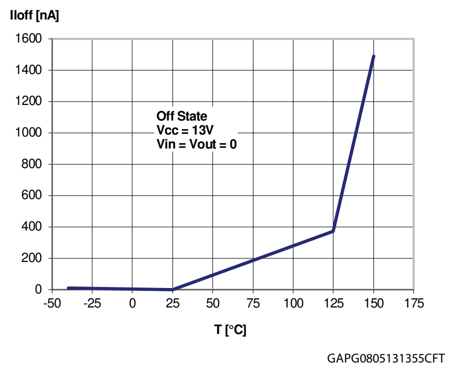


Figure 16: Standby current

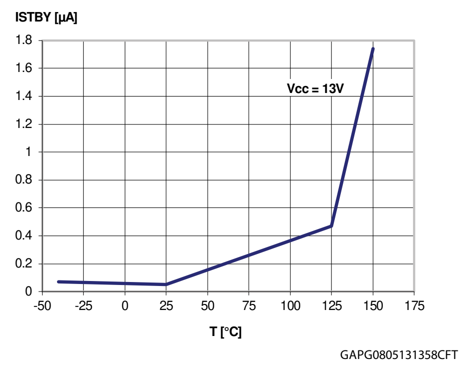


Figure 17: IGND(ON) vs. Iout

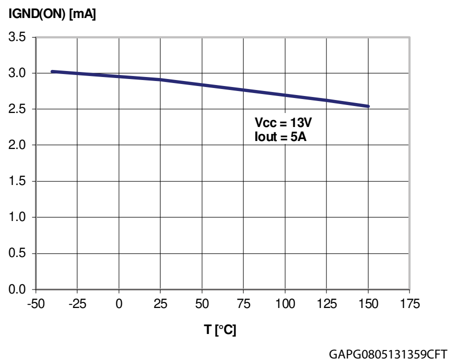


Figure 18: Logic Input high level voltage

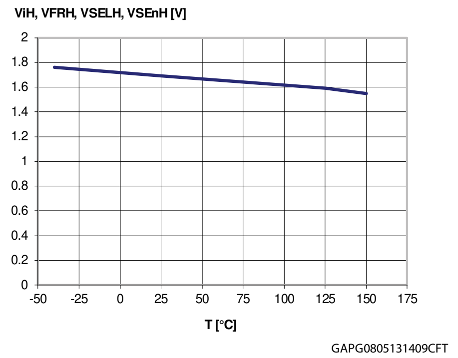


Figure 19: Logic Input low level voltage

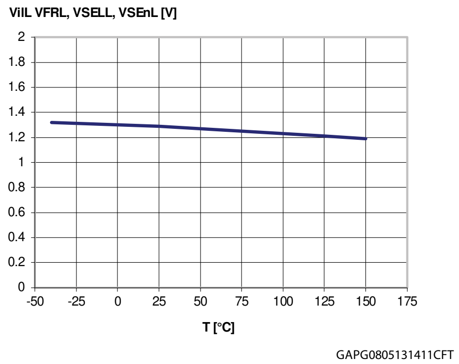


Figure 20: High level logic input current

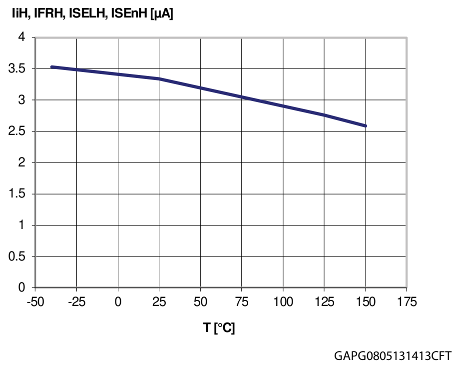


Figure 21: Low level logic input current

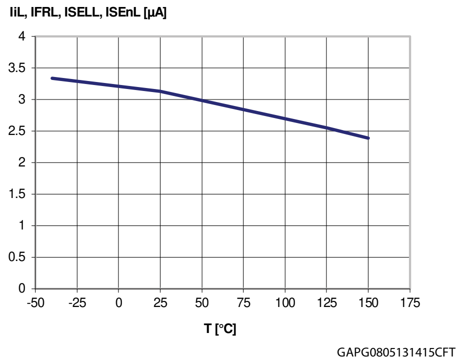


Figure 22: Logic Input hysteresis voltage

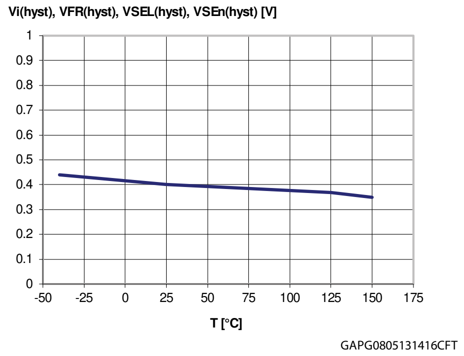


Figure 23: FaultRST Input clamp voltage

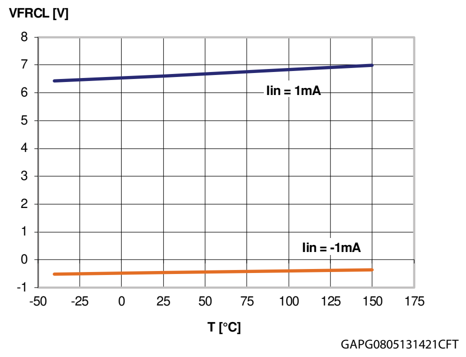


Figure 24: Undervoltage shutdown

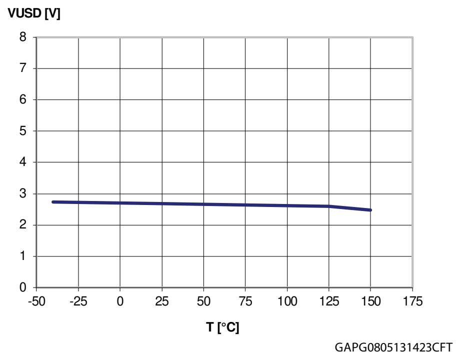


Figure 25: On-state resistance vs. Tcase

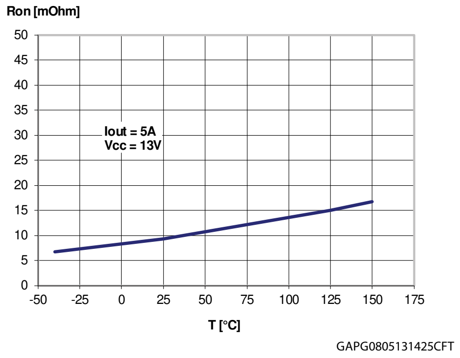


Figure 26: On-state resistance vs. VCC

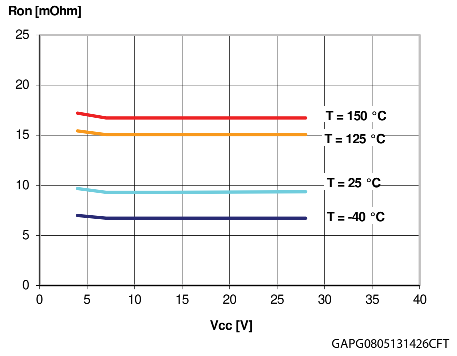


Figure 27: Turn-on voltage slope

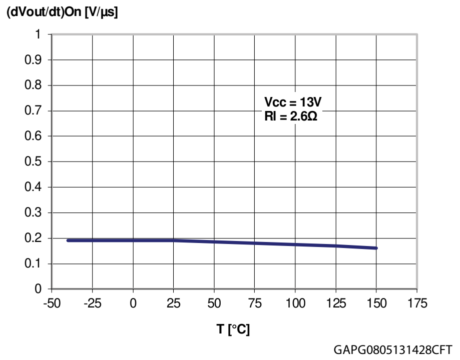


Figure 28: Turn-off voltage slope

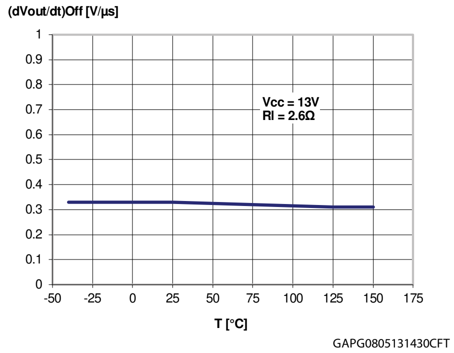


Figure 29: Won vs. Tcase

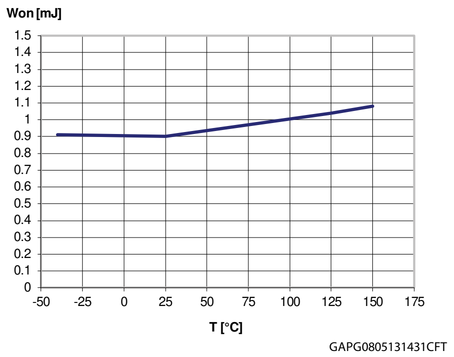


Figure 30: Woff vs. Tcase

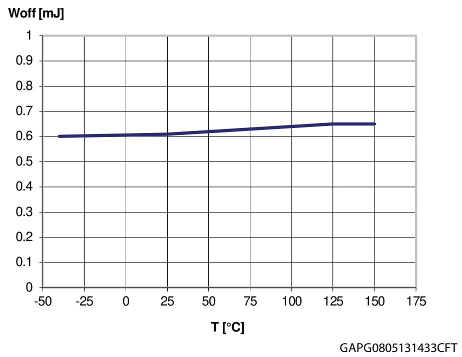


Figure 31: ILIMH vs. Tcase

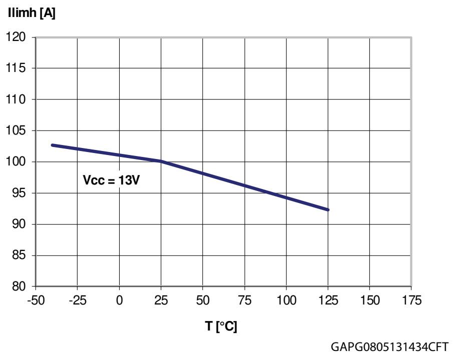


Figure 32: OFF-state open-load voltage detection threshold

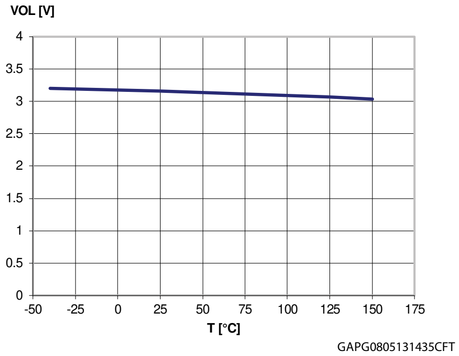


Figure 33: Vsense clamp vs. Tcase

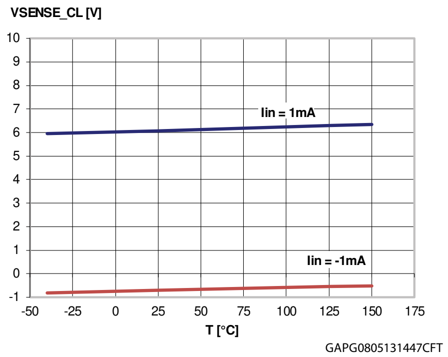
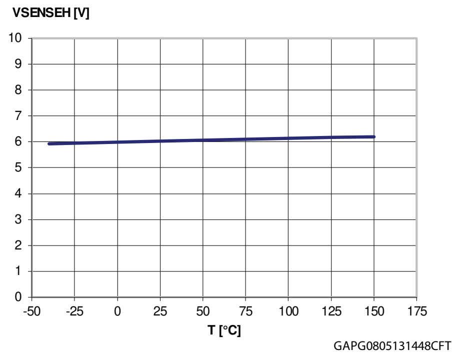


Figure 34: Vsenseh vs. Tcase



3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_j through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_j exceeds the safety level of ΔT_{j_SD}. According to the voltage level on the FaultRST pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled (FaultRST = Low) or remains off (FaultRST = High). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the FaultRST pin, the device switches on again as soon as its junction temperature drops to T_R (FaultRST = Low) or remains off (FaultRST = High).

3.3 Current limitation

The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH}, by operating the output power MOSFET in the active region.

3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches a negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG}, allowing the inductor energy to be dissipated without damaging the device.