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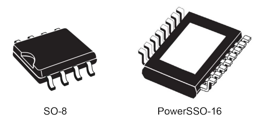
# High-side driver with MultiSense analog feedback for automotive applications

Datasheet - production data




## Features

| | | |
|---|---|---|
| Max transient supply voltage | $V_{CC}$ | 40 V |
| Operating voltage range | $V_{CC}$ | 4 to 28 V |
| Typ. on-state resistance (per Ch) | $R_{ON}$ | 50 mΩ |
| Current limitation (typ) | $I_{LIMH}$ | 30 A |
| Standby current (max) | $I_{STBY}$ | 0.5 µA |

- AEC-Q100 qualified
- General
  - Single channel smart high-side driver with MultiSense analog feedback
  - Very low standby current
  - Compatible with 3 V and 5 V CMOS outputs
- MultiSense diagnostic functions
  - Multiplexed analog feedback of: load current with high precision proportional current mirror, $V_{CC}$ supply voltage and $T_{CHIP}$ device temperature
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
  - OFF-state open-load detection
  - Output short to $V_{CC}$ detection
  - Sense enable/disable
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Configurable latch-off on overtemperature or power limitation with dedicated fault reset pin
  - Loss of ground and loss of $V_{CC}$
  - Reverse battery with external components
  - Electrostatic discharge protection

## Applications

- All types of Automotive resistive, inductive and capacitive loads
- Specially intended for Automotive Turn Indicators (up to P27W or SAE1156 or LED Rear Combinations)

## Description

The devices are single channel high-side drivers manufactured using ST proprietary VIPower® M0-7 technology and housed in PowerSSO-16 and SO-8 packages. The devices are designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, and to provide protection and diagnostics.

The devices integrate advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off.

A $\overline{FaultRST}$ pin unlatches the output in case of fault or disables the latch-off functionality.

A dedicated multifunction multiplexed analog output pin delivers sophisticated diagnostic functions including high precision proportional load current sense, supply voltage feedback and chip temperature sense, in addition to the detection of overload and short circuit to ground, short to $V_{CC}$ and OFF-state open-load.

A sense enable pin allows OFF-state diagnosis to be disabled during the module low-power mode as well as external sense resistor sharing among similar devices.



This is information on a product in full production.

# Contents

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# 1 Block diagram and pin description

**Figure 1: Block diagram**

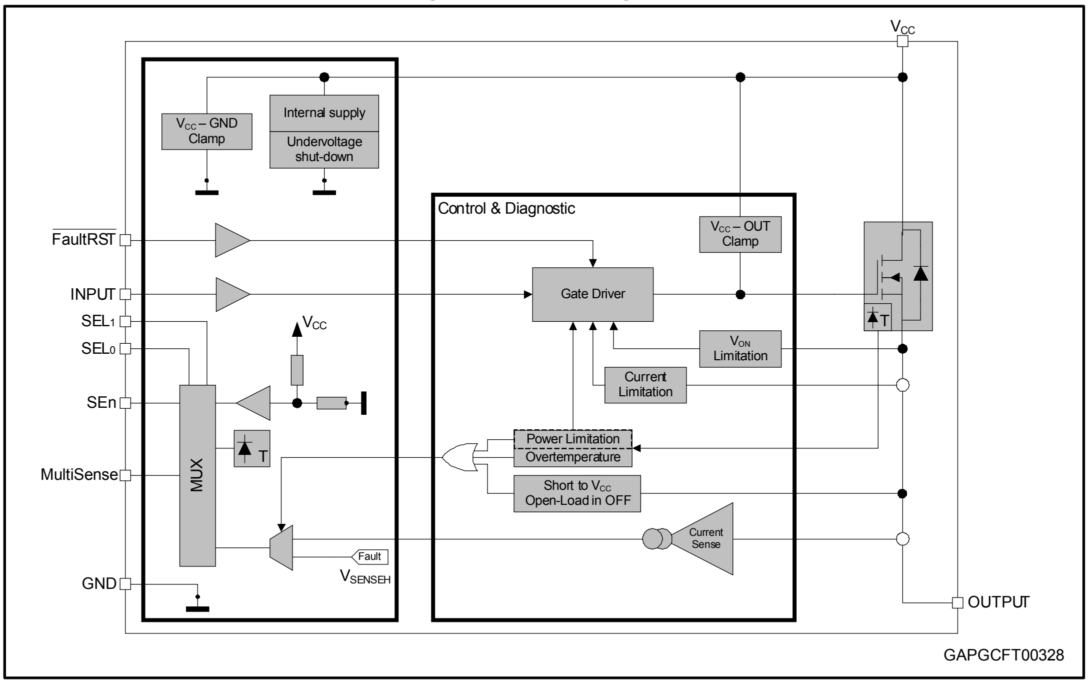



**Table 1: Pin functions**

| Name | Function |
|---|---|
| $V_{CC}$ | Battery connection. |
| OUTPUT | Power outputs. |
| GND | Ground connection. Must be reverse battery protected by an external diode / resistor network. |
| INPUT | Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. It controls output switch state. |
| MultiSense | Multiplexed analog sense output pin; it delivers a current proportional to the selected diagnostic: load current, supply voltage or chip temperature. |
| SEn | Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the MultiSense diagnostic pin. |
| $SEL_{0,1}$ | Active high compatible with 3 V and 5 V CMOS outputs pin; they address the MultiSense multiplexer. |
| $\overline{FaultRST}$ | Active low compatible with 3 V and 5 V CMOS outputs pin; it unlatches the output in case of fault; If kept low, sets the outputs in auto-restart mode. |

**Figure 2: Configuration diagram (top view)**

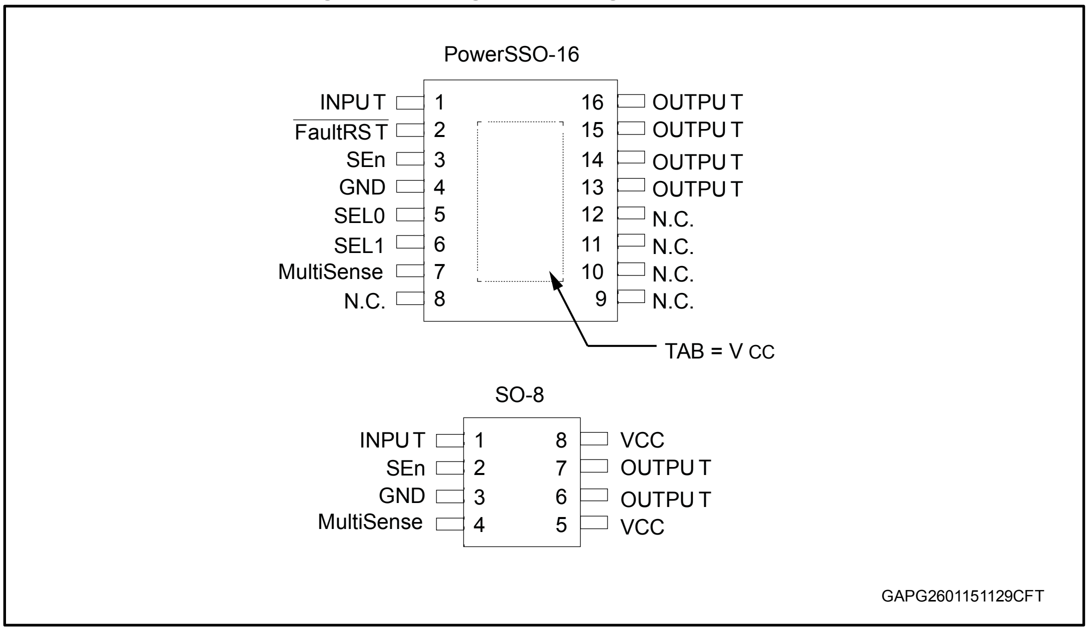



**Table 2: Suggested connections for unused and not connected pins**

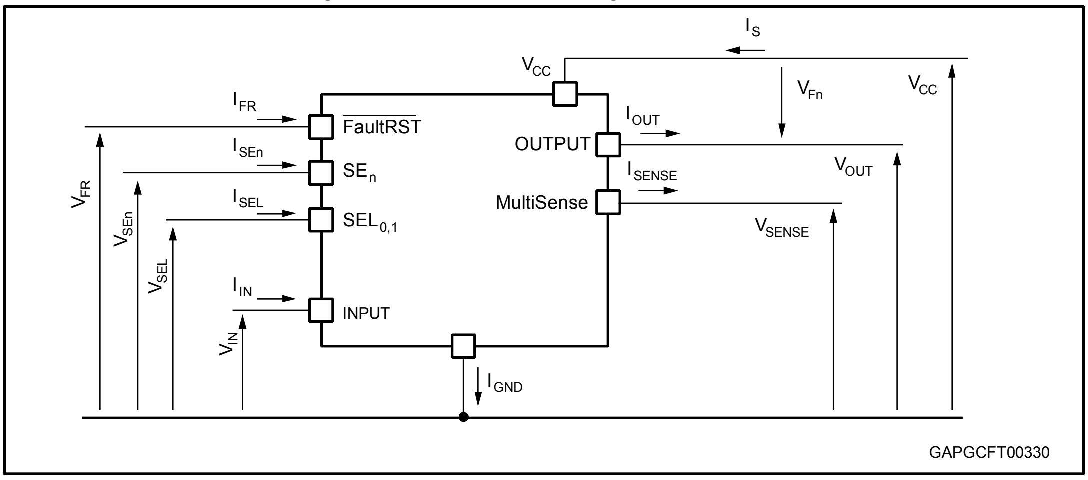
| Connection / pin | MultiSense | N.C. | Output | Input | SEn, SELx, FaultRST |
|---|---|---|---|---|---|
| Floating | Not allowed | X [(1)] | X | X | X |
| To ground | Through 1 kΩ resistor | X | Not allowed | Through 15 kΩ resistor | Through 15 kΩ resistor |

**Notes:**

[(1)] X: do not care.

# 2 Electrical specification

**Figure 3: Current and voltage conventions**




$V_F = V_{OUT} - V_{CC}$ during reverse battery condition.

## 2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 3: "Absolute maximum ratings"* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

**Table 3: Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC supply voltage | 38 | V |
| $-V_{CC}$ | Reverse DC supply voltage | 0.3 | |
| $V_{CCPK}$ | Maximum transient supply voltage (ISO 16750-2:2010 Test B clamped to 40 V; $R_L$ = 4 Ω) | 40 | V |
| $V_{CCJS}$ | Maximum jump start voltage for single pulse short circuit protection | 28 | V |
| $-I_{GND}$ | DC reverse ground pin current | 200 | mA |
| $I_{OUT}$ | OUTPUT DC output current | Internally limited | A |
| $-I_{OUT}$ | Reverse DC output current | 10 | |
| $I_{IN}$ | INPUT DC input current | -1 to 10 | mA |
| $I_{SEn}$ | SEn DC input current | | |
| $I_{SEL}$ | $SEL_{0,1}$ DC input current | | |
| $I_{FR}$ | FaultRST DC input current | | |
| $V_{FR}$ | FaultRST DC input voltage | 7.5 | V |

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{SENSE}$ | MultiSense pin DC output current ($V_{GND}$ = $V_{CC}$ and $V_{SENSE}$ < 0 V) | 10 | mA |
| | MultiSense pin DC output current in reverse ($V_{CC}$ < 0 V) | -20 | |
| $E_{MAX}$ | Maximum switching energy (single pulse) ($T_{DEMAG}$ = 0.4 ms; $T_{jstart}$ = 150 °C) | 30 | mJ |
| $V_{ESD}$ | Electrostatic discharge (JEDEC 22A-114F)<br>• INPUT<br>• MultiSense<br>• SEn, $SEL_{0,1}$, FaultRST<br>• OUTPUT<br>• $V_{CC}$ | <br>4000<br>2000<br>4000<br>4000<br>4000 | <br>V<br>V<br>V<br>V<br>V |
| $V_{ESD}$ | Charge device model (CDM-AEC-Q100-011) | 750 | V |
| $T_j$ | Junction operating temperature | -40 to 150 | °C |
| $T_{stg}$ | Storage temperature | -55 to 150 | |

## 2.2 Thermal data

**Table 4: Thermal data**

| Symbol | Parameter | Typ. value | | Unit |
|---|---|---|---|---|
| | | SO-8 | PowerSSO-16 | Unit |
| $R_{thj-board}$ | Thermal resistance junction-board (JEDEC JESD 51-8) (1) | 29.4 | 6.8 | °C/W |
| $R_{thj-amb}$ | Thermal resistance junction-ambient (JEDEC JESD 51-2)(2) | 67.5 | 58.5 | |
| $R_{thj-amb}$ | Thermal resistance junction-ambient (JEDEC JESD 51-2)(1) | 45.8 | 24.5 | |

**Notes:**

(1)Device mounted on four-layers 2s2p PCB

(2)Device mounted on two-layers 2s0p PCB with 2 $cm^2$ heatsink copper trace

## 2.3 Main electrical characteristics

7 V < $V_{CC}$ < 28 V; -40°C < $T_j$ < 150°C, unless otherwise specified.

All typical values refer to $V_{CC}$ = 13 V; $T_j$ = 25°C, unless otherwise specified.

**Table 5: Power section**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Operating supply voltage | | 4 | 13 | 28 | V |
| $V_{USD}$ | Undervoltage shutdown | | | | 4 | V |
| $V_{USDReset}$ | Undervoltage shutdown reset | | | | 5 | V |
| $V_{USDhyst}$ | Undervoltage shutdown hysteresis | | | 0.3 | | V |
| $R_{ON}$ | On-state resistance | $I_{OUT}$ = 2 A; $T_j$ = 25°C | | 50 | | mΩ |
| | | $I_{OUT}$ = 2 A; $T_j$ = 150°C | | | 100 | |
| | | $I_{OUT}$ = 2 A; $V_{CC}$ = 4 V; $T_j$ = 25°C | | | 75 | |
| $V_{clamp}$ | Clamp voltage | $I_S$ = 20 mA; 25°C < $T_j$ < 150°C | 41 | 46 | 52 | V |
| | | $I_S$ = 20 mA; $T_j$ = -40°C | 38 | | | V |
| $I_{STBY}$ | Supply current in standby at $V_{CC}$ = 13 V (1) | $V_{CC}$ = 13 V; $V_{IN}$ = $V_{OUT}$ = $V_{FR}$ = $V_{SEn}$ = 0 V; $V_{SEL0,1}$ = 0 V; $T_j$ = 25°C | | | 0.5 | µA |
| | | $V_{CC}$ = 13 V; $V_{IN}$ = $V_{OUT}$ = $V_{FR}$ = $V_{SEn}$ = 0 V; $V_{SEL0,1}$ = 0 V; $T_j$ = 85°C (2) | | | 0.5 | |
| | | $V_{CC}$ = 13 V; $V_{IN}$ = $V_{OUT}$ = $V_{FR}$ = $V_{SEn}$ = 0 V; $V_{SEL0,1}$ = 0 V; $T_j$ = 125°C | | | 3 | |
| $t_{D\_STBY}$ | Standby mode blanking time | $V_{CC}$ = 13 V; $V_{IN}$ = $V_{OUT}$ = $V_{FR}$ = $V_{SEL0,1}$ = 0 V; $V_{SEn}$ = 5 V to 0 V | 60 | 300 | 550 | µs |
| $I_{S(ON)}$ | Supply current | $V_{CC}$ = 13 V; $V_{SEn}$ = 0 V; $V_{SEL0,1}$ = $V_{FR}$ = 0 V; $V_{IN}$ = 5 V; $I_{OUT}$ = 0 A | | 3 | 5 | mA |
| $I_{GND(ON)}$ | Control stage current consumption in ON-state. All channels active. | $V_{CC}$ = 13 V; $V_{SEn}$ = 5 V; $V_{FR}$ = $V_{SEL0,1}$ = 0 V; $V_{IN}$ = 5 V; $I_{OUT}$ = 2 A | | | 6 | mA |
| $I_{L(off)}$ | Off-state output current at $V_{CC}$ = 13 V | $V_{IN}$ = $V_{OUT}$ = 0 V; $V_{CC}$ = 13 V; $T_j$ = 25°C | 0 | 0.01 | 0.5 | µA |
| | | $V_{IN}$ = $V_{OUT}$ = 0 V; $V_{CC}$ = 13 V; $T_j$ = 125°C | 0 | | 3 | |
| $V_F$ | Output - $V_{CC}$ diode voltage | $I_{OUT}$ = -2 A; $T_j$ = 150°C | | | 0.7 | V |

**Notes:**

(1)PowerMOS leakage included.

(2)Parameter specified by design; not subjected to production test.

**Table 6: Switching**

| $V_{CC}$ = 13 V; -40°C < $T_j$ < 150°C, unless otherwise specified | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Test conditions** | **Min.** | **Typ.** | **Max.** | **Unit** |
| $t_{d(on)}$ (1) | Turn-on delay time at $T_j$ = 25 °C | $R_L$ = 6.5 Ω | 10 | 60 | 120 | μs |
| $t_{d(off)}$ (1) | Turn-off delay time at $T_j$ = 25 °C | | 10 | 40 | 100 | |
| $(dV_{OUT}/dt)_{on}$ (1) | Turn-on voltage slope at $T_j$ = 25 °C | $R_L$ = 6.5 Ω | 0.1 | 0.3 | 0.7 | V/μs |
| $(dV_{OUT}/dt)_{off}$ (1) | Turn-off voltage slope at $T_j$ = 25 °C | | 0.1 | 0.32 | 0.7 | |
| $W_{ON}$ | Switching energy losses at turn-on ($t_{won}$) | $R_L$ = 6.5 Ω | — | 0.25 | 0.33 (2) | mJ |
| $W_{OFF}$ | Switching energy losses at turn-off ($t_{woff}$) | $R_L$ = 6.5 Ω | — | 0.23 | 0.31 (2) | mJ |
| $t_{SKEW}$ (1) | Differential Pulse skew ($t_{PHL}$ - $t_{PLH}$) | $R_L$ = 6.5 Ω | -80 | -30 | 20 | μs |

**Notes:**

(1)See *Figure 6: "Switching time and Pulse skew"*.

(2)Parameter guaranteed by design and characterization; not subjected to production test.

**Table 7: Logic inputs**

| 7 V < $V_{CC}$ < 28 V; -40°C < $T_j$ < 150°C | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Test conditions** | **Min.** | **Typ.** | **Max.** | **Unit** |
| **INPUT characteristics** | | | | | | |
| $V_{IL}$ | Input low level voltage | | | | 0.9 | V |
| $I_{IL}$ | Low level input current | $V_{IN}$ = 0.9 V | 1 | | | μA |
| $V_{IH}$ | Input high level voltage | | 2.1 | | | V |
| $I_{IH}$ | High level input current | $V_{IN}$ = 2.1 V | | | 10 | μA |
| $V_{I(hyst)}$ | Input hysteresis voltage | | 0.2 | | | V |
| $V_{ICL}$ | Input clamp voltage | $I_{IN}$ = 1 mA | 5.3 | | 7.2 | V |
| | | $I_{IN}$ = -1 mA | | -0.7 | | |
| **$\overline{FaultRST}$ characteristics (VN7050AJ only)** | | | | | | |
| $V_{FRL}$ | Input low level voltage | | | | 0.9 | V |
| $I_{FRL}$ | Low level input current | $V_{IN}$ = 0.9 V | 1 | | | μA |
| $V_{FRH}$ | Input high level voltage | | 2.1 | | | V |
| $I_{FRH}$ | High level input current | $V_{IN}$ = 2.1 V | | | 10 | μA |
| $V_{FR(hyst)}$ | Input hysteresis voltage | | 0.2 | | | V |
| $V_{FRCL}$ | Input clamp voltage | $I_{IN}$ = 1 mA | 5.3 | | 7.5 | V |
| | | $I_{IN}$ = -1 mA | | -0.7 | | |
| **$SEL_{0,1}$ characteristics (VN7050AJ only)(7 V < $V_{CC}$ < 18 V)** | | | | | | |
| $V_{SELL}$ | Input low level voltage | | | | 0.9 | V |
| $I_{SELL}$ | Low level input current | $V_{IN}$ = 0.9 V | 1 | | | μA |
| $V_{SELH}$ | Input high level voltage | | 2.1 | | | V |
| $I_{SELH}$ | High level input current | $V_{IN}$ = 2.1 V | | | 10 | μA |

| 7 V < $V_{CC}$ < 28 V; -40°C < $T_j$ < 150°C | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Test conditions** | **Min.** | **Typ.** | **Max.** | **Unit** |
| $V_{SEL(hyst)}$ | Input hysteresis voltage | | 0.2 | | | V |
| $V_{SELCL}$ | Input clamp voltage | $I_{IN}$ = 1 mA | 5.3 | | 7.2 | V |
| | | $I_{IN}$ = -1 mA | | -0.7 | | |
| **SEn characteristics (7 V < $V_{CC}$ < 18 V)** | | | | | | |
| $V_{SEnL}$ | Input low level voltage | | | | 0.9 | V |
| $I_{SEnL}$ | Low level input current | $V_{IN}$ = 0.9 V | 1 | | | µA |
| $V_{SEnH}$ | Input high level voltage | | 2.1 | | | V |
| $I_{SEnH}$ | High level input current | $V_{IN}$ = 2.1 V | | | 10 | µA |
| $V_{SEn(hyst)}$ | Input hysteresis voltage | | 0.2 | | | V |
| $V_{SEnCL}$ | Input clamp voltage | $I_{IN}$ = 1 mA | 5.3 | | 7.2 | V |
| | | $I_{IN}$ = -1 mA | | -0.7 | | |

**Table 8: Protections**

| 7 V < $V_{CC}$ < 18 V; -40°C < $T_j$ < 150°C | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Test conditions** | **Min.** | **Typ.** | **Max.** | **Unit** |
| $I_{LIMH}$ | DC short circuit current | $V_{CC}$ = 13 V | 21 | 30 | 42 | A |
| | | 4 V < $V_{CC}$ < 18 V [(1)] | | | | |
| $I_{LIML}$ | Short circuit current during thermal cycling | $V_{CC}$ = 13 V; $T_R$ < $T_j$ < $T_{TSD}$ | | 10 | | |
| $T_{TSD}$ | Shutdown temperature | | 150 | 175 | 200 | °C |
| $T_R$ | Reset temperature[(1)] | | $T_{RS}$ + 1 | $T_{RS}$ + 7 | | |
| $T_{RS}$ | Thermal reset of fault diagnostic indication | $V_{FR}$ = 0 V; $V_{SEn}$ = 5 V | 135 | | | |
| $T_{HYST}$ | Thermal hysteresis($T_{TSD}$ - $T_R$)[(1)] | | | 7 | | |
| $\Delta T_{J\_SD}$ | Dynamic temperature | $T_j$ = -40°C; $V_{CC}$ = 13 V | | 60 | | K |
| $t_{LATCH\_RST}$ | Fault reset time for output unlatch[(1)] (only for VN7050AJ) | $V_{FR}$ = 5 V to 0 V; $V_{SEn}$ = 5 V; $V_{IN}$ = 5 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 0 V | 3 | 10 | 20 | µs |
| $V_{DEMAG}$ | Turn-off output voltage clamp | $I_{OUT}$ = 2 A; L = 6 mH; $T_j$ = -40°C | $V_{CC}$ - 38 | | | V |
| | | $I_{OUT}$ = 2 A; L = 6 mH; $T_j$ = 25°C to 150°C | $V_{CC}$ - 41 | $V_{CC}$ - 46 | $V_{CC}$ - 52 | V |
| $V_{ON}$ | Output voltage drop limitation | $I_{OUT}$ = 0.2 A | | 20 | | mV |

**Notes:**

[(1)]Parameter guaranteed by design and characterization; not subjected to production test.

Table 9: MultiSense

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **7 V < $V_{CC}$ < 18 V; -40°C < $T_j$ < 150°C** | | | | | | |
| $V_{SENSE\_CL}$ | MultiSense clamp voltage | $V_{SEn}$ = 0 V; $I_{SENSE}$ = 1 mA | -17 | | -12 | V |
| | | $V_{SEn}$ = 0 V; $I_{SENSE}$ = -1 mA | | 7 | | |
| **CurrentSense characteristics** | | | | | | |
| $K_{OL}$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 0.01 A; $V_{SENSE}$ = 0.5 V; $V_{SEn}$ = 5 V | 440 | | | |
| $dK_{cal}/K_{cal}$ (1)(2) | Current sense ratio drift at calibration point | $I_{OUT}$ = 0.01 A to 0.03 A; $I_{cal}$ = 17.5 mA; $V_{SENSE}$ = 0.5 V; $V_{SEn}$ = 5 V | -30 | | 30 | % |
| $K_{LED}$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 0.05 A; $V_{SENSE}$ = 0.5 V; $V_{SEn}$ = 5 V | 530 | 1445 | 2200 | |
| $dK_{LED}/K_{LED}$ (1)(2) | Current sense ratio drift | $I_{OUT}$ = 0.05 A; $V_{SENSE}$ = 0.5 V; $V_{SEn}$ = 5 V | -25 | | 25 | % |
| $K_0$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 0.2 A; $V_{SENSE}$ = 0.5 V; $V_{SEn}$ = 5 V | 830 | 1330 | 1935 | |
| $dK_0/K_0$ (1)(2) | Current sense ratio drift | $I_{OUT}$ = 0.2 A; $V_{SENSE}$ = 0.5 V; $V_{SEn}$ = 5 V | -20 | | 20 | % |
| $K_1$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 0.4 A; $V_{SENSE}$ = 4 V; $V_{SEn}$ = 5 V | 915 | 1290 | 1700 | |
| $dK_1/K_1$ (1)(2) | Current sense ratio drift | $I_{OUT}$ = 0.4 A; $V_{SENSE}$ = 4 V; $V_{SEn}$ = 5 V | -15 | | 15 | % |
| $K_2$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 1.5 A; $V_{SENSE}$ = 4 V; $V_{SEn}$ = 5 V | 980 | 1200 | 1470 | |
| $dK_2/K_2$ (1)(2) | Current sense ratio drift | $I_{OUT}$ = 1.5 A; $V_{SENSE}$ = 4 V; $V_{SEn}$ = 5 V | -10 | | 10 | % |
| $K_3$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 4.5 A; $V_{SENSE}$ = 4 V; $V_{SEn}$ = 5 V | 1050 | 1190 | 1290 | |
| $dK_3/K_3$ (1)(2) | Current sense ratio drift | $I_{OUT}$ = 4.5 A; $V_{SENSE}$ = 4 V; $V_{SEn}$ = 5 V | -5 | | 5 | % |
| $I_{SENSE0}$ | MultiSense leakage current | MultiSense disabled: $V_{SEn}$ = 0 V | 0 | | 0.5 | µA |
| | | MultiSense disabled: -1 V < $V_{SENSE}$ < 5 V (1) | -0.5 | | 0.5 | |
| | | MultiSense enabled: $V_{SEn}$ = 5 V; Channel ON; $I_{OUT}$ = 0 A; Diagnostic selected; $V_{IN}$ = 5 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 0 V; $I_{OUT}$ = 0 A | 0 | | 2 | |
| | | MultiSense enabled: $V_{SEn}$ = 5 V; Channel OFF; Diagnostic selected: $V_{IN}$ = 0 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 0 V | 0 | | 2 | |

| 7 V < $V_{CC}$ < 18 V; -40°C < $T_j$ < 150°C | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Test conditions** | **Min.** | **Typ.** | **Max.** | **Unit** |
| $V_{OUT\_MSD}$[(1)] | Output Voltage for MultiSense shutdown | $V_{IN}$ = 5 V; $V_{SEn}$ = 5 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 0 V; $R_{SENSE}$ = 2.7 kΩ; $I_{OUT}$ = 2 A | | 5 | | V |
| $V_{SENSE\_SAT}$ | Multisense saturation voltage | $V_{CC}$ = 7 V; $R_{SENSE}$ = 2.7 kΩ; $V_{SEn}$ = 5 V; $V_{IN}$ = 5 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 0 V; $I_{OUT}$ = 2 A; $T_j$ = 150°C | 5 | | | V |
| $I_{SENSE\_SAT}$[(1)] | CS saturation current | $V_{CC}$ = 7 V; $V_{SENSE}$ = 4 V; $V_{IN}$ = 5 V; $V_{SEn}$ = 5 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 0 V; $T_j$ = 150°C | 4 | | | mA |
| $I_{OUT\_SAT}$[(1)] | Output saturation current | $V_{CC}$ = 7 V; $V_{SENSE}$ = 4 V; $V_{IN}$ = 5 V; $V_{SEn}$ = 5 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 0 V; $T_j$ = 150°C | 6 | | | A |
| **OFF-state diagnostic** | | | | | | |
| $V_{OL}$ | OFF-state open-load voltage detection threshold | $V_{IN}$ = 0 V; $V_{SEn}$ = 5 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 0 V | 2 | 3 | 4 | V |
| $I_{L(off2)}$ | OFF-state output sink current | $V_{IN}$ = 0 V; $V_{OUT}$ = $V_{OL}$ | -100 | | -15 | µA |
| $t_{DSTKON}$ | OFF-state diagnostic delay time from falling edge of INPUT (see *Figure 9: "TDSTKON"*) | $V_{IN}$ = 5 V to 0 V; $V_{SEn}$ = 5 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 0 V; $I_{OUT}$ = 0 A; $V_{OUT}$ = 4 V | 100 | 350 | 700 | µs |
| $t_{D\_OL\_V}$ | Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn | $V_{IN}$ = 0 V; $V_{FR}$ = 0 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 0 V; $V_{OUT}$ = 4 V; $V_{SEn}$ = 0 V to 5 V | | | 60 | µs |
| $t_{D\_VOL}$ | OFF-state diagnostic delay time from rising edge of $V_{OUT}$ | $V_{IN}$ = 0 V; $V_{SEn}$ = 5 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 0 V; $V_{OUT}$ = 0 V to 4 V | | 5 | 30 | µs |
| **Chip temperature analog feedback (VN7050AJ only)** | | | | | | |
| $V_{SENSE\_TC}$ | MultiSense output voltage proportional to chip temperature | $V_{SEn}$ = 5 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 5 V; $V_{IN}$ = 0 V; $R_{SENSE}$ = 1 kΩ; $T_j$ = -40°C | 2.325 | 2.41 | 2.495 | V |
| | | $V_{SEn}$ = 5 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 5 V; $V_{IN}$ = 0 V; $R_{SENSE}$ = 1 kΩ; $T_j$ = 25°C | 1.985 | 2.07 | 2.155 | V |
| | | $V_{SEn}$ = 5 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 5 V; $V_{IN}$ = 0 V; $R_{SENSE}$ = 1 kΩ; $T_j$ = 125°C | 1.435 | 1.52 | 1.605 | V |
| $dV_{SENSE\_TC}/dT$[(1)] | Temperature coefficient | $T_j$ = -40°C to 150°C | | -5.5 | | mV/K |

| 7 V < $V_{CC}$ < 18 V; -40°C < $T_j$ < 150°C | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Test conditions** | **Min.** | **Typ.** | **Max.** | **Unit** |
| Transfer function | | $V_{SENSE\_TC}$ (T) = $V_{SENSE\_TC}$ ($T_0$) + $dV_{SENSE\_TC}$ / dT * (T - $T_0$) | | | | |
| **$V_{CC}$ supply voltage analog feedback (VN7050AJ only)** | | | | | | |
| $V_{SENSE\_VCC}$ | MultiSense output voltage proportional to $V_{CC}$ supply voltage | $V_{CC}$ = 13 V; $V_{SEn}$ = 5 V; $V_{SEL0}$ = 5 V; $V_{SEL1}$ = 5 V; $V_{IN}$ = 0 V; $R_{SENSE}$ = 1 kΩ | 3.16 | 3.23 | 3.3 | V |
| Transfer function (3) | | $V_{SENSE\_VCC}$ = $V_{CC}$ / 4 | | | | |
| **Fault diagnostic feedback (see *Table 10: "Truth table"*)** | | | | | | |
| $V_{SENSEH}$ | MultiSense output voltage in fault condition | $V_{CC}$ = 13 V; $V_{IN}$ = 0 V; $V_{SEn}$ = 5 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 0 V; $I_{OUT}$ = 0 A; $V_{OUT}$ = 4 V; $R_{SENSE}$ = 1 kΩ; | 5 | | 6.6 | V |
| $I_{SENSEH}$ | MultiSense output current in fault condition | $V_{CC}$ = 13 V; $V_{SENSE}$ = 5 V | 7 | 20 | 30 | mA |
| **MultiSense timings (current sense mode - see *Figure 7: "MultiSense timings (current sense mode)"*)(4)** | | | | | | |
| $t_{DSENSE1H}$ | Current sense settling time from rising edge of SEn | $V_{IN}$ = 5 V; $V_{SEn}$ = 0 V to 5 V; $R_{SENSE}$ = 1 kΩ; $R_L$ = 6.5 Ω | | | 60 | µs |
| $t_{DSENSE1L}$ | Current sense disable delay time from falling edge of SEn | $V_{IN}$ = 5 V; $V_{SEn}$ = 5 V to 0 V; $R_{SENSE}$ = 1 kΩ; $R_L$ = 6.5 Ω | | 5 | 20 | µs |
| $t_{DSENSE2H}$ | Current sense settling time from rising edge of INPUT | $V_{IN}$ = 0 V to 5 V; $V_{SEn}$ = 5 V; $R_{SENSE}$ = 1 kΩ; $R_L$ = 6.5 Ω | | 100 | 250 | µs |
| $\Delta t_{DSENSE2H}$ | Current sense settling time from rising edge of $I_{OUT}$ (dynamic response to a step change of $I_{OUT}$) | $V_{IN}$ = 5 V; $V_{SEn}$ = 5 V; $R_{SENSE}$ = 1 kΩ; $I_{SENSE}$ = 90 % of $I_{SENSEMAX}$; $R_L$ = 6.5 Ω | | | 100 | µs |
| $t_{DSENSE2L}$ | Current sense turn-off delay time from falling edge of INPUT | $V_{IN}$ = 5 V to 0 V; $V_{SEn}$ = 5 V; $R_{SENSE}$ = 1 kΩ; $R_L$ = 6.5 Ω | | 50 | 250 | µs |
| **MultiSense timings (chip temperature sense mode - see *Figure 8: "Multisense timings (chip temperature and VCC sense mode) (VN7050AJ only)"*) (VN7050AJ only)(4)** | | | | | | |
| $t_{DSENSE3H}$ | $V_{SENSE\_TC}$ settling time from rising edge of SEn | $V_{SEn}$ = 0 V to 5 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 5 V; $R_{SENSE}$ = 1 kΩ | | | 60 | µs |
| $t_{DSENSE3L}$ | $V_{SENSE\_TC}$ disable delay time from falling edge of SEn | $V_{SEn}$ = 5 V to 0 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 5 V; $R_{SENSE}$ = 1 kΩ | | | 20 | µs |

| 7 V < $V_{CC}$ < 18 V; -40°C < $T_j$ < 150°C | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Test conditions** | **Min.** | **Typ.** | **Max.** | **Unit** |
| **MultiSense timings ($V_{CC}$ voltage sense mode - see *Figure 8: "Multisense timings (chip temperature and VCC sense mode) (VN7050AJ only)"*) (VN7050AJ only)[(4)]** | | | | | | |
| $t_{DSENSE4H}$ | $V_{SENSE\_VCC}$ settling time from rising edge of SEn | $V_{SEn}$ = 0 V to 5 V; $V_{SEL0}$ = 5 V; $V_{SEL1}$ = 5 V; $R_{SENSE}$ = 1 kΩ | | | 60 | µs |
| $t_{DSENSE4L}$ | $V_{SENSE\_VCC}$ disable delay time from falling edge of SEn | $V_{SEn}$ = 5 V to 0 V; $V_{SEL0}$ = 5 V; $V_{SEL1}$ = 5 V; $R_{SENSE}$ = 1 kΩ | | | 20 | µs |
| **MultiSense timings (Multiplexer transition times) (VN7050AJ only)[(4)]** | | | | | | |
| $t_{D\_CStoTC}$ | MultiSense transition delay from current sense to $T_C$ sense | $V_{IN}$ = 5 V; $V_{SEn}$ = 5 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 0 V to 5 V; $I_{OUT}$ = 1 A; $R_{SENSE}$ = 1 kΩ | | | 60 | µs |
| $t_{D\_TCtoCS}$ | MultiSense transition delay from $T_C$ sense to current sense | $V_{IN}$ = 5 V; $V_{SEn}$ = 5 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 5 V to 0 V; $I_{OUT}$ = 1 A; $R_{SENSE}$ = 1 kΩ | | | 20 | µs |
| $t_{D\_CStoVCC}$ | MultiSense transition delay from current sense to $V_{CC}$ sense | $V_{IN}$ = 5 V; $V_{SEn}$ = 5 V; $V_{SEL0}$ = 5 V; $V_{SEL1}$ = 0 V to 5 V; $I_{OUT}$ = 1 A; $R_{SENSE}$ = 1 kΩ | | | 60 | µs |
| $t_{D\_VCCtoCS}$ | MultiSense transition delay from $V_{CC}$ sense to current sense | $V_{IN}$ = 5 V; $V_{SEn}$ = 5 V; $V_{SEL0}$ = 5 V; $V_{SEL1}$ = 5 V to 0 V; $I_{OUT}$ = 1 A; $R_{SENSE}$ = 1 kΩ | | | 20 | µs |
| $t_{D\_TCtoVCC}$ | MultiSense transition delay from $T_C$ sense to $V_{CC}$ sense | $V_{CC}$ = 13 V; $T_j$ = 125°C; $V_{SEn}$ = 5 V; $V_{SEL0}$ = 0 V to 5 V; $V_{SEL1}$ = 5 V; $R_{SENSE}$ = 1 kΩ | | | 20 | µs |
| $t_{D\_VCCtoTC}$ | MultiSense transition delay from $V_{CC}$ sense to $T_C$ sense | $V_{CC}$ = 13 V; $T_j$ = 125°C; $V_{SEn}$ = 5 V; $V_{SEL0}$ = 5 V to 0 V; $V_{SEL1}$ = 5 V; $R_{SENSE}$ = 1 kΩ | | | 20 | µs |

**Notes:**

(1)Parameter specified by design; not subjected to production test.

(2)All values refer to $V_{CC}$ = 13 V; $T_j$ = 25°C, unless otherwise specified.

(3)$V_{CC}$ sensing and $T_C$ are referred to GND potential.

(4)Transition delay are measured up to +/- 10% of final conditions.

Figure 4: IOUT/ISENSE versus IOUT

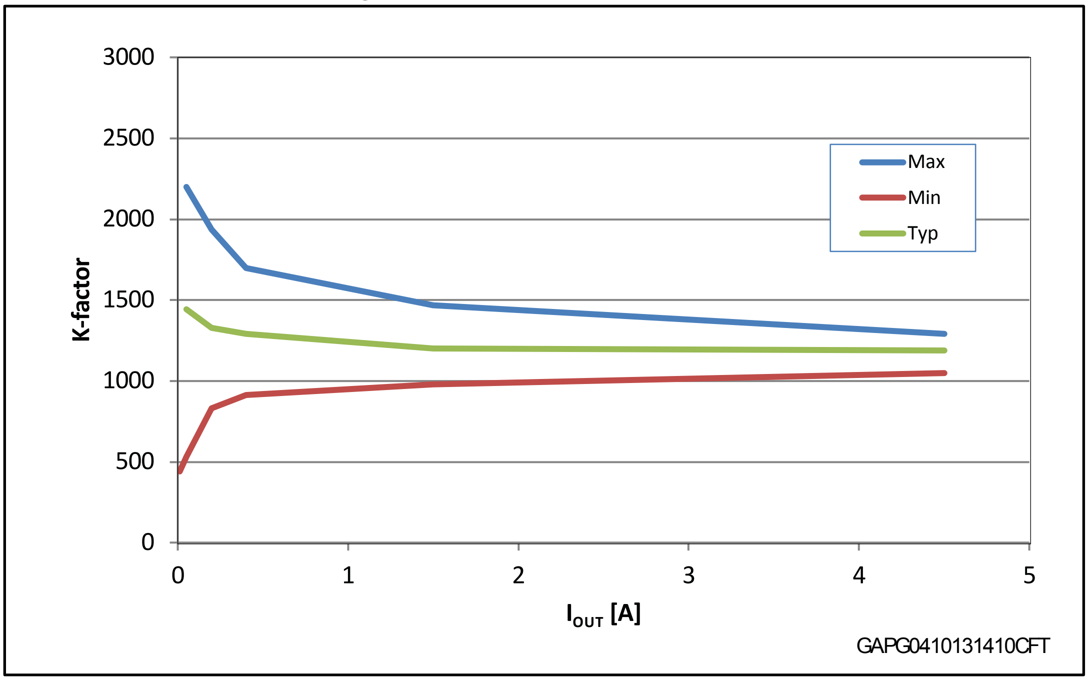



Figure 5: Current sense accuracy versus IOUT

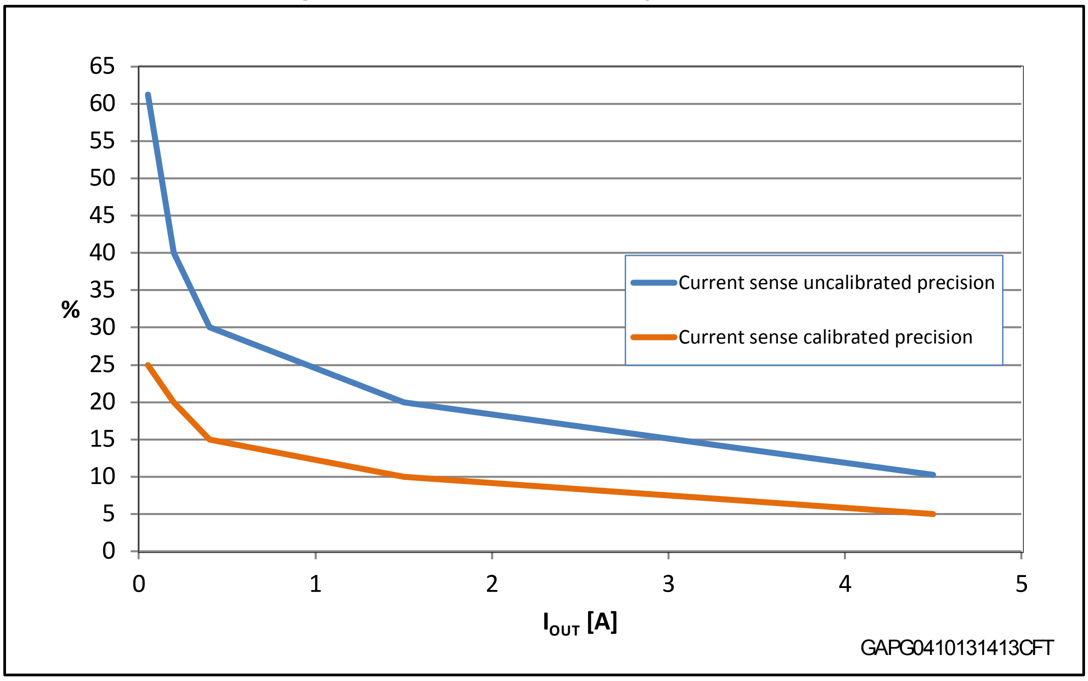


**Figure 6: Switching time and Pulse skew**

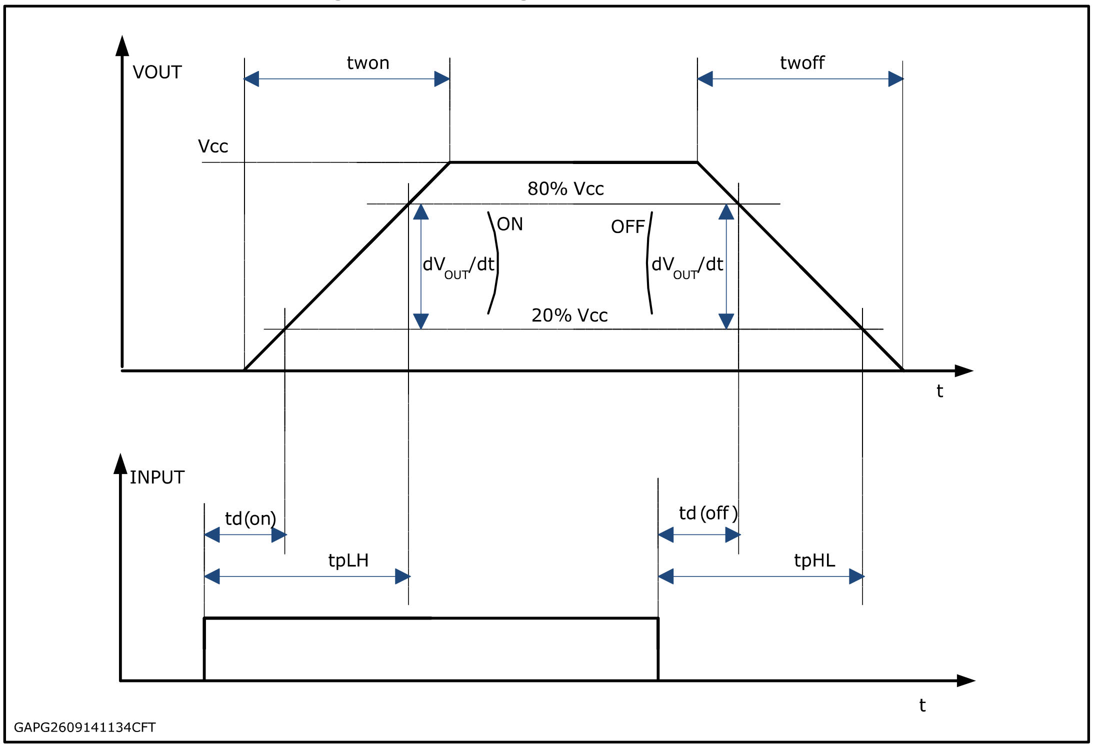



**Figure 7: MultiSense timings (current sense mode)**

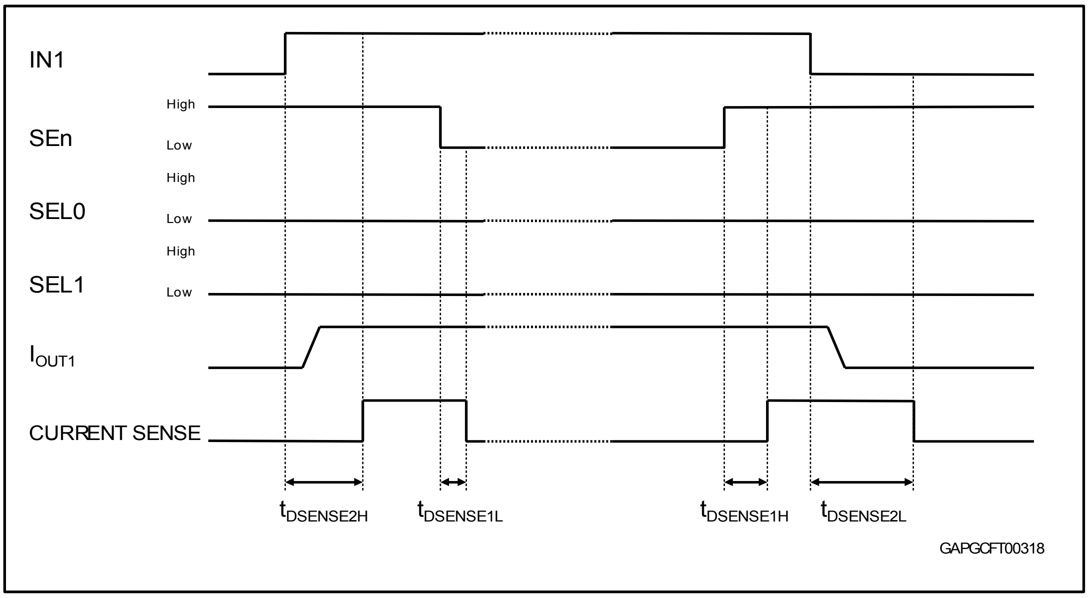


**Figure 8: Multisense timings (chip temperature and VCC sense mode) (VN7050AJ only)**

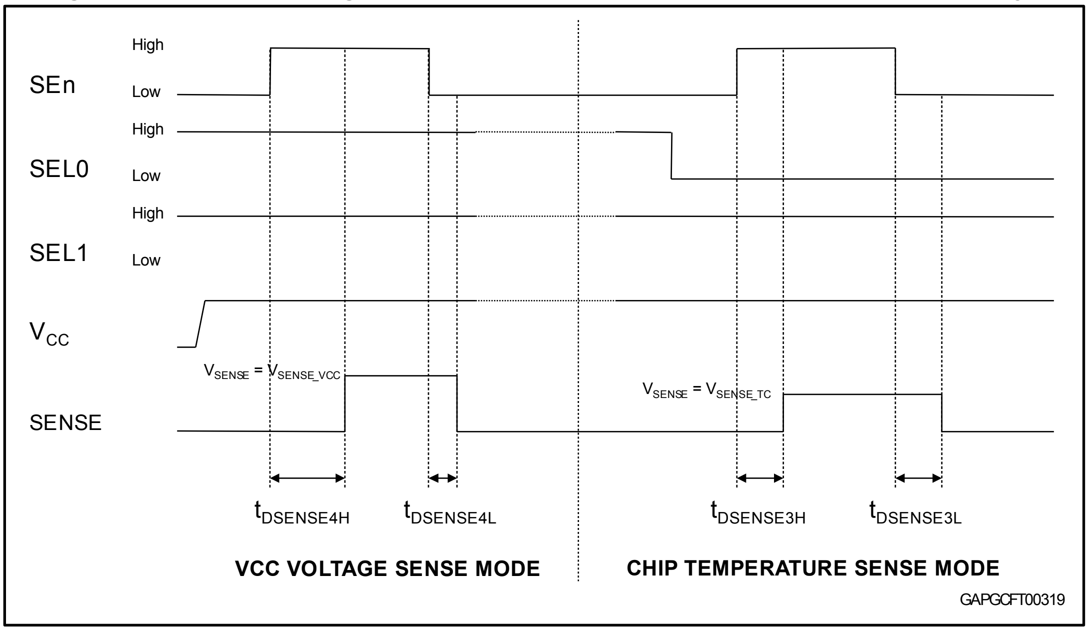



**Figure 9: TDSTKON**

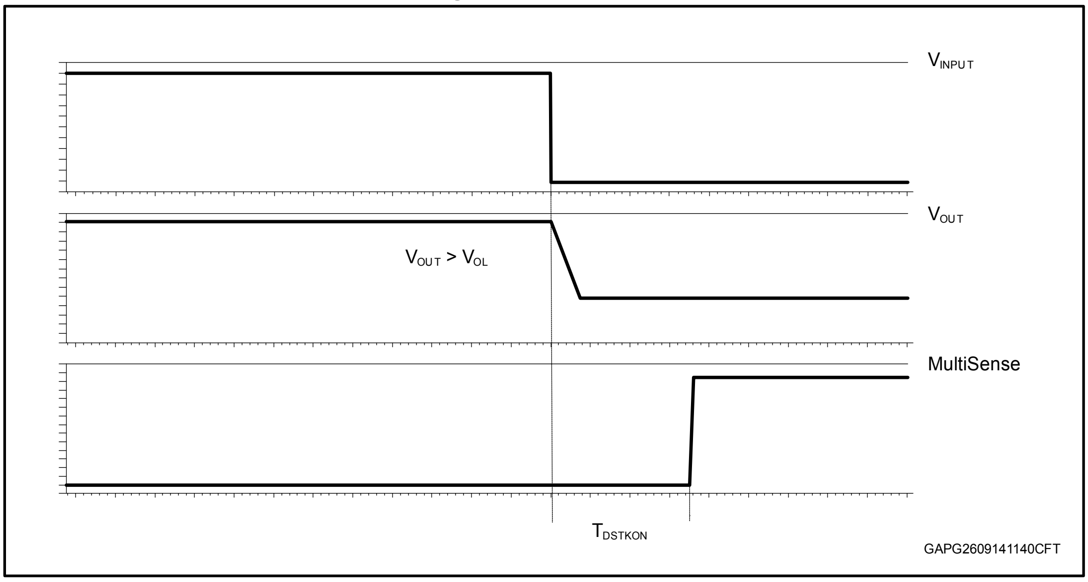



**Table 10: Truth table**

| Mode | Conditions | $IN_X$ | FR(1) | SEn | $SEL_X$(1) | $OUT_X$ | MultiSense | Comments |
|---|---|---|---|---|---|---|---|---|
| Standby | All logic inputs low | L | L | L | L | L | Hi-Z | Low quiescent current consumption |
| Normal | Nominal load connected; $T_j$ < 150 °C | L | X | See (2) | | L | See (2) | |
| | | H | L | | | H | See (2) | Outputs configured for auto-restart |

| Mode | Conditions | INx | FR[1] | SEn | SELx[1] | OUTx | MultiSense | Comments |
|---|---|---|---|---|---|---|---|---|
| | | H | H | | | H | See [2] | Outputs configured for latch-off[1] |
| Overload | Overload or short to GND causing: $T_j > T_{TSD}$ or $\Delta T_j > \Delta T_{j\_SD}$ | L | X | See [2] | | L | See [2] | |
| | | H | L | | | H | See [2] | Output cycles with temperature hysteresis |
| | | H | H | | | L | See [2] | Output latches-off[1] |
| Undervoltage | $V_{CC} < V_{USD}$ (falling) | X | X | X | X | L<br>L | Hi-Z<br>Hi-Z | Re-start when $V_{CC} > V_{USD} + V_{USDhyst}$ (rising) |
| OFF-state diagnostics | Short to $V_{CC}$ | L | X | See [2] | | H | See [2] | |
| | Open-load | L | X | | | H | See [2] | External pull-up |
| Negative output voltage | Inductive loads turn-off | L | X | See [2] | | < 0 V | See [2] | |

**Notes:**

[1]VN7050AJ only

[2]Refer to *Table 11: "MultiSense multiplexer addressing"*

**Table 11: MultiSense multiplexer addressing**

| SEn | $SEL_1$ | $SEL_0$ | MUX channel | MultiSense output | | | |
|---|---|---|---|---|---|---|---|
| | | | | Normal mode | Overload | OFF-state diag. [1] | Negative output |
| SO-8 | | | | | | | |
| L | N.A. | N.A. | N.A. | Hi-Z | | | |
| H | N.A. | N.A. | Channel diagnostic | $I_{SENSE}$ = 1/K * $I_{OUT}$ | $V_{SENSE} = V_{SENSEH}$ | $V_{SENSE} = V_{SENSEH}$ | Hi-Z |
| PowerSSO-16 | | | | | | | |
| H | L | L | Channel diagnostic | $I_{SENSE}$ = 1/K * $I_{OUT}$ | $V_{SENSE} = V_{SENSEH}$ | $V_{SENSE} = V_{SENSEH}$ | Hi-Z |
| H | L | H | Channel diagnostic | $I_{SENSE}$ = 1/K * $I_{OUT}$ | $V_{SENSE} = V_{SENSEH}$ | $V_{SENSE} = V_{SENSEH}$ | Hi-Z |
| H | H | L | $T_{CHIP}$ Sense | $V_{SENSE} = V_{SENSE\_TC}$ | | | |
| H | H | H | $V_{CC}$ Sense | $V_{SENSE} = V_{SENSE\_VCC}$ | | | |

**Notes:**

[1]In case the output channel corresponding to the selected MUX channel is latched off while the relevant input is low, Multisense pin delivers feedback according to OFF-State diagnostic. Example 1: FR = 1; IN = 0; OUT = L (latched); MUX channel = channel 0 diagnostic; Mutisense = 0. Example 2: FR = 1; IN = 0; OUT = latched, $V_{OUT} > V_{OL}$; MUX channel = channel 0 diagnostic; Mutisense = $V_{SENSEH}$

## 2.4 Waveforms

**Figure 10: Latch functionality - behavior in hard short circuit condition (TAMB << TTSD)**

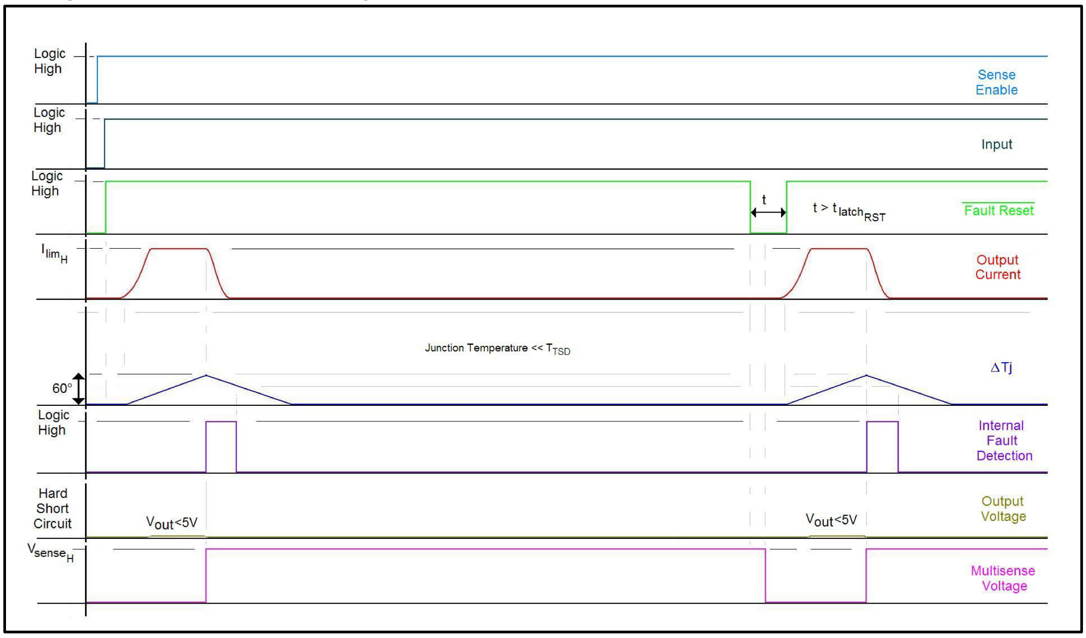



**Figure 11: Latch functionality - behavior in hard short circuit condition**

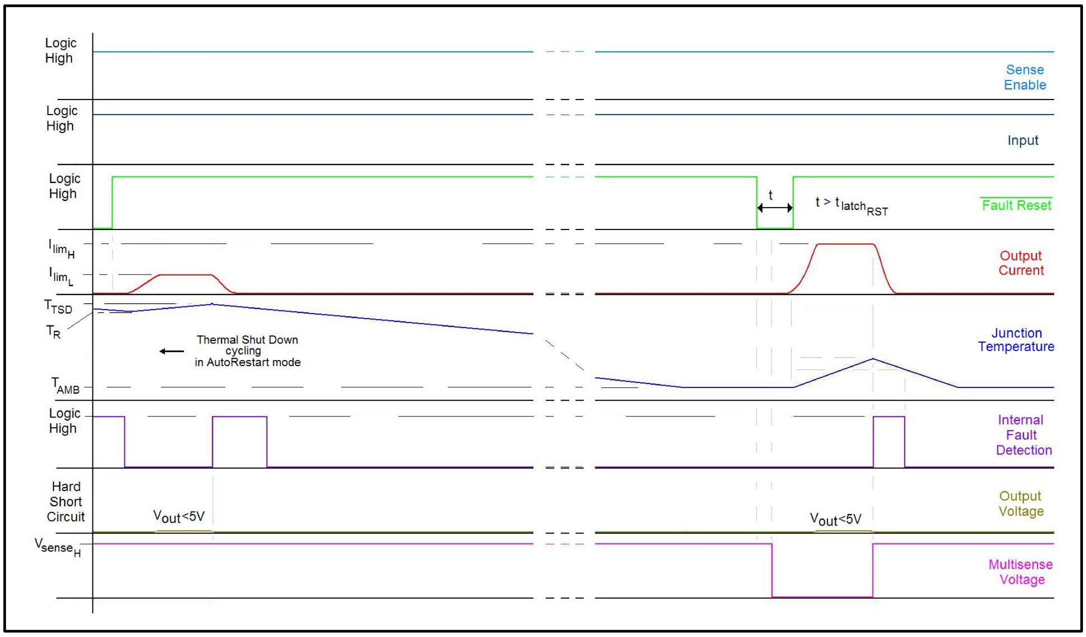


Figure 12: Latch functionality - behavior in hard short circuit condition (autorestart mode + latch off)

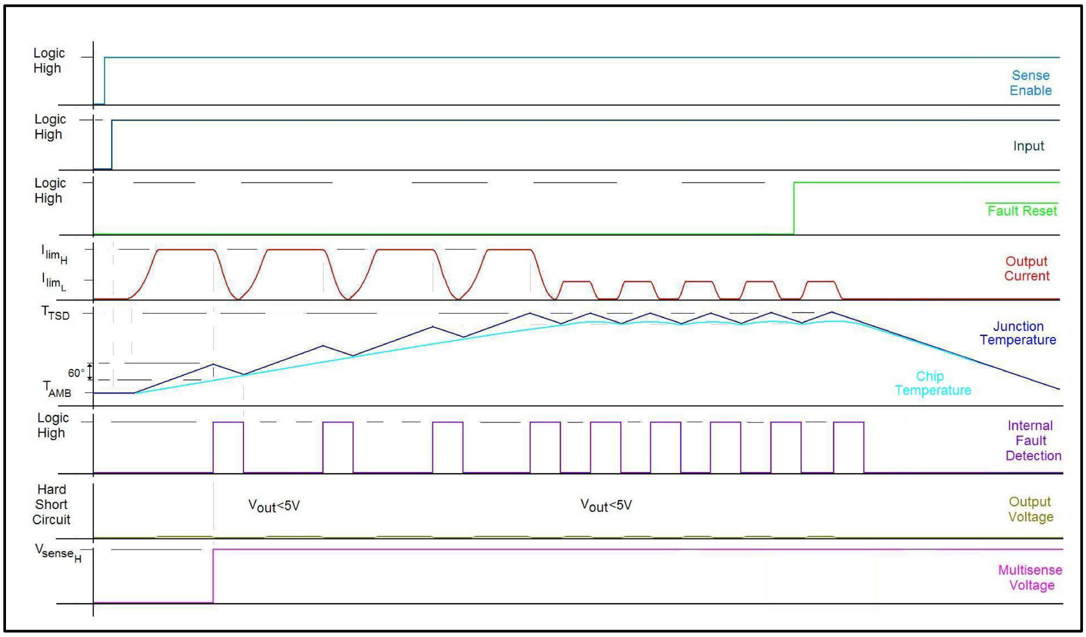



Figure 13: Standby mode activation

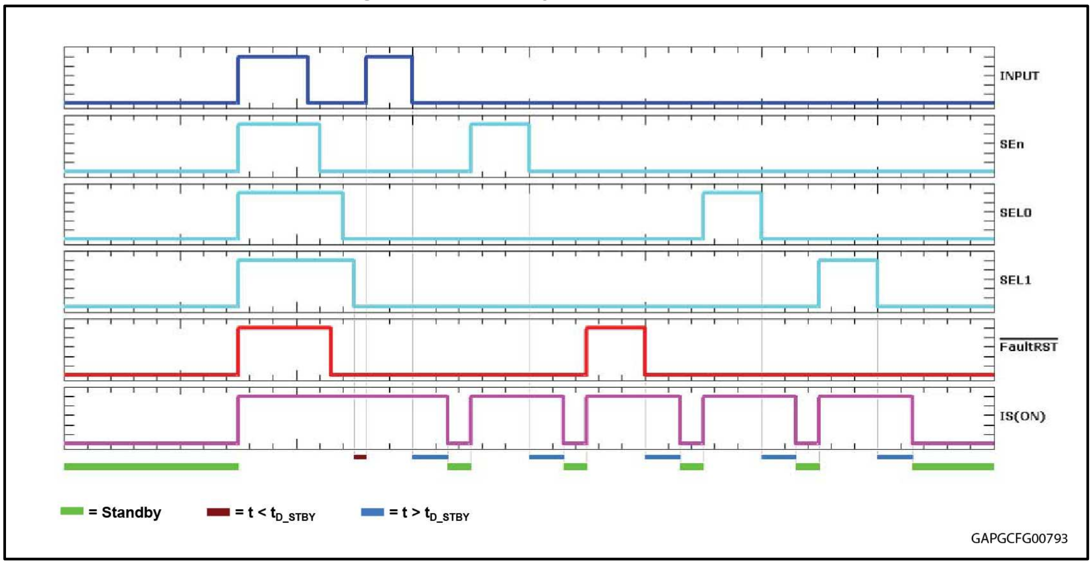
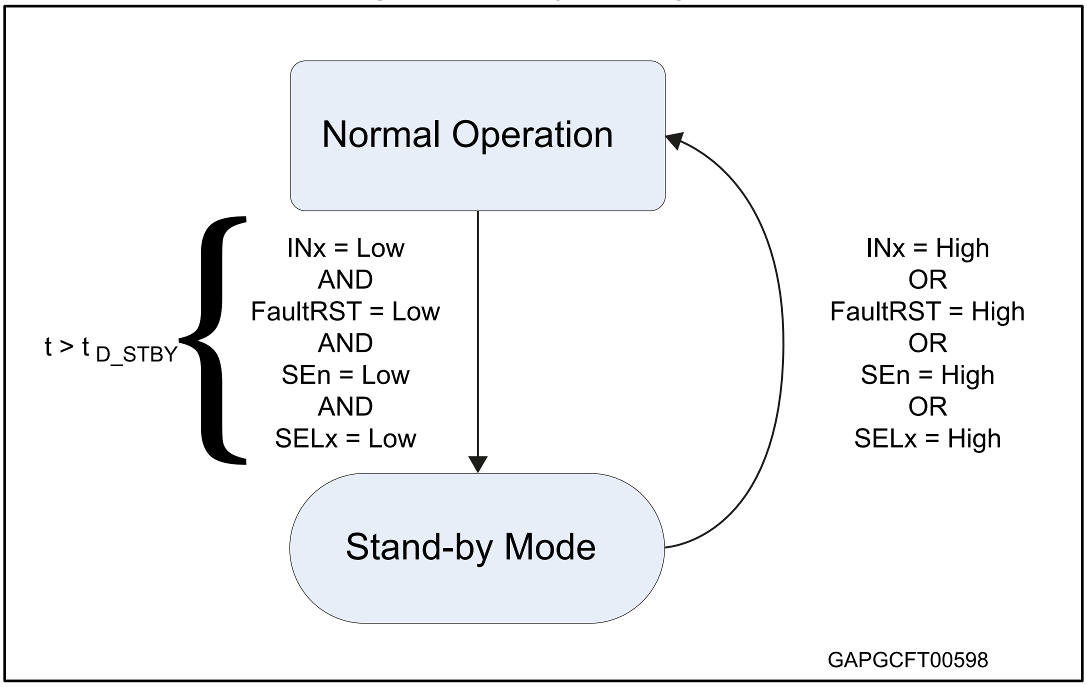


**Figure 14: Standby state diagram**




## 2.5 Electrical characteristics curves

**Figure 15: OFF-state output current**

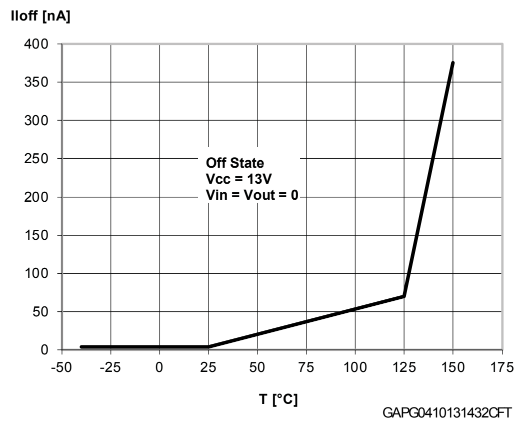



**Figure 16: Standby current**

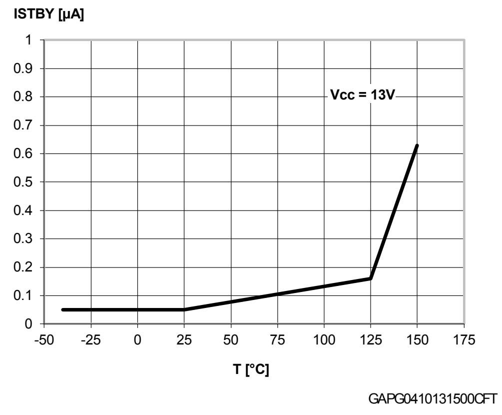


**Figure 17: IGND(ON) vs. Tcase**

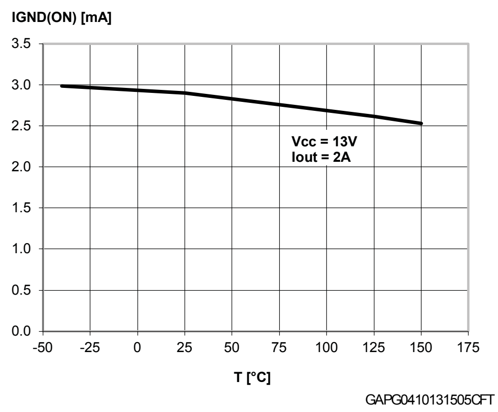



**Figure 18: Logic Input high level voltage**

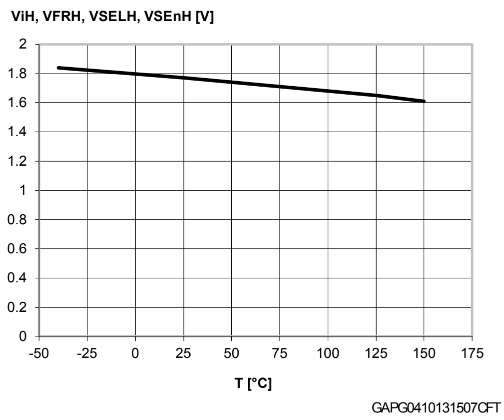



**Figure 19: Logic Input low level voltage**

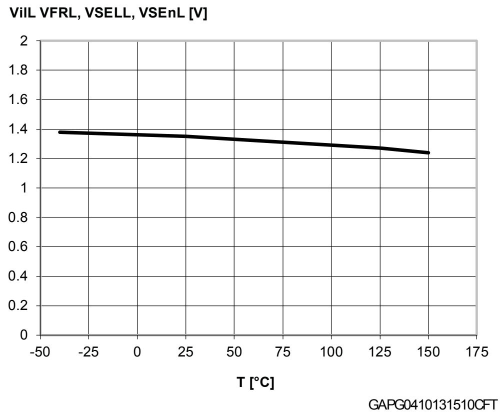



**Figure 20: High level logic input current**

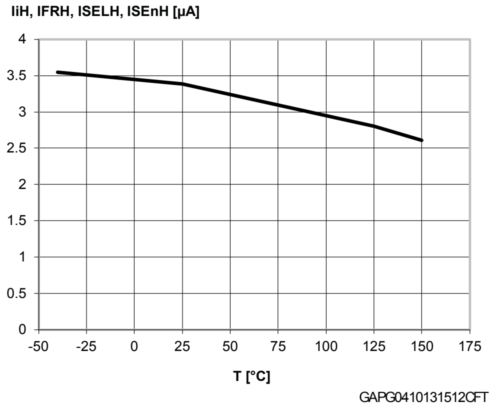



**Figure 21: Low level logic input current**

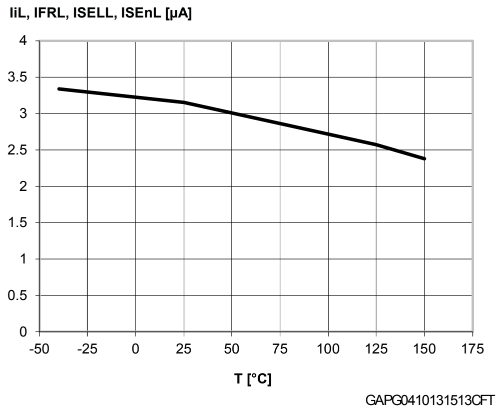



**Figure 22: Logic Input hysteresis voltage**