Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

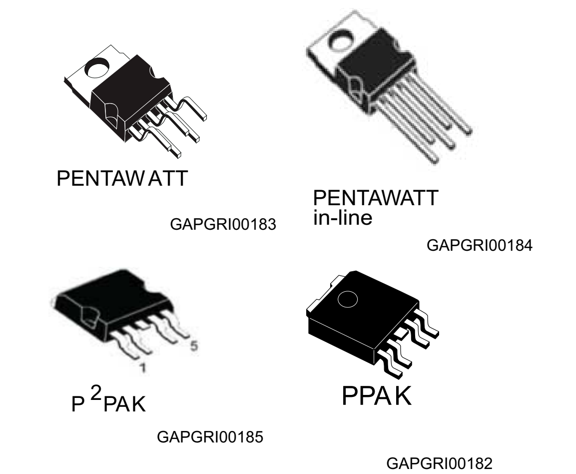
High-side driver

Datasheet — production data

Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN750-E VN750PT-E VN750B5-E VN750-12-E	60 mΩ	6 A	36 V

- ECOPACK®: lead free and RoHS compliant
- Automotive Grade: compliance with AEC guidelines
- CMOS compatible input
- On-state open-load detection
- Off-state open-load detection
- Shorted load protection
- Undervoltage and overvoltage shutdown
- Protection against loss of ground
- Very low standby current
- Reverse battery protection



Description

The VN750-E is a monolithic device designed in STMicroelectronics® VIPower® M0-3 technology intended for driving any kind of load with one side connected to ground.

Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). Active current limitation combined with thermal shutdown and automatic restart help protect the device against overload.

The device detects open load condition in on-state and off-state. Output shorted to V_{CC} is detected in the off-state. Device automatically turns off in case of ground pin disconnection.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PENTAWATT	VN750-E	-
P^2PAK	VN750B5-E	VN750B5TR-E
PPAK	VN750PT-E	VN750PTTR-E
PENTAWATT in-line	VN750-12-E	-

This is information on a product in full production. www.st.com

Contents

1 Block diagram and pin description 5

2 Electrical specifications 6

2.1 Absolute maximum ratings 6

2.2 Thermal data 7

2.3 Electrical characteristics 7

2.4 Electrical characteristics curves 13

2.5 GND protection network against reverse battery 16

2.5.1 Solution 1: resistor in the ground line (RGND only) 16

2.5.2 Solution 2: diode (DGND) in the ground line 17

2.6 Load dump protection 17

2.7 Microcontroller I/Os protection 17

2.8 Open-load detection in off-state 17

2.9 PPAK/P^{2}PAK maximum demagnetization energy (VCC=13.5V) 19

3 Package and PCB thermal data 20

3.1 P^{2}PAK thermal data 20

3.2 PPAK thermal data 22

4 Package and packing information 25

4.1 ECOPACK® packages 25

4.2 PENTAWATT mechanical data 25

4.2.1 PENTAWATT (in-line) mechanical data 27

4.3 P^{2}PAK mechanical data 29

4.4 PPAK mechanical data 31

4.5 PENTAWATT packing information 33

4.6 P^{2}PAK packing information 33

4.7 PPAK packing information 35

5 Revision history 37

List of tables

Table 1. Device summary 1
Table 2. Suggested connections for unused and not connected pins 5
Table 3. Absolute maximum ratings 6
Table 4. Thermal data. 7
Table 5. Electrical characteristics 7
Table 6. Truth table. 10
Table 7. Electrical transient requirements on V_{CC} pin (part 1/3). 10
Table 8. Electrical transient requirements on V_{CC} pin (part 2/3). 11
Table 9. Electrical transient requirements on V_{CC} pin (part 3/3). 11
Table 10. P^2PAK thermal parameter 22
Table 11. PPAK thermal parameter 24
Table 12. PENTAWATT mechanical data 25
Table 13. PENTAWATT (in-line) mechanical data 27
Table 14. P^2PAK mechanical data 30
Table 15. PPAK mechanical data. 32
Table 16. Document revision history 37

List of figures

Figure 1. Block diagram . . . 5
Figure 2. Configuration diagram (top view) . . . 5
Figure 3. Current and voltage conventions . . . 6
Figure 4. Status timings . . . 9
Figure 5. Switching time waveforms . . . 10
Figure 6. Waveforms . . . 12
Figure 7. Off-state output current . . . 13
Figure 8. High level input current . . . 13
Figure 9. Input clamp voltage . . . 13
Figure 10. Status leakage current . . . 13
Figure 11. Status low output voltage . . . 13
Figure 12. Status clamp voltage . . . 13
Figure 13. On-state resistance Vs T_{case} . . . 14
Figure 14. On-state resistance Vs V_{CC} . . . 14
Figure 15. Open-load on-state detection threshold . . . 14
Figure 16. Input high level . . . 14
Figure 17. Input low level . . . 14
Figure 18. Input hysteresis voltage . . . 14
Figure 19. Overvoltage shutdown . . . 15
Figure 20. Open-load off-state voltage detection threshold . . . 15
Figure 21. Turn-on voltage slope . . . 15
Figure 22. Turn-off voltage slope . . . 15
Figure 23. I_{lim} Vs T_{case} . . . 15
Figure 24. Application schematic . . . 16
Figure 25. Open-load detection in off-state . . . 18
Figure 26. PPAK /P^2PAK maximum turn-off current versus inductance . . . 19
Figure 27. P^2PAK PC board . . . 20
Figure 28. P^2PAK Rthj-amb Vs. PCB copper area in open box free air condition . . . 20
Figure 29. P^2PAK thermal impedance junction ambient single pulse . . . 21
Figure 30. P^2PAK thermal fitting model of a single channel . . . 21
Figure 31. PPAK PC board . . . 22
Figure 32. PPAK Rthj-amb Vs. PCB copper area in open box free air condition . . . 23
Figure 33. PPAK thermal impedance junction ambient single pulse . . . 23
Figure 34. PPAK thermal fitting model of a single channel . . . 24
Figure 35. PENTAWATT package dimensions . . . 25
Figure 36. PENTAWATT (in-line) package dimensions . . . 27
Figure 37. P^2PAK package dimensions . . . 29
Figure 38. PPAK package dimensions . . . 31
Figure 39. PENTAWATT tube shipment (no suffix) . . . 33
Figure 40. P^2PAK tube shipment (no suffix) . . . 33
Figure 41. P^2PAK tape and reel (suffix “13TR”) . . . 34
Figure 42. PPAK suggested pad layout . . . 35
Figure 43. PPAK tube shipment (no suffix) . . . 35
Figure 44. PPAK tape and reel . . . 36

1 Block diagram and pin description

Figure 1. Block diagram

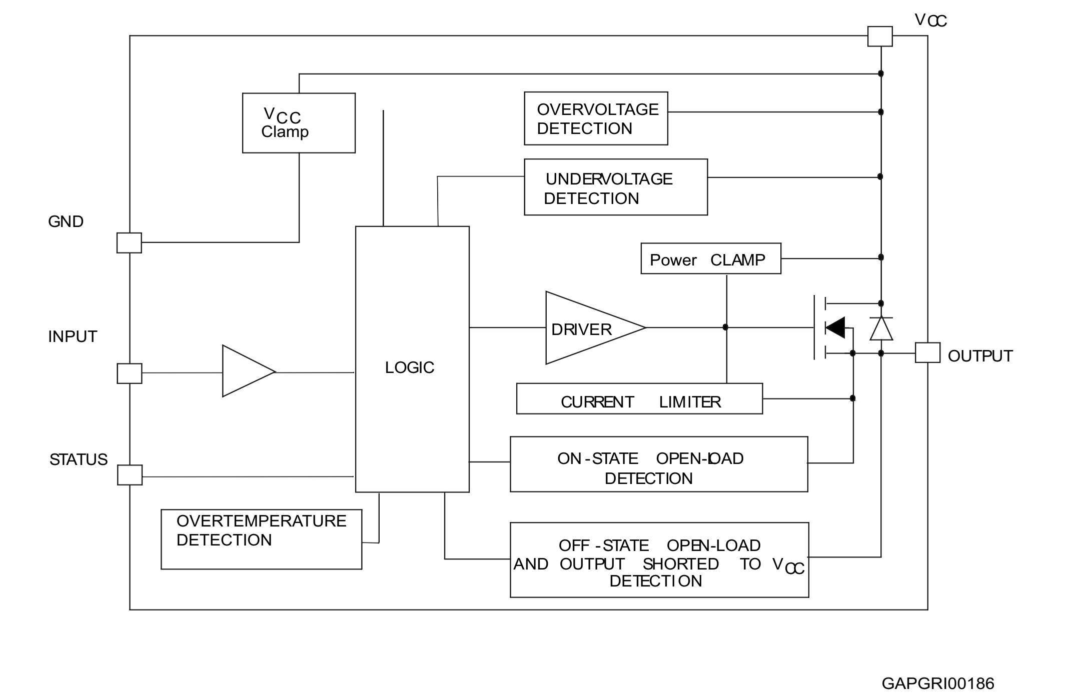


Figure 2. Configuration diagram (top view)

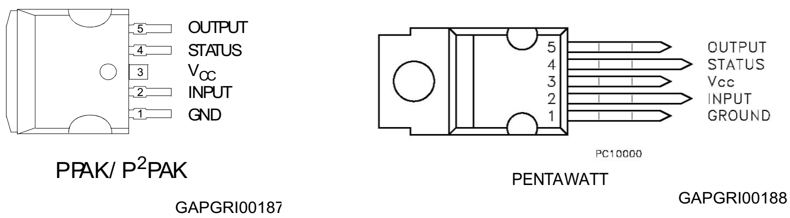
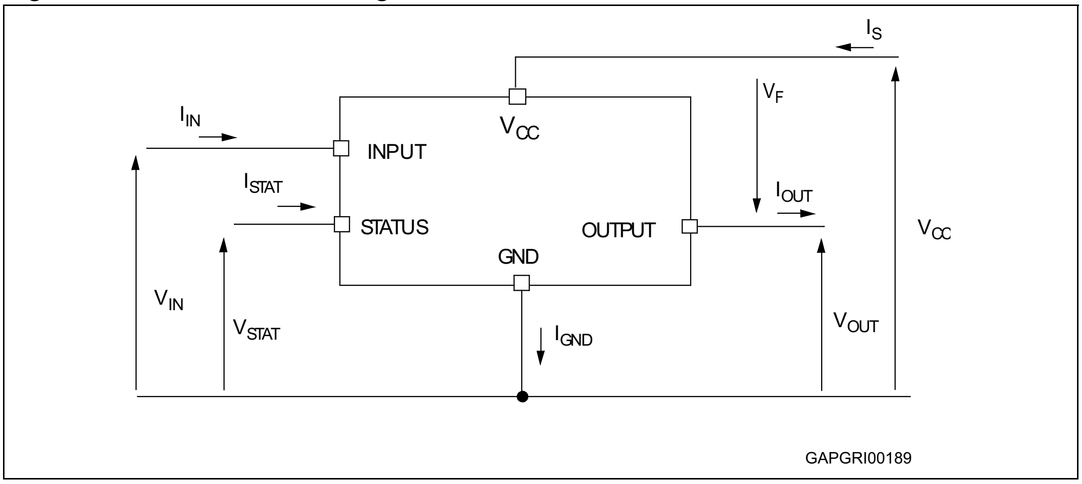


Table 2. Suggested connections for unused and not connected pins

Connection/pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground		X		Through 10 KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stress values that exceed those listed in the "Absolute maximum ratings" table can cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions greater than those, indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics sure program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		PENTAWATT	P^2PAK	PPAK	
V_{CC}	DC supply voltage	41			V
$-V_{CC}$	Reverse DC supply voltage	- 0.3			V
$-I_{gnd}$	DC reverse ground pin current	- 200			mA
I_{OUT}	DC output current	Internally limited			A
$-I_{OUT}$	Reverse DC output current	- 6			A
I_{IN}	DC input current	+/- 10			mA
I_{STAT}	DC status current	+/- 10			mA
V_{ESD}	Electrostatic discharge (human body model: R=1.5 KΩ; C=100pF) - Input - Status - Output - V_{CC}	 4000 4000 5000 5000			 V V V V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value			Unit
		PENTAWATT	P^2PAK	PPAK	
E_{MAX}	Maximum switching energy (L=2.46 mH; R_L=0 Ω; V_{bat}=13.5 V; T_{jstart}=150 °C; I_L=9 A)		138	138	mJ
P_{tot}	Power dissipation T_C=25°C	60			W
T_j	Junction operating temperature	Internally limited			°C
T_c	Case operating temperature	- 40 to 150			°C
T_{stg}	Storage temperature	- 55 to 150			°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value			Unit
		PENTAWATT	P^2PAK	PPAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.1	2.1	2.1	°C/W
$R_{thj\text{-}lead}$	Thermal resistance junction-lead	-	-	-	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.1	52.1(1)	77.1(1)	°C/W
		62.1	37(2)	44(2)	°C/W

1. When mounted on a standard single-sided FR-4 board with 0.5cm^2 of Cu (at least 35µm thick). Horizontal mounting and no artificial air flow.
2. When mounted on a standard single-sided FR-4 board with 6cm^2 of Cu (at least 35µm thick). Horizontal mounting and no artificial air flow.

2.3 Electrical characteristics

Values specified in this section are for 8 V<V_{CC}<36 V; -40 °C< Tj <150 °C, unless otherwise stated.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Power						
V_{CC}	Operating supply voltage		5.5	13	36	V
V_{USD}	Undervoltage shutdown		3	4	5.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
V_{OV}	Overvoltage shutdown		36			V
R_{ON}	On-state resistance	I_{OUT}=2 A; T_j=25 °C; V_{CC}> 8 V I_{OUT}=2 A; V_{CC}>8 V			60 120	mΩ mΩ

Table 5. **Electrical characteristics (continued)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Supply current	Off-state; V_{CC}=13 V; V_{IN}=V_{OUT}=0 V Off-state; V_{CC}=13 V; V_{IN}=V_{OUT}=0 V; T_j=25 °C On-state; V_{CC}=13 V; V_{IN}=5 V; I_{OUT}=0 A		10 10 2	25 20 3.5	µA µA mA
$I_{L(off1)}$	Off-state output current	V_{IN}=V_{OUT}=0 V	0		50	µA
$I_{L(off2)}$	Off-state output current	V_{IN}=0V; V_{OUT}=3.5 V	-75		0	µA
$I_{L(off3)}$	Off-state output current	V_{IN}=V_{OUT}=0 V; Vcc=13 V; T_j =125 °C			5	µA
$I_{L(off4)}$	Off-state output current	V_{IN}=V_{OUT}=0 V; Vcc=13 V; T_j =25 °C			3	µA
Switching (V_{CC}=13 V)						
$t_{d(on)}$	Turn-on delay time	R_L=6.5 Ω from V_{IN} rising edge to V_{OUT}=1.3 V		40		µs
$t_{d(off)}$	Turn-off delay time	R_L=6.5 Ω from V_{IN} falling edge to V_{OUT}=11.7 V		30		µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L=6.5 Ω from V_{OUT}=1.3 V to V_{OUT}=10.4 V		See *Figure 21.*		V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L=6.5 Ω from V_{OUT}=11.7 V to V_{OUT}=1.3 V		See *Figure 22.*		V/µs
Input pin						
V_{IL}	Input low level				1.25	V
I_{IL}	Low level input current	V_{IN}=1.25 V	1			µA
V_{IH}	Input high level		3.25			V
I_{IH}	High level input current	V_{IN}=3.25 V			10	µA
V_{hyst}	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	I_{IN}=1 mA I_{IN}=-1 mA	6	6.8 -0.7	8	V V
V_{CC} output diode						
V_F	Forward on voltage	$-I_{OUT}$=1.3 A; T_j=150 °C			0.6	V
Status pin						
V_{STAT}	Status low output voltage	I_{STAT}=1.6 mA			0.5	V
I_{LSTAT}	Status leakage current	Normal operation; V_{STAT}=5 V			10	µA
C_{STAT}	Status pin input capacitance	Normal operation; V_{STAT}=5 V			100	pF
V_{SCL}	Status clamp voltage	I_{STAT}=1mA I_{STAT}=-1mA	6	6.8 -0.7	8	V V
Protections(1)						
T_{TSD}	Shutdown temperature		150	175	200	°C

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_R	Reset temperature		135			°C
T_{hyst}	Thermal hysteresis		7	15		°C
t_{SDL}	Status delay in overload condition	$T_j > T_{jsh}$			20	ms
I_{lim}	Current limitation	9 V<V_{CC}<36 V 5 V<V_{CC}<36 V	6	9	15 15	A A
V_{demag}	Turn-off output clamp voltage	I_{OUT}=2 A; V_{IN}=0 V; L=6 mH	V_{CC}-41	V_{CC}-48	V_{CC}-55	V
Open-load detection						
I_{OL}	Open-load on state detection threshold	V_{IN}= 5 V	50		200	mA
$t_{DOL(on)}$	Open-load on state detection delay	I_{OUT}= 0 A			200	µs
V_{OL}	Open-load off state voltage detection threshold	V_{IN}= 0 V	1.5		3.5	V
$t_{DOL(off)}$	Open-load detection delay at turn-off				1000	µs

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device operates under abnormal conditions this software must limit the duration and number of activation cycles.

Figure 4. Status timings

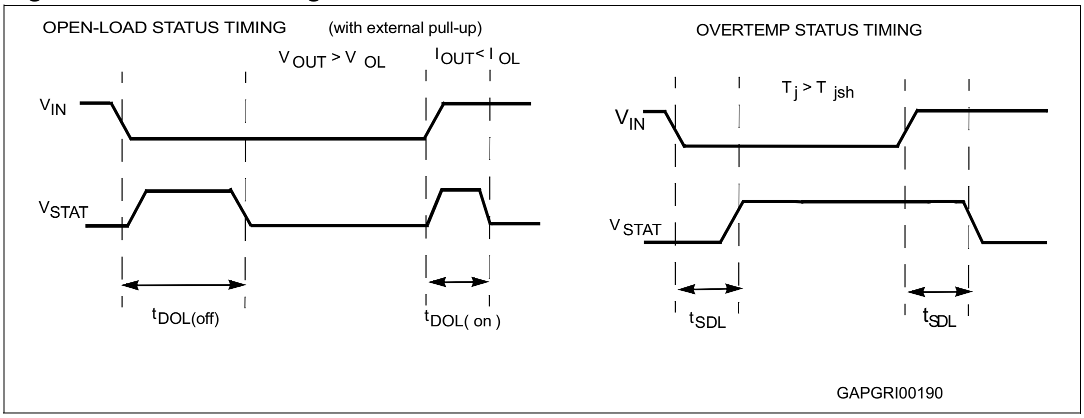


Figure 5. Switching time waveforms

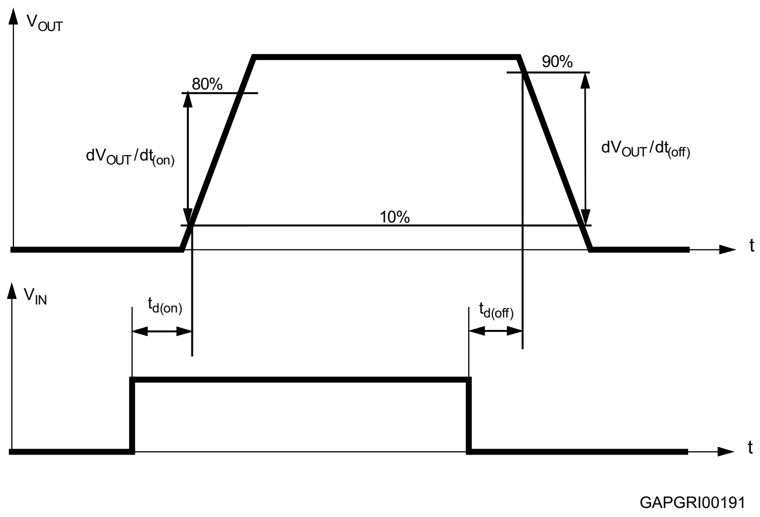


Table 6. Truth table

Conditions	Input	Output	Status
Normal operation	L H	L H	H H
Current limitation	L H H	L X X	H ($T_j < T_{TSD}$) H ($T_j > T_{TSD}$) L
Over temperature	L H	L L	H L
Undervoltage	L H	L L	X X
Overvoltage	L H	L L	H H
Output voltage > V_{OL}	L H	H H	L H
Output current < I_{OL}	L H	L H	H L

Table 7. Electrical transient requirements on V_{CC} pin (part 1/3)

ISO T/R 7637/1 test pulse	Test levels				
	I	II	III	IV	Delays and impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 µs 50 Ω

Table 7. Electrical transient requirements on V_{CC} pin (part 1/3) (continued)

ISO T/R 7637/1 test pulse	Test levels				
	I	II	III	IV	Delays and impedance
3b	+25 V	+50 V	+75 V	+100 V	0.1 µs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

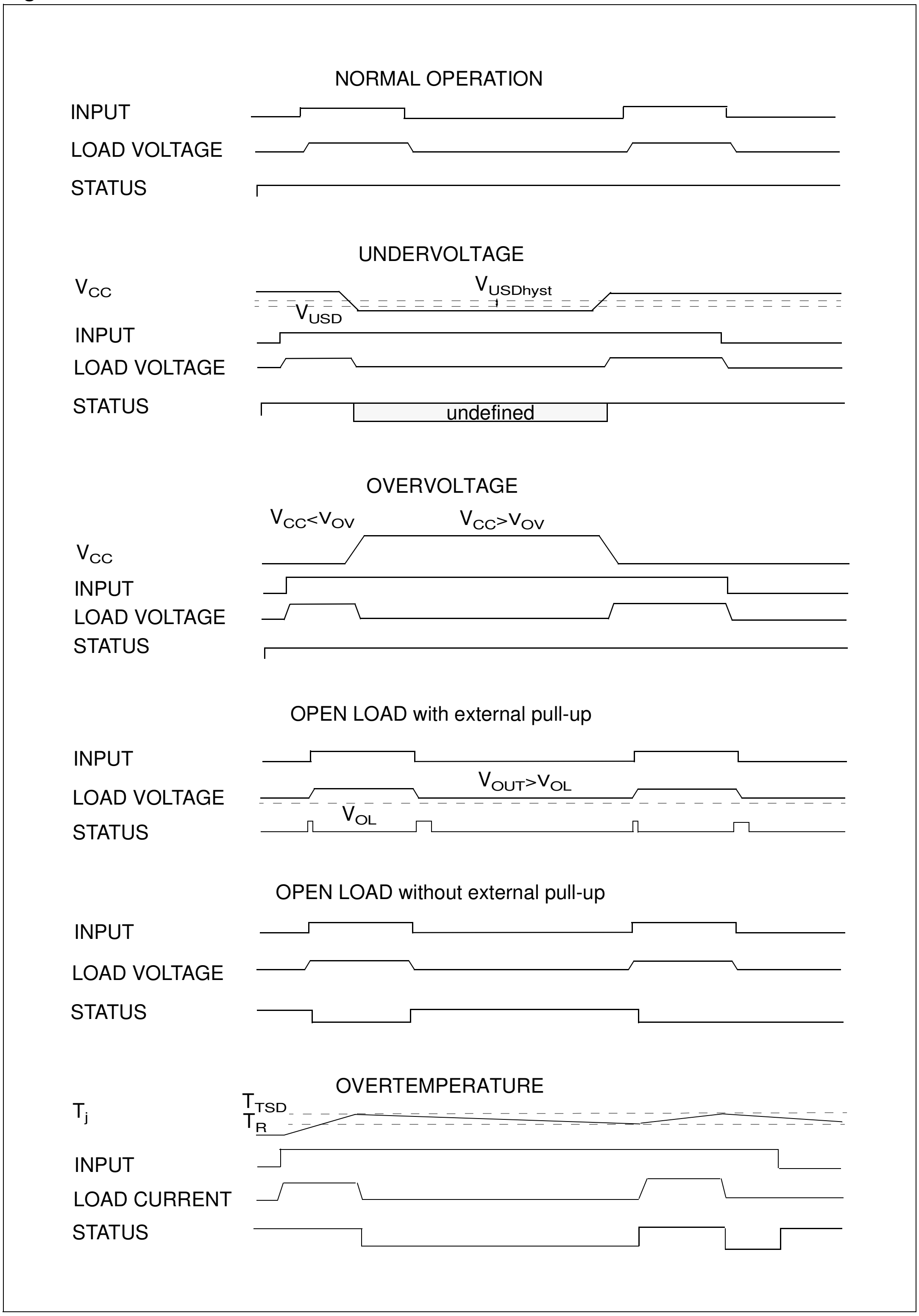
Table 8. Electrical transient requirements on V_{CC} pin (part 2/3)

ISO T/R 7637/1 test pulse	Test levels results			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Table 9. Electrical transient requirements on V_{CC} pin (part 3/3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 6. Waveforms



2.4 Electrical characteristics curves

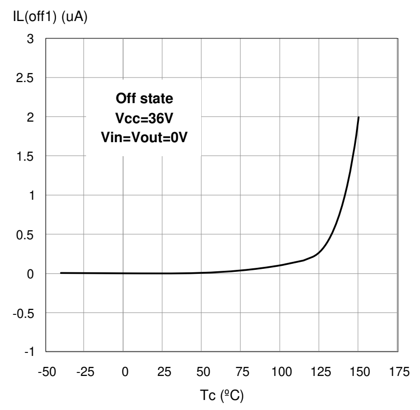


Figure 7. Off-state output current

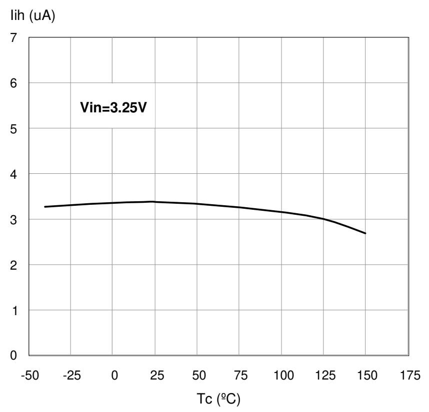


Figure 8. High level input current

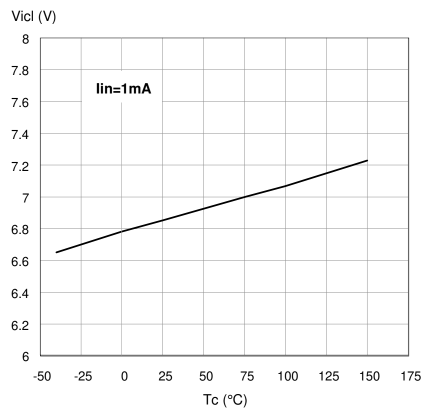


Figure 9. Input clamp voltage

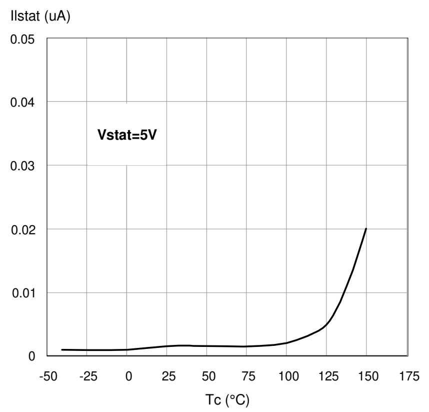


Figure 10. Status leakage current

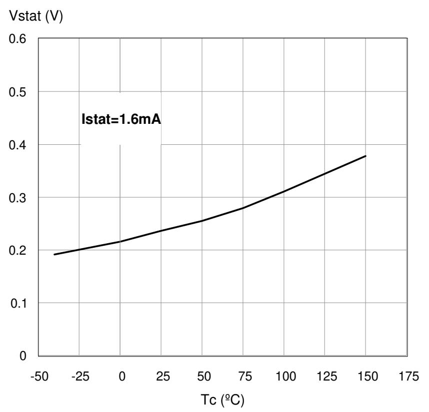


Figure 11. Status low output voltage

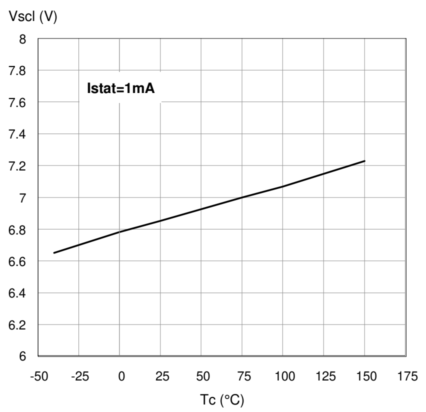


Figure 12. Status clamp voltage

Figure 13. On-state resistance Vs T_{case}

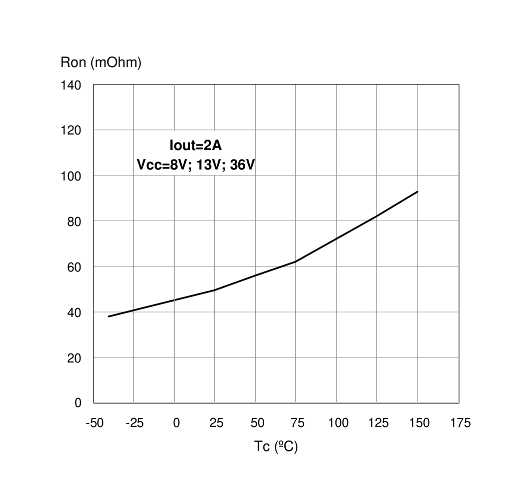


Figure 14. On-state resistance Vs V_{CC}

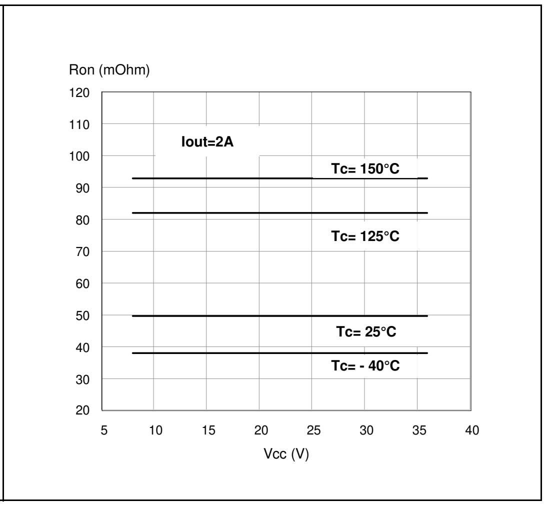


Figure 15. Open-load on-state detection threshold

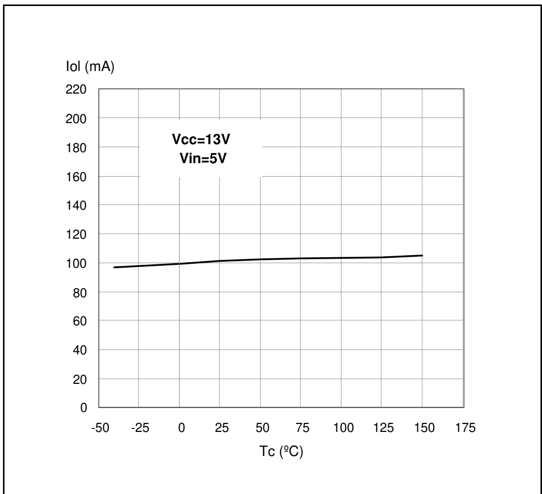


Figure 16. Input high level

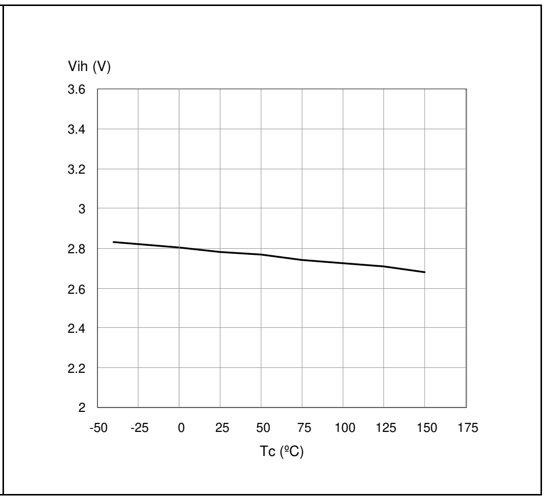


Figure 17. Input low level

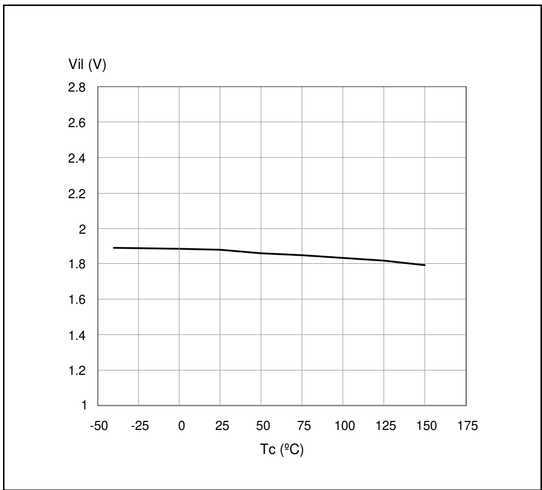


Figure 18. Input hysteresis voltage

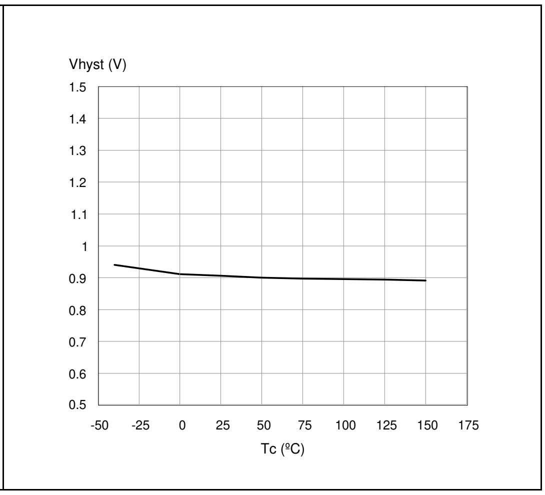


Figure 19. Overvoltage shutdown

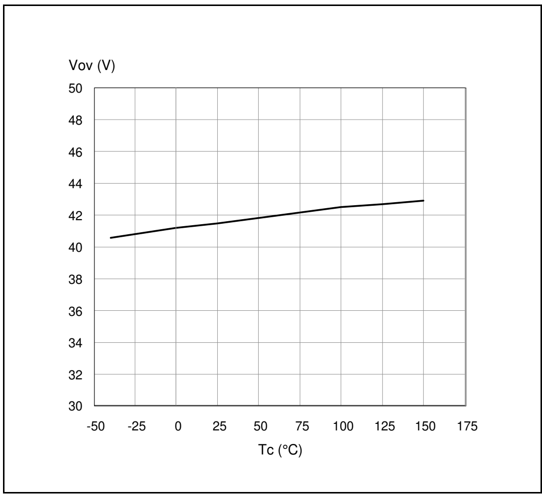


Figure 20. Open-load off-state voltage detection threshold

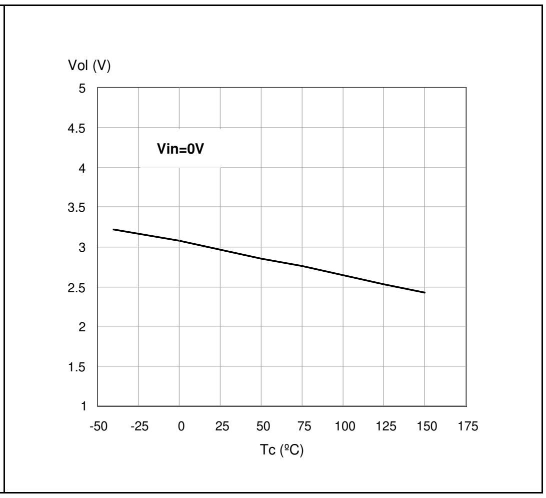


Figure 21. Turn-on voltage slope

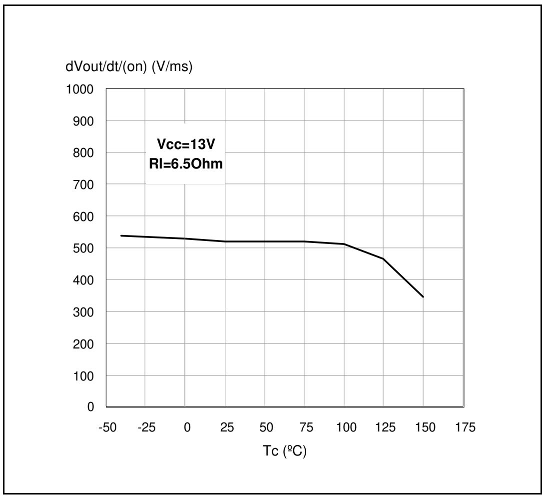


Figure 22. Turn-off voltage slope

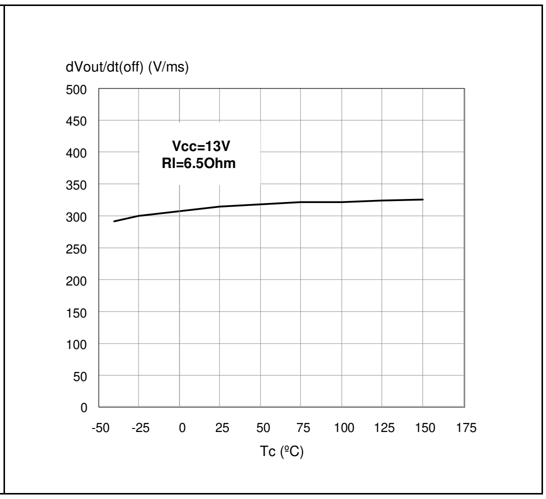


Figure 23. I_{lim} Vs T_{case}

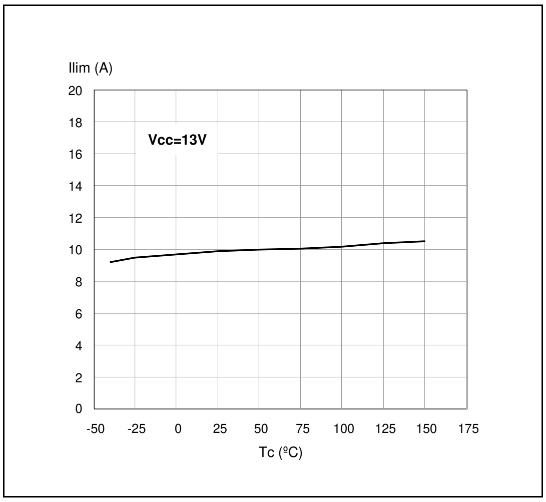
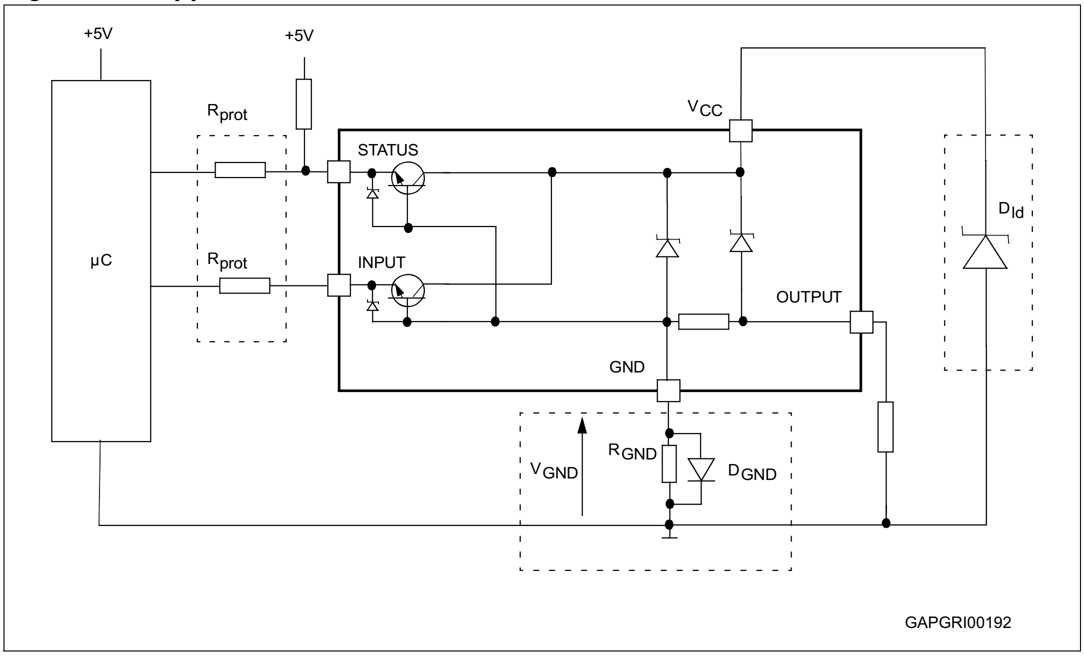


Figure 24. Application schematic



2.5 GND protection network against reverse battery

2.5.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to size the R_{GND} resistor.

1. $R_{GND} \leq 600mV / (I_{S(on)max})$.
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when V_{CC}<0: during reverse battery situations) is:

$P_D = (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} produces a shift ($I_{S(on)max}$ * R_{GND}) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (*2.5.2: Solution 2: diode (DGND) in the ground line*).

2.5.2 Solution 2: diode (D_{GND}) in the ground line

A resistor (R_{GND}=1 kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift (≈600mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

Series resistor in input and status lines are also required to prevent that, during battery voltage transient, the current exceeds the absolute maximum rating.

The safest configuration for unused input and status pin is to leave them unconnected.

2.6 Load dump protection

D_{ld} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

2.7 Microcontroller I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins are pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with from latching-up limit of µC I/Os.

$-V_{CCpeak}/I_{latchup} \le R_{prot} \le (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak}= - 100 V and $I_{latchup} \ge$ 20 mA; $V_{OH\mu C} \ge$ 4.5 V

5 kΩ $\le R_{prot} \le$ 65 kΩ.

Recommended values: R_{prot} =10 kΩ.

2.8 Open-load detection in off-state

Off-state open-load detection requires an external pull-up resistor (R_{PU}) connected between output pin and a positive supply voltage (V_{PU}) like the +5 V line used to supply the microprocessor.

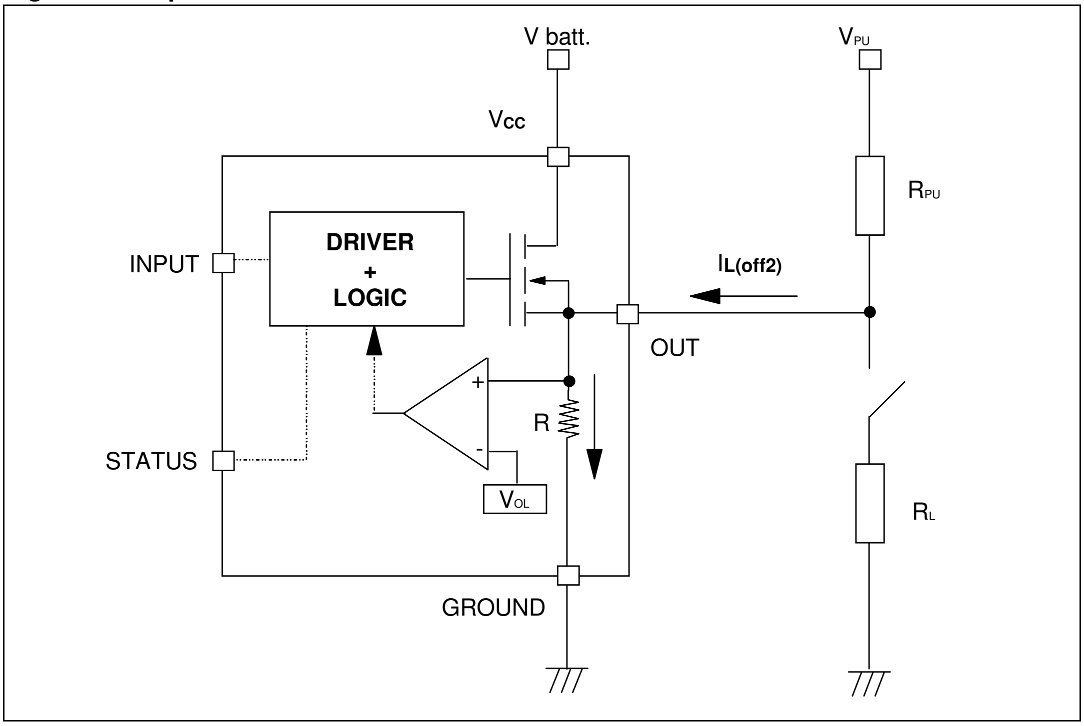
The external resistor has to be selected according to the following requirements:

1. no false open-load indication when load is connected: in this case we have to avoid V_{OUT} to be higher than V_{Olmin}; this results in the following condition $V_{OUT}=(V_{PU}/(R_L+R_{PU}))R_L<V_{Olmin}$.
2. no misdetection when load is disconnected: in this case the V_{OUT} has to be higher than V_{OLmax}; this results in the following condition $R_{PU}<(V_{PU}-V_{OLmax})/I_{L(off2)}$.

Because $I_{s(OFF)}$ may significantly increase if V_{out} is pulled high (up to several mA), the pull-up resistor R_{PU} should be connected to a supply that is switched off when the module is in standby.

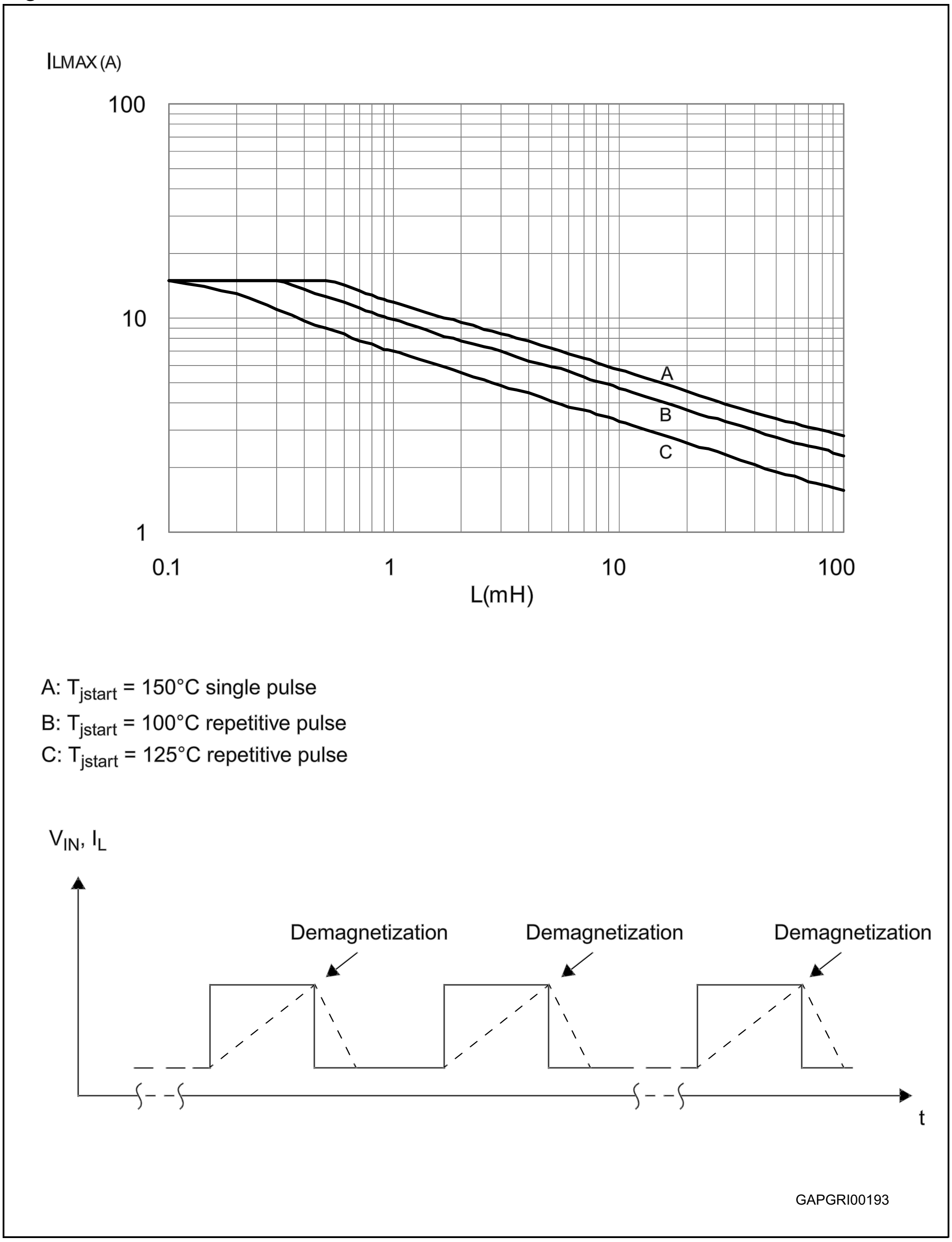
The values of V_{OLmin}, V_{OLmax} and $I_{L(off2)}$ are available in the electrical characteristics section.

Figure 25. Open-load detection in off-state



2.9 PPAK/P^{2}PAK maximum demagnetization energy (V_{CC}=13.5V)

Figure 26. PPAK /P^{2}PAK maximum turn-off current versus inductance

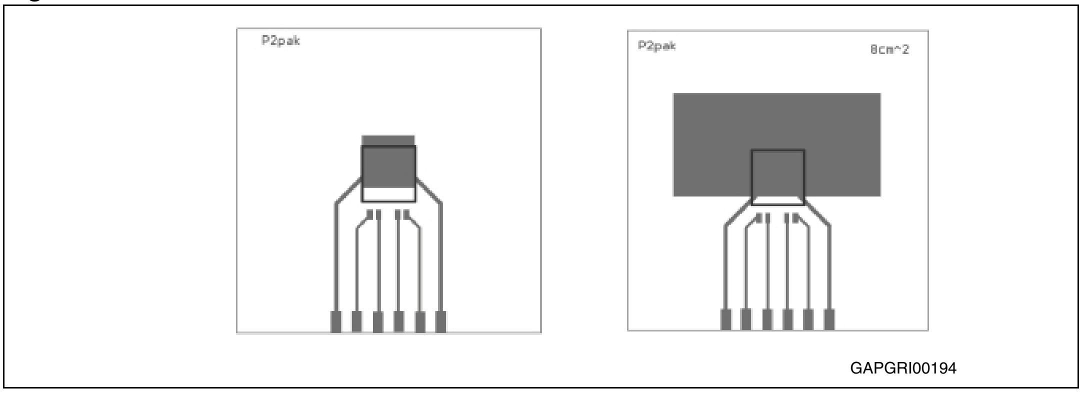


Note: *Values are generated with R_L =0 Ω.In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.*

3 Package and PCB thermal data

3.1 P^2PAK thermal data

Figure 27. P^2PAK PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 60 mm x 60 mm, PCB thickness = 2 mm, Cu thickness=35 µm, Copper areas: 0.97 cm^2, 8 cm^2).

Figure 28. P^2PAK $R_{thj\text{-}amb}$ Vs. PCB copper area in open box free air condition

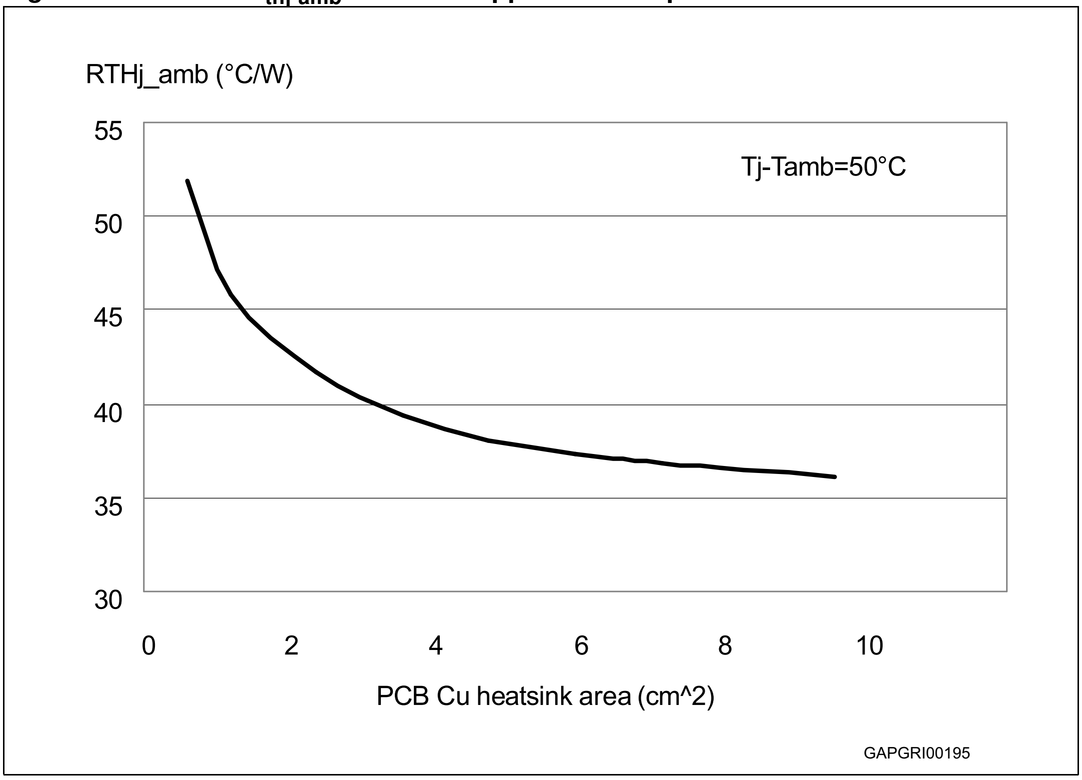
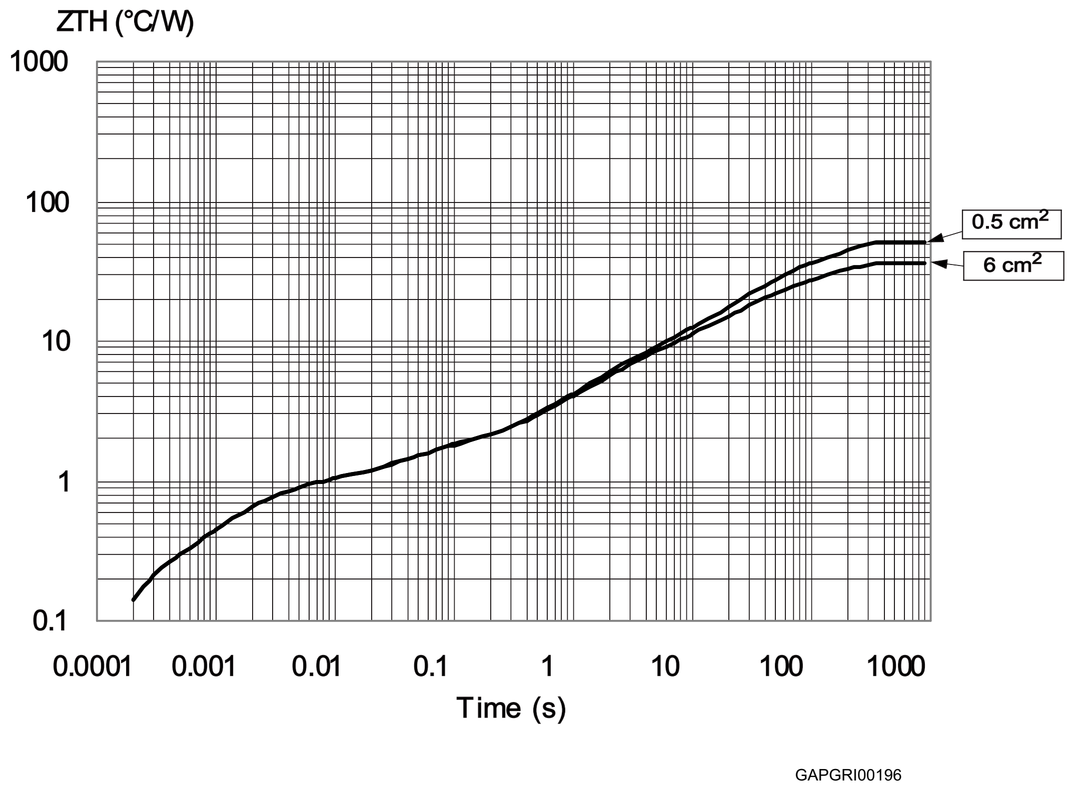


Figure 29. P^2PAK thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 30. P^2PAK thermal fitting model of a single channel

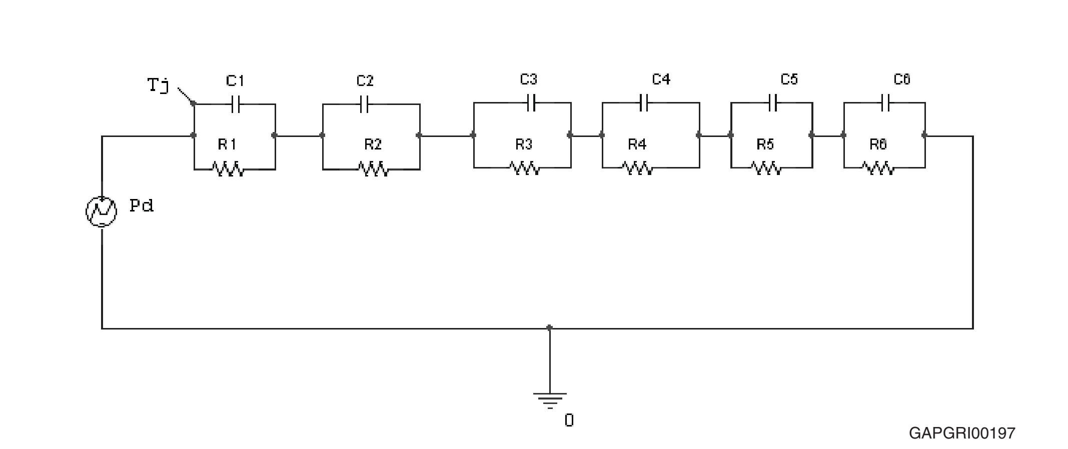
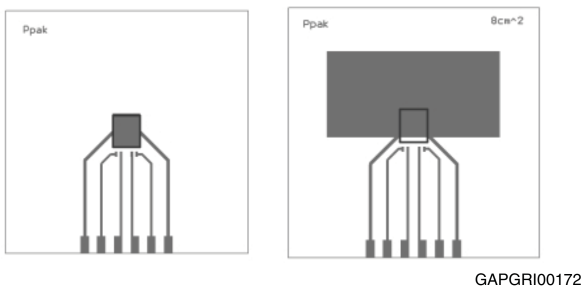


Table 10. P^2PAK thermal parameter

Area/island (cm^2)	0.5	6
R1 (°C/W)	0.15	
R2 (°C/W)	0.7	
R3 (°C/W)	0.7	
R4 (°C/W)	4	
R5 (°C/W)	9	
R6 (°C/W)	37	22
C1 (W·s/°C)	0.0006	
C2 (W·s/°C)	0.0025	
C3 (W·s/°C)	0.055	
C4 (W·s/°C)	0.4	
C5 (W·s/°C)	2	
C6 (W·s/°C)	3	5

3.2 PPAK thermal data

Figure 31. PPAK PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 60 mm x 60 mm, PCB thickness = 2 mm, Cu thickness=35 µm, Copper areas: 0.44 cm^2, 8 cm^2).

Figure 32. PPAK $R_{thj-amb}$ Vs. PCB copper area in open box free air condition

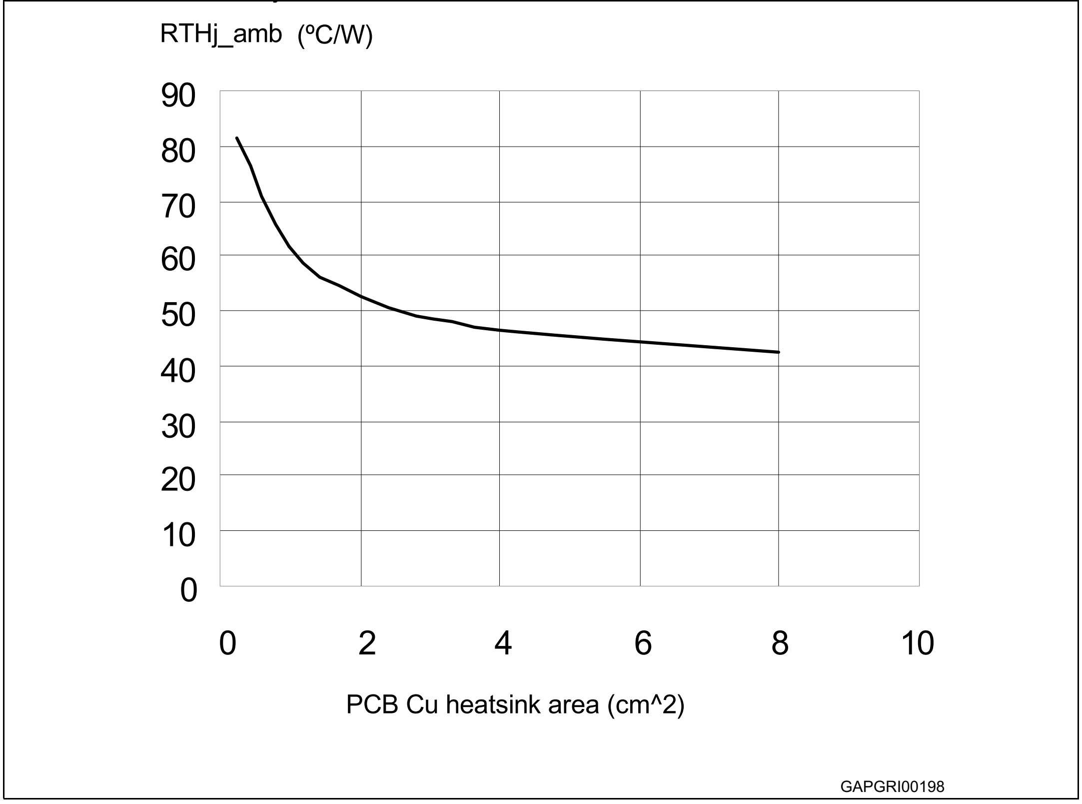
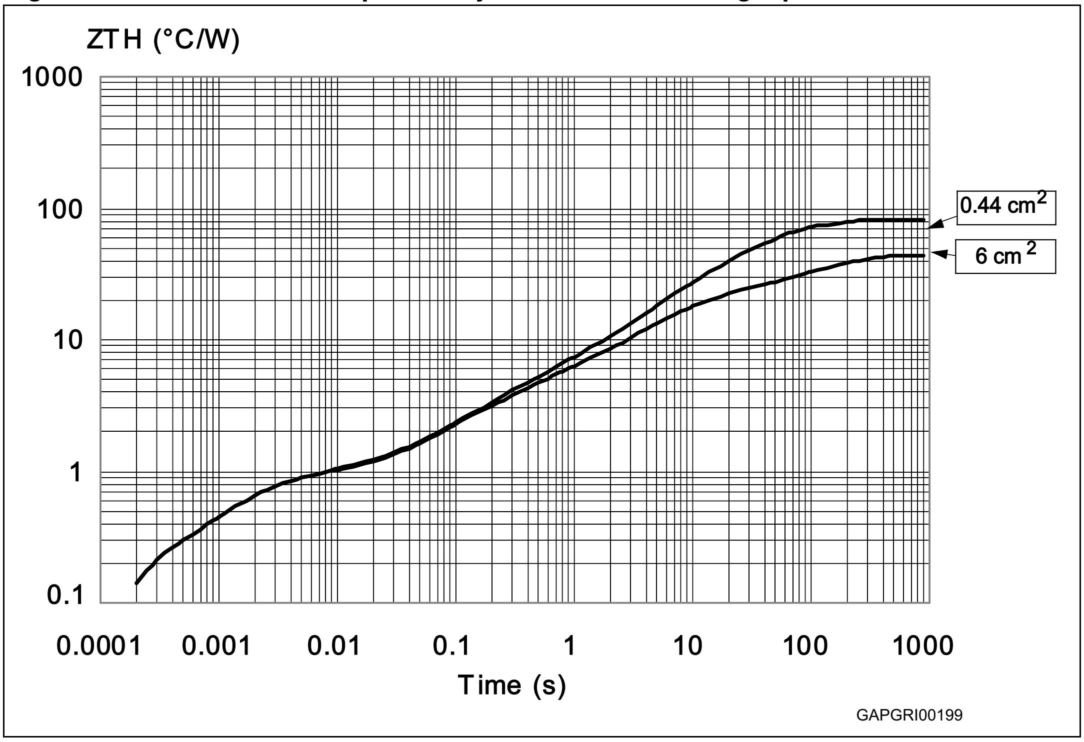


Figure 33. PPAK thermal impedance junction ambient single pulse



Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 34. PPAK thermal fitting model of a single channel

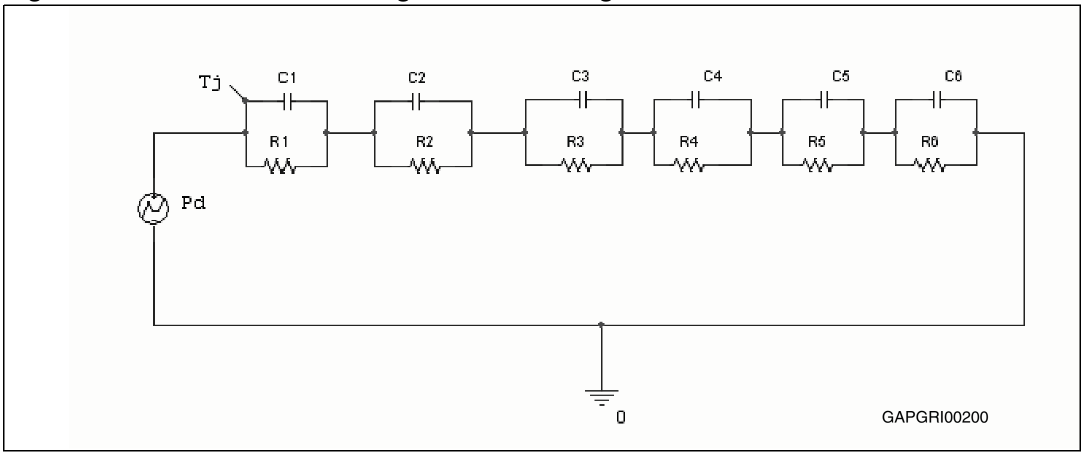


Table 11. PPAK thermal parameter

Area/island (cm²)	0.5	6
R1 (°C/W)	0.15	
R2 (°C/W)	0.7	
R3 (°C/W)	1.6	
R4 (°C/W)	2	
R5 (°C/W)	15	
R6 (°C/W)	61	24
C1 (W·s/°C)	0.0006	
C2 (W·s/°C)	0.0025	
C3 (W·s/°C)	0.08	
C4 (W·s/°C)	0.3	
C5 (W·s/°C)	0.45	
C6 (W·s/°C)	0.8	5

4 Package and packing information

4.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

4.2 PENTAWATT mechanical data

Figure 35. PENTAWATT package dimensions

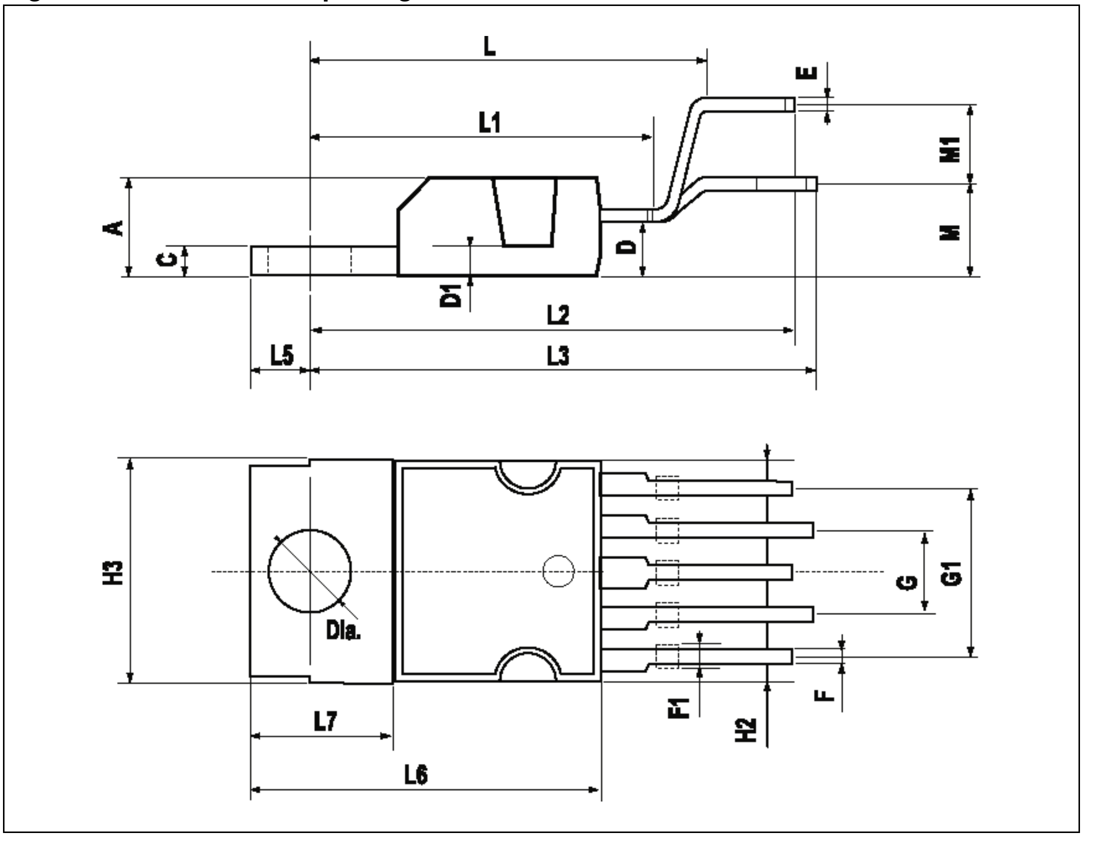


Table 12. PENTAWATT mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			4.8
C			1.37
D	2.4		2.8