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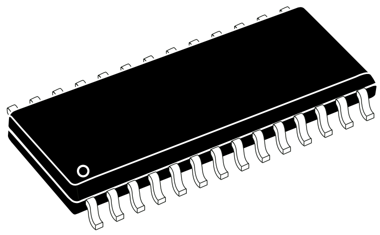
VN770KP-E

Quad smart power solid state relay for complete H-bridge configurations

Datasheet - production data



Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN770KP-E	225 mΩ(1)	9 A(2)	36 V

1. Total resistance of one side in bridge configuration
2. Typical current limitation value

- ECOPACK®: lead free and RoHS compliant
- Automotive Grade: compliance with AEC guidelines
- Suited as low voltage bridge
- Linear current limitation
- Very low standby power dissipation
- Short circuit protected
- Status flag diagnostic (open drain)
- Integrated clamping circuits
- Undervoltage protection
- ESD protection

Description

The VN770KP-E is a device formed by three monolithic chips housed in a standard SO-28 package: a double high side and two low side switches. Both the double high side and low side switches are made using STMicroelectronics VIPower™ M0-3 Technology.

This device is suitable to drive a DC motor in a bridge configuration as well as to be used as a quad switch for any low voltage application.

The dual high side switches have built-in thermal shutdown to protect the chips from over temperature and current limiter blocks to protect the device from short circuit. Status output is provided to indicate open load in off and on-state and over temperature.

The low side switches are two OMNIFET II types (fully auto protected Power MOSFET in VIPower™ technology). They have built-in thermal shutdown, linear current limitation and overvoltage clamping. Fault feedback for thermal intervention can be detected by monitoring the voltage at the input pin.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
SO-28	VN770KP-E	VN770KPTR -E

Contents

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List of figures

1 Block diagram and pin description

Figure 1. Block diagram

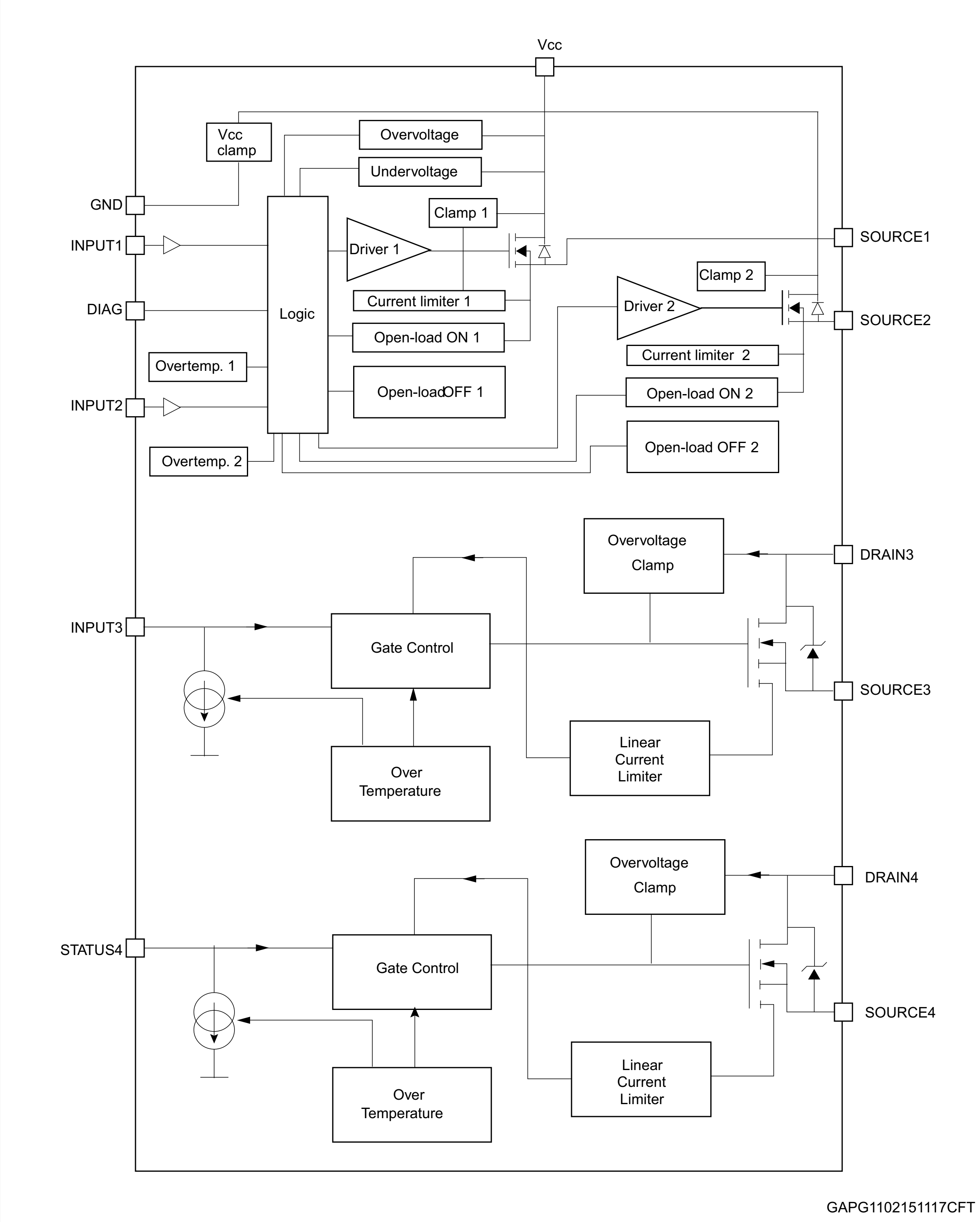
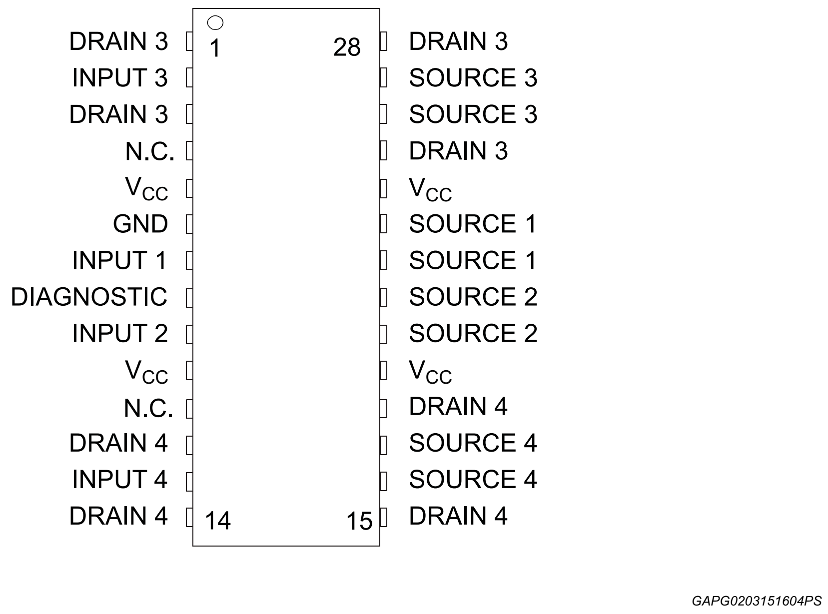


Table 2. Pin definition and function

No	Name	Function
1, 3, 25, 28	DRAIN 3	Drain of switch 3 (low-side switch)
2	INPUT 3	Input of switch 3 (low-side switch)
4, 11	N.C.	Not connected
5, 10, 19, 24	V_{CC}	Drain of switches 1 and 2 (high-side switches) and power supply voltage
6	GND	Ground of switches 1 and 2 (high-side switches)
7	INPUT 1	Input of switch 1 (high-side switches)
8	DIAGNOSTIC	Diagnostic of switches 1 and 2 (high-side switches)
9	INPUT 2	Input of switch 2 (high-side switch)
12, 14, 15, 18	DRAIN 4	Drain of switch 4 (low-side switch)
13	INPUT 4	Input of switch 4 (low-side switch)
16, 17	SOURCE 4	Source of switch 4 (low-side switch)
20, 21	SOURCE 2	Source of switch 2 (high-side switch)
22, 23	SOURCE 1	Source of switch 1 (high-side switch)
26, 27	SOURCE 3	Source of switch 3 (low-side switch)

Figure 2. Connection diagram



2 Electrical specifications

2.1 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value Max (°C/W)
$R_{thj\text{-}case}$	Thermal resistance junction-case (high side switch)	20
$R_{thj\text{-}case}$	Thermal resistance junction-case (low side switch)	20
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (with 6 cm^2 of Cu heat sink)	See *Figure 49*

2.2 Absolute maximum ratings

Table 4. Dual high side switch

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	-0.3	V
$-I_{GND}$	DC reverse ground pin current	-200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-6	A
I_{IN}	DC input current	±10	mA
I_{STAT}	DC status current	±10	mA
V_{ESD}	Electrostatic discharge (human body model: R = 1.5 KΩ; C = 100 pF) – Input – Status – Output – Vcc	 4000 4000 5000 5000	 V V V V
P_{tot}	Power dissipation (T_C = 25°C)	6	W
T_j	Junction operating temperature	Internally limited	°C
T_c	Case operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

Table 5. Low side switch

Symbol	Parameter	Value	Unit
V_{DS}	Drain source voltage (V_{IN} = 0 V)	Internally clamped	V
V_{IN}	Input voltage	Internally clamped	V
I_{IN}	Input current	±20	mA

Table 5. Low side switch (continued)

Symbol	Parameter	Value	Unit
$R_{IN\ MIN}$	Minimum input series impedance	150	Ω
I_D	Drain current	Internally limited	A
I_R	Reverse DC output current	-10.5	A
V_{ESD1}	Electrostatic discharge (R = 1.5 KΩ, C = 100 pF)	4000	V
V_{ESD2}	Electrostatic discharge on output pin only (human body model: R = 330 Ω, C = 150 pF)	5000	V
P_{tot}	Power dissipation (T_C = 25°C)	6	W
T_j	Operating junction temperature	Internally limited	°C
T_c	Case operating temperature	Internally limited	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.3 Electrical characteristics for dual high side switch

8 V < V_{CC}< 36 V; -40°C < T_j < 150°C, unless otherwise specified.

Table 6. Power outputs (per each channel)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CC}(1)	Operating supply voltage		5.5	13	36	V
V_{USD}(1)	Undervoltage shutdown		3	4	5.5	V
V_{OV}(1)	Overvoltage shutdown		36	-	-	V
R_{ON}	On-state resistance	I_{OUT} = 1 A; T_j = 25°C			160	mΩ
		I_{OUT} = 1 A; V_{CC} > 8 V			320	mΩ
I_S(1)	Supply current	Off-state; V_{CC} = 13 V; V_{IN} = V_{OUT} =0 V		12	40	µA
		Off-state; V_{CC} = 13 V; V_{IN} = V_{OUT} =0 V; T_j = 25°C		12	25	µA
		On-state; V_{CC} = 13V; V_{IN} = 5V; I_{OUT} = 0 V		5	7	mA
$I_{L(off1)}$	Off-state output current	V_{IN} = V_{OUT} = 0 V	0		50	µA
$I_{L(off2)}$	Off-state output current	V_{IN} = 0 V; V_{OUT} = 3.5 V	-75		0	µA
$I_{L(off3)}$	Off-state output current	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 125°C			5	µA
$I_{L(off4)}$	Off-state output current	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 25°C			3	µA

1. Per device.

Table 7. Switching (per each channel) (V_{CC} = 13 V)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 13 Ω from V_{IN} rising edge to V_{OUT} = 1.3 V	—	30	—	µs
$t_{d(off)}$	Turn-off delay time	R_L = 13 Ω from V_{IN} falling edge to V_{OUT} = 11.7 V	—	30	—	µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L = 13 Ω from V_{OUT} = 1.3 V to V_{OUT} = 10.4 V	—	(1)	—	V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L = 13 Ω from V_{OUT} = 11.7 V to V_{OUT} = 1.3 V	—	(1)	—	V/µs

1. See relative diagram

Table 8. Logic input (per each channel)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IL}	Input low level				1.25	V
I_{IL}	Low level input current	V_{IN} = 1.25 V	1			µA
V_{IH}	Input high level		3.25			V
I_{IH}	High level input current	V_{IN} = 3.25 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	6	6.8	8	V
		I_{IN} = -1 mA		-0.7		V

Table 9. Status pin (per each channel)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{STAT}	Status low output voltage	I_{STAT} = 1.6 mA			0.5	V
I_{LSTAT}	Status leakage current	Normal operation; V_{STAT} = 5 V			10	µA
C_{STAT}	Status pin input capacitance	Normal operation; V_{STAT} = 5 V			100	pF
V_{SCL}	Status clamp voltage	I_{STAT} = 1 mA	6	6.8	8	V
		I_{STAT} = -1 mA		-0.7		V

Table 10. Protections (per each channel)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		135	-		°C
T_{hyst}	Thermal hysteresis		7	15		°C
t_{SDL}	Status delay in overload conditions	$T_j > T_{TSD}$			20	µs

Table 10. Protections (per each channel) (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{lim}	Current limitation		7	10	13	A
		T_j = 125 °C	8		13	A
		5.5 V < V_{CC} < 36 V			13	A
V_{demag}	Turn-off output clamp voltage	I_{OUT} = 1 A; L = 6 mH	V_{CC} - 41	V_{CC} - 48	V_{CC} - 55	V

Note: To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 11. Openload detection (per each channel)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{OL}	Openload on-state detection threshold	V_{IN} = 5 V	20	40	80	mA
$t_{DOL(on)}$	Openload on-state detection delay	I_{OUT} = 0 A			200	µs
V_{OL}	Openload off-state voltage detection threshold	V_{IN} = 0 V	1.5	2.5	3.5	V
$t_{DOL(off)}$	Openload detection delay at turn-off				1000	µs

2.4 Electrical characteristics for low side switches

-40°C < T_j < 150°C, unless otherwise specified.

Table 12. Off-state

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CLAMP}	Drain source clamp voltage	V_{IN} = 0 V; I_D = 3.5 A	40	45	55	V
V_{CLTH}	Drain source clamp threshold voltage	V_{IN} = 0 V; I_D = 2 mA	36			V
V_{INTH}	Input threshold voltage	V_{DS} = V_{IN}; I_D = 1 mA	0.5		2.5	V
I_{ISS}	Supply current from input pin	V_{DS} = 0 V; V_{IN} = 5 V		100	150	µA
V_{INCL}	Input-source clamp voltage	I_{IN} = 1 mA	6	6.8	8	V
		I_{IN} = -1 mA	-1.0		-0.3	V
I_{DSS}	Zero input voltage drain current (V_{IN} = 0 V)	V_{DS} = 13 V; V_{IN} = 0 V; T_j = 25°C			30	µA
		V_{DS} = 25 V; V_{IN} = 0 V			75	µA

Table 13. On-state

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$R_{DS(on)}$	Static drain source on resistance	V_{IN} = 5 V; I_D = 3.5 A; T_j = 25°C	—	—	65	mΩ
		V_{IN} = 5 V; I_D = 3.5 A	—	—	130	mΩ

T_j = 25°C, unless otherwise specified.

Table 14. Dynamic

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
g_{fs} (1)	Forward trans conductance	V_{DD} = 13 V; I_D = 3.5 A	—	9	—	S
C_{OSS}	Output capacitance	V_{DS} = 13 V; f = 1 MHz; V_{IN} = 0 V	—	220	—	pF

1. Pulsed: Pulse duration = 300µs, duty cycle 1.5%

Table 15. Switching

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V; I_D = 3.5 A; V_{gen} = 5 V; R_{gen} = $R_{IN\ MIN}$ = 150 Ω	—	100	300	ns
t_r	Rise time		—	470	1500	ns
$t_{d(off)}$	Turn-off delay time		—	500	1500	ns
t_f	Fall time		—	350	1000	ns
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V; I_D = 3.5 A; V_{gen} = 5 V; R_{gen} = 2.2 KΩ	—	0.75	2.3	µs
t_r	Rise time		—	4.6	14	µs
$t_{d(off)}$	Turn-off delay time		—	5.4	16	µs
t_f	Fall time		—	3.6	11	µs
$(dI/dt)_{on}$	Turn-on current slope	V_{DD} = 15 V; I_D = 3.5 A; V_{gen} = 5 V; R_{gen} = $R_{IN\ MIN}$ = 150 Ω	—	6.5		A/µs
Q_i	Total input charge	V_{DD} = 12 V; I_D = 3.5 A; V_{IN} = 5 V; I_{gen} = 2.13 mA	—	18		nC

Table 16. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 3.5 A; V_{IN} = 0 V	—	0.8	—	V
t_{rr}	Reverse recovery time	I_{SD} = 3.5 A; dI/dt = 20 A/µs; V_{DD} = 30 V; L = 200 µH	—	220	—	ns
Q_{rr}	Reverse recovery charge		—	0.28	—	µC
I_{RRM}	Reverse recovery current		—	2.5	—	A

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

-40°C < T_j < 150°C, unless otherwise specified.

Table 17. Protections

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{lim}	Drain current limit	V_{IN} = 5 V; V_{DS} = 13 V	6	9	12	A
		V_{IN} = 5 V; V_{DS} = 13 V; T_j = 125°C	6.5		12	A
t_{dlim}	Step response current limit	V_{IN} = 5 V; V_{DS} = 13 V		4		µs
T_{jsh}	Over temperature shutdown		150	175		°C
T_{jrs}	Over temperature reset		135			°C
I_{gf}	Fault sink current	V_{IN} = 5 V; V_{DS} = 13 V; T_j = T_{jsh}		15		mA
E_{as}	Single pulse avalanche energy	Starting T_j = 25 °C; V_{DD} = 24 V; V_{IN} = 5 V; R_{gen} = $R_{IN\ MIN}$ = 150 Ω; L = 24 mH	200			mJ

2.5 Dual high-side switch timing data

Figure 3. Switching time waveforms

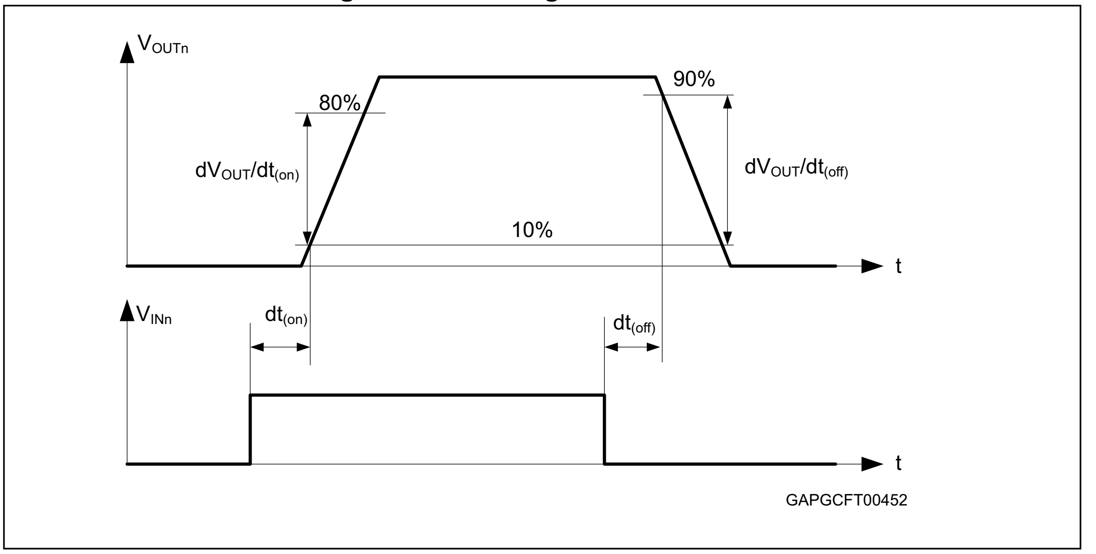


Table 18. Truth table

Conditions	Input	Output	Status
Normal operation	L H	L H	H H
Current limitation	L H H	L X X	H (T_j < T_{TSD}) H (T_j > T_{TSD}) L
Over temperature	L H	L L	H L

Table 18. Truth table (continued)

Conditions	Input	Output	Status
Undervoltage	L H	L L	X X
Overvoltage	L H	L L	H H
Output voltage > V_{OL}	L H	H H	L H
Output current < I_{OL}	L H	L H	H L

Figure 4. Open-load status timing (with external pull-up)

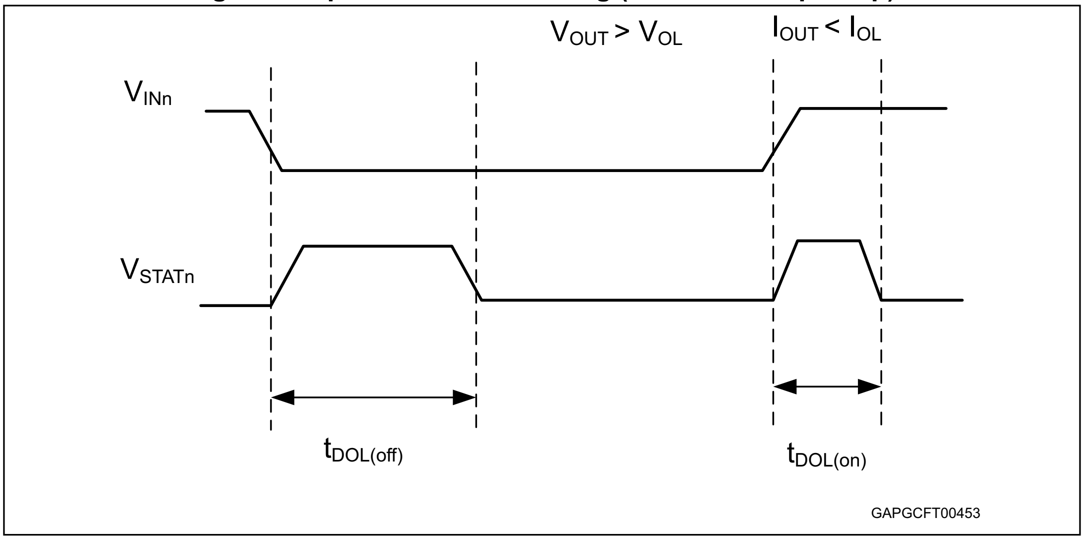
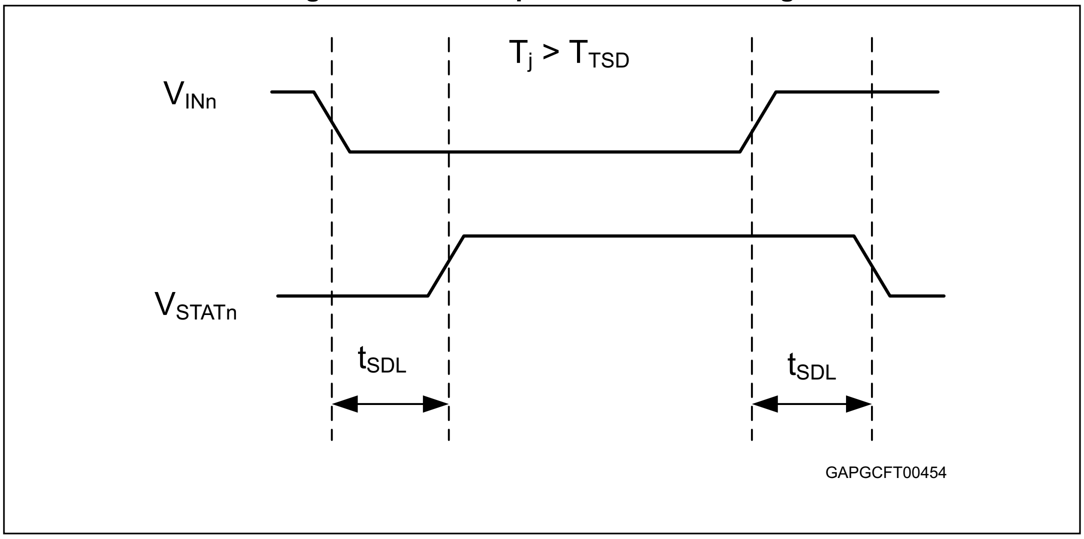


Figure 5. Over temperature status timing



2.6 Electrical characterization for dual high side switch

Figure 6. Off-state output current

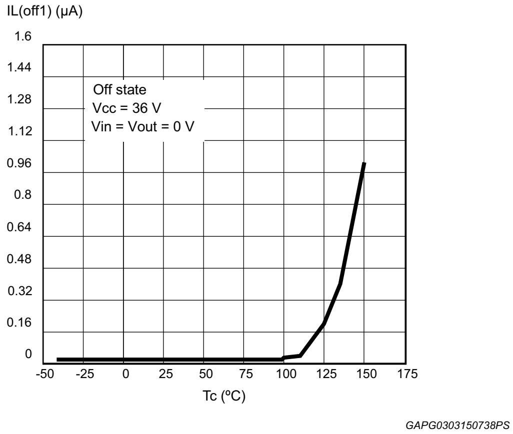


Figure 7. Input clamp voltage

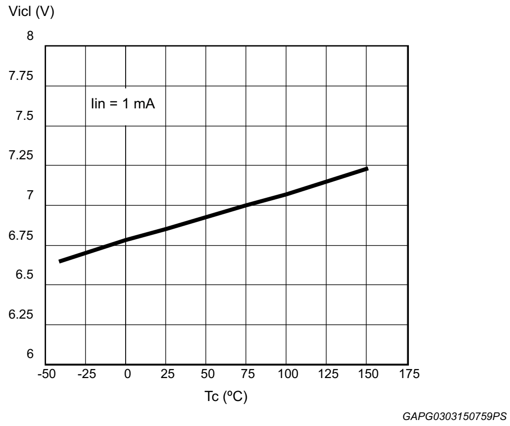


Figure 8. High level input current

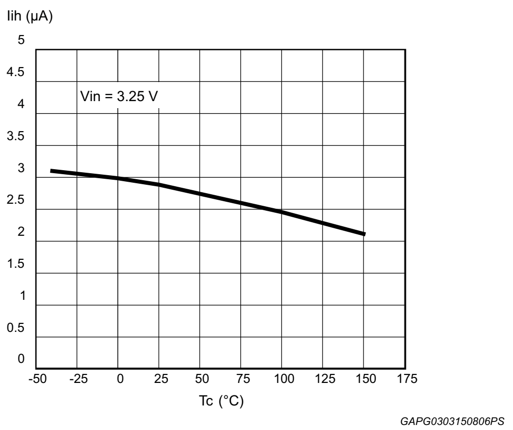


Figure 9. Input high level voltage

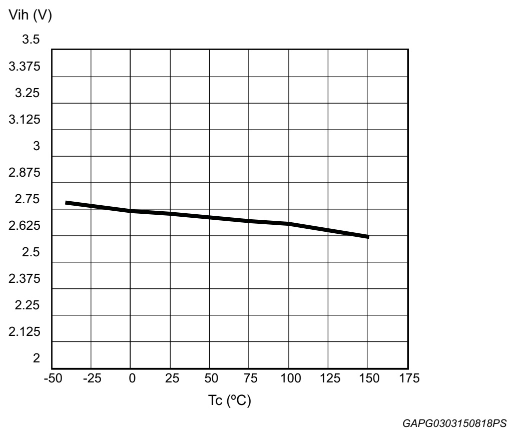


Figure 10. Input low level voltage

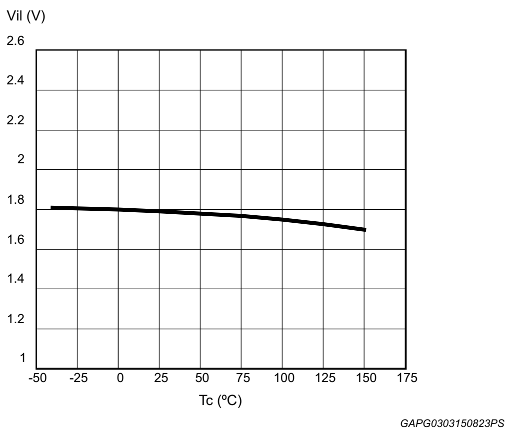


Figure 11. Input hysteresis voltage

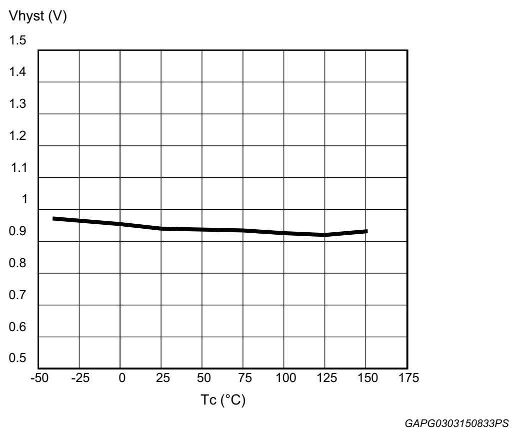


Figure 12. Overvoltage shutdown

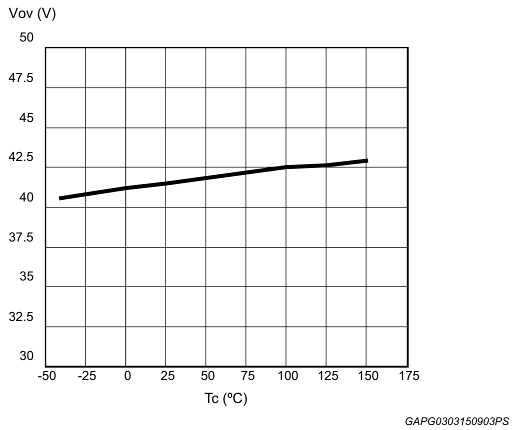


Figure 13. I_{LIM} vs T_{case}

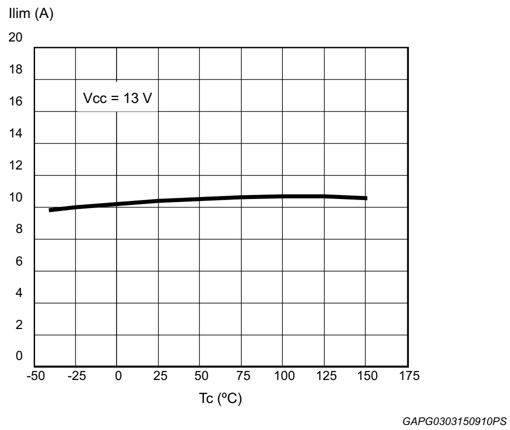


Figure 14. Turn-on voltage slope

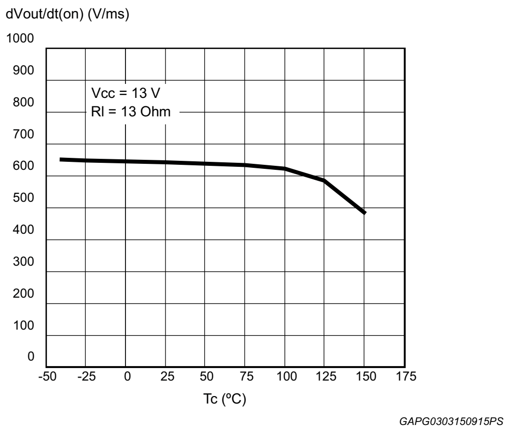


Figure 15. Turn-off voltage slope

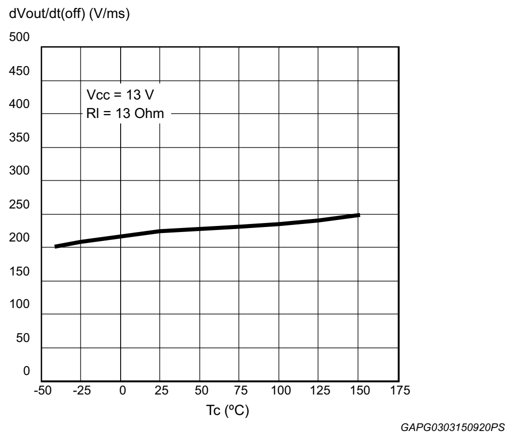


Figure 16. On-state resistance vs T_{case}

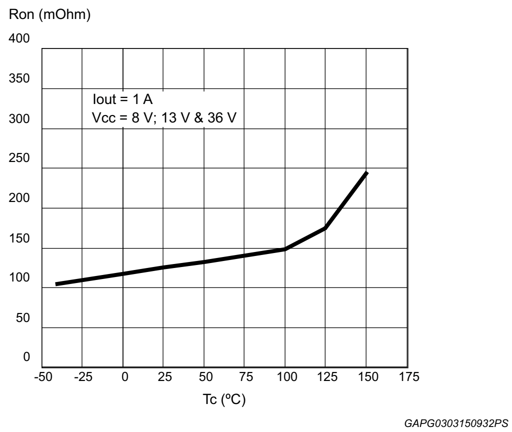


Figure 17. On-state resistance vs V_{CC}

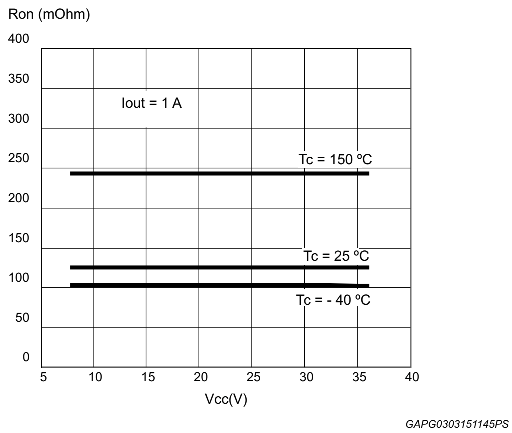


Figure 18. Status leakage current

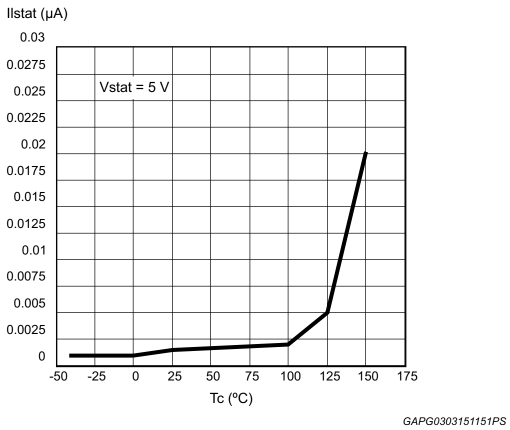


Figure 19. Status low output voltage

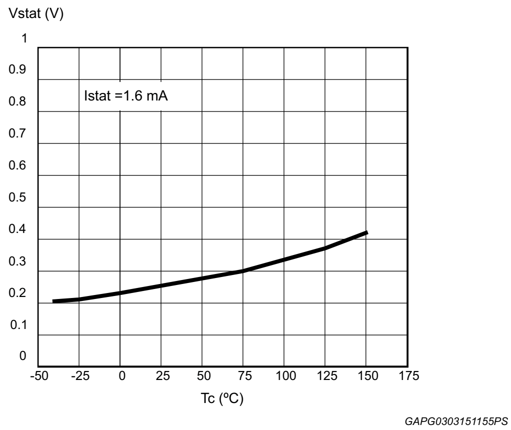


Figure 20. Openload on-state detection threshold

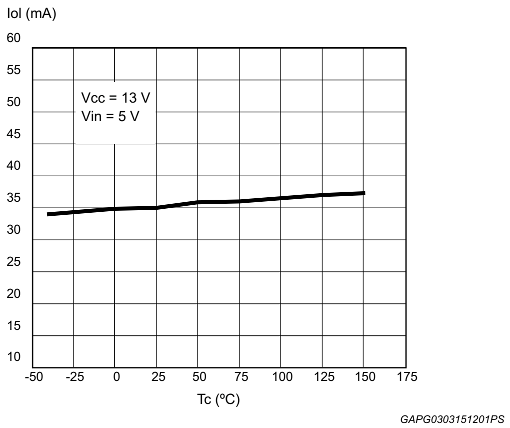


Figure 21. Openload off-state voltage detection threshold

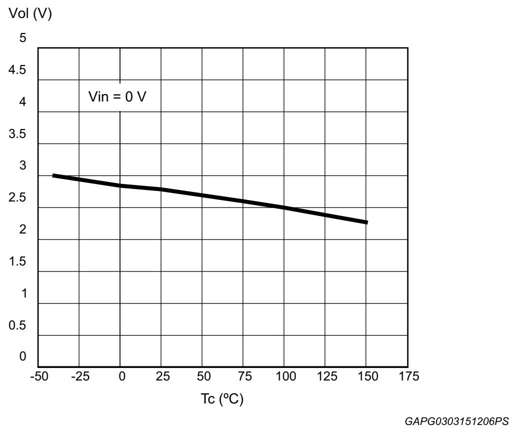
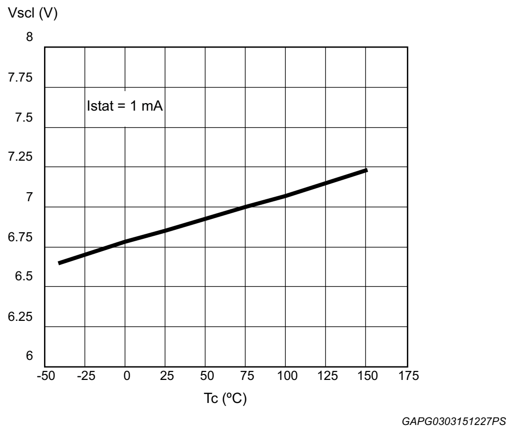


Figure 22. Status clamp voltage



2.7 Electrical characterization for low side switches

Figure 23. Static drain source on resistance

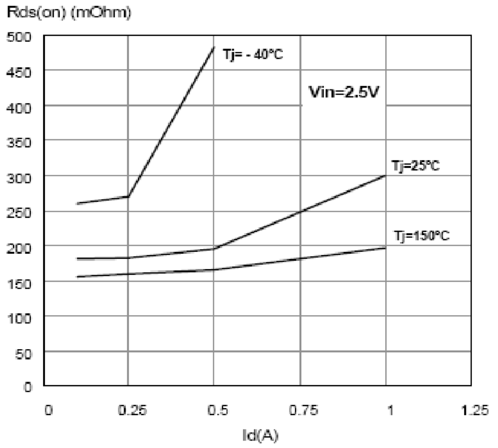


Figure 24. Derating curve

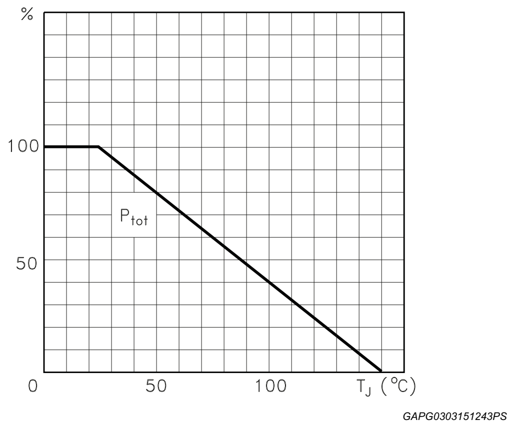


Figure 25. Transconductance

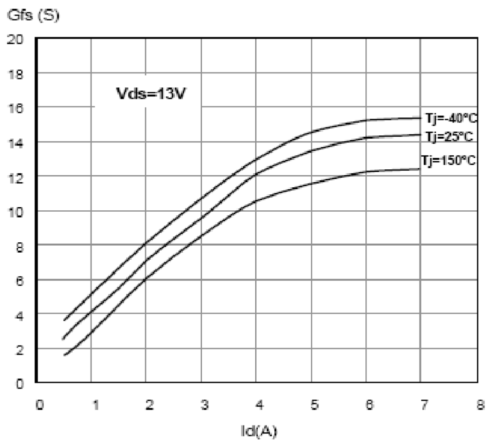


Figure 26. Transfer characteristics

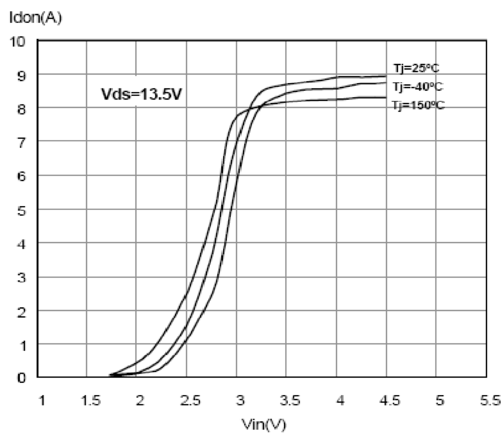


Figure 27. Turn-on current slope (V_{in} = 5 V)

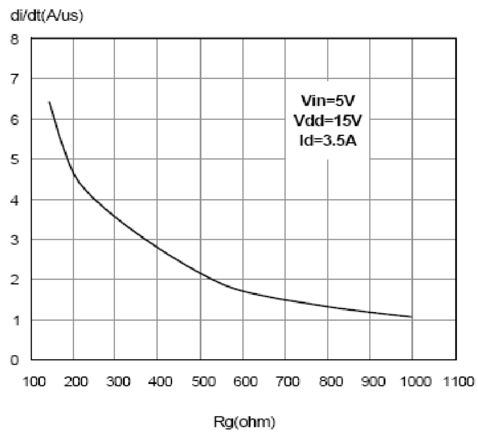


Figure 28. Turn-on current slope (V_{in} = 3.5 V)

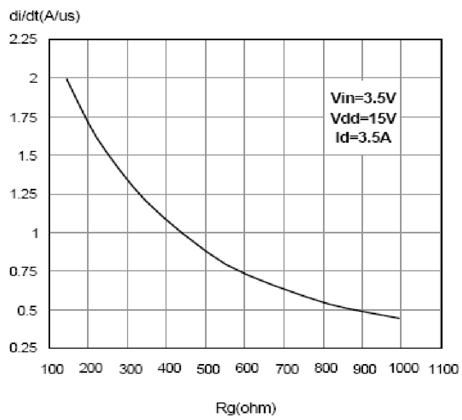


Figure 29. Input voltage vs input charge

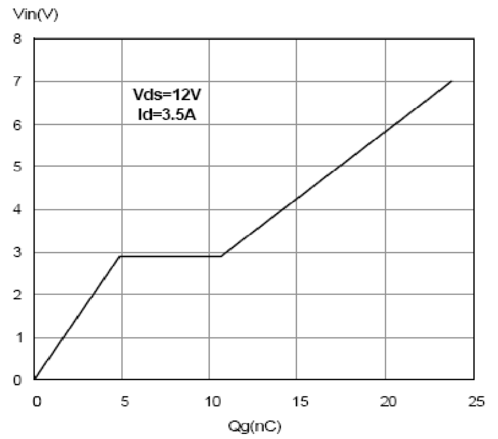


Figure 30. Capacitance variations

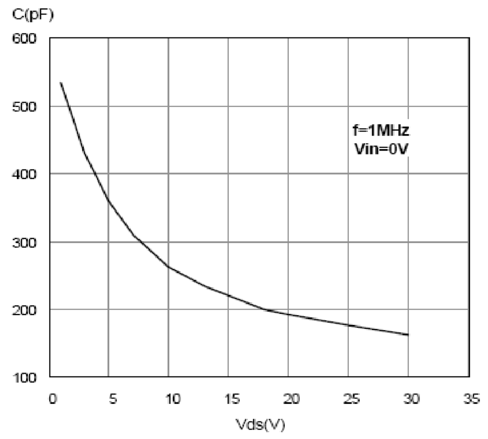


Figure 31. Switching time resistive load (V_{in} = 5 V)

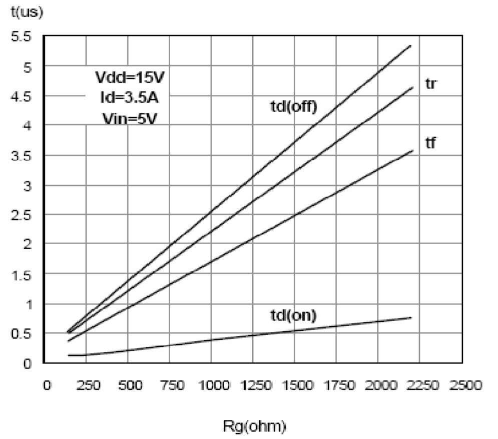


Figure 32. Switching time resistive load (R_g = 10 Ohm)]

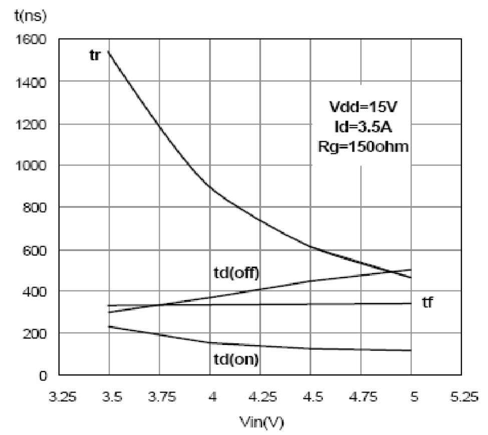


Figure 33. Output characteristics

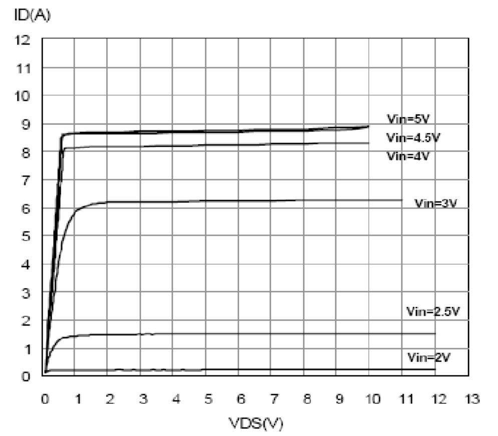


Figure 34. Step response current limit

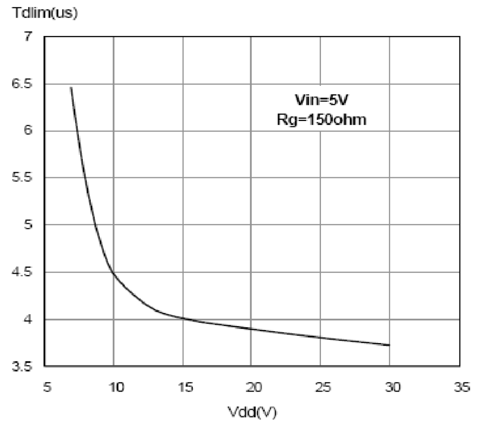


Figure 35. Source drain diode forward characteristics

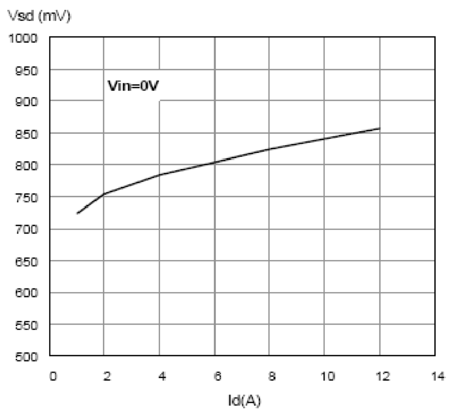


Figure 36. Static drain source on resistance vs I_d

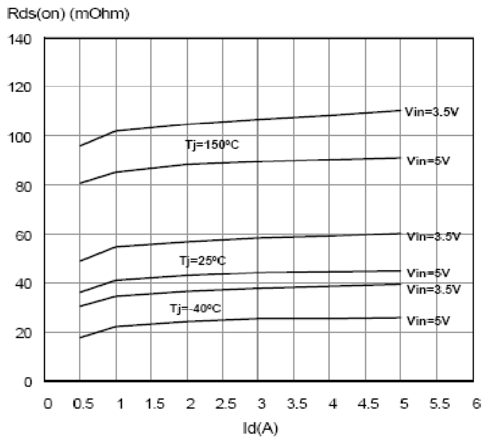


Figure 37. Static drain source on resistance vs input voltage (I_d = 7 A)

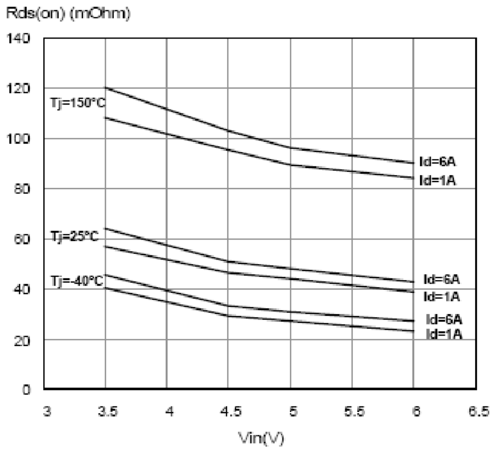


Figure 38. Static drain source on resistance vs input voltage

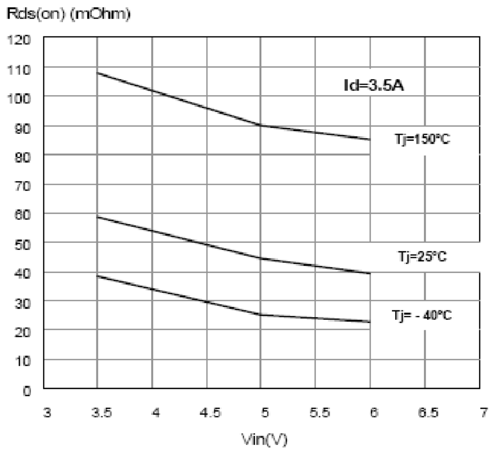


Figure 39. Normalized input threshold voltage vs temperature

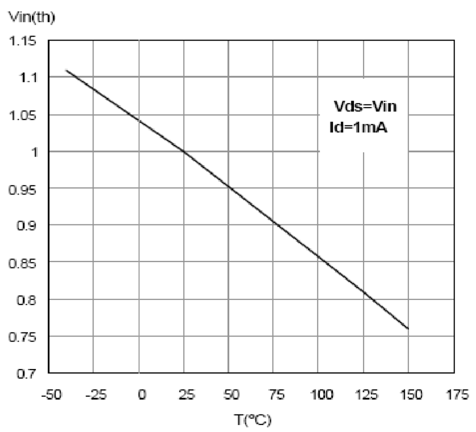


Figure 40. Normalized on resistance vs temperature

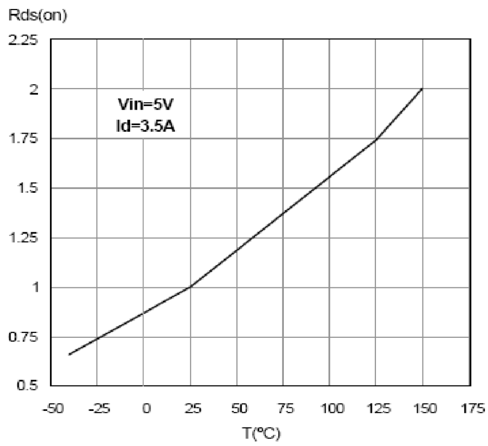


Figure 41. Turn-off drain source voltage slope (V_{in} = 3.5 V)

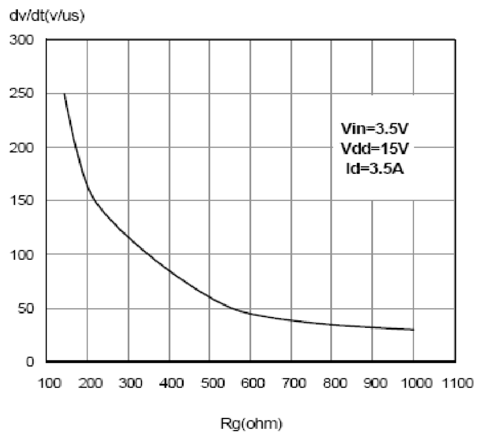


Figure 42. Turn-off drain source voltage slope (V_{in} = 5 V)

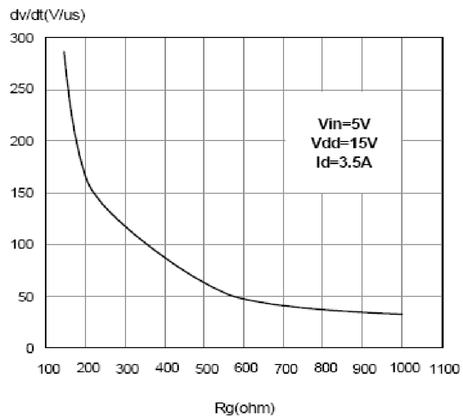
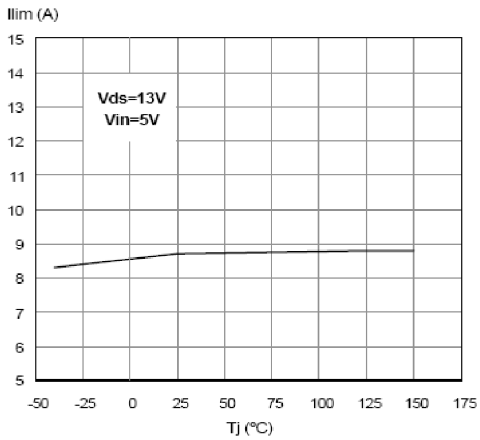
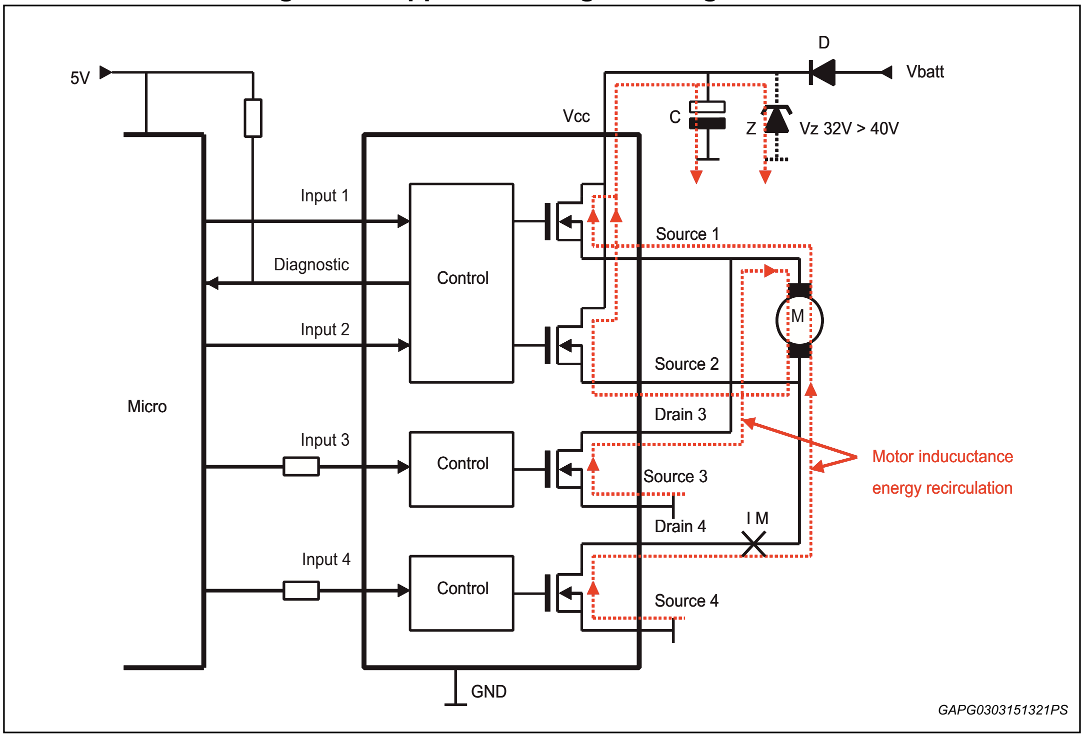


Figure 43. Current limit vs junction temperature



3 Application recommendations

Figure 44. Application diagram bridge drivers



Most motor bridge drivers use a reverse battery protection diode (D) inside the supply rail. This diode prevents a reverse current flow back to V_{BATT} in case the bridge becomes disabled via the logic inputs while motor inductance still carries energy. In order to prevent a hazardous overvoltage at circuit supply terminal (V_{CC}), a blocking capacitor (C) is needed to limit the voltage overshoot. As basic orientation, 50 µF per 1 A load current is recommended. As an alternative, a Zener protection (Z) is also suitable.

Even if a reverse polarity diode is not present, it is recommended to use a capacitor or Zener at V_{CC} because a similar problem appears in case the supply terminal of the module has intermittent electrical contact to the battery or gets disconnected while the motor is operating.

Figure 45. Recommended motor operation

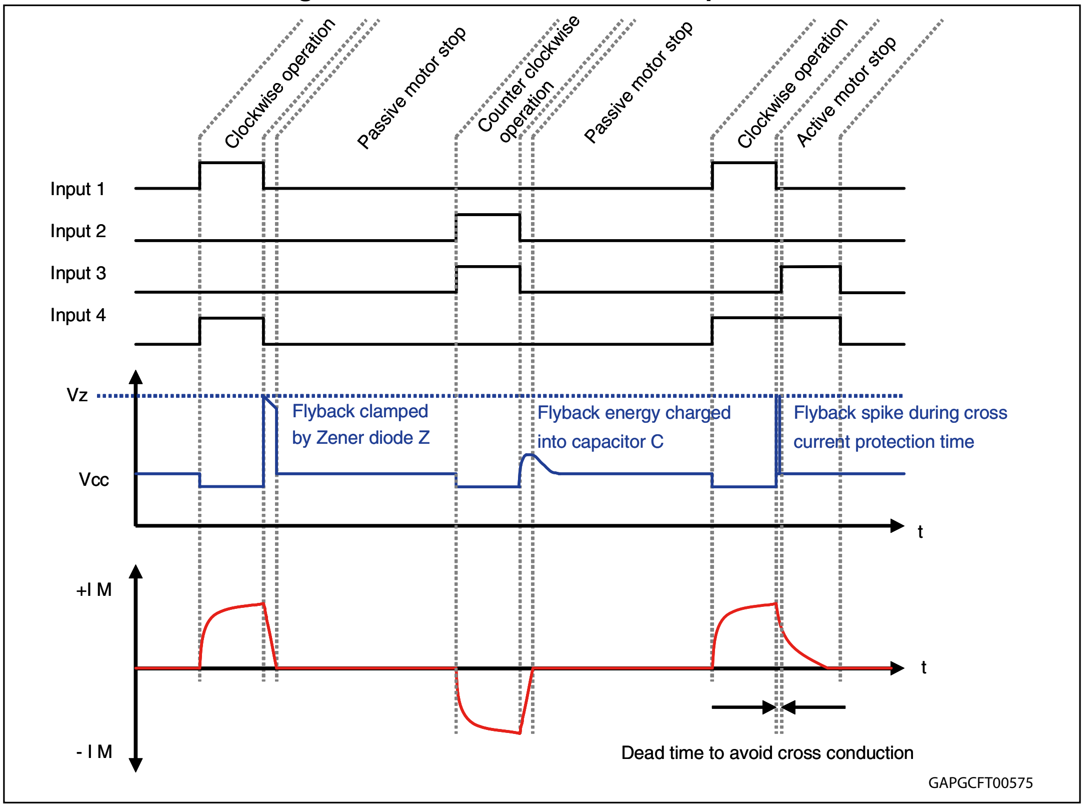
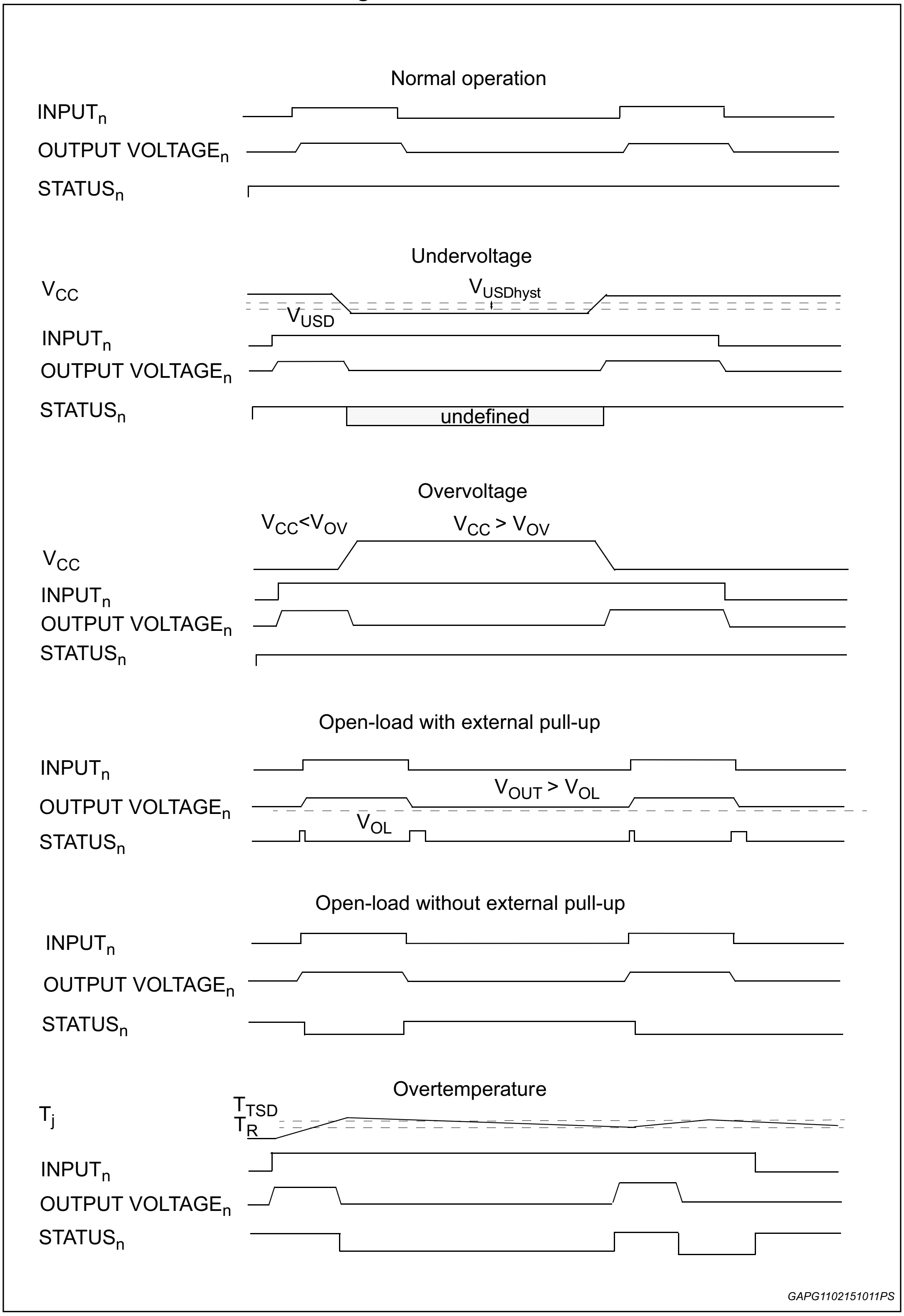


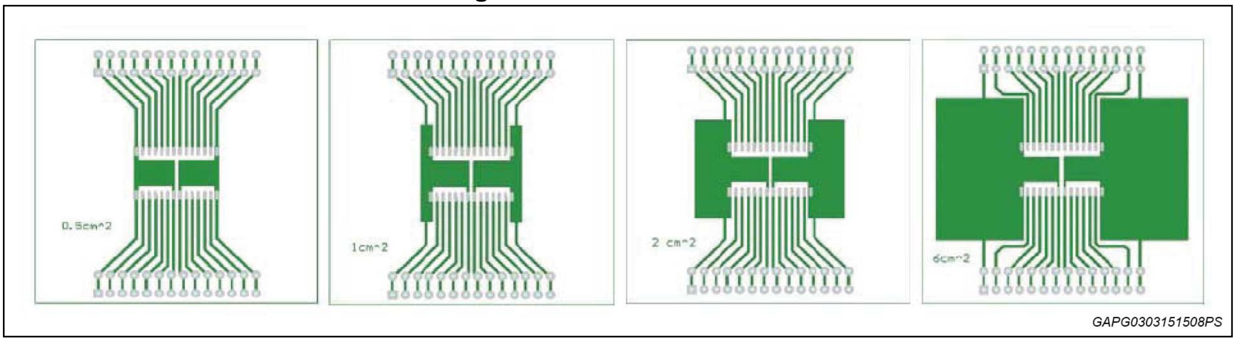
Figure 46. Waveforms



4 Thermal data

4.1 SO-28 thermal data

Figure 47. SO-28 PC board



Note: Layout condition of Rth and Zth measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2mm, Cu thickness = 35 µm, Copper areas: from minimum pad layout to 6 cm^2).

Figure 48. Chipset configuration

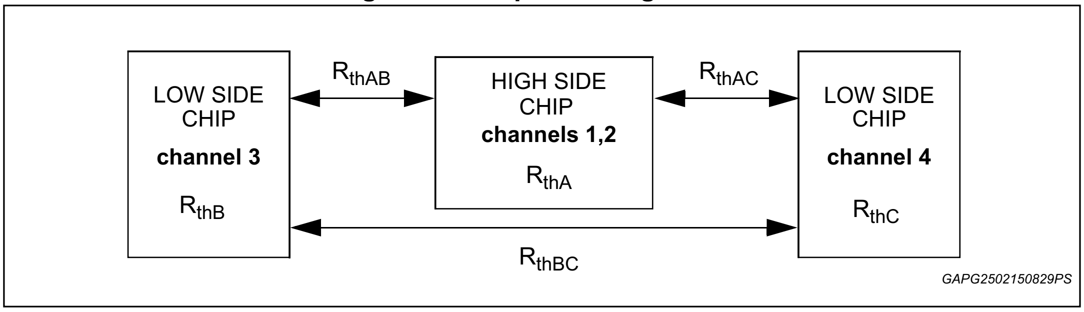
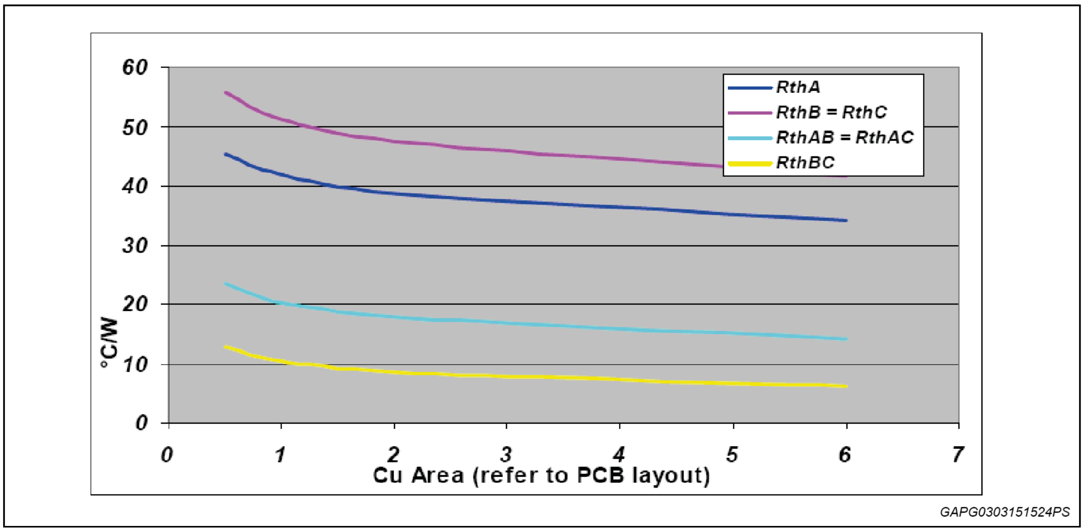


Figure 49. Auto and mutual Rthj-amb vs PCB copper area in open box free air condition



Note: See definitions in Section 5.2 on page 31.