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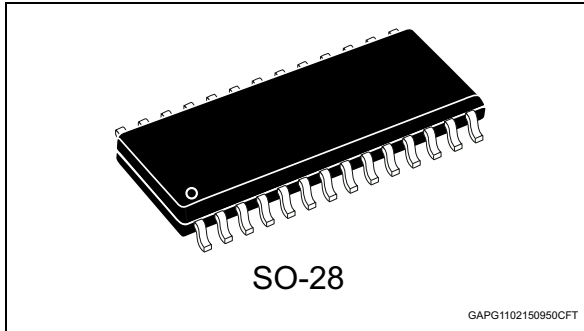
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Quad smart power solid state relay for complete H-bridge configurations

Datasheet - production data



Description

The VN772KP-E is a device formed by three monolithic chips housed in a standard SO-28 package: a double high-side and two low-side switches. Both the double high-side and low-side switches are made using STMicroelectronics VIPower[®] M0-3 Technology.

This device is suitable to drive a DC motor in a bridge configuration as well as to be used as a quad switch for any low voltage application.

The dual high-side switches have built-in thermal shutdown to protect the chips from over temperature and current limiter blocks to protect the device from short circuit. Status output is provided to indicate open-load in OFF and ON-state and overtemperature.

The low-side switches are two OMNIFET II types (fully auto protected Power MOSFET in VIPower technology). They have built-in thermal shutdown, linear current limitation and overvoltage clamping. Fault feedback for thermal intervention can be detected by monitoring the voltage at the input pin.

Features

Type	R _{DS(on)}	I _{OUT}	V _{CC}
VN772KP-E	125 mΩ ⁽¹⁾	9 A ⁽²⁾	36 V

1. Total resistance of one side in bridge configuration
2. Typical current limitation value

- ECOPACK[®]: lead free and RoHS compliant
- Automotive Grade: compliant with AEC guidelines
- Suited as low voltage bridge
- Linear current limitation
- Very low standby power dissipation
- Short circuit protected
- Status flag diagnostic (open drain)
- Integrated clamping circuits
- Undervoltage protection
- ESD protection

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
SO-28	VN772KP-E	VN772KPTR-E

Contents

- 1 Block diagram and pin description 6**
- 2 Electrical specifications 8**
 - 2.1 Thermal data 8
 - 2.2 Absolute maximum ratings 8
 - 2.3 Electrical characteristics for dual high side switch 9
 - 2.4 Electrical characteristics for low-side switches 11
 - 2.5 Dual high-side switch timing data 13
 - 2.6 Electrical characterization for dual high-side switch 16
 - 2.7 Electrical characterization for low-side switches 19
- 3 Application recommendations 23**
- 4 Thermal data 26**
 - 4.1 SO-28 thermal data 26
 - 4.2 Thermal calculation in clockwise and anti-clockwise operation in steady state mode 27
 - 4.2.1 Thermal resistances definition 27
 - 4.2.2 Thermal calculation in transient mode 27
 - 4.2.3 Single pulse thermal impedance definition 27
 - 4.2.4 Pulse calculation formula 27
- 5 Package mechanical data 30**
 - 5.1 SO-28 mechanical data 30
 - 5.2 SO-28 Packing information 32
- 6 Revision history 33**

List of tables

Table 1.	Device summary	1
Table 2.	Pin definition and function.	7
Table 3.	Thermal data	8
Table 4.	Dual high-side switch	8
Table 5.	Low-side switch	8
Table 6.	Power outputs (per each channel)	9
Table 7.	Switching (per each channel) ($V_{CC} = 13\text{ V}$)	10
Table 8.	Logic input (per each channel)	10
Table 9.	Status pin (per each channel).	10
Table 10.	Protections (per each channel).	10
Table 11.	Open-load detection (per each channel)	11
Table 12.	Off-state	11
Table 13.	On-state	12
Table 14.	Dynamic	12
Table 15.	Switching	12
Table 16.	Source drain diode	12
Table 17.	Protections	13
Table 18.	Truth table.	14
Table 19.	Thermal calculation in clockwise and anti-clockwise operation in steady state mode	27
Table 20.	Thermal parameters	29
Table 21.	SO-28 mechanical data	31
Table 22.	Document revision history	33

List of figures

Figure 1.	Block diagram	6
Figure 2.	Connection diagram	7
Figure 3.	Switching time waveforms	13
Figure 4.	Open-load status timing (with external pull-up)	14
Figure 5.	Over temperature status timing	15
Figure 6.	Off-state output current	16
Figure 7.	Input clamp voltage	16
Figure 8.	High level input current	16
Figure 9.	Input high level voltage	16
Figure 10.	Input low level voltage	16
Figure 11.	Input hysteresis voltage	16
Figure 12.	Overvoltage shutdown	17
Figure 13.	I_{LIM} vs T_{case}	17
Figure 14.	Turn-on voltage slope	17
Figure 15.	Turn-off voltage slope	17
Figure 16.	On-state resistance vs T_{case}	17
Figure 17.	On-state resistance vs V_{CC}	17
Figure 18.	Status leakage current	18
Figure 19.	Status low output voltage	18
Figure 20.	Open-load on-state detection threshold	18
Figure 21.	Open-load off-state voltage detection threshold	18
Figure 22.	Status clamp voltage	18
Figure 23.	Static drain source on resistance	19
Figure 24.	Derating curve	19
Figure 25.	Transconductance	19
Figure 26.	Transfer characteristics	19
Figure 27.	Turn-on current slope ($V_{IN} = 5$ V)	19
Figure 28.	Turn-on current slope ($V_{IN} = 3.5$ V)	19
Figure 29.	Input voltage vs input charge	20
Figure 30.	Capacitance variations	20
Figure 31.	Switching time resistive load ($V_{IN} = 5$ V)	20
Figure 32.	Switching time resistive load ($R_g = 10$ Ω)	20
Figure 33.	Output characteristics	20
Figure 34.	Step response current limit	20
Figure 35.	Source drain diode forward characteristics	21
Figure 36.	Static drain source on resistance vs I_D	21
Figure 37.	Static drain source on resistance vs input voltage ($I_D = 7$ A)	21
Figure 38.	Static drain source on resistance vs input voltage	21
Figure 39.	Normalized input threshold voltage vs temperature	21
Figure 40.	Normalized on resistance vs temperature	21
Figure 41.	Turn-off drain source voltage slope ($V_{IN} = 3.5$ V)	22
Figure 42.	Turn-off drain source voltage slope ($V_{IN} = 5$ V)	22
Figure 43.	Current limit vs junction temperature	22
Figure 44.	Application diagram bridge drivers	23
Figure 45.	Recommended motor operation	24
Figure 46.	Waveforms	25
Figure 47.	SO-28 PC board	26
Figure 48.	Chipset configuration	26

Figure 49.	Auto and mutual $R_{thj-amb}$ vs PCB copper area in open box free air condition	26
Figure 50.	SO-28 HSD thermal impedance junction ambient single pulse	28
Figure 51.	SO-28 LSD thermal impedance junction ambient single pulse.	28
Figure 52.	Thermal fitting model of an H-bridge in SO-28	29
Figure 53.	SO-28 package outline	30
Figure 54.	Tube dimensions (no suffix)	32
Figure 55.	Tape and reel dimensions (suffix "13TR")	32

1 Block diagram and pin description

Figure 1. Block diagram

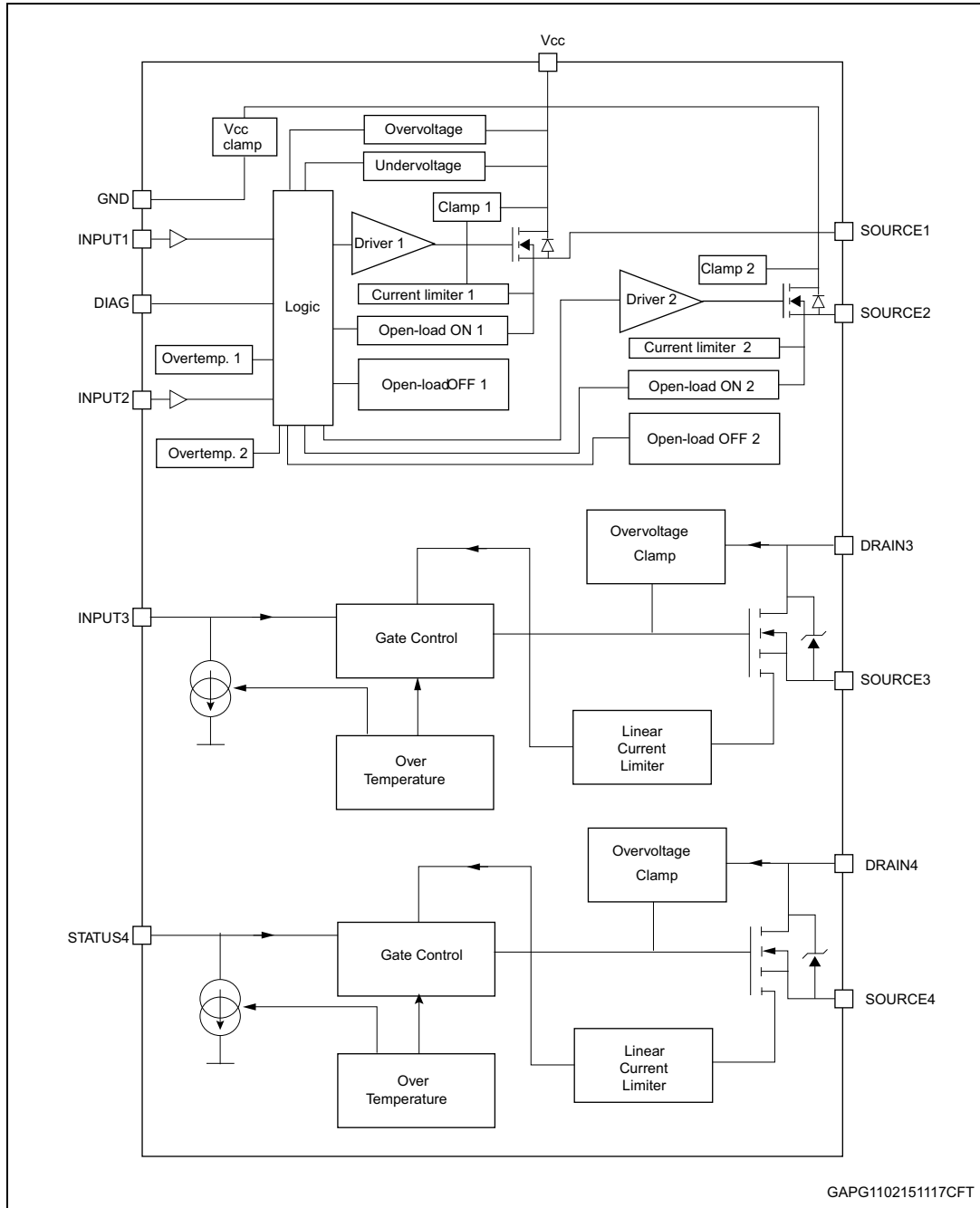
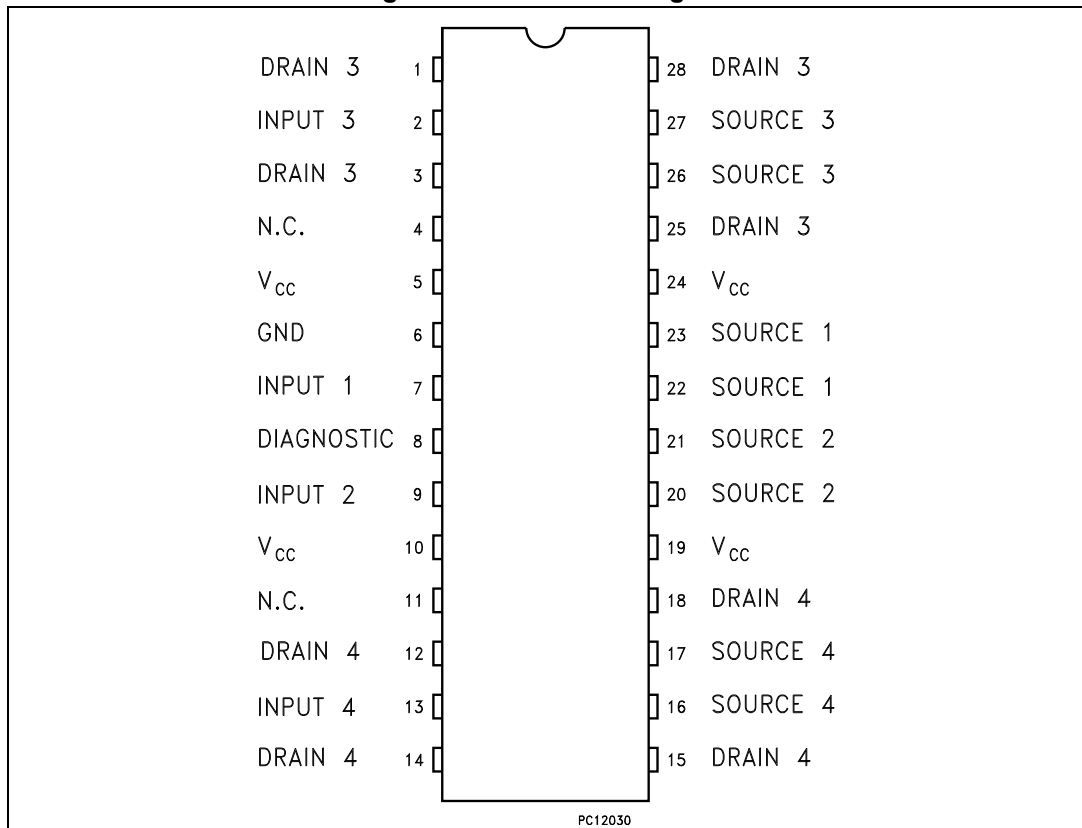


Table 2. Pin definition and function

No	Name	Function
1, 3, 25, 28	DRAIN 3	Drain of switch 3 (low-side switch)
2	INPUT 3	Input of switch 3 (low-side switch)
4, 11	N.C.	Not connected
5, 10, 19, 24	V _{CC}	Drain of switches 1 and 2 (high-side switches) and power supply voltage
6	GND	Ground of switches 1 and 2 (high-side switches)
7	INPUT 1	Input of switch 1 (high-side switches)
8	DIAGNOSTIC	Diagnostic of switches 1 and 2 (high-side switches)
9	INPUT 2	Input of switch 2 (high-side switch)
12, 14, 15, 18	DRAIN 4	Drain of switch 4 (low-side switch)
13	INPUT 4	Input of switch 4 (low-side switch)
16, 17	SOURCE 4	Source of switch 4 (low-side switch)
20, 21	SOURCE 2	Source of switch 2 (high-side switch)
22, 23	SOURCE 1	Source of switch 1 (high-side switch)
26, 27	SOURCE 3	Source of switch 3 (low-side switch)

Figure 2. Connection diagram



2 Electrical specifications

2.1 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value Max (°C/W)
$R_{thj-case}$	Thermal resistance junction-case (high side switch)	20
$R_{thj-case}$	Thermal resistance junction-case (low side switch)	20
$R_{thj-amb}$	Thermal resistance junction-ambient (with 6 cm ² of Cu heat sink)	See Figure 49

2.2 Absolute maximum ratings

Table 4. Dual high-side switch

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	-0.3	V
$-I_{GND}$	DC reverse ground pin current	-200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-6	A
I_{IN}	DC input current	±10	mA
I_{STAT}	DC status current	±10	mA
V_{ESD}	Electrostatic discharge (human body model: R = 1.5 KΩ; C = 100 pF)		
	– Input	4000	V
	– Status	4000	V
	– Output	5000	V
	– V_{CC}	5000	V
P_{tot}	Power dissipation ($T_C = 25\text{ °C}$)	6	W
T_j	Junction operating temperature	Internally limited	°C
T_C	Case operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

Table 5. Low-side switch

Symbol	Parameter	Value	Unit
V_{DS}	Drain source voltage ($V_{IN} = 0\text{ V}$)	Internally clamped	V
V_{IN}	Input voltage	Internally clamped	V
I_{IN}	Input current	±20	mA

Table 5. Low-side switch (continued)

Symbol	Parameter	Value	Unit
$R_{IN\ MIN}$	Minimum input series impedance	150	Ω
I_D	Drain current	Internally limited	A
I_R	Reverse DC output current	-10.5	A
V_{ESD1}	Electrostatic discharge (R = 1.5 K Ω , C = 100 pF)	4000	V
V_{ESD2}	Electrostatic discharge on output pin only (human body model: R = 330 Ω , C = 150 pF)	5000	V
P_{tot}	Power dissipation ($T_C = 25^\circ\text{C}$)	6	W
T_j	Operating junction temperature	Internally limited	$^\circ\text{C}$

2.3 Electrical characteristics for dual high side switch

8 V < V_{CC} < 36 V; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified.

Table 6. Power outputs (per each channel)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{CC}^{(1)}$	Operating supply voltage		5.5	13	36	V
$V_{USD}^{(1)}$	Undervoltage shutdown		3	4	5.5	V
$V_{OV}^{(1)}$	Overvoltage shutdown		36			V
R_{ON}	On-state resistance	$I_{OUT} = 2\ \text{A}; T_j = 25^\circ\text{C}$			60	m Ω
		$I_{OUT} = 2\ \text{A}; V_{CC} > 8\ \text{V}$			120	m Ω
$I_S^{(1)}$	Supply current	Off-state; $V_{CC} = 13\ \text{V}; V_{IN} = V_{OUT} = 0\ \text{V}$		12	40	μA
		Off-state; $V_{CC} = 13\ \text{V}; V_{IN} = V_{OUT} = 0\ \text{V}; T_j = 25^\circ\text{C}$		12	25	μA
		On-state; $V_{CC} = 13\ \text{V}$		5	7	mA
$I_{L(off1)}$	Off-state output current	$V_{IN} = V_{OUT} = 0\ \text{V}; V_{CC} = 36\ \text{V}; T_j = 125^\circ\text{C}$	0		50	μA
$I_{L(off2)}$	Off-state output current	$V_{IN} = 0\ \text{V}; V_{OUT} = 3.5\ \text{V}$	-75		0	μA
$I_{L(off3)}$	Off-state output current	$V_{IN} = V_{OUT} = 0\ \text{V}; V_{CC} = 13\ \text{V}; T_j = 125^\circ\text{C}$			5	μA
$I_{L(off4)}$	Off-state output current	$V_{IN} = V_{OUT} = 0\ \text{V}; V_{CC} = 13\ \text{V}; T_j = 25^\circ\text{C}$			3	μA

1. Per device.

Table 7. Switching (per each channel) ($V_{CC} = 13\text{ V}$)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 6.5\ \Omega$ from V_{IN} rising edge to $V_{OUT} = 1.3\text{ V}$	—	30	—	μs
$t_{d(off)}$	Turn-off delay time	$R_L = 6.5\ \Omega$ from V_{IN} falling edge to $V_{OUT} = 11.7\text{ V}$	—	30	—	μs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 6.5\ \Omega$ from $V_{OUT} = 1.3\text{ V}$ to $V_{OUT} = 10.4\text{ V}$	—	(1)	—	$\text{V}/\mu\text{s}$
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 6.5\ \Omega$ from $V_{OUT} = 11.7\text{ V}$ to $V_{OUT} = 1.3\text{ V}$	—	(1)	—	$\text{V}/\mu\text{s}$

1. See relative diagram

Table 8. Logic input (per each channel)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IL}	Input low level				1.25	V
I_{IL}	Low level input current	$V_{IN} = 1.25\text{ V}$	1			μA
V_{IH}	Input high level		3.25			V
I_{IH}	High level input current	$V_{IN} = 3.25\text{ V}$			10	μA
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	$I_{IN} = 1\text{ mA}$	6	6.8	8	V
		$I_{IN} = -1\text{ mA}$		-0.7		V

Table 9. Status pin (per each channel)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{STAT}	Status low output voltage	$I_{STAT} = 1.6\text{ mA}$			0.5	V
I_{LSTAT}	Status leakage current	Normal operation; $V_{STAT} = 5\text{ V}$			10	μA
C_{STAT}	Status pin input capacitance	Normal operation; $V_{STAT} = 5\text{ V}$			100	pF
V_{SCL}	Status clamp voltage	$I_{STAT} = 1\text{ mA}$	6	6.8	8	V
		$I_{STAT} = -1\text{ mA}$		-0.7		V

Table 10. Protections (per each channel)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
T_{TSD}	Shutdown temperature		150	175	200	$^{\circ}\text{C}$
T_R	Reset temperature		135			$^{\circ}\text{C}$
T_{hyst}	Thermal hysteresis		7	15		$^{\circ}\text{C}$
t_{SDL}	Status delay in overload conditions	$T_j > T_{TSD}$			20	μs

Table 10. Protections (per each channel) (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{lim}	Current limitation		6	9	15	A
		$T_j = 125^\circ\text{C}$	8.5		15	A
		$5.5\text{ V} < V_{CC} < 36\text{ V}$			15	A
V_{demag}	Turn-off output clamp voltage	$I_{OUT} = 2\text{ A}; L = 6\text{ mH}$	$V_{CC} - 41$	$V_{CC} - 48$	$V_{CC} - 55$	V

Note: To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 11. Open-load detection (per each channel)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{OL}	Open-load on-state detection threshold	$V_{IN} = 5\text{ V}$	50	100	200	mA
$t_{DOL(on)}$	Open-load on-state detection delay	$I_{OUT} = 0\text{ A}$			200	μs
V_{OL}	Open-load off-state voltage detection threshold	$V_{IN} = 0\text{ V}$	1.5	2.5	3.5	V
$t_{DOL(off)}$	Open-load detection delay at turn-off				1000	μs

2.4 Electrical characteristics for low-side switches

$-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified.

Table 12. Off-state

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CLAMP}	Drain source clamp voltage	$V_{IN} = 0\text{ V}; I_D = 3.5\text{ A}$	40	45	55	V
V_{CLTH}	Drain source clamp threshold voltage	$V_{IN} = 0\text{ V}; I_D = 2\text{ mA}$	36			V
V_{INTH}	Input threshold voltage	$V_{DS} = V_{IN}; I_D = 1\text{ mA}$	0.5		2.5	V
I_{ISS}	Supply current from input pin	$V_{DS} = 0\text{ V}; V_{IN} = 5\text{ V}$		100	150	μA
V_{INCL}	Input-source clamp voltage	$I_{IN} = 1\text{ mA}$	6	6.8	8	V
		$I_{IN} = -1\text{ mA}$	-1.0		-0.3	V
I_{DSS}	Zero input voltage drain current ($V_{IN} = 0\text{ V}$)	$V_{DS} = 13\text{ V}; V_{IN} = 0\text{ V}; T_j = 25^\circ\text{C}$			30	μA
		$V_{DS} = 25\text{ V}; V_{IN} = 0\text{ V}$			75	μA

Table 13. On-state

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
R _{DS(on)}	Static drain source on resistance	V _{IN} = 5 V; I _D = 3.5 A; T _j = 25°C	—	—	65	mΩ
		V _{IN} = 5 V; I _D = 3.5 A	—	—	130	mΩ

T_j = 25°C, unless otherwise specified.

Table 14. Dynamic

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
g _{fs} ⁽¹⁾	Forward trans conductance	V _{DD} = 13 V; I _D = 3.5 A	—	9	—	S
C _{OSS}	Output capacitance	V _{DS} = 13 V; f = 1 MHz; V _{IN} = 0 V	—	220	—	pF

1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5%

Table 15. Switching

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 15 V; I _D = 3.5 A; V _{gen} = 5 V; R _{gen} = R _{IN MIN} = 150 Ω	—	100	300	ns
t _r	Rise time		—	470	1500	ns
t _{d(off)}	Turn-off delay time		—	500	1500	ns
t _f	Fall time		—	350	1000	ns
t _{d(on)}	Turn-on delay time	V _{DD} = 15 V; I _D = 3.5 A; V _{gen} = 5 V; R _{gen} = 2.2 kΩ	—	0.75	2.3	μs
t _r	Rise time		—	4.6	14	μs
t _{d(off)}	Turn-off delay time		—	5.4	16	μs
t _f	Fall time		—	3.6	11	μs
(di/dt) _{on}	Turn-on current slope	V _{DD} = 15 V; I _D = 3.5 A; V _{gen} = 5 V; R _{gen} = R _{IN MIN} = 150 Ω	—	6.5		A/μs
Q _i	Total input charge	V _{DD} = 12 V; I _D = 3.5 A; V _{IN} = 5 V; I _{gen} = 2.13 mA	—	18		nC

Table 16. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V _{SD} ⁽¹⁾	Forward on voltage	I _{SD} = 3.5 A; V _{IN} = 0 V	—	0.8	—	V
t _{rr}	Reverse recovery time	I _{SD} = 3.5 A; di/dt = 20 A/μs; V _{DD} = 30 V; L = 200 μH	—	220	—	ns
Q _{rr}	Reverse recovery charge		—	0.28	—	μC
I _{RRM}	Reverse recovery current		—	2.5	—	A

1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5%

-40 °C < T_j < 150 °C, unless otherwise specified.

Table 17. Protections

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I _{lim}	Drain current limit	V _{IN} = 5 V; V _{DS} = 13 V	6	9	12	A
		V _{IN} = 5 V; V _{DS} = 13 V; T _j = 125°C	6.5		12	A
t _{dlim}	Step response current limit	V _{IN} = 5 V; V _{DS} = 13 V		4		µs
T _{jsh}	Overtemperature shutdown		150	175		°C
T _{jrs}	Overtemperature reset		135			°C
I _{gf}	Fault sink current	V _{IN} = 5 V; V _{DS} = 13 V; T _j = T _{jsh}		15		mA
E _{as}	Single pulse avalanche energy	Starting T _j = 25 °C; V _{DD} = 24 V; V _{IN} = 5 V; R _{gen} = R _{IN MIN} = 150 Ω; L = 24 mH	200			mJ

2.5 Dual high-side switch timing data

Figure 3. Switching time waveforms

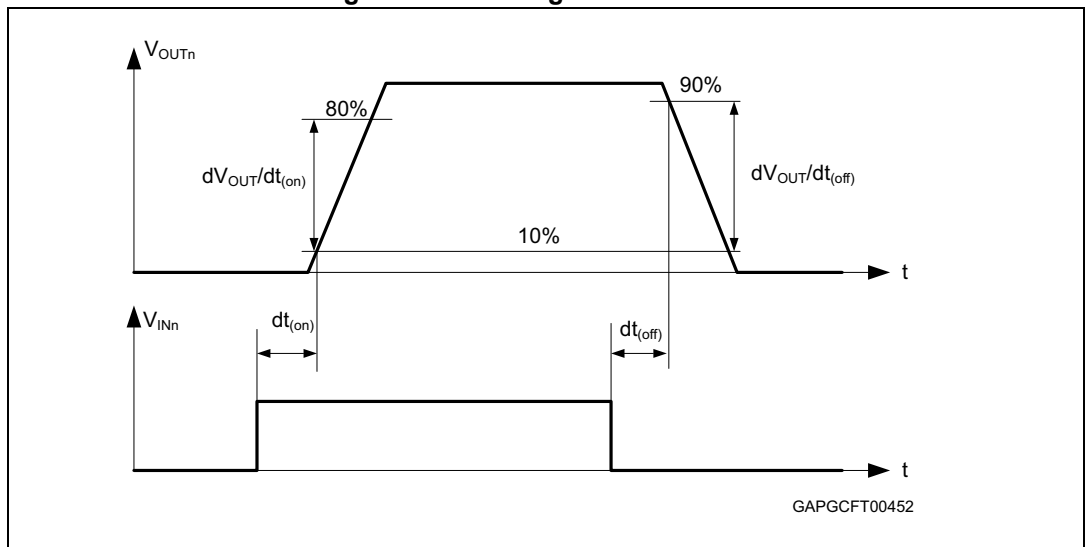


Table 18. Truth table

Conditions	Input	Output	Status
Normal operation	L	L	H
	H	H	H
Current limitation	L	L	H
	H	X	($T_j < T_{TSD}$) H ($T_j > T_{TSD}$) L
Over temperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H
Output voltage $> V_{OL}$	L	H	L
	H	H	H
Output current $< I_{OL}$	L	L	H
	H	H	L

Figure 4. Open-load status timing (with external pull-up)

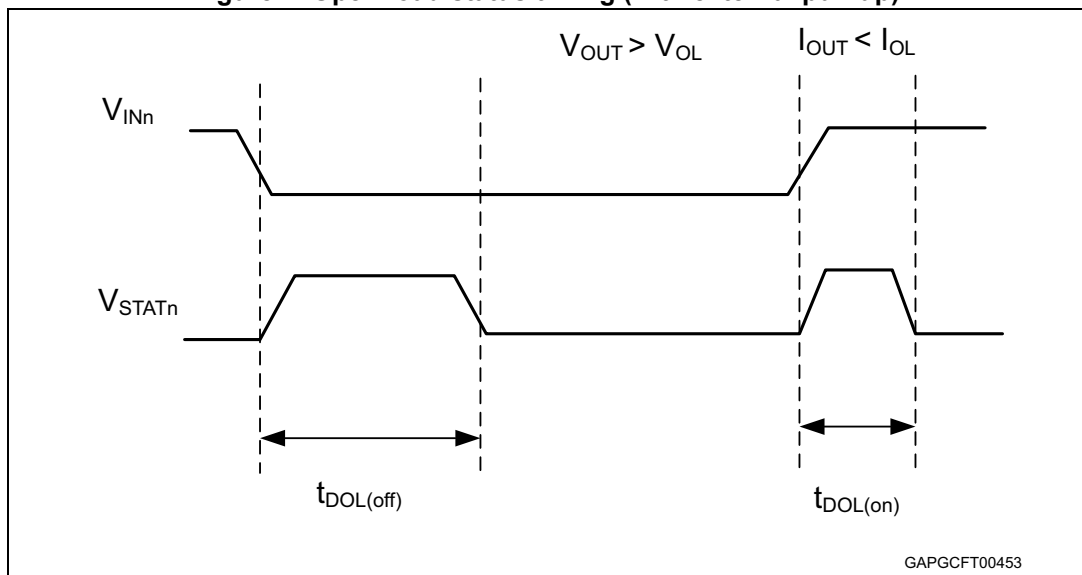
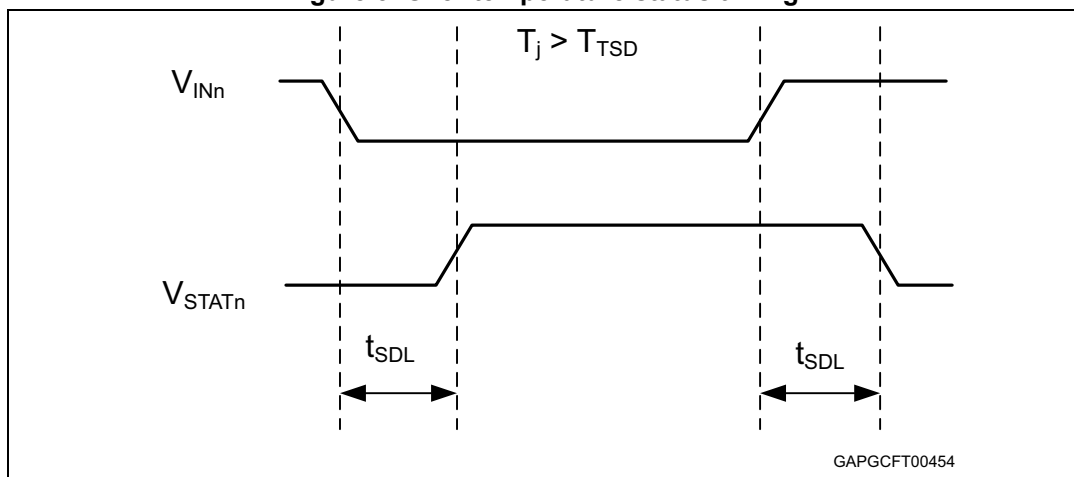
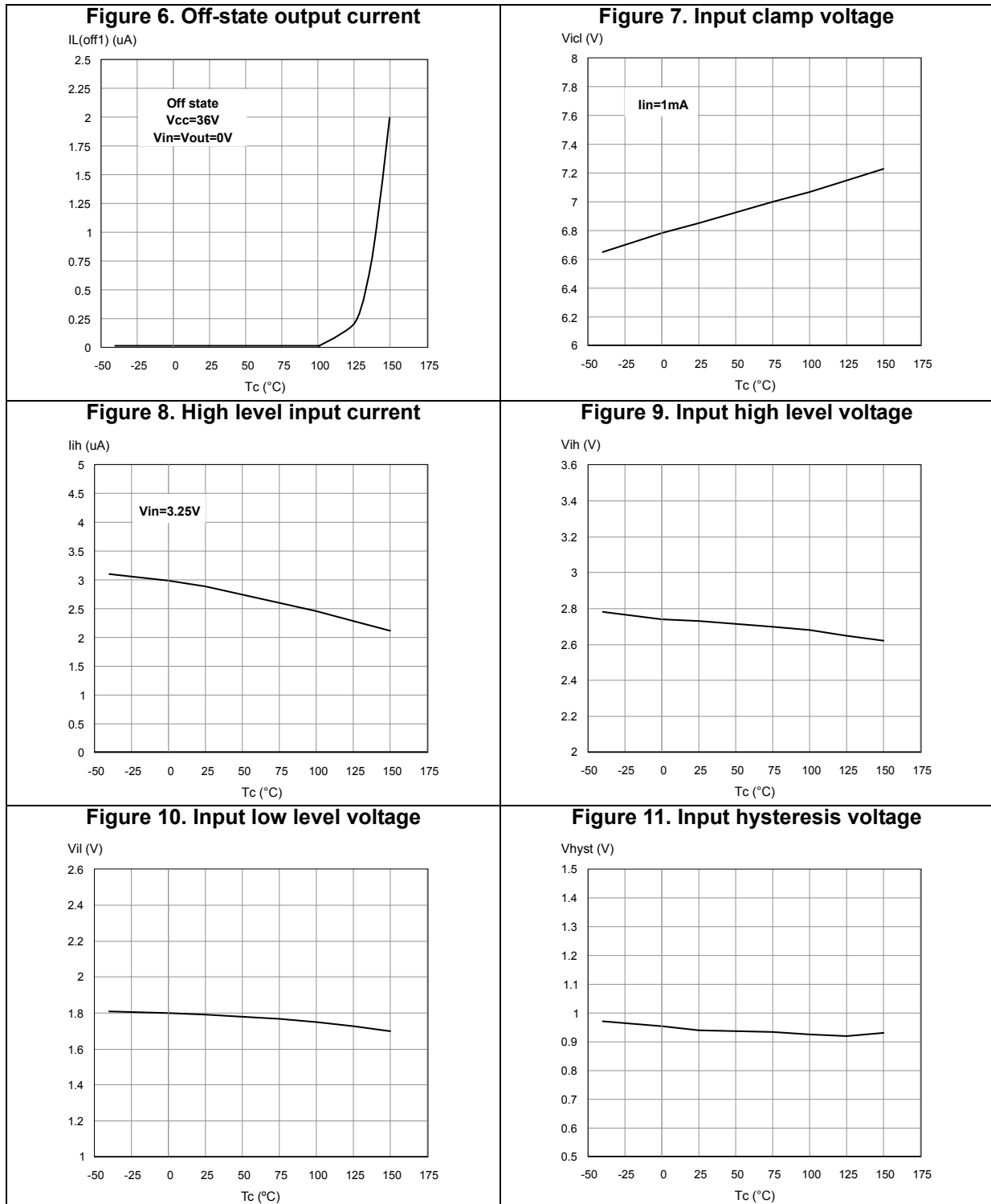
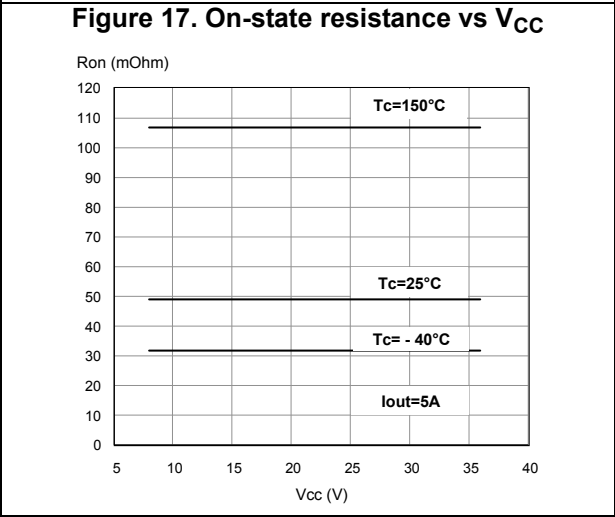
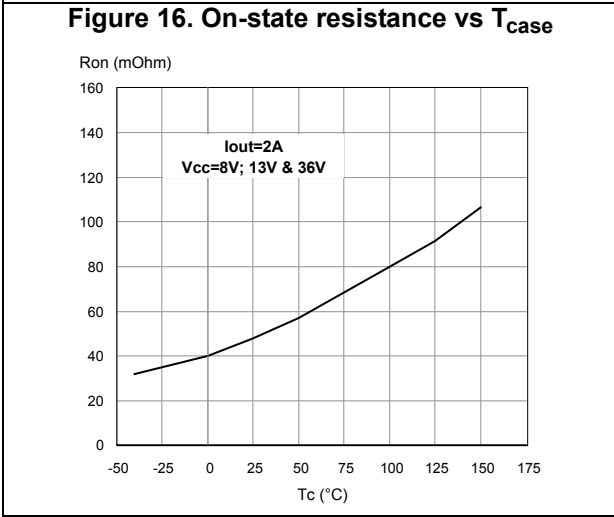
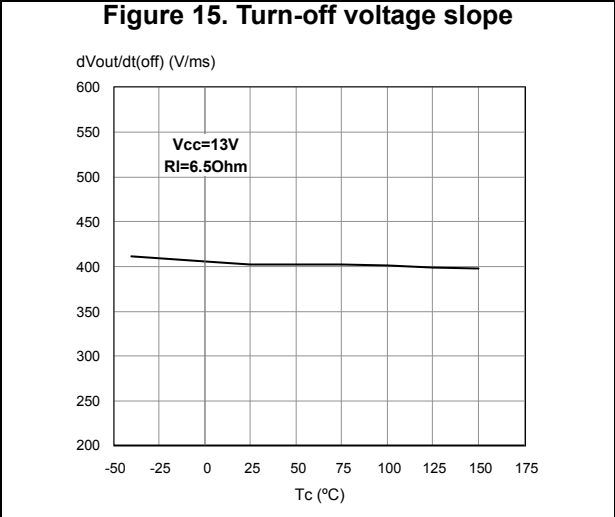
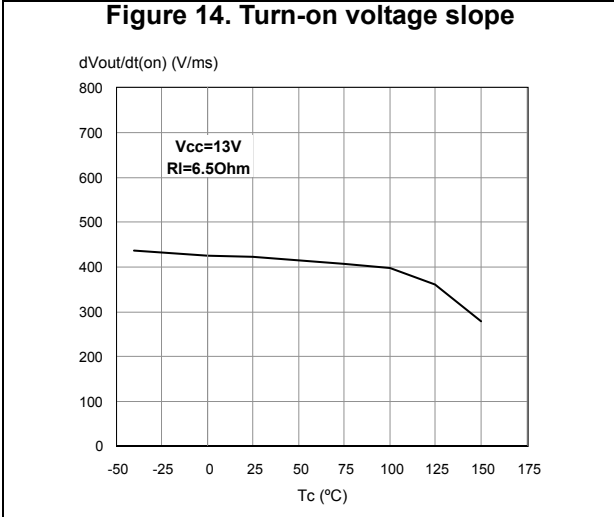
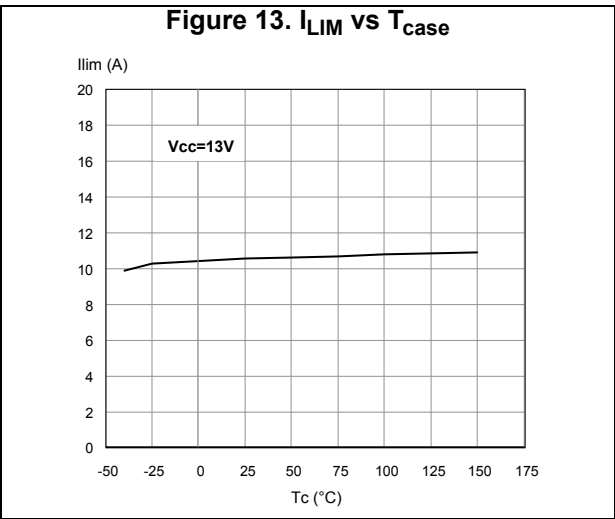
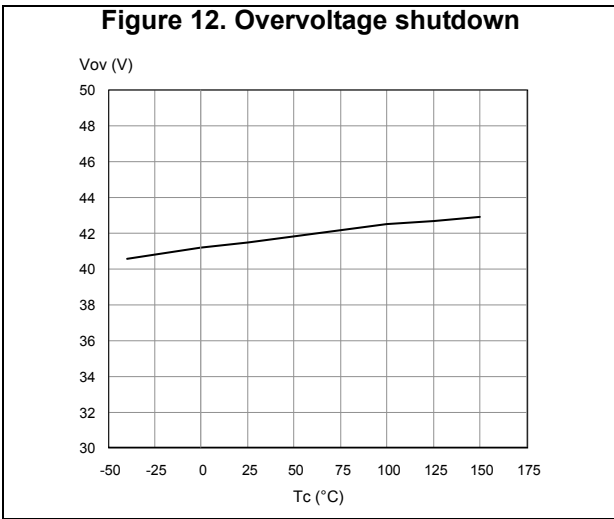


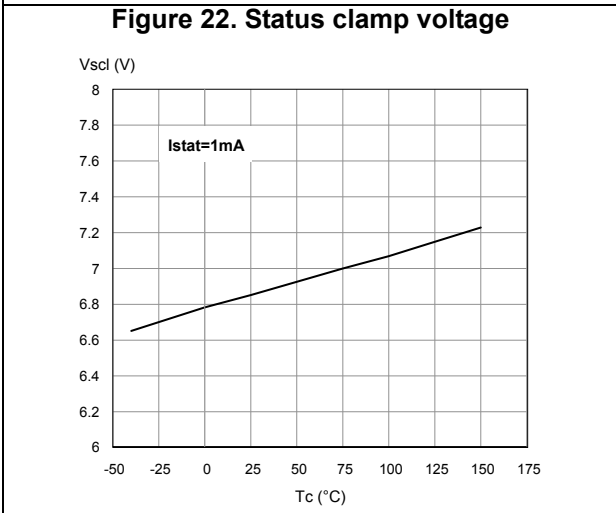
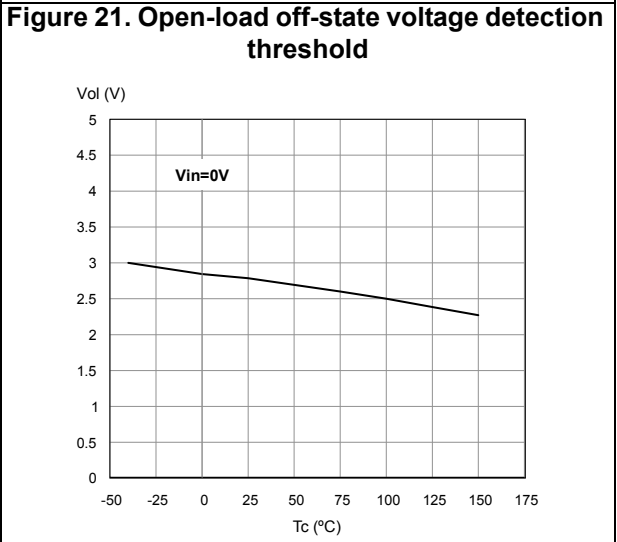
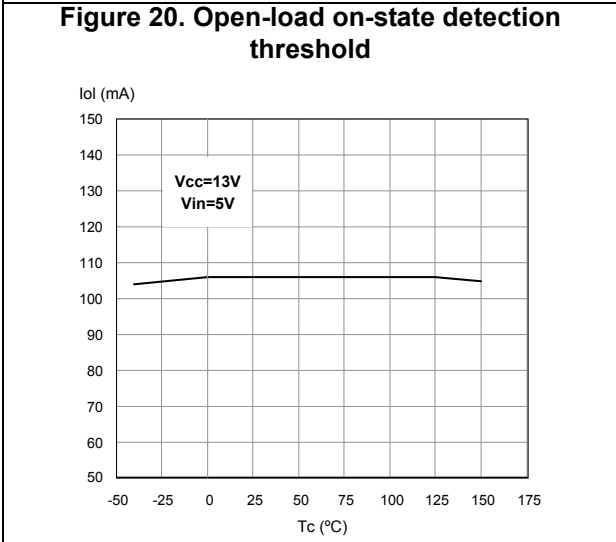
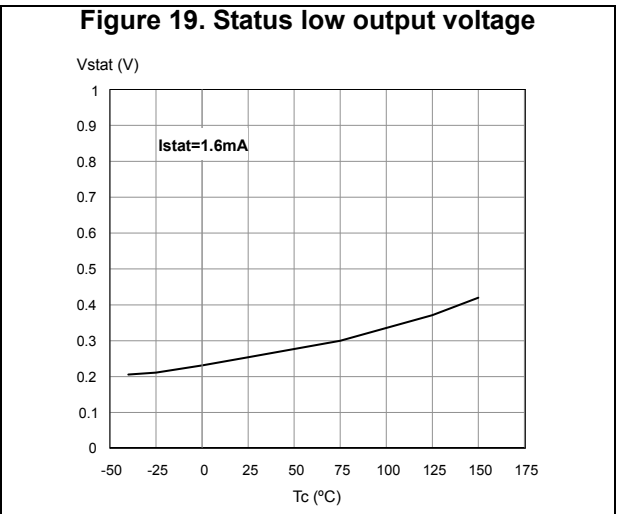
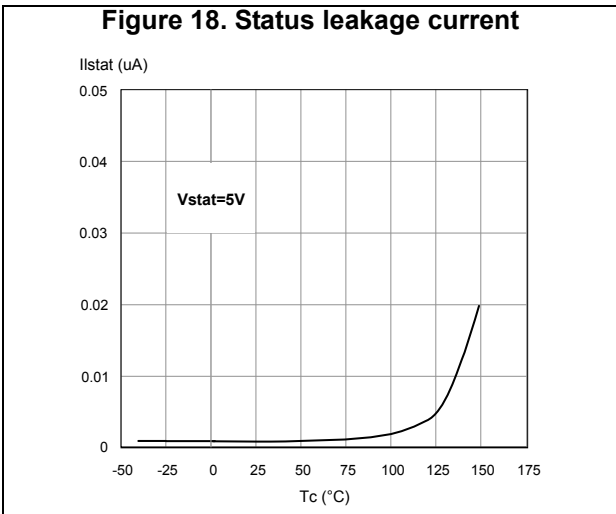
Figure 5. Over temperature status timing



2.6 Electrical characterization for dual high-side switch







2.7 Electrical characterization for low-side switches

Figure 23. Static drain source on resistance

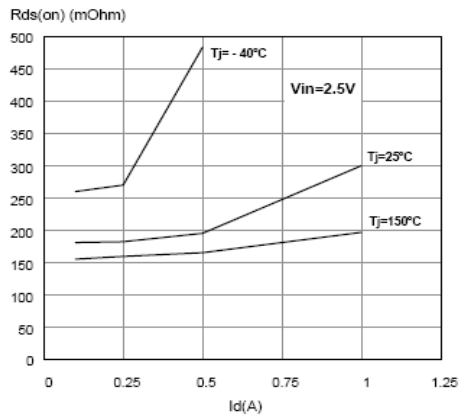


Figure 24. Derating curve

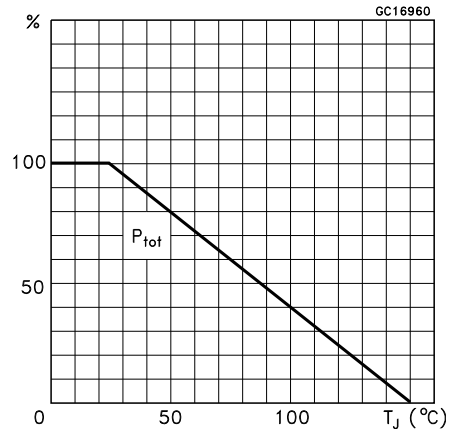


Figure 25. Transconductance

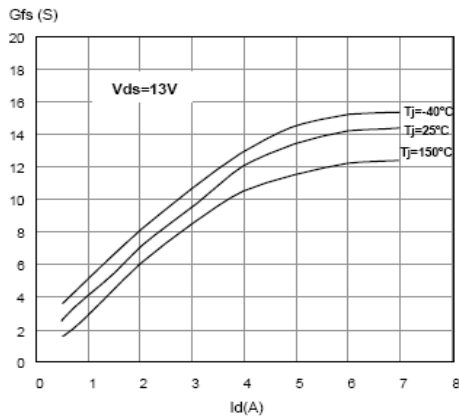


Figure 26. Transfer characteristics

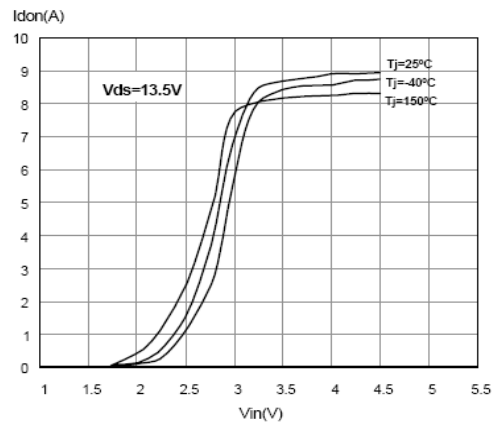


Figure 27. Turn-on current slope ($V_{IN} = 5\text{ V}$)

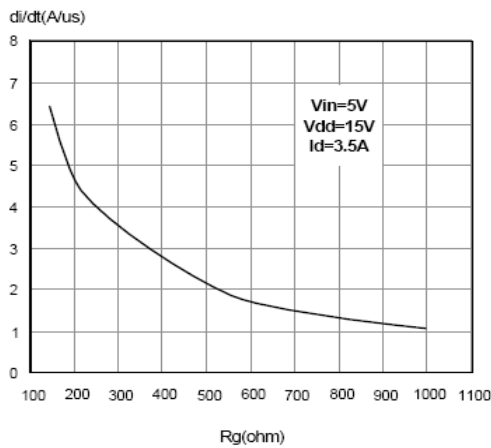


Figure 28. Turn-on current slope ($V_{IN} = 3.5\text{ V}$)

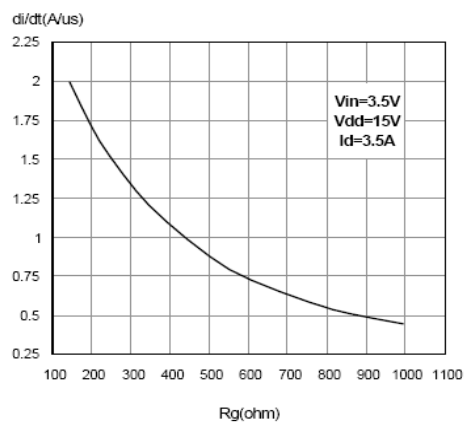


Figure 29. Input voltage vs input charge

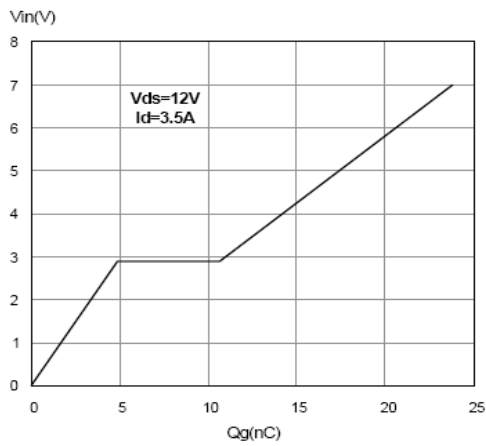


Figure 30. Capacitance variations

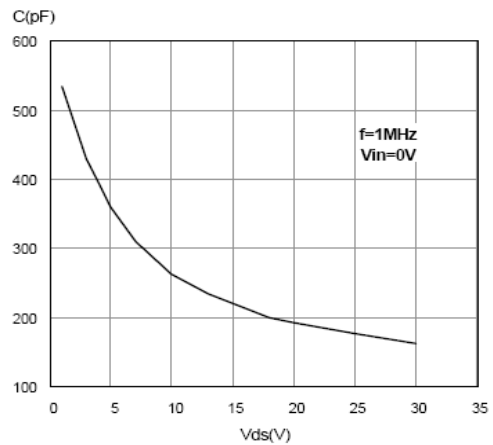


Figure 31. Switching time resistive load ($V_{IN} = 5 V$)

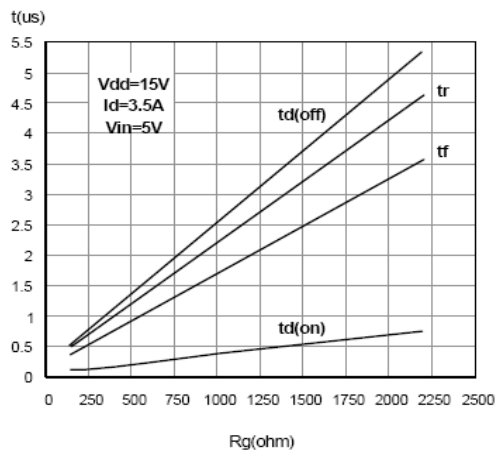


Figure 32. Switching time resistive load ($R_g = 10 \Omega$)

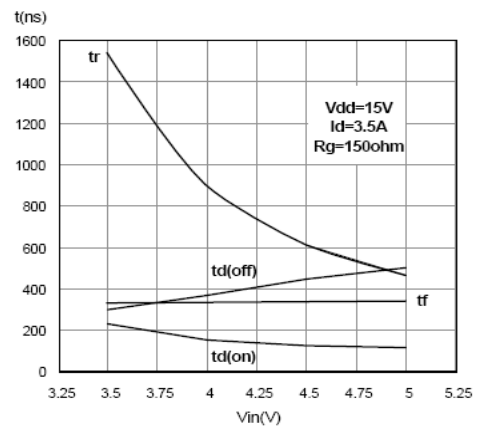


Figure 33. Output characteristics

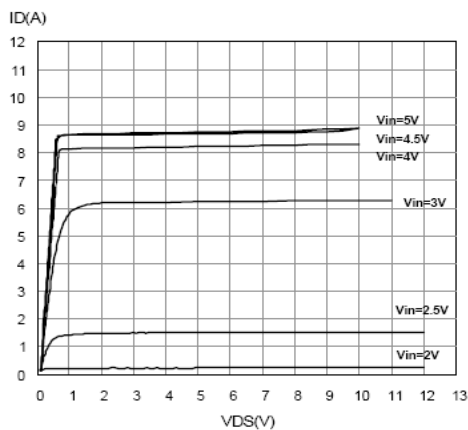


Figure 34. Step response current limit

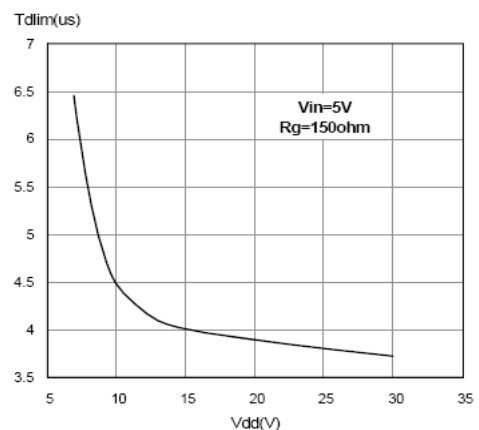


Figure 35. Source drain diode forward characteristics

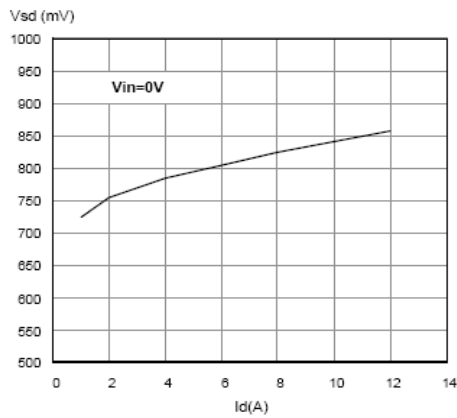


Figure 36. Static drain source on resistance vs I_D

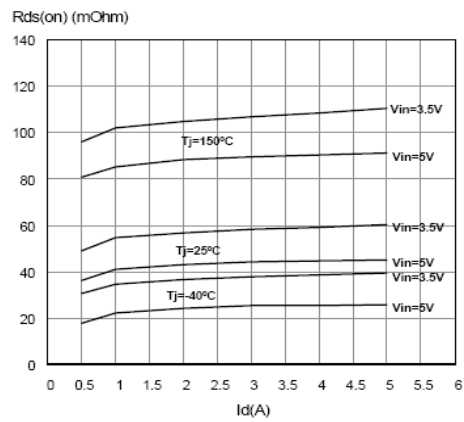


Figure 37. Static drain source on resistance vs input voltage ($I_D = 7 A$)

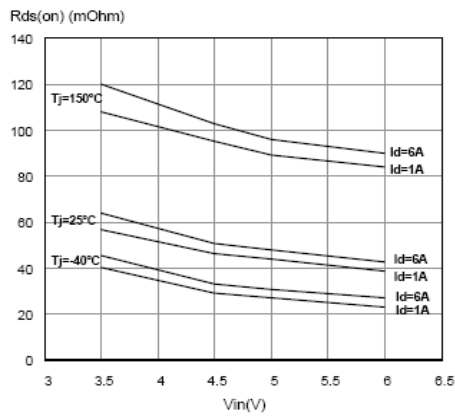


Figure 38. Static drain source on resistance vs input voltage

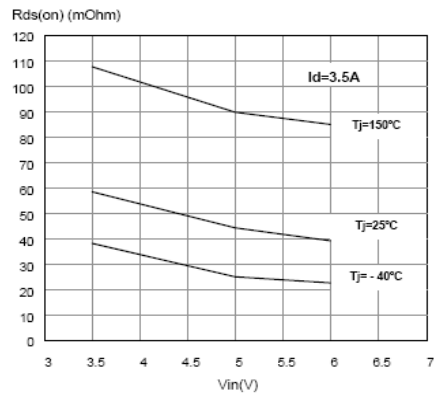


Figure 39. Normalized input threshold voltage vs temperature

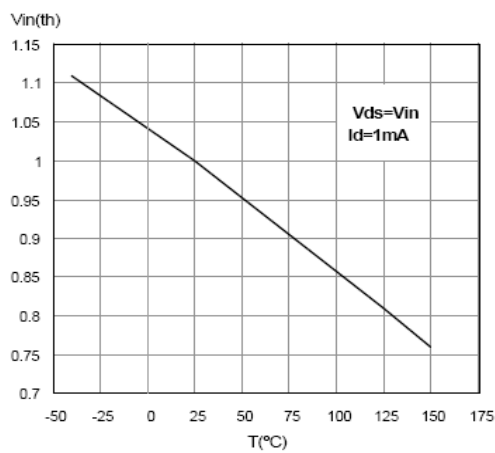


Figure 40. Normalized on resistance vs temperature

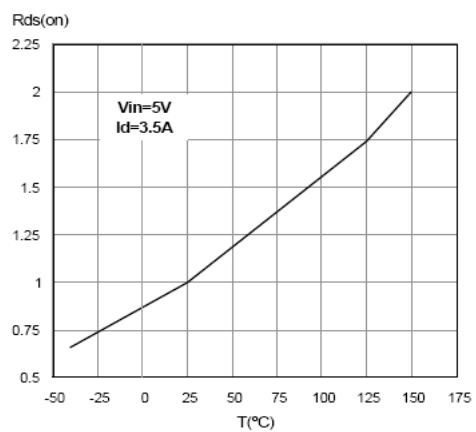


Figure 41. Turn-off drain source voltage slope ($V_{IN} = 3.5\text{ V}$)

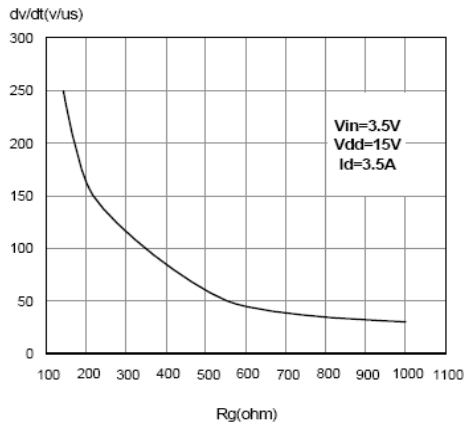


Figure 42. Turn-off drain source voltage slope ($V_{IN} = 5\text{ V}$)

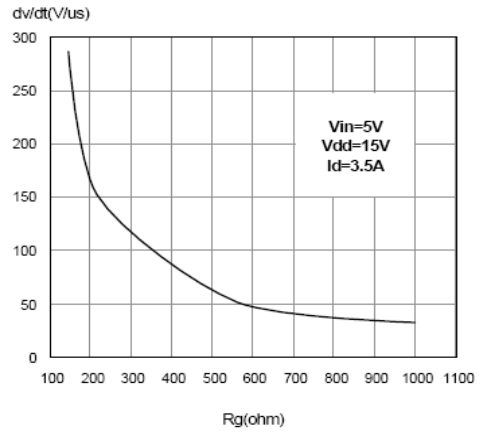
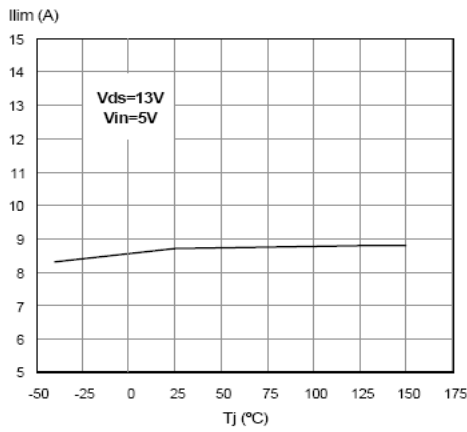
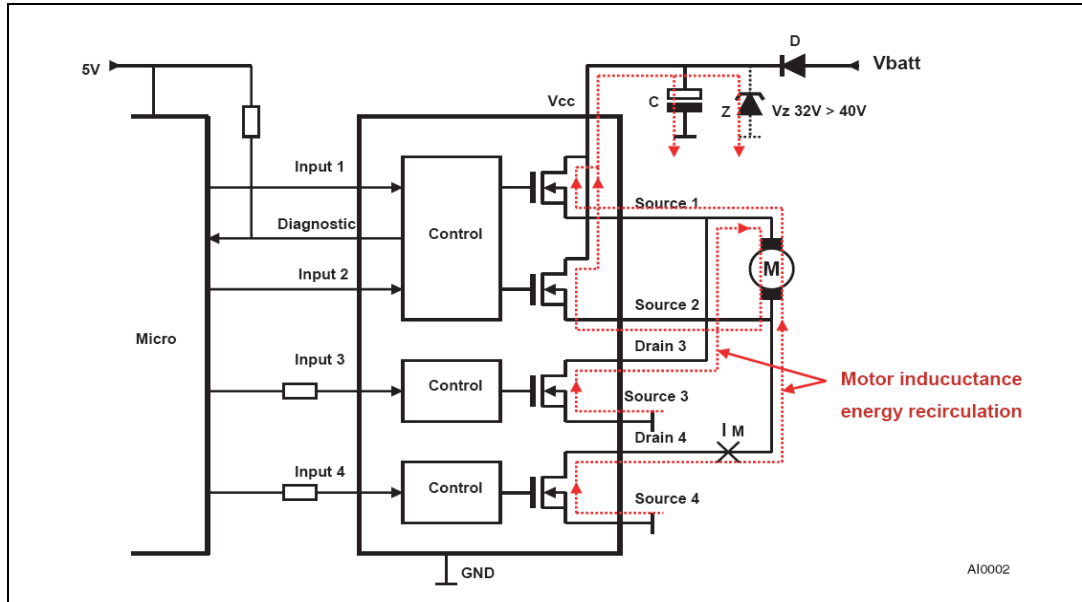


Figure 43. Current limit vs junction temperature



3 Application recommendations

Figure 44. Application diagram bridge drivers



Most motor bridge drivers use a reverse battery protection diode (D) inside the supply rail. This diode prevents a reverse current flow back to V_{BATT} in case the bridge becomes disabled via the logic inputs while motor inductance still carries energy. In order to prevent a hazardous overvoltage at circuit supply terminal (V_{CC}), a blocking capacitor (C) is needed to limit the voltage overshoot. As basic orientation, 50 μF per 1 A load current is recommended. As an alternative, a Zener protection (Z) is also suitable.

Even if a reverse polarity diode is not present, it is recommended to use a capacitor or Zener at V_{CC} because a similar problem appears in case the supply terminal of the module has intermittent electrical contact to the battery or gets disconnected while the motor is operating.

Figure 45. Recommended motor operation

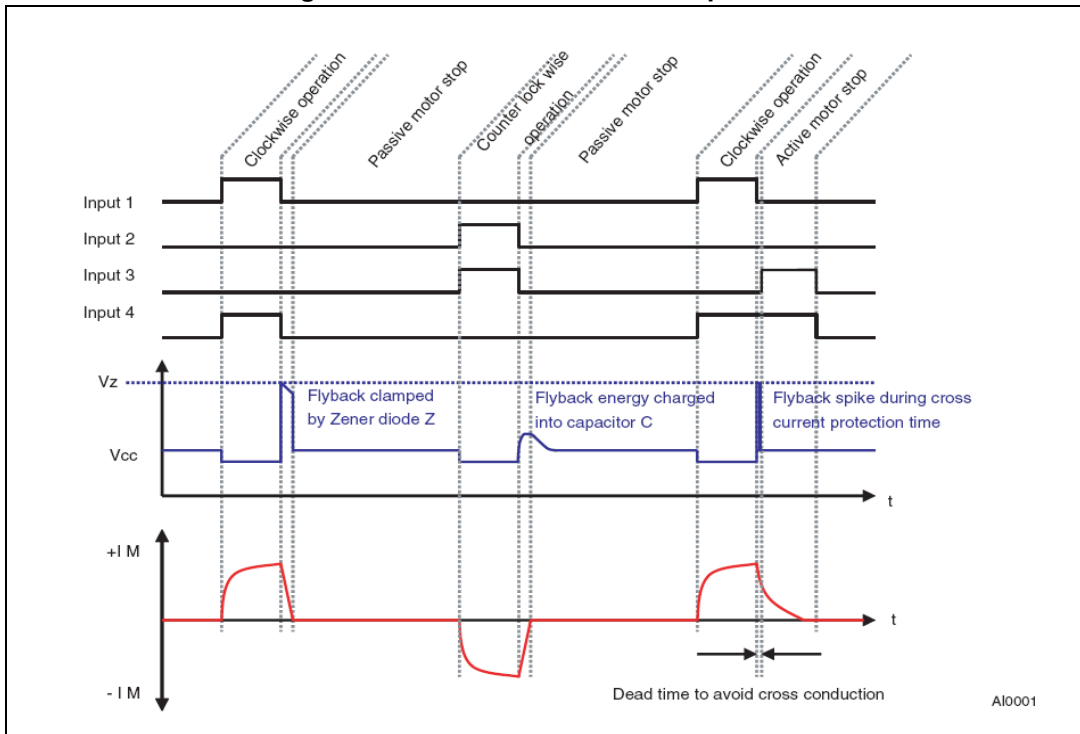


Figure 46. Waveforms

