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VNB14N04 - VNK14N04FM VNV14N04

"OMNIFET"
fully autoprotected Power MOSFET

Features

Type	V _{clamp}	R _{DS(on)}	I _{lim}
VNB14N04	42 V	0.07 Ω	14 A
VNK14N04FM	42 V	0.07 Ω	14 A
VNV14N04	42 V	0.07 Ω	14 A

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the power MOSFET (analog driving)
- Compatible with standard power MOSFET



Description

The VNB14N04, VNK14N04FM and VNV14N04 are monolithic devices made using STMicroelectronics VIPower M0 Technology, intended for replacement of standard power MOSFETS in DC to 50 kHz applications. Built-in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environment.

Fault feedback can be detected by monitoring the voltage at the input pin.

Table 1. Device summary

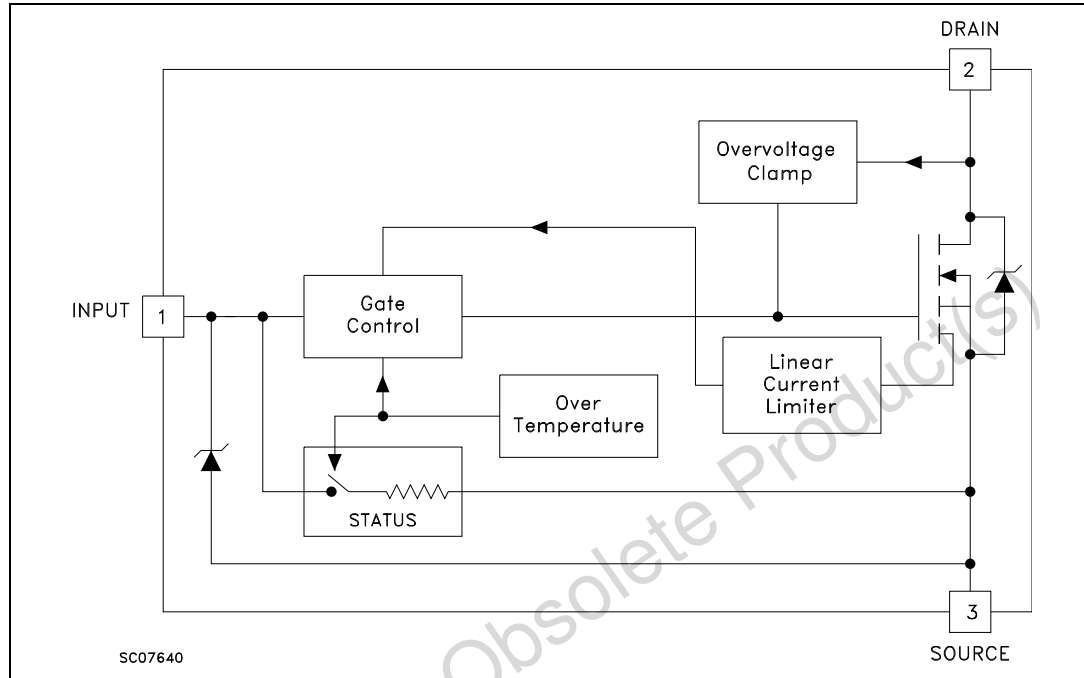
Part number	Order code
VNB14N04	VNB14N04, VNB14N04-E, VNB14N0413TR, VNB14N04TR-E
VNK14N04FM	VNK14N04FM
VNV14N04	VNV14N04, VNV14N04-E

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1 Block diagram

Figure 1. Block diagram



1. PowerSO-10 pin configuration : INPUT = 6,7,8,9,10; SOURCE = 1,2,4,5; DRAIN = TAB

2 Electrical specification

2.1 Absolute maximum rating

Table 2. Absolute maximum rating

Symbol	Parameter	Value		Unit
		PowerSO-10 D2PAK	SOT-82FM	
V _{DS}	Drain-source voltage (V _{in} = 0)	Internally clamped		V
V _{in}	Input voltage	18		V
I _D	Drain current	Internally limited		A
I _R	Reverse DC output current	-14		A
V _{esd}	Electrostatic discharge (C = 100 pF, R=1.5 KΩ)	2000		V
P _{tot}	Total dissipation at T _c = 25 °C	50	9.5	W
T _j	Operating junction temperature	Internally limited		°C
T _c	Case operating temperature	Internally limited		°C
T _{stg}	Storage temperature	-55 to 150		°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	PowerSO-10	SOT82-FM	D2PAK	Unit
R _{thj-case}	Thermal resistance junction-case max	2.5	13	2.5	°C/W
R _{thj-amb}	Thermal resistance junction-ambient max	50	100	62.5	°C/W

2.3 Electrical characteristics

T_{case} = 25 °C unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Off						
V _{CLAMP}	Drain-source clamp voltage	I _D = 200 mA V _{in} = 0	36	42	48	V
V _{CLTH}	Drain-source clamp threshold voltage	I _D = 2 mA V _{in} = 0	35			V
V _{INCL}	Input-source reverse clamp voltage	I _{in} = -1 mA	-1		-0.3	V

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
I_{DSS}	Zero input voltage drain current ($V_{in} = 0$)	$V_{DS} = 13\text{ V } V_{in} = 0$			50	μA	
		$V_{DS} = 25\text{ V } V_{in} = 0$			200	μA	
I_{ISS}	Supply current from input pin	$V_{DS} = 0\text{ V } V_{in} = 10\text{ V}$		250	500	μA	
On⁽¹⁾							
$V_{IN(th)}$	Input threshold voltage	$V_{DS} = V_{in} I_D + I_{in} = 1\text{ mA}$	0.8		3	V	
$R_{DS(on)}$	Static drain-source on resistance	$V_{in} = 10\text{ V } I_D = 7\text{ A}$			0.7	Ω	
		$V_{in} = 5\text{ V } I_D = 7\text{ A}$			0.1	Ω	
Dynamic							
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 13\text{ V } I_D = 7\text{ A}$	8	10		S	
C_{OSS}	Output capacitance	$V_{DS} = 13\text{ V } f = 1\text{ MHz } V_{in} = 0$		400	500	pF	
Switching⁽²⁾							
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V } I_d = 7\text{ A}$ $V_{gen} = 10\text{ V } R_{gen} = 10\ \Omega$ (see Figure 26)			60	120	ns
					t_r	Rise time	160
$t_{d(off)}$	Turn-off delay time				250	400	ns
					t_f	Fall time	100
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V } I_d = 7\text{ A}$ $V_{gen} = 10\text{ V } R_{gen} = 1000\ \Omega$ (see Figure 26)			300	500	ns
					t_r	Rise time	1.5
$t_{d(off)}$	Turn-off delay time				5.5	7.5	μs
					t_f	Fall time	1.8
$(di/dt)_{on}$	Turn-on current slope	$V_{DD} = 15\text{ V } I_D = 7\text{ A}$ $V_{in} = 10\text{ V } R_{gen} = 10\ \Omega$		120		A/ μs	
Q_i	Total input charge	$V_{DD} = 12\text{ V } I_D = 7\text{ A } V_{in} = 10\text{ V}$		30		nC	
Source drain diode							
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 7\text{ A } V_{in} = 0$			1.6	V	
$t_{rr}^{(2)}$	Reverse recovery time	$I_{SD} = 7\text{ A } di/dt = 100\text{ A}/\mu\text{s}$		110		ns	
$Q_{rr}^{(2)}$	Reverse recovery charge	$V_{DD} = 30\text{ V } T_j = 25\text{ }^\circ\text{C}$		0.34		μC	
$I_{RRM}^{(2)}$	Reverse recovery current	(see test circuit, Figure 28)		6.1		A	
Protection							
I_{lim}	Drain current limit	$V_{in} = 10\text{ V } V_{DS} = 13\text{ V}$	10	14	20	A	
		$V_{in} = 5\text{ V } V_{DS} = 13\text{ V}$	10	14	20	A	
$t_{dlim}^{(2)}$	Step response Current limit	$V_{in} = 10\text{ V}$		30	60	μs	
		$V_{in} = 5\text{ V}$		80	150	μs	
$T_{jsh}^{(2)}$	Overtemperature shutdown		150			$^\circ\text{C}$	
$T_{jrs}^{(2)}$	Overtemperature reset		135			$^\circ\text{C}$	

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{gf}^{(2)}$	Fault sink current	$V_{in} = 10\text{ V } V_{DS} = 13\text{ V}$ $V_{in} = 5\text{ V } V_{DS} = 13\text{ V}$		50 20		mA mA
$E_{as}^{(2)}$	Single pulse avalanche energy	starting $T_j = 25^\circ\text{C } V_{DD} = 20\text{ V}$ $V_{in} = 10\text{ V } R_{gen} = 1\text{ K}\Omega L = 10\text{ mH}$	0.65			J

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %
2. Parameters guaranteed by design/characterization

Obsolete Product(s) - Obsolete Product(s)

3 Protection features

During normal operation, the Input pin is electrically connected to the gate of the internal power MOSFET. The device then behaves like a standard power MOSFET and can be used as a switch from DC to 50 kHz. The only difference from the user's standpoint is that a small DC current (I_{ISS}) flows into the Input pin in order to supply the internal circuitry.

The device integrates:

- Overvoltage clamp protection: internally set at 42 V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- Linear current limiter circuit: limits the drain current I_D to I_{lim} whatever the Input pin voltage. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh} .
- Overtemperature and short circuit protection: these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs at minimum 150 °C. The device is automatically restarted when the chip temperature falls below 135 °C.
- Status feedback: in the case of an overtemperature fault condition, a Status Feedback is provided through the Input pin. The internal protection circuit disconnects the input from the gate and connects it instead to ground via an equivalent resistance of 100 Ω. The failure can be detected by monitoring the voltage at the Input pin, which will be close to ground potential.

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit (with a small increase in $R_{DS(on)}$).

Figure 2. Thermal impedance for D2PAK/PowerSO-10

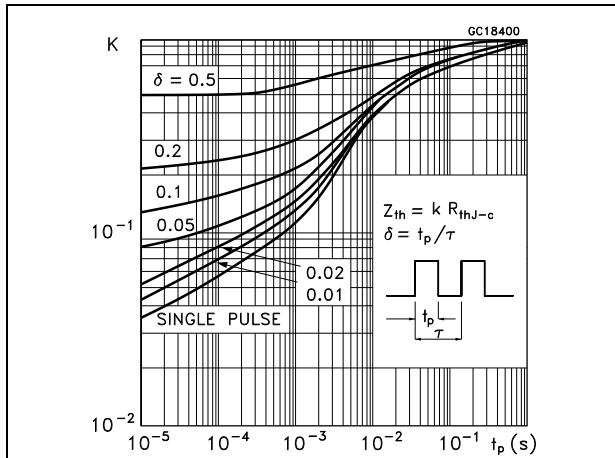


Figure 3. Derating curve

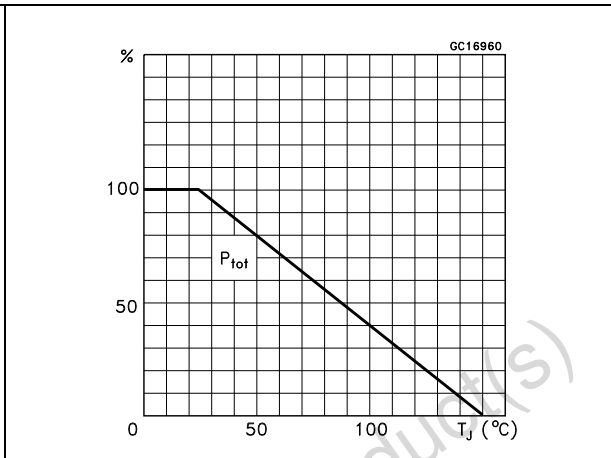


Figure 4. Output characteristics

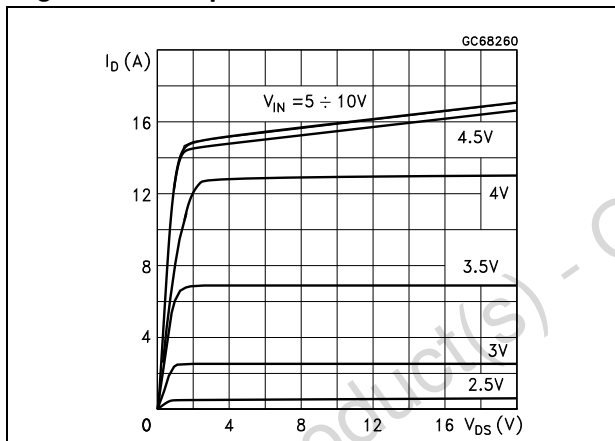


Figure 5. Transconductance

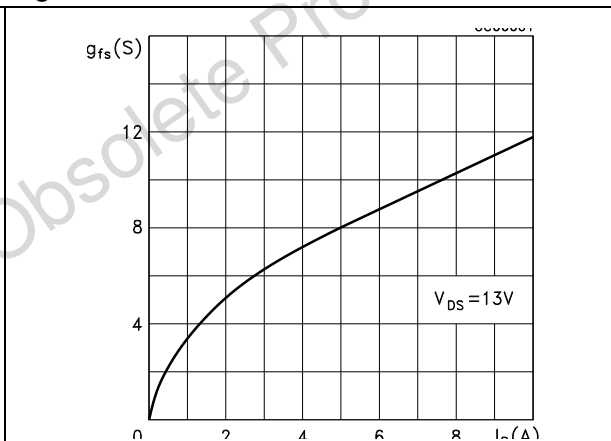


Figure 6. Static drain-source on resistance vs input voltage

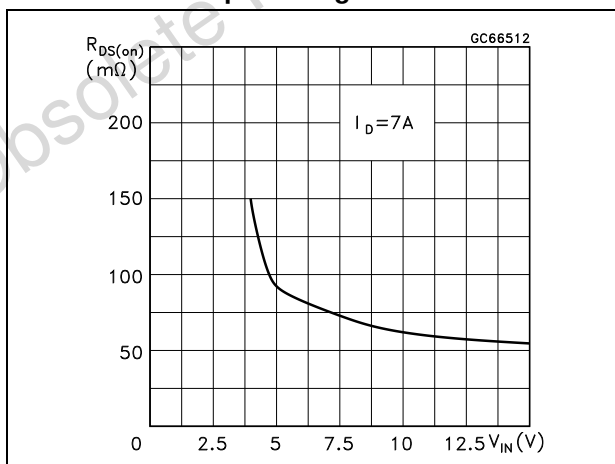


Figure 7. Static drain-source on resistance (part 1/2)

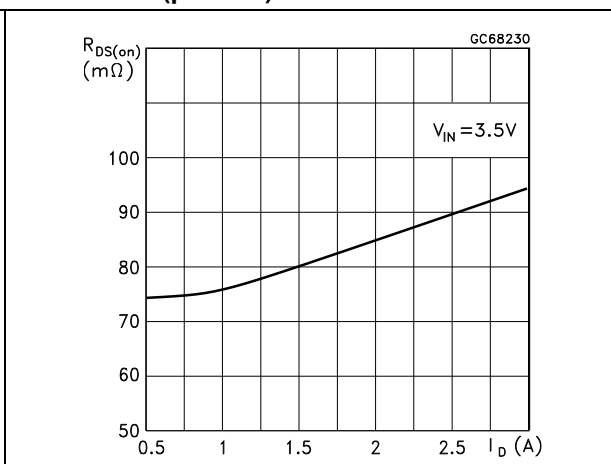


Figure 8. Static drain-source on resistance (part 2/2)

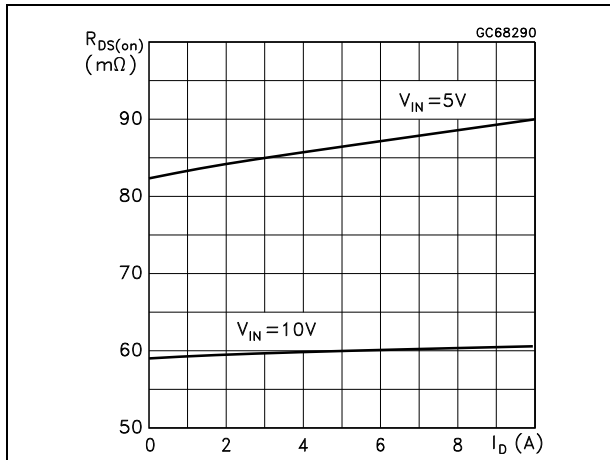


Figure 9. Input charge vs input voltage

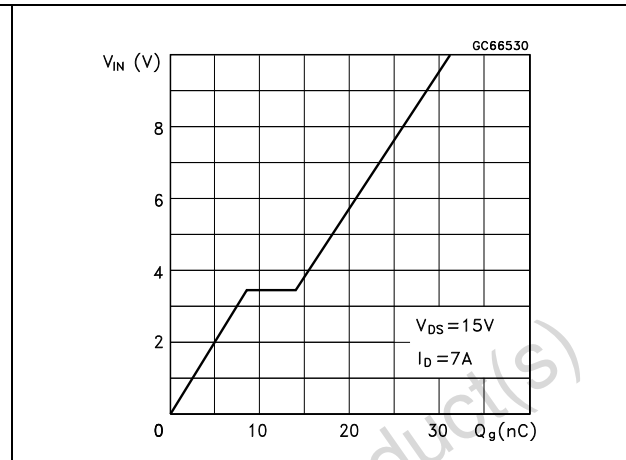


Figure 10. Capacitance variations

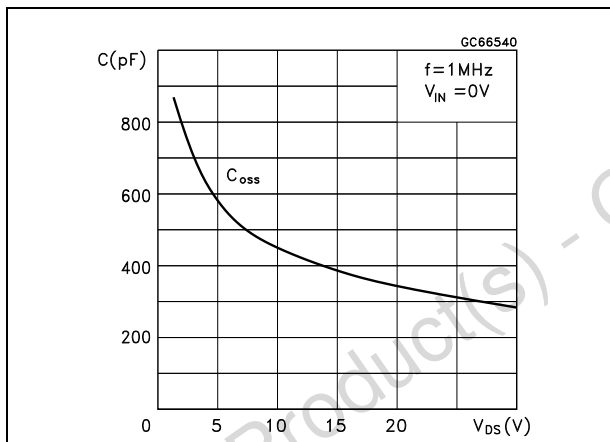


Figure 11. Normalized input threshold voltage vs temperature

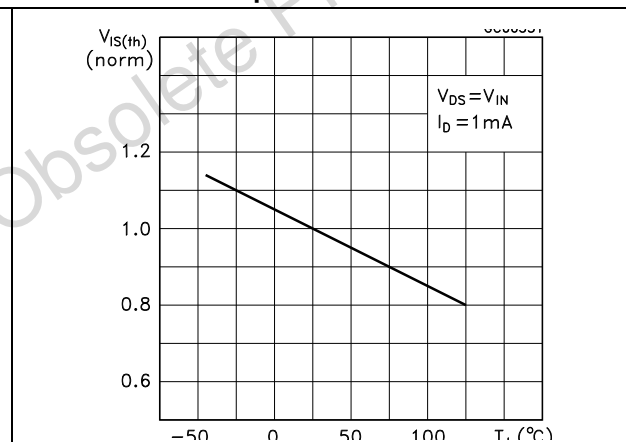


Figure 12. Normalized on resistance vs temperature (part 1/2)

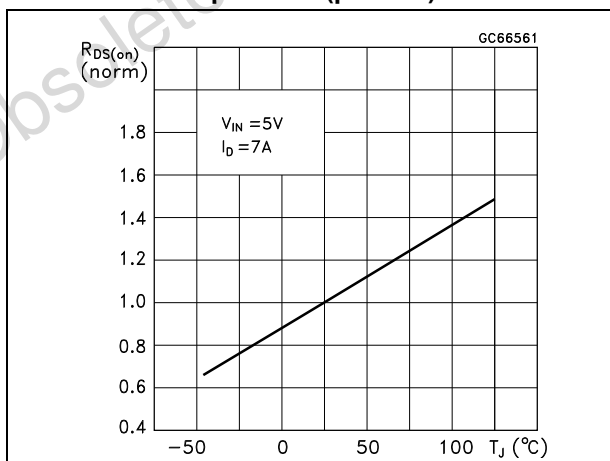


Figure 13. Normalized on resistance vs temperature (part 2/2)

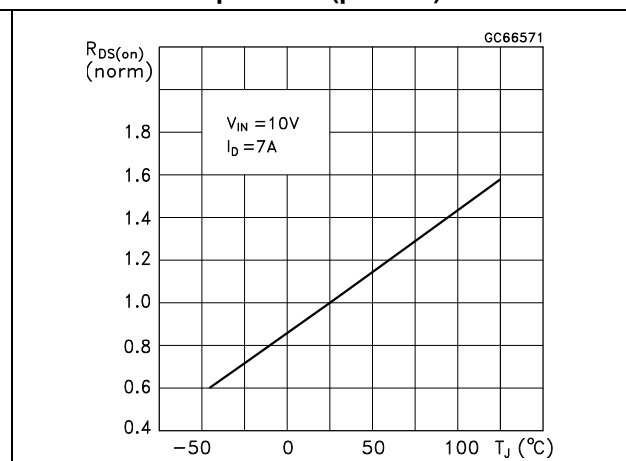


Figure 14. Turn-on current slope(part 1/2)

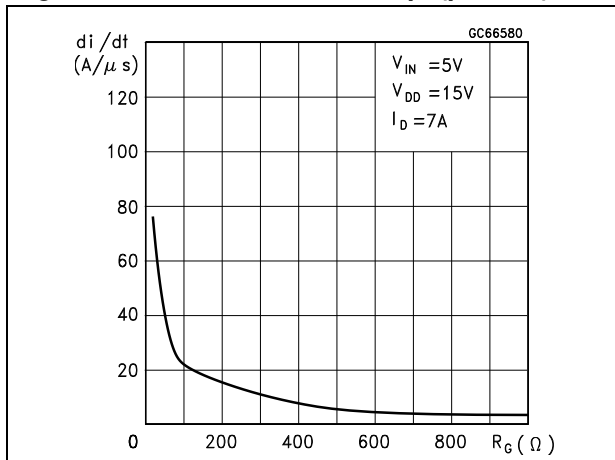


Figure 15. Turn-on current slope (part 2/2)

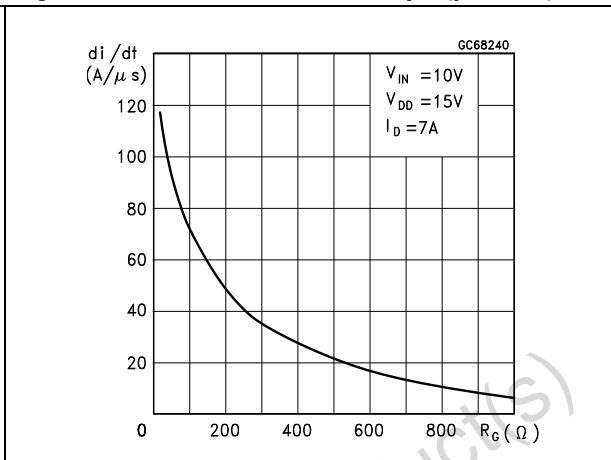


Figure 16. Turn-off drain-source voltage slope (part 1/2)

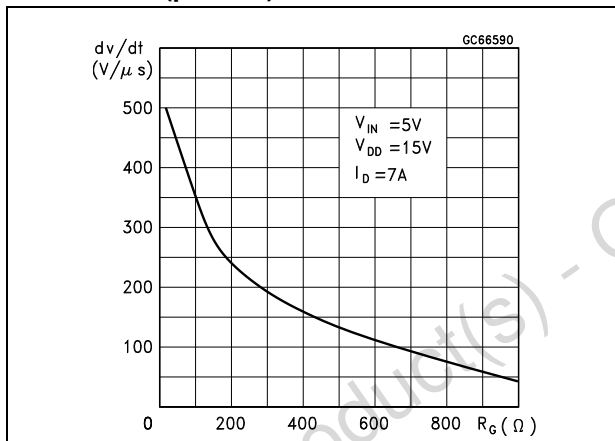


Figure 17. Turn-off drain-source voltage slope (part 2/2)

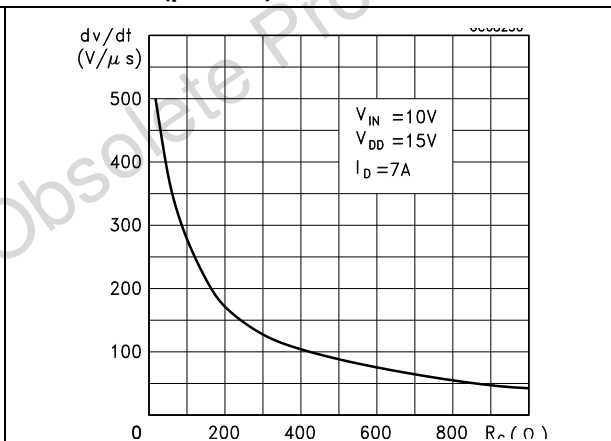


Figure 18. Switching time resistive load (part 1/3)

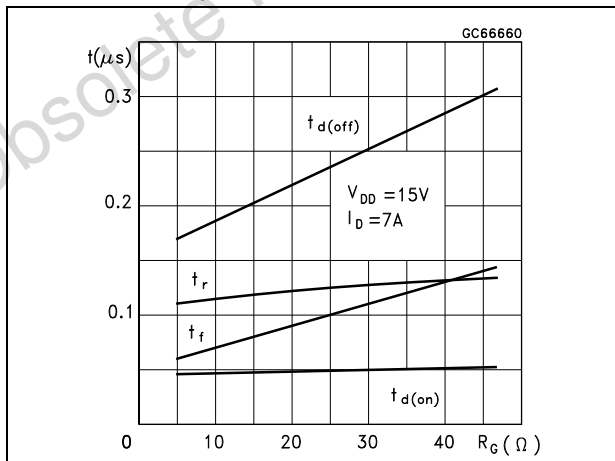


Figure 19. Switching time resistive load (part 2/3)

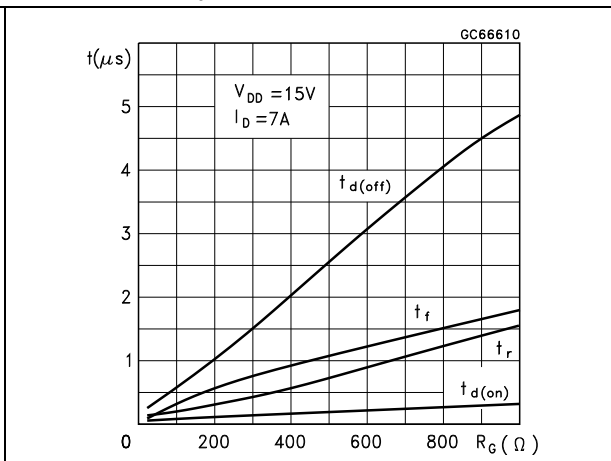


Figure 20. Switching time resistive load (part 3/3)

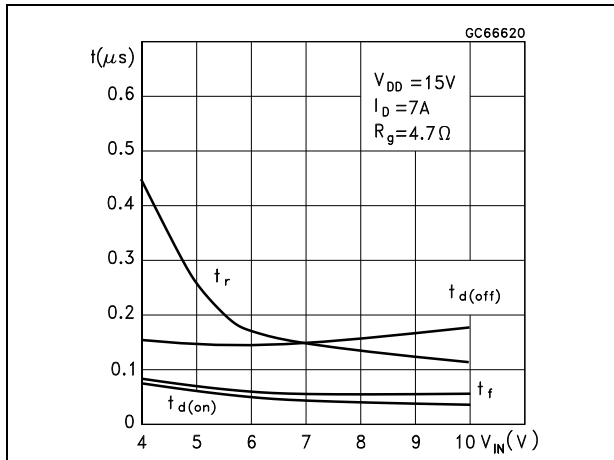


Figure 22. Step response current limit

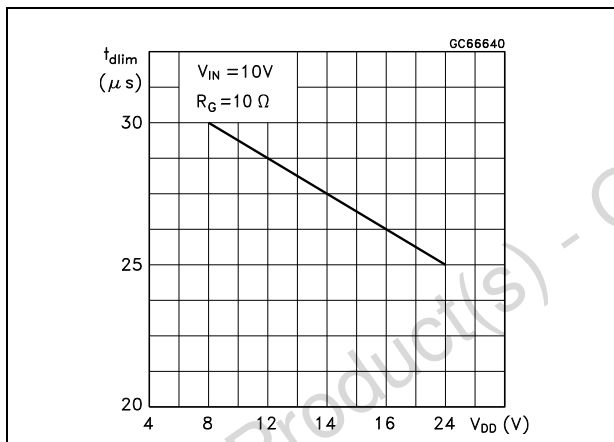


Figure 21. Current limit vs junction temperature

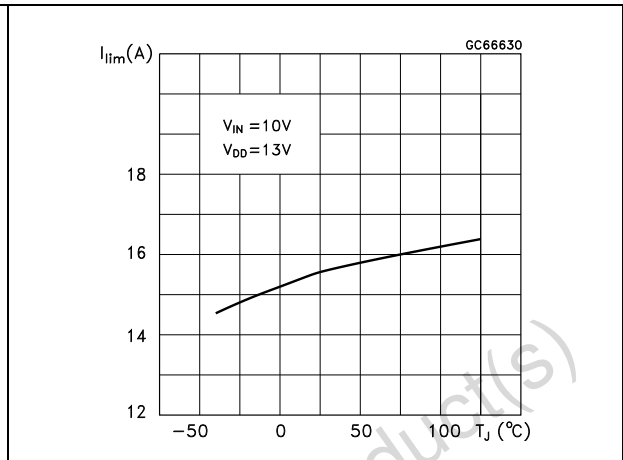


Figure 23. Source drain diode forward characteristics

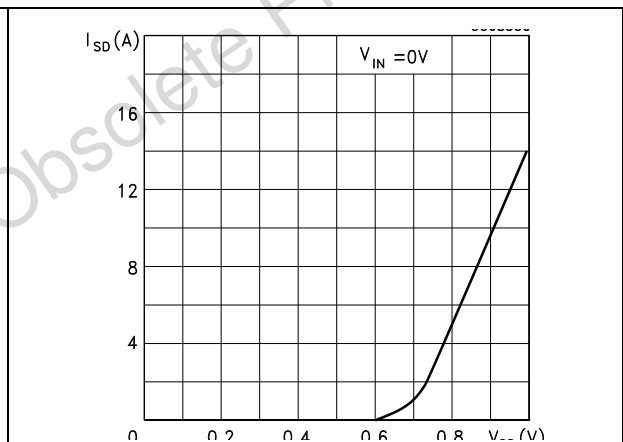


Figure 24. Unclamped inductive load test circuits

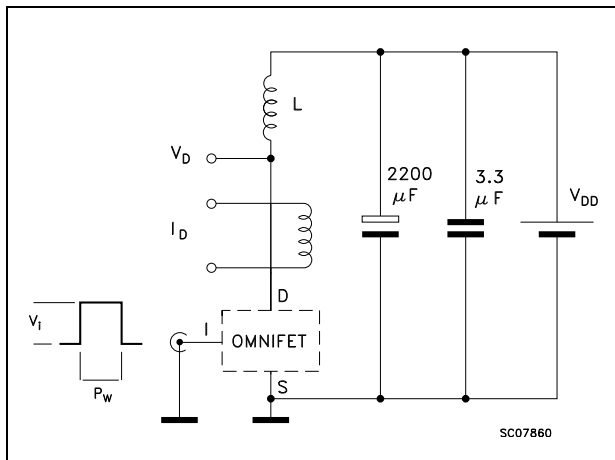


Figure 25. Unclamped inductive waveforms

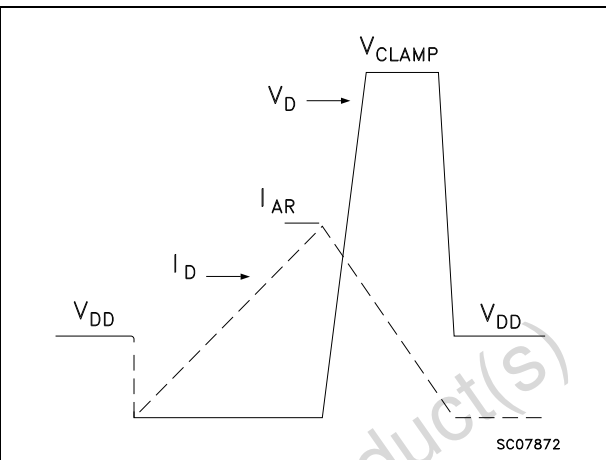


Figure 26. Switching times test circuits for resistive load

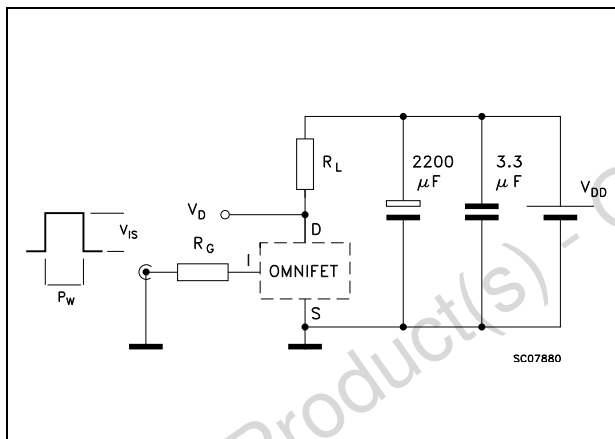


Figure 27. Input charge test circuit

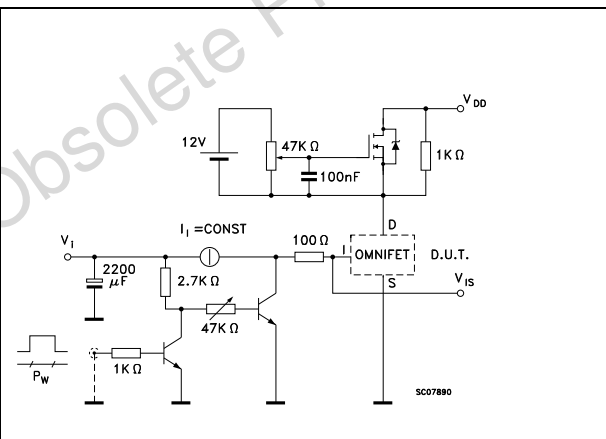


Figure 28. Test circuit for inductive load switching and diode recovery times

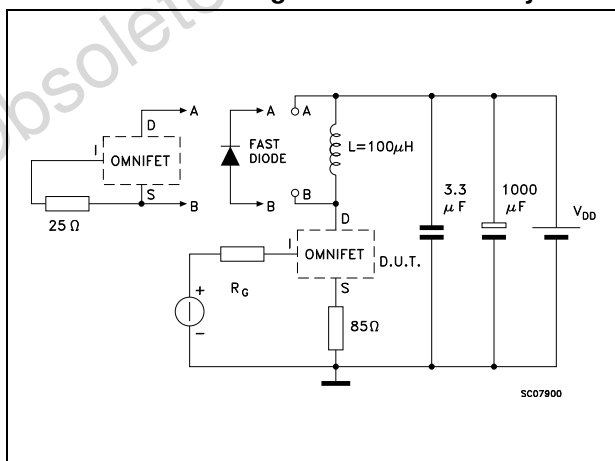
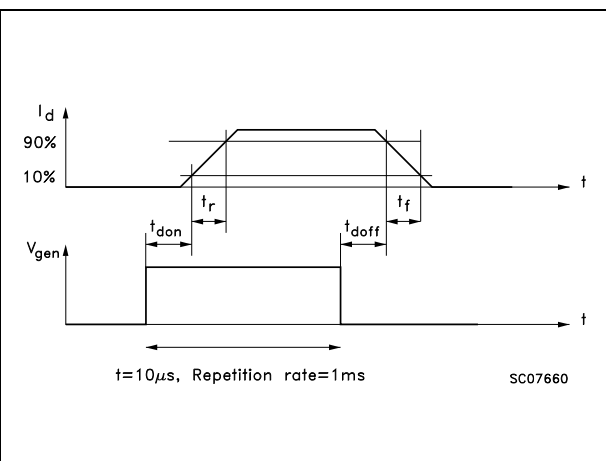


Figure 29. Waveforms



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

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Figure 30. TO-263 (D2PAK) mechanical data

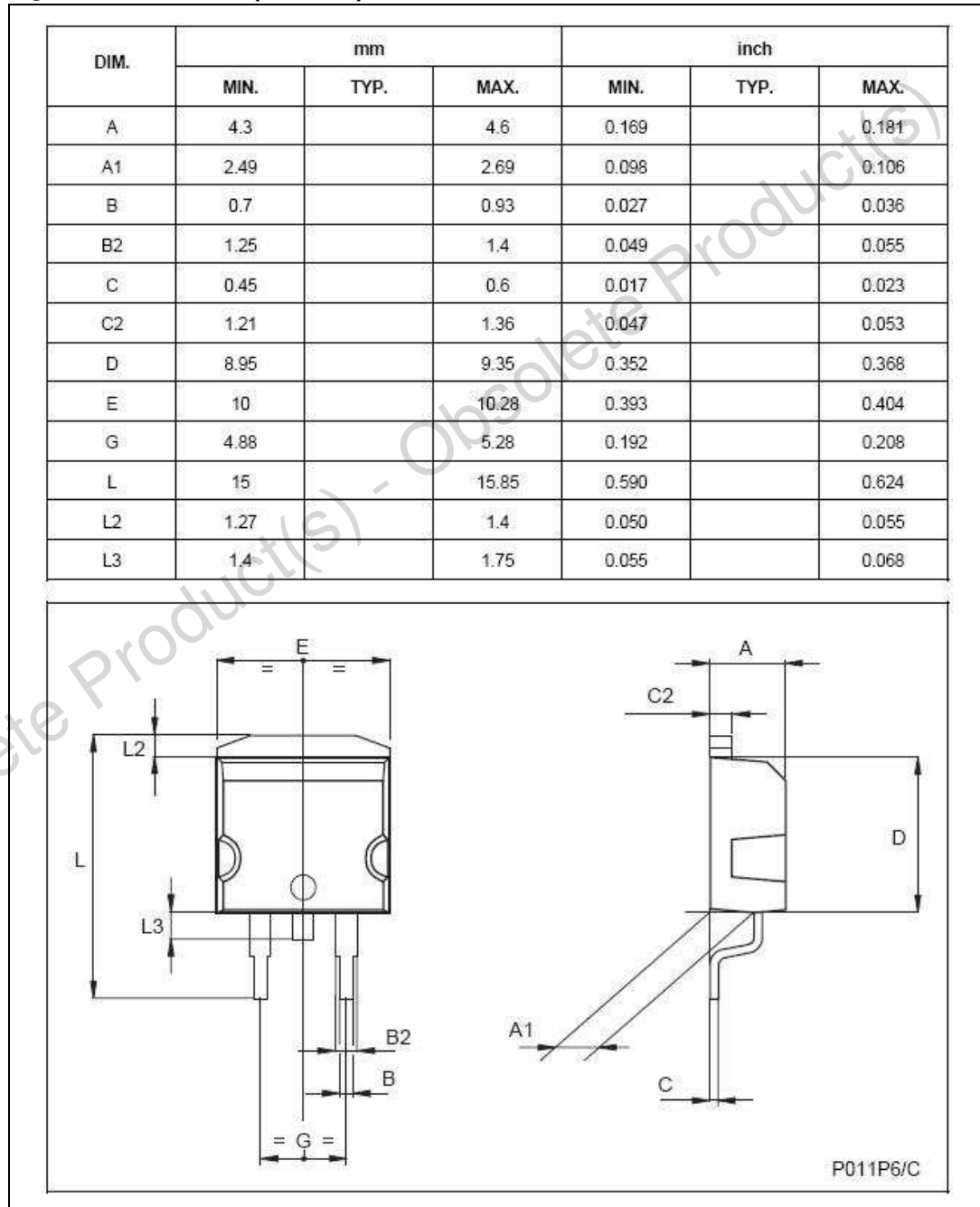


Figure 31. SOT82-FM mechanical data

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.85		3.05	1.122		1.200
A1	1.47		1.67	0.578		0.657
b	0.40		0.60	0.157		0.236
b1	1.4		1.6	0.551		0.630
b2	1.3		1.5	0.511		0.590
c	0.45		0.6	0.177		0.236
D	10.5		10.9	4.133		4.291
e	2.2		2.8	0.866		1.102
E	7.45		7.75	2.933		3.051
L	15.5		15.9	6.102		6.260
L1	1.95		2.35	0.767		0.925

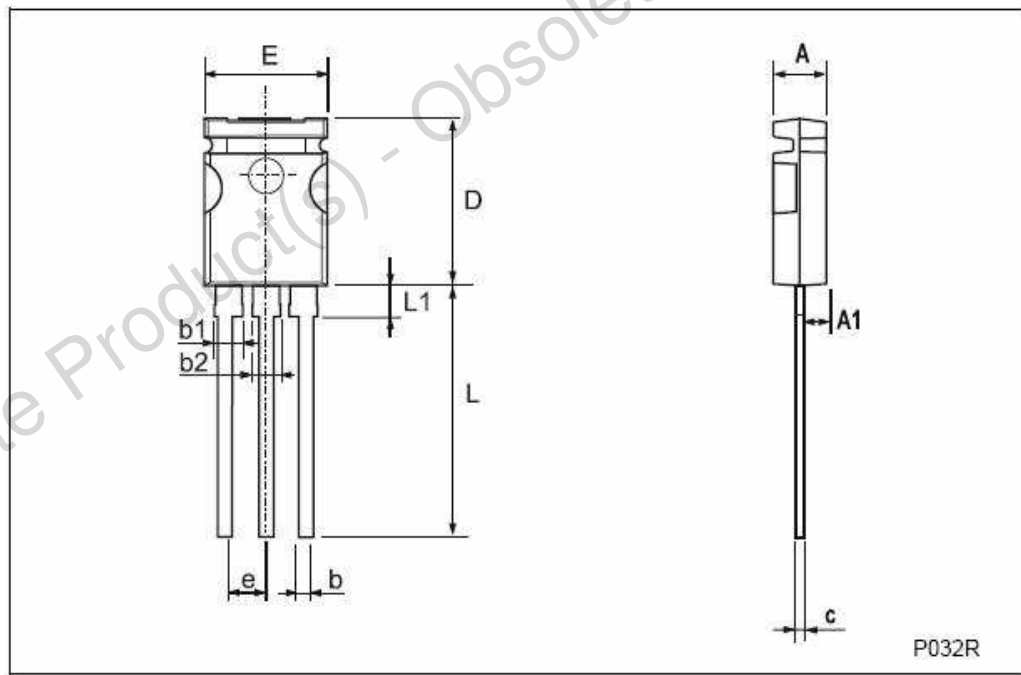
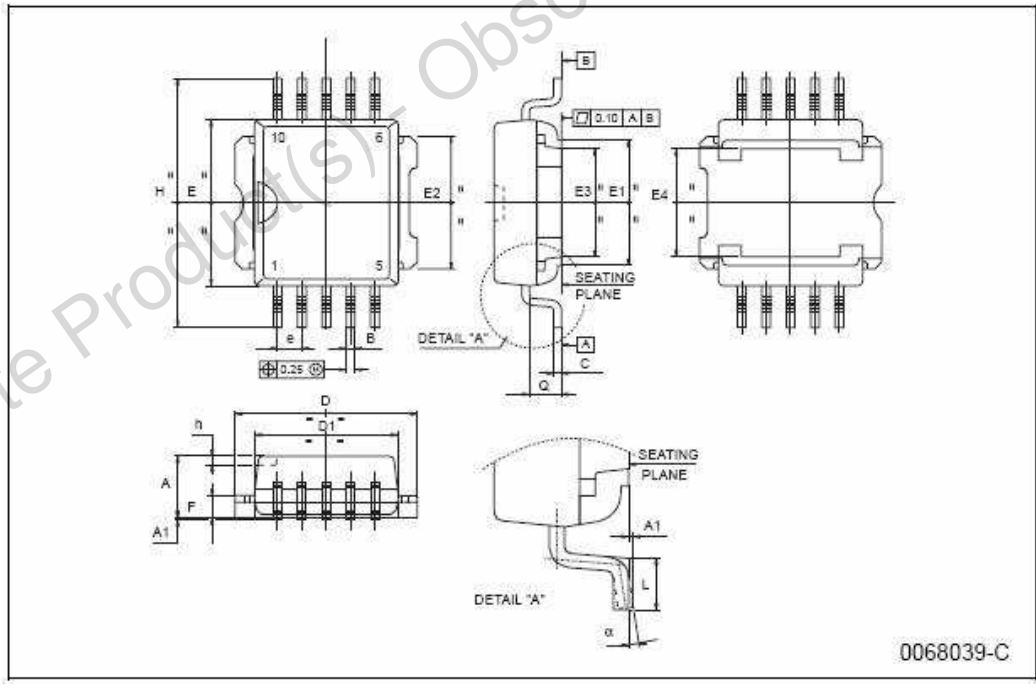


Figure 32. PowerSO-10 mechanical data

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
c	0.35		0.55	0.013		0.022
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
H	13.80		14.40	0.543		0.567
h		0.50			0.002	
L	1.20		1.80	0.047		0.071
q		1.70			0.067	
α	0°		8°			



5 Revision history

Table 5. Document revision history

Date	Revision	Changes
20-Jan-1998	1	Initial release.
21-Jun-2004	5	Update.
08-Apr-2009	6	Document reformatted. Added Table 1: Device summary on page 1 . Updated Section 4: Package information on page 13
25-Sep-2013	7	Updated Disclaimer.

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