Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Future Technology Devices International Ltd

Vinculum-II

Embedded Dual USB Host Controller IC

VINCULUM

Vinculum-II is FTDI's 2nd generation of USB Host device. The CPU has been upgraded from the previous VNC1L device, dramatically increasing the processing power. The IC architecture has been designed to take care of most of the general USB data transfers, thus freeing up processing power for user applications. Flash and RAM memory have been increased providing larger user areas of memory for the designer to incorporate his own code. The designers also have the ability to create their own firmware using the new suite of software development tools.

VNC2 has the following advanced features:

- Embedded processor core
- 16 bit Harvard architecture
- Two full-speed or low-speed USB 2.0 interfaces capable of host or slave functions
- 256kbytes on-chip E-Flash Memory (128k x 16-bits)
- 16kbytes on-chip Data RAM (4k x 32-bits
- Programmable UART up to 6Mbaud
- Two SPI (Serial Peripheral) slave interfaces and one SPI master interface
- Reduced power modes capability
- Variable instruction length
- Native support for 8, 16 and 32 bit data types
- Eight bit wide FIFO Interface
- Firmware upgrades via UART, SPI, and FIFO interface
- 12MHz oscillator using external crystal
- General-purpose timers
- +3.3V single supply operation with 5V safe inputs
- Software development suite of tools to create customised firmware. Compiler Linker – Debugger – IDE
- Available in six RoHS compliant packages - 32 LQFP, 32 QFN, 48 LQFP, 48 QFN, 64 LQFP and 64 QFN
- VNC2-48L1 package option compatible with VNC1L-1A
- 44 configurable I/O pins on the 64 pin device, 28 I/O pins on the 48 pin device and 12 I/O on the 32 pin device using the I/O multiplexer
- -40°C to +85°C extended operating temperature range
- Simultaneous multiple file access on BOMS devices
- Eight Pulse Width Modulation outputs to allow connectivity with motor control applications
- Debugger interface module
- System Suspend Modes

1 Typical Applications

- Add USB host capability to embedded products
- Interface USB Flash drive to MCU/PLD/FPGA – data storage and firmware updates
- USB Flash drive data storage or firmware updates
- USB Flash drive to USB Flash drive file transfer interface
- Digital camera to USB Flash drive*
- PDA to USB Flash drive*
- MP3 Player to USB Flash drive or other USB slave device interface
- OSI Wireless Interface
- USB wireless process controller
- Telecom system calls logging to replace printer log
- Data logging
- Mobile phone to USB Flash drive*
- GPS to mobile phone interface
- Instrumentation USB Flash drive*
- Data-logger USB Flash drive*
- Set Top Box - USB device interface
- GPS tracker with USB Flash disk storage
- USB webcam
- Flash drive to SD Card data transfer
- Vending machine connectivity
- TLM Serial converter
- Geotagging of photos – GPS location linked to image
- Motorcycle system telemetry logging
- Medical systems
- PWM applications for motor control applications e.g. Toys
- FPGA Interfacing

* Or similar USB slave device interface e.g. USB external drive.

1.1 Part Numbers

Part Number	Package
VNC2-64L1B	64 Pin LQFP
VNC2-64Q1B	64 Pin QFN
VNC2-48L1B	48 Pin LQFP
VNC2-48Q1B	48 Pin QFN
VNC2-32L1B	32 Pin LQFP
VNC2-32Q1B	32 Pin QFN

Table 1.1 Part Numbers

Please refer to **section 11** for all package mechanical parameters.

1.2 USB Compliant

At time of writing this data sheet, VNC2 has not completed USB compliancy testing.

2 VNC2 Block Diagram

For a description of each function please refer to Section 4.

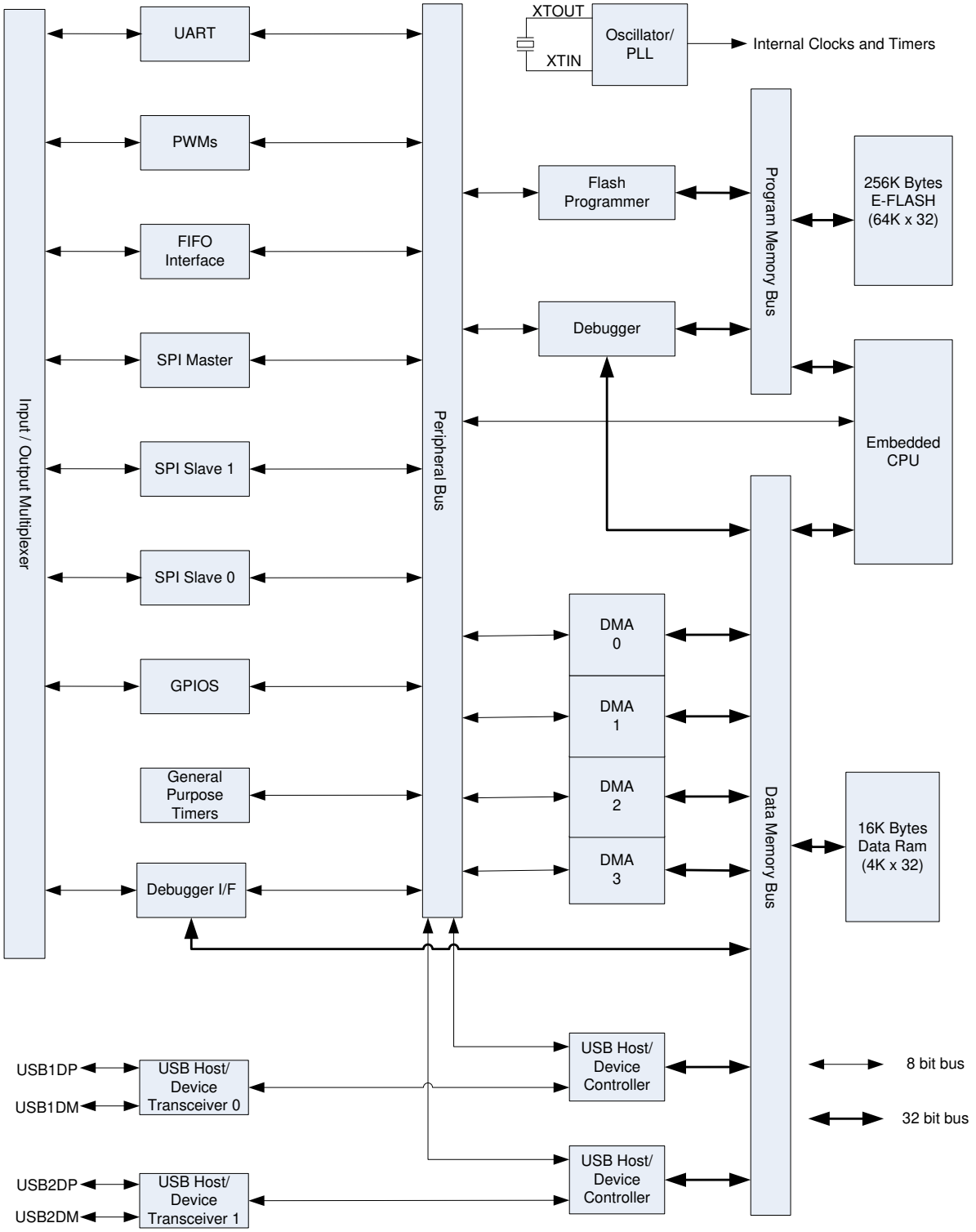

Figure 2.1 Simplified VNC2 Block Diagram

Table of Contents

3 Device Pin Out and Signal Description Summary

VNC2 is available in six packages: 32 pin LQFP, 32 pin QFN, 48 pin LQFP (pin compatible with VNC1L), 48 pin QFN, 64 pin LQFP and 64 pin QFN. **Figure 3.3** shows how the VNC2 pins map to the VNC1L pins (VNC2 pins labelled in bold text):

3.1 Pin Out - 32 pin LQFP

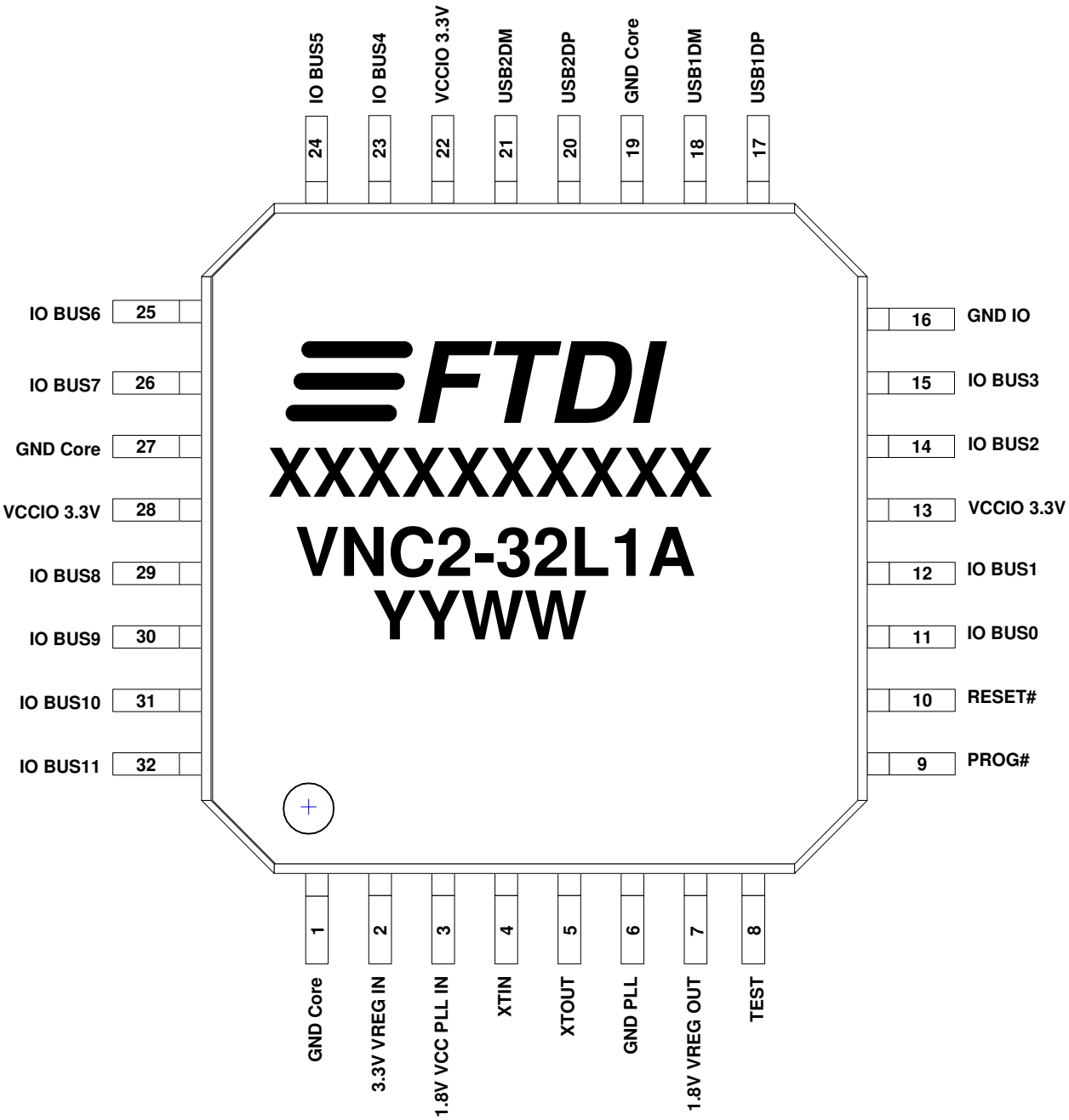

Figure 3.1 32 Pin LQFP – Top Down View

3.2 Pin Out - 32 pin QFN

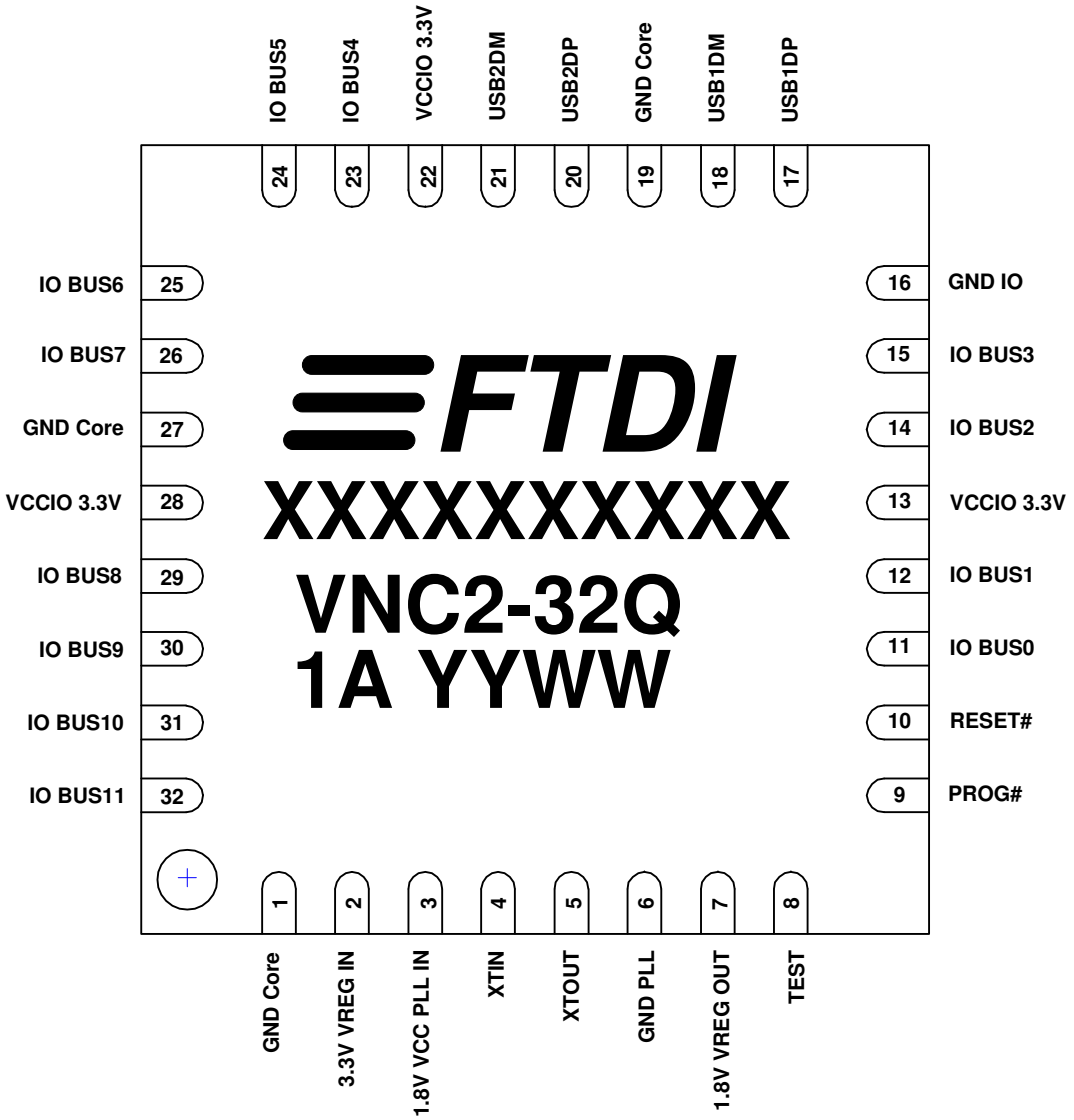

Figure 3.2 32 Pin QFN – Top Down View

3.3 Pin Out - 48 pin LQFP

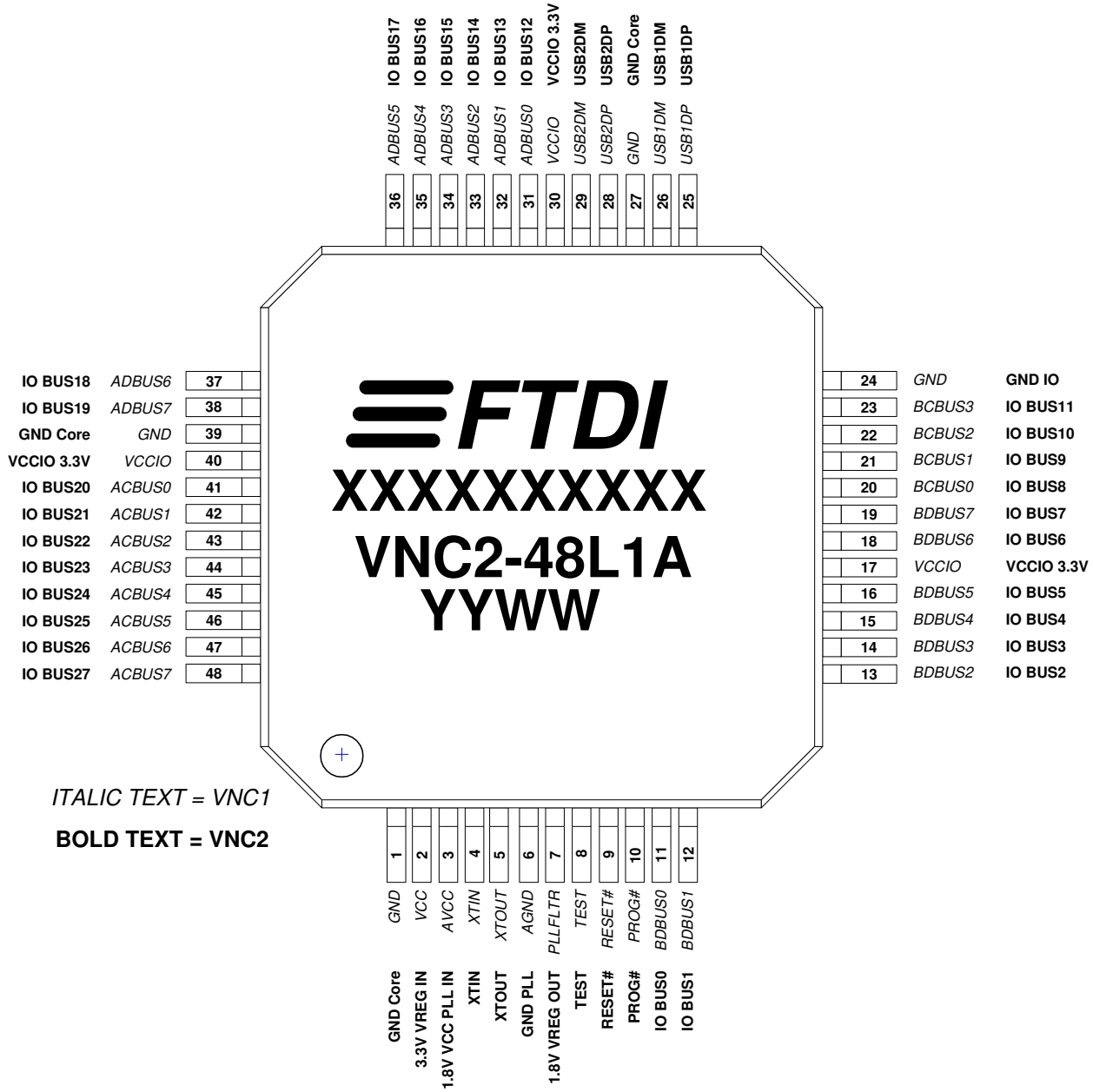

Figure 3.3 48 Pin LQFP – Top Down View

3.4 Pin Out - 48 pin QFN

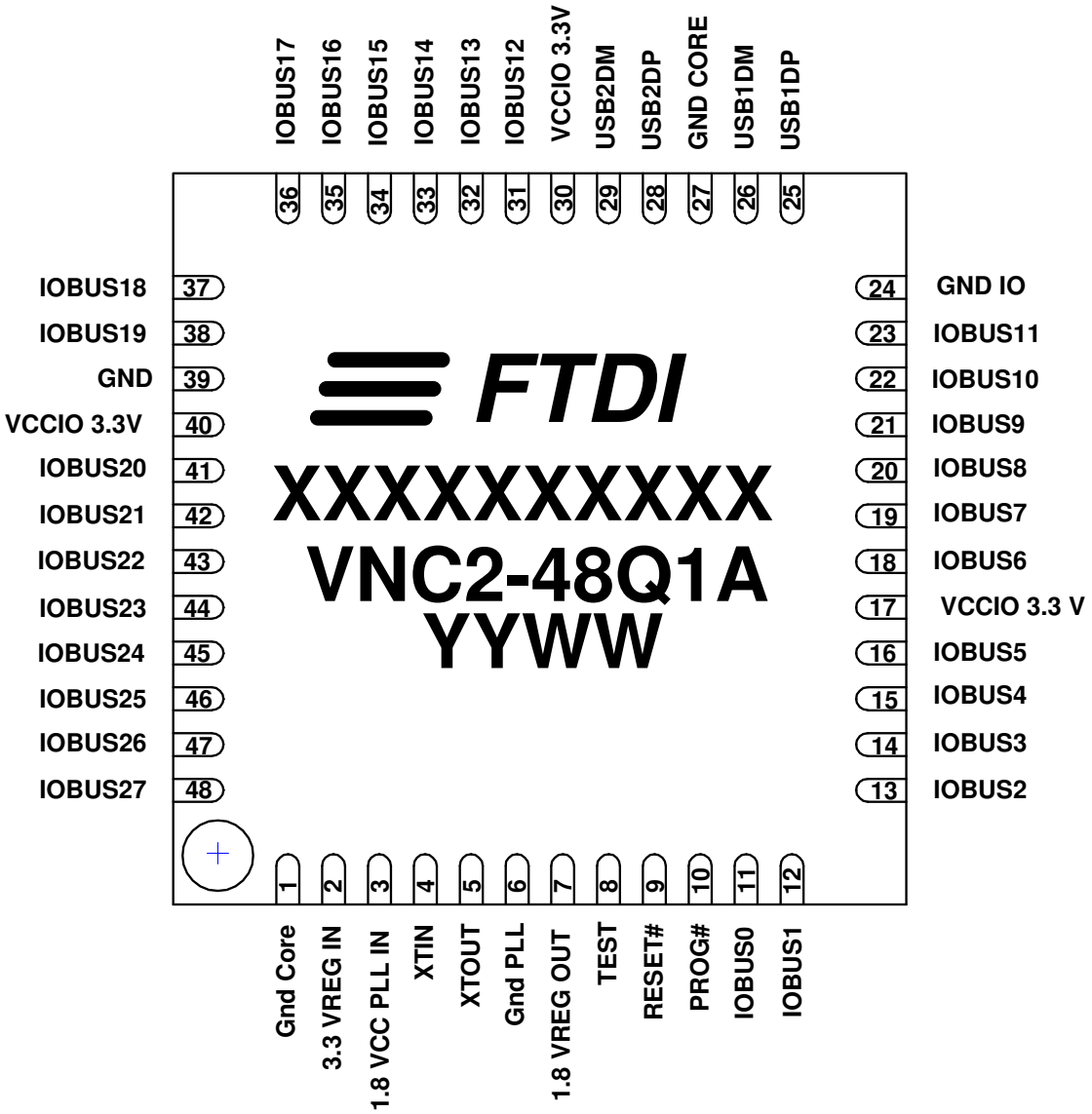

Figure 3.4 48 Pin QFN – Top Down View

3.5 Pin Out - 64 pin LQFP

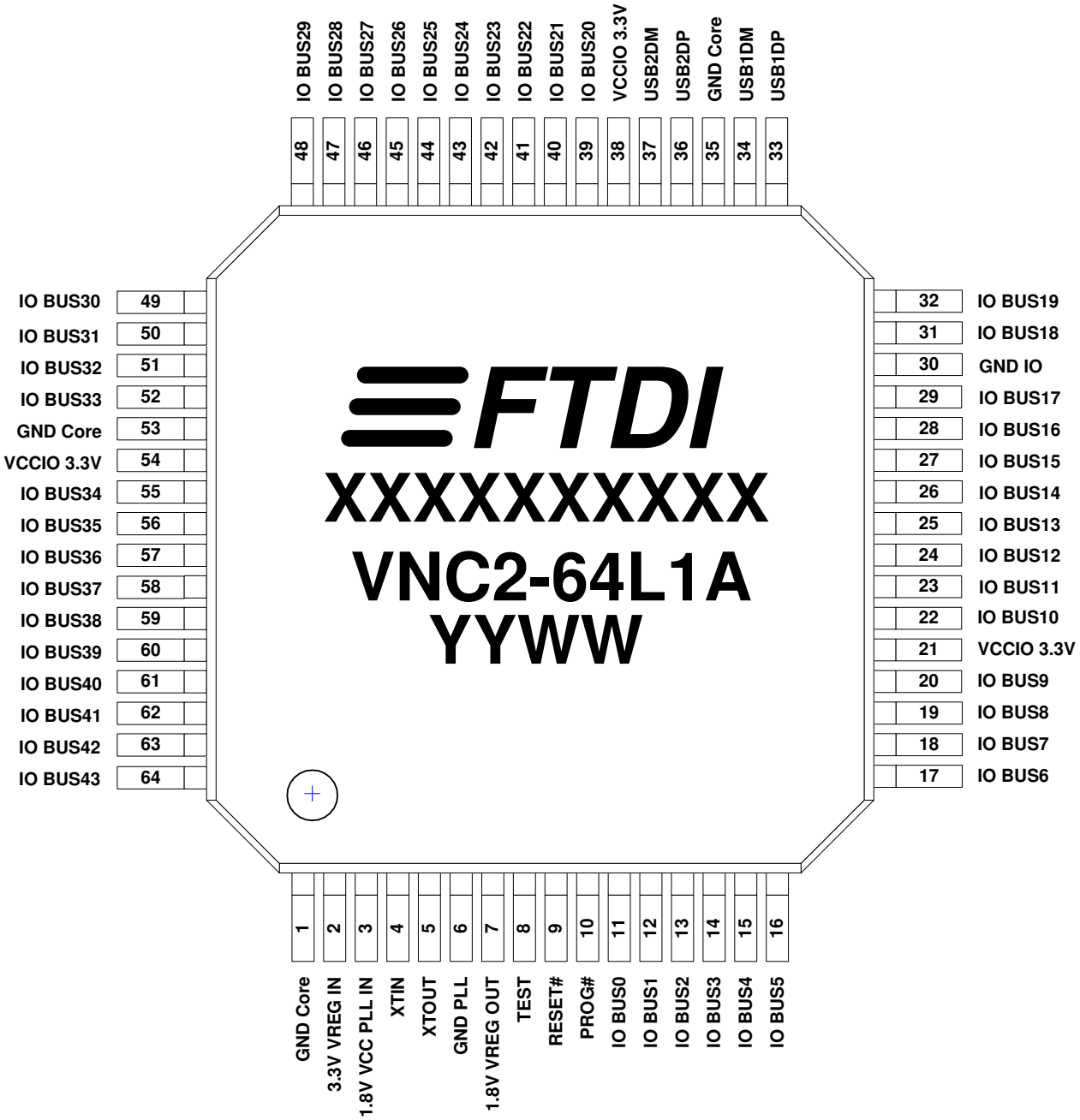

Figure 3.5 64 Pin LQFP – Top Down View

3.6 Pin Out - 64 pin QFN

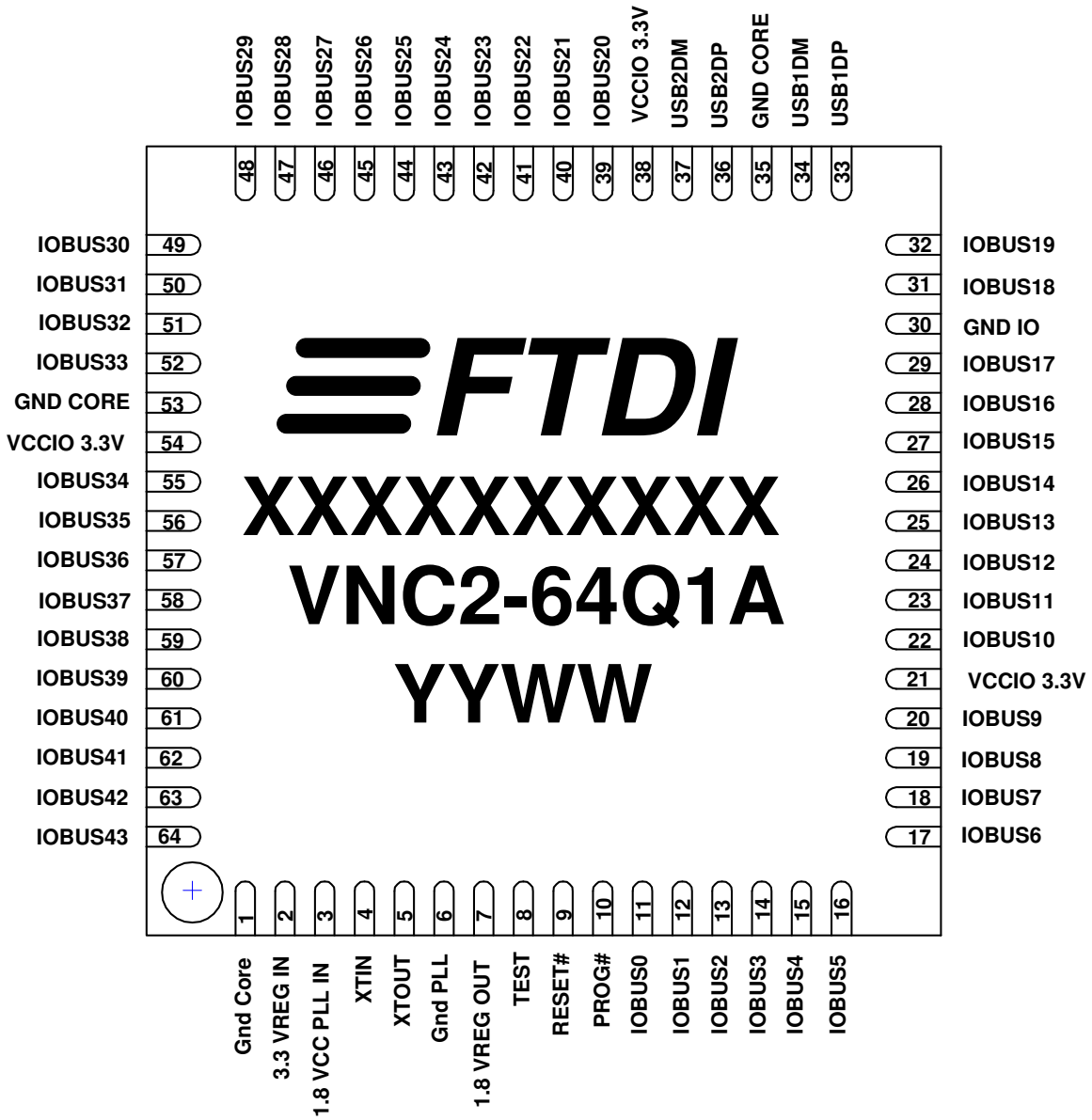

Figure 3.6 64 Pin QFN – Top Down View

3.7 VNC2 Schematic symbol 32 Pin

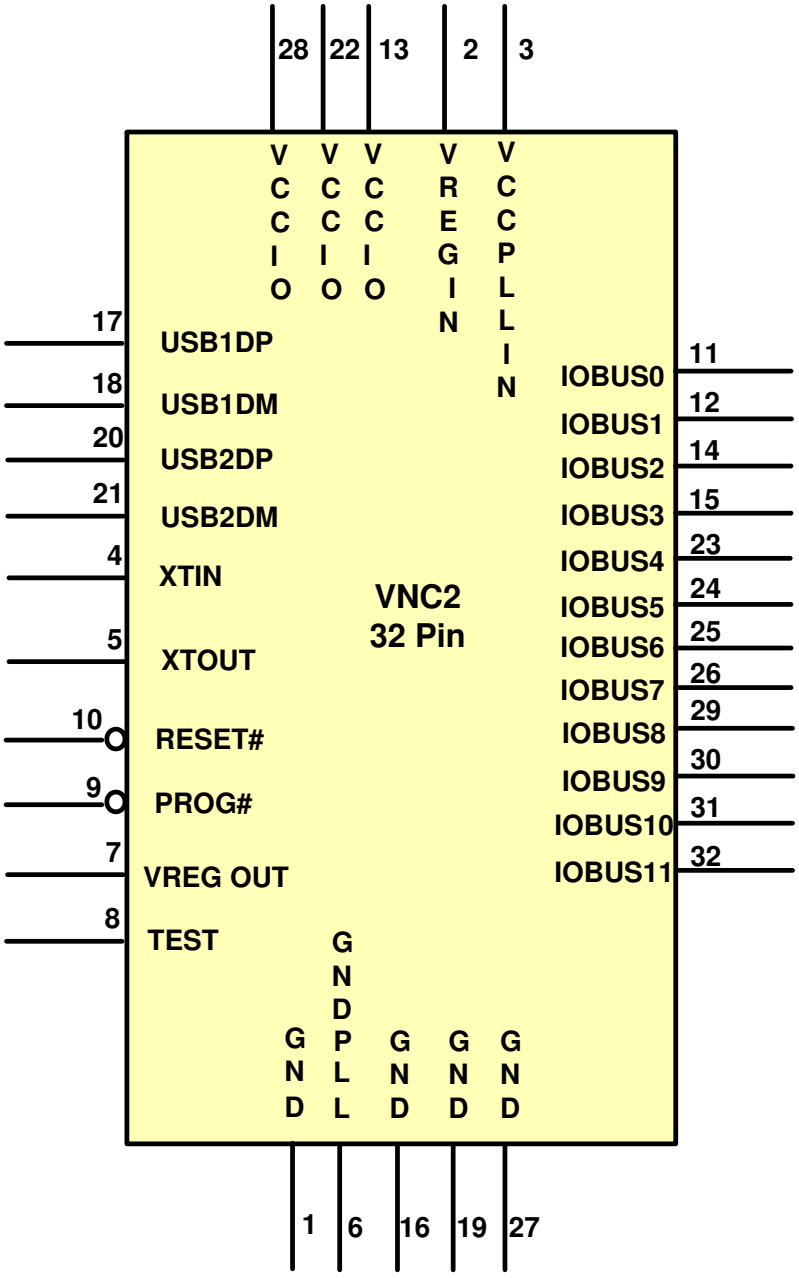

Figure 3.7 Schematic Symbol 32 Pin

3.8 VNC2 Schematic symbol 48 Pin

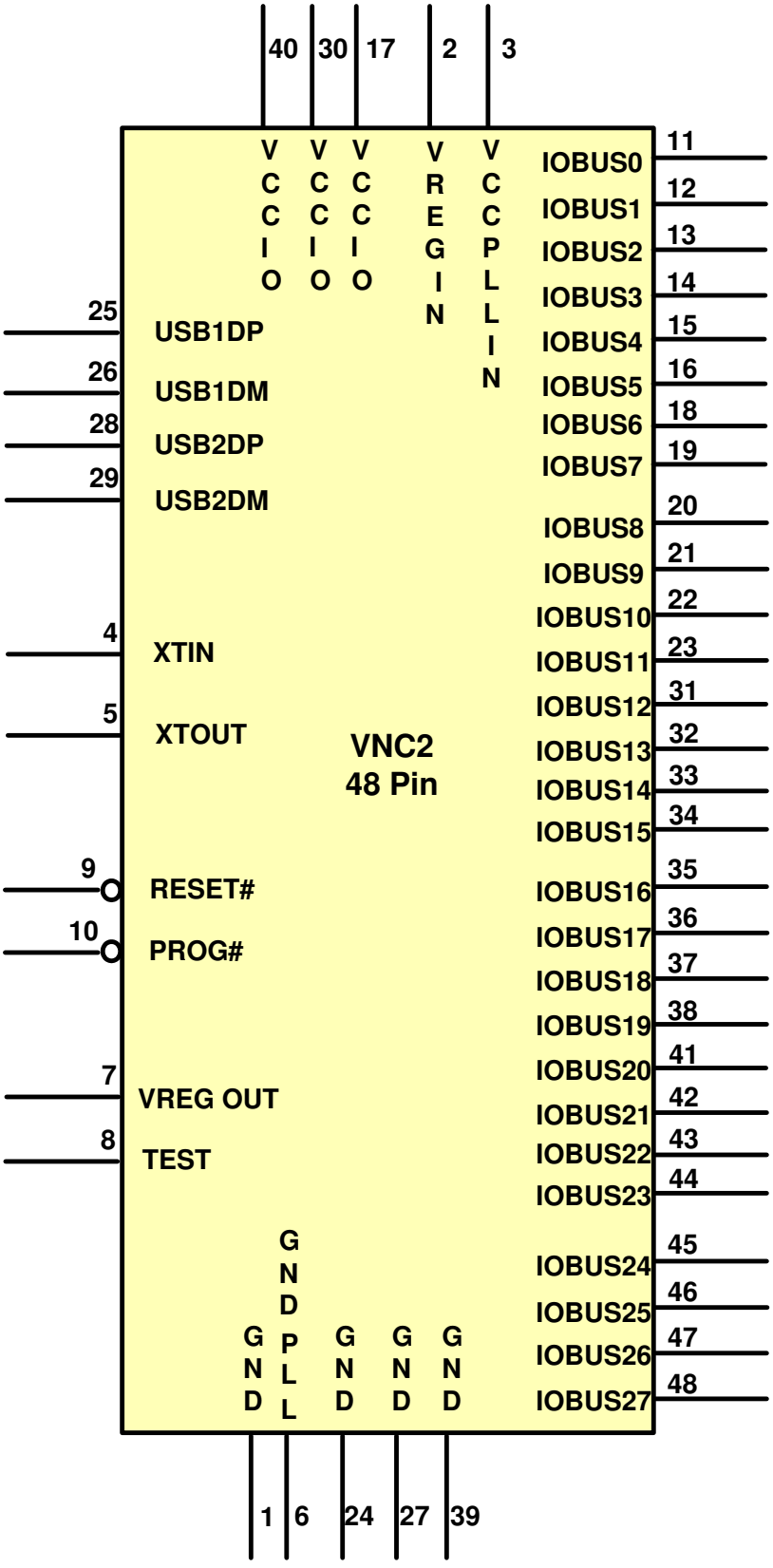

Figure 3.8 Schematic Symbol 48 Pin

3.9 VNC2 Schematic symbol 64 Pin

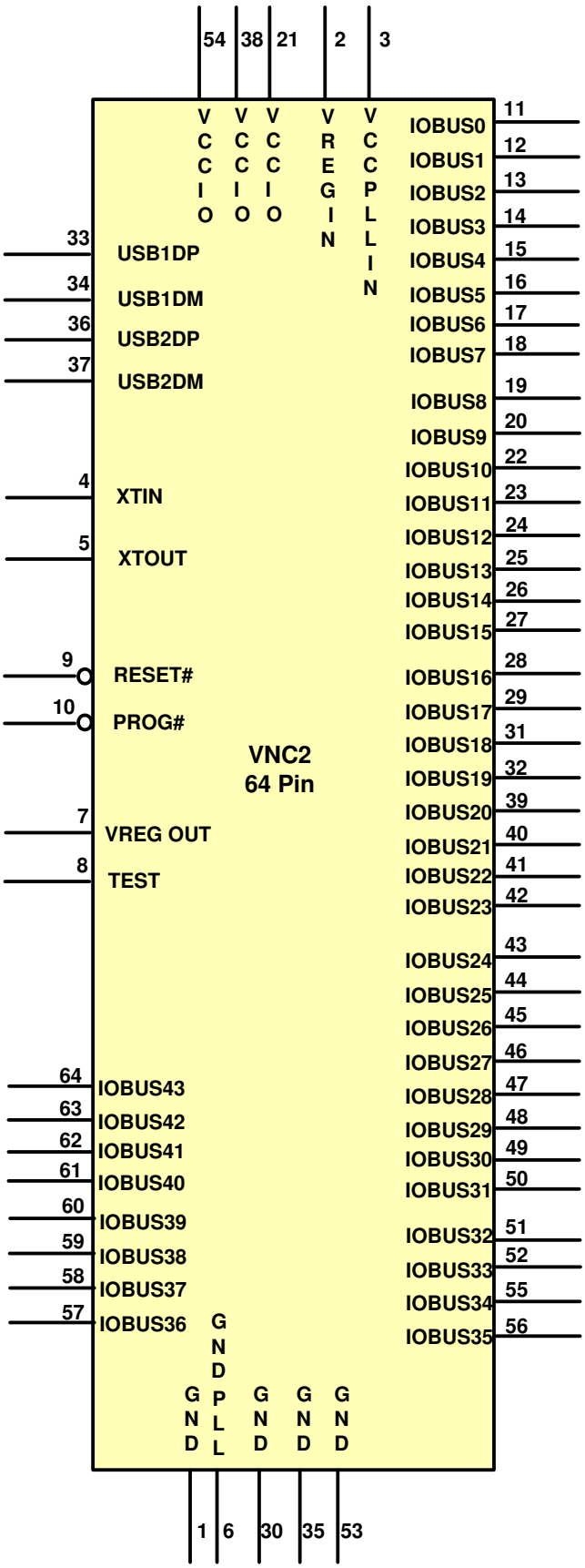

Figure 3.9 Schematic Symbol 64 Pin

3.10 Pin Configuration USB and Power

Pin No			Name	Type	Description
64 pin	48 pin	32 pin			
33	25	17	USB1DP	I/O	USB host/slave port 1 - USB Data Signal Plus with integrated pull-up/pull-down resistor.
34	26	18	USB1DM	I/O	USB host/slave port 1 - USB Data Signal Minus with integrated pull-up/pull-down resistor.
36	28	20	USB2DP	I/O	USB host/slave port 2 - USB Data Signal Plus with integrated pull-up/pull-down resistor.
37	29	21	USB2DM	I/O	USB host/slave port 2 - USB Data Signal Minus with integrated pull-up/pull-down resistor.

Table 3.1 USB Interface Group

Pin No			Name	Type	Description
64 pin	48 pin	32 pin			
1, 30, 35, 53	1, 24, 27, 39	1, 16, 19, 27	GND	PWR	Device ground supply pins.
2	2	2	3.3V VREGIN	PWR	+3.3V supply to the regulator.
3	3*	3	1.8V VCC PLL IN	PWR	+1.8V supply to the internal clock multiplier. This pin requires a 100nF decoupling capacitor. * 48 pin LQFP package only – This power input is internally connected to VREG_OUT. All other packages need this pin connected to a 1.8V power source. Most common applications will connect this to VREG_OUT.
6	6	6	GND PLL	PWR	Device analogue ground supply for internal clock multiplier.
7	7*	7	VREG OUT	Output	1.8V output from regulator to device core * N/C on 48 pin LQFP package only. All other packackages will typically need to connect pins 7 and 3.
21, 38, 54	17, 30, 40	13, 22, 28	VCCIO	PWR	+3.3V supply to the input / output. Interface pins (IOBUS). Leaving the VCCIO unconnected will lead to unpredictable operation on the interface pins.

Table 3.2 Power and Ground

3.11 Miscellaneous Signals

Pin No			Name	Type	Description
64 pin	48 pin	32 pin			
4	4	4	XTIN	Input	Input to 12MHz Oscillator Cell. Connect 12MHz crystal across pins 4 and 5.
5	5	5	XTOUT	Output	Output from 12MHz Oscillator Cell. Connect 12MHz crystal across pins 4 and 5.
8	8	8	TEST	Input	Test Input. Must be tied to GND for normal operation.
9	9	10	RESET#	Input	Can be used by an external device to reset VNC2.
10	10	9	PROG#	Input	Asserting PROG# on its own enables programming mode.

Table 3.3 Miscellaneous Signal Group

Note 1: # is used to indicate an active low signal.

Note 2: Pin 8, 9 and 10 are 5V safe inputs

3.12 Pin Configuration Input / Output

VNC2 has multiple interfaces available for connecting to external devices. These are UART, FIFO, SPI slave, SPI master, GPIO and PWM. The Interface I/O Multiplexer is used to share the available I/O Pins between each peripheral.

VNC2 is configured with default settings for the I/O pins however they can be easily changed to suit the needs of a designer. This is explained in **Section 5 – I/O Multiplexer.** Default configuration for each package type is shown in **Table 3.4- Default I/O Configuration.** The signal names are also indicated for the VNC1L device as it is pin-compatible with the 48 pin LQFP VNC2 device.

Note: The default value of the pins listed in the following table are only available when the I/O Mux is enabled. A blank VNC2 chip defaults to all I/O pins as inputs.

Pin No			Name	64 Pin	48 Pin	32 PIN	Type	Description
64 Pin	48 Pin	32 Pin	(VINC1-L)	Default	Default	Default		
11	11	11	IOBUS0 (BDBUS0)	debug_if	debug_if	debug_if	I/O	GPIO
12	12	12	IOBUS1 (BDBUS1)	Input	pwm[1]	gpio[A1]	I/O	GPIO
13	13	14	IOBUS2 (BDBUS2)	Input	pwm[2]	gpio[A2]	I/O	GPIO
14	14	15	IOBUS3 (BDBUS3)	Input	pwm[3]	gpio[A3]	I/O	GPIO
15	15	23	IOBUS4 (BDBUS4)	fifo_data[0]	spi_s0_clk	uart_txd	I/O	GPIO
16	16	24	IOBUS5 (BDBUS5)	fifo_data[1]	spi_s0_mosi	uart_rxd	I/O	GPIO
17	18	25	IOBUS6 (BDBUS6)	fifo_data[2]	spi_s0_miso	uart_rts#	I/O	GPIO
18	19	26	IOBUS7 (BDBUS7)	fifo_data[3]	spi_s0_ss#	uart_cts#	I/O	GPIO
19	20	29	IOBUS8 (BCBUS0)	fifo_data[4]	spi_m_clk	spi_s0_clk	I/O	GPIO
20	21	30	IOBUS9 (BCBUS1)	fifo_data[5]	spi_m_mosi	spi_s0_mosi	I/O	GPIO
22	22	31	IOBUS10 (BCBUS2)	fifo_data[6]	spi_m_miso	spi_s0_miso	I/O	GPIO
23	23	32	IOBUS11 (BCBUS3)	fifo_data[7]	spi_m_ss_0#	spi_s0_ss#	I/O	GPIO
24	31	-	IOBUS12 (ADBUS0)	fifo_rxf#	uart_txd		I/O	GPIO
25	32	-	IOBUS13 (ADBUS1)	fifo_txe#	uart_rxd		I/O	GPIO
26	33	-	IOBUS14 (ADBUS2)	fifo_rd#	uart_rts#		I/O	GPIO

Pin No			Name	64 Pin	48 Pin	32 PIN	Type	Description
64 Pin	48 Pin	32 Pin	(VINC1-L)	Default	Default	Default		
27	34	-	IOBUS15 (ADBUS3)	fifo_wr#	uart_cts#		I/O	GPIO
28	35	-	IOBUS16 (ADBUS4)	fifo_oe#	uart_dtr#		I/O	GPIO
29	36	-	IOBUS17 (ADBUS5)	Input	uart_dsr#		I/O	GPIO
31	37	-	IOBUS18 (ADBUS6)	Input	uart_dcd#		I/O	GPIO
32	38	-	IOBUS19 (ADBUS7)	Input	uart_ri#		I/O	GPIO
39	41	-	IOBUS20 (ACBUS0)	uart_txd	uart_tx_active		I/O	GPIO
40	42	-	IOBUS21 (ACBUS1)	uart_rxd	gpio[A5]		I/O	GPIO
41	43	-	IOBUS22 (ACBUS2)	uart_rts#	gpio[A6]		I/O	GPIO
42	44	-	IOBUS23 (ACBUS3)	uart_cts#	gpio[A7]		I/O	GPIO
43	45	-	IOBUS24 (ACBUS4)	uart_dtr#	gpio[A0]		I/O	GPIO
44	46	-	IOBUS25 (ACBUS5)	uart_dsr#	gpio[A1]		I/O	GPIO
45	47	-	IOBUS26 (ACBUS6)	uart_dcd#	gpio[A2]		I/O	GPIO
46	48	-	IOBUS27 (ACBUS7)	uart_ri#	gpio[A3]		I/O	GPIO
47	-	-	IOBUS28	uart_tx_active			I/O	GPIO
48	-	-	IOBUS29	Input			I/O	GPIO
49	-	-	IOBUS30	Input			I/O	GPIO
50	-	-	IOBUS31	Input			I/O	GPIO
51	-	-	IOBUS32	spi_s0_clk			I/O	GPIO
52	-	-	IOBUS33	spi_s0_mosi			I/O	GPIO
55	-	-	IOBUS34	spi_s0_miso			I/O	GPIO
56	-	-	IOBUS35	spi_s0_ss#			I/O	GPIO
57	-	-	IOBUS36	spi_s1_clk			I/O	GPIO

Pin No			Name (VINC1-L)	64 Pin Default	48 Pin Default	32 PIN Default	Type	Description
64 Pin	48 Pin	32 Pin						
58	-	-	IOBUS37	spi_s1_mosi			I/O	GPIO
59	-	-	IOBUS38	spi_s1_miso			I/O	GPIO
60	-	-	IOBUS39	spi_s1_ss#			I/O	GPIO
61	-	-	IOBUS40	spi_m_clk			I/O	GPIO
62	-	-	IOBUS41	spi_m_mosi			I/O	GPIO
63	-	-	IOBUS42	spi_m_miso			I/O	GPIO
64	-	-	IOBUS43	spi_m_ss_0#			I/O	GPIO

Table 3.4 Default I/O Configuration

Note: All GPIO are 5V safe inputs

4 Function Description

VNC2 is the second of FTDIs Vinculum family of Embedded USB host controller integrated circuit devices. VNC2 can encapsulate certain USB device classes by handling the USB Host Interface and data transfer functions using the in-built EMCU and embedded Flash memory. When interfacing to mass storage devices, such as USB Flash drives, VNC2 transparently handles the FAT file structure using a simple to implement command set. VNC2 provides a cost effective solution for introducing USB host capability into products that previously did not have the hardware resources to do so.

VNC2 has an associated software development tool suite to allow users to create customised firmware.

4.1 Key Features

VNC2 is a programmable SoC device with a powerful embedded microprocessor core and dual USB interfaces, large RAM and Flash capacity and the ability to develop and customise firmware using the VNC2 Toolchain. VNC2 has an enhanced feature list over and above VNC1L, however the 48 pin LQFP package is backward compatible with the VNC1L.

4.2 Functional Block Descriptions

The following paragraphs describe each function within VNC2. Please refer to the block diagram shown in **Figure 2.1**

4.2.1 Embedded CPU

The processor core is based on FTDIs proprietary 16-bit embedded MCU architecture. The EMCU has a Harvard architecture with separate code and data space.

4.2.2 Flash Module

VNC2 has 256k bytes (128k x 16-bits) of embedded Flash (E-FLASH) memory. No special programming voltages are necessary for programming the onboard E-FLASH as these are provided internally on-chip.

4.2.3 Flash Programming Module

The purpose of the flash programmer module is to perform all necessary operations for programming the flash, from general usage to first power on sequencing. This block is responsible for handling device firmware upgrades which can be accessed by the debugger interface, a USB cable or Flash drive interface.

4.2.4 Input / Output Multiplexer Module

VNC2 peripheral interfaces are UART, SPI slave0, SPI slave1, SPI master, FIFO-Asynchronous, FIFO-Synchronous, GPIO, debug interface and PWM.

The I/O multiplexer allows the designer to select which peripherals are connected to the device I/O pins.

The selectable peripheral interfaces are only limited by the number of I/O pins available. All peripherals are available across the package range except synchronous FIFO mode which cannot be selected on 32 pin packages. The available configurable I/O pins per package are as follows:

- 32 pin package – 12 I/O pins
- 48 pin package – 28 I/O pins
- 64 pin package – 44 I/O pins

Table 4.1 lists the peripherals which can be multiplexed to I/O and the maximum number of pins required for each one. The designer can choose any mix of peripheral configurations as long as they are within the specific package I/O pin count. Depending on the design not all 9 UART pins need to be configured. Similarly the GIPO peripheral does not need all pins configured.

e.g. The 48 pin package has 28 I/O pins which could be configured as UART – 9 pins, SPI Master – 5 pins, FIFO Asynchronous – 12 pins and GPIO – 2 pins. This makes a total of 28 pins.

Please refer to **Section 5** for a detailed description of the I/O multiplexer.

Peripherals	Maximum pins required
UART	9
SPI Slave 0	4
SPI Slave 1	4
SPI Master	5
FIFO Asynchronous	12
FIFO Synchronous	14
GPIO	40
Debug	1
PWM	8

Table 4.1 - Peripheral Pin Requirements

4.2.5 Peripheral DMA Modules 0, 1, 2 & 3

The peripheral DMA has the capability to transfer data to and from an I/O device. The CPU can offload the transfer of data between the processor and the peripheral freeing the CPU to execute other instructions.

The DMA module collects or transmits data from memory to an I/O address space, it is also capable of copying data in memory and transferring it to another location.

The DMA is not accessible by the user as it automatically controlled by the CPU.

4.2.6 RAM Module

The RAM module consists of 16k bytes on-chip (4k x 32-bits) data memory. The RAM is byte addressable.

4.2.7 Peripheral Interface Modules

VNC2 has nine peripheral interface modules. Full descriptions of each module are described in **section 6.**

- Debugger Interface
- UART
- PWM
- FIFO
- SPI Master
- SPI Slave 0 & 1
- GPIO - General purpose I/O pins
- General purpose timers

4.2.8 USB Transceivers 0 and 1

Two USB transceiver cells provide the physical USB device interface supporting USB 1.1 and USB 2.0 standards. Low-speed and full-speed USB data rates are supported. Each output driver provides +3.3V level slew rate control signalling, whilst a differential receiver and two single ended receivers provide USB DATA IN, SE0 and USB Reset condition detection. These cells also include integrated internal USB pull-up or pull-down resistors as required for host or slave mode.

4.2.9 USB Host / Device Controllers

These blocks handle the parallel-to-serial and serial-to-parallel conversion of the USB physical layer. This includes bit stuffing, CRC generation, USB frame generation and protocol error checking. The Host / Device controller is autonomous and therefore requires limited load from the CPU.

4.2.10 12MHz Oscillator

The 12MHz Oscillator cell generates a 12MHz reference clock input to the Clock Multiplier PLL from an external 12MHz crystal. The external crystal is connected across Pin 4 – XTIN and Pin 5 – XTOUT in the configuration shown in **Figure 10.1.**

4.2.11 Power Saving Modes and Standby mode.

VNC2 can be set to operate in three frequencies allowing the user to select a slower speed to reduce power consumption. Three operating frequencies available are 12MHz, 24MHz and normal operation of 48MHz. These operating modes can be configured using the RTOS. Full details are available in the RTOS manual available from the FTDI website.

When a particular peripheral is not used, it is powered down internally thus saving power.

Standby mode is available under firmware control, this mode puts the VNC2 in a state with no clocks running or system blocks powered. The device will wake up out of this mode by toggling any of the following signals: USB0/1 DP or DM, SPI slave 0 select (spi_s0_ss#), SPI slave 1select(spi_s1_ss#) or UART ring indicator (uart_ri#).

5 I/O Multiplexer

FTDI devices typically have multiple interfaces available to communicate with external devices. VNC2 has UART, SPI slave0, SPI slave1, SPI master, FIFO, GPIO, and PWM peripherals. The available packages for VNC2 provide any of these interfaces to be active on the available pins through the use of an I/O Multiplexer. **Table 5.1** lists the signals available for each peripheral. **Table 5.2 to 12** explain the use of the I/O multiplexer.

Multiplexers are used to connect the VNC2 peripherals to the external IOBUS pins. This enables the designer to select which IOBUS pins he wishes to map a particular peripheral to. Peripheral signals are allocated to one of four groups, which connect to the I/O multiplexer. Each I/O peripheral signal can connect to one out of every four external IOBUS pins. The IOBUS pin that a peripheral signal can connect to is dictated by the peripheral signal's group. For example, if a peripheral signal is allocated to group 0 then it can connect to IOBUS0, IOBUS4, IOBUS8, IOBUS12 and so on. If a peripheral signal is allocated to group 1 then it can connect to IOBUS1, IOBUS5, IOBUS9, IOBUS13 and so on. Figure 5.1 details the I/O multiplexer concept, where, for example, a white peripheral signal can connect to any white IOBUS pin, a green peripheral signal can connect to a green IOBUS pin. Figure 5.2, Figure 5.3 and Figure 5.4 give examples of connecting peripheral signals to differing IOBUS pins.

The IO Multiplexer also provides the following features:

- Ability to configure an I/O pad as an input, output or bidirectional pad.
- At power on reset, all pins are set as inputs by default. Whenever the I/O Mux is enabled the pins are configured as their default values listed Table 6 within section **3.12**.

Note: It is recommended not to reassign the debug interface signal (debug_if) from its default setting of IOBUS0 (Pin 11 on all packages). This assumes that the debug pin is required in the application design, if not, pin 11 can be assigned to any other group 0 signal.

An application (IOMUX) within the RTOS is available to aid with pin configuration, **Section 5.2** has more details.

Further details of the IO Multiplexer are available within Application Note AN_139 Vinculum-II IO Mux Explained.

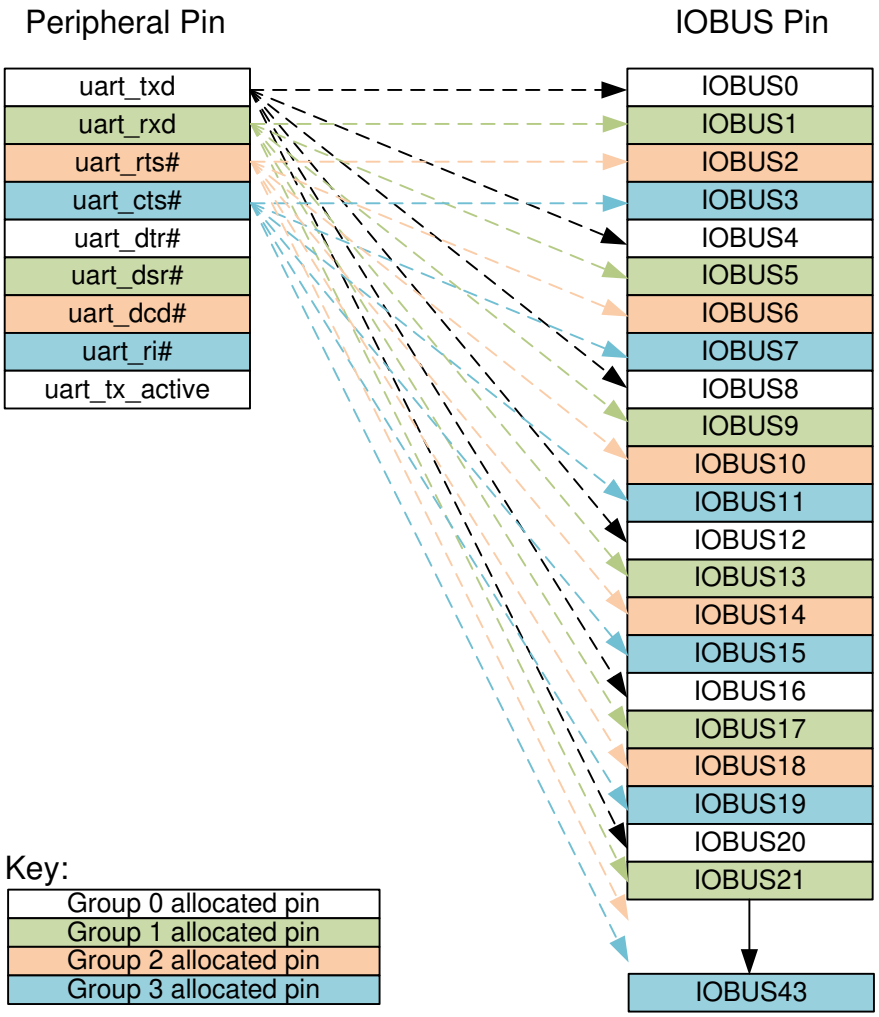

Figure 5.1 IOBUS to Group Relationship-64 Pin