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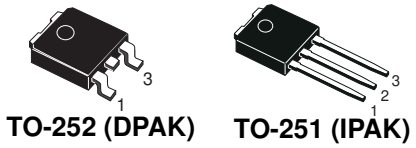
VNB14NV04, VND14NV04 VND14NV04-1, VNS14NV04

"OMNIFET II" fully autoprotected Power MOSFET

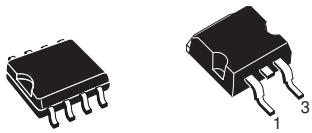
Features

TYPE	$R_{DS(on)}$	I_{lim}	V_{clamp}
VNB14NV04 VND14NV04 VND14NV04-1 VNS14NV04	35 mΩ	12 A	40 V

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFET



TO-252 (DPAK) TO-251 (IPAK)



SO-8 D²PAK

Description

The VNB14NV04, VND14NV04, VND14NV04-1 and VNS14NV04 are monolithic devices made using STMicroelectronics VIPower™ M0 technology, intended for replacement of standard power MOSFETS in DC to 50 KHz applications. Built-in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

Table 1. Device summary

Package	Tube	Tube (lead free)	Tape and reel	Tape and reel (lead free)
D²PAK	VNB14NV04	VNB14NV04-E	VNB14NV0413TR	VNB14NV04TR-E
TO-252 (DPAK)	VND14NV04	VND14NV04-E	VND14NV0413TR	VND14NV04TR-E
TO-251 (IPAK)	VND14NV04-1	VND14NV04-1-E	-	-
SO-8	VNS14NV04	-	-	-

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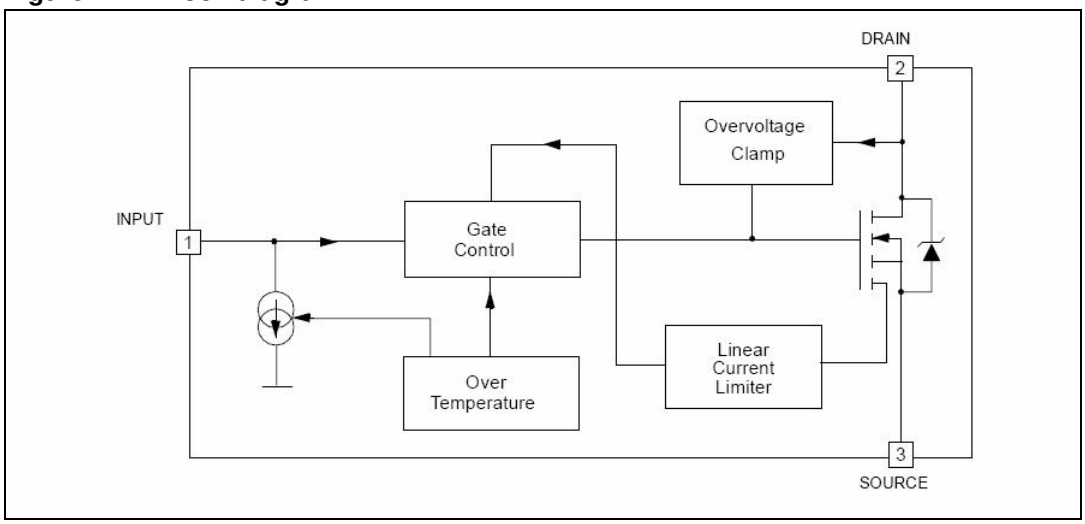
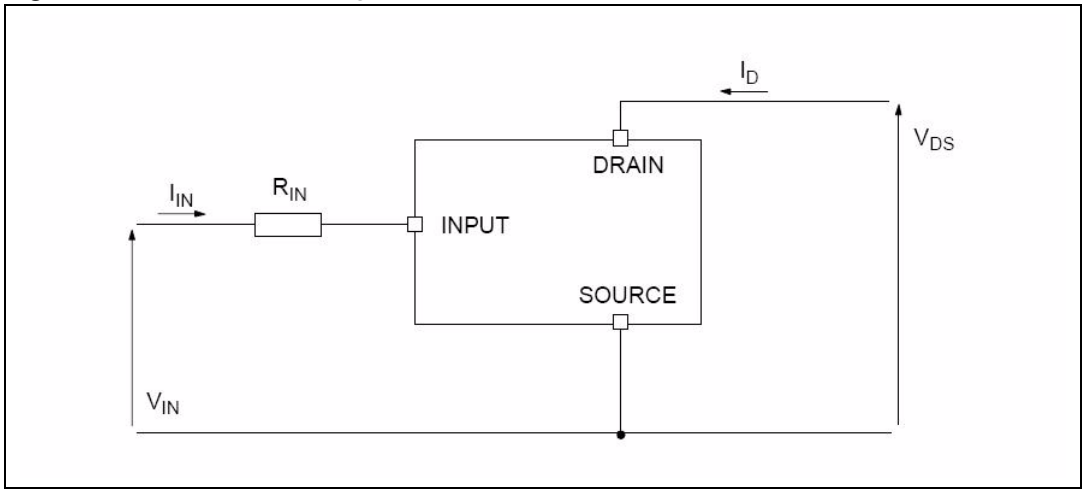
1 Block diagram

Figure 1. Block diagram



2 Electrical specification

Figure 2. Current and voltage conventions



2.1 Absolute maximum rating

Table 2. Absolute maximum rating

Symbol	Parameter	Value				Unit
		SO-8	DPAK	IPAK	D^2PAK	
V_{DS}	Drain-source voltage (V_{IN}=0 V)	Internally clamped				V
V_{IN}	Input voltage	Internally clamped				V
I_{IN}	Input current	+/-20				mA
$R_{IN\ MIN}$	Minimum input series impedance	10				Ω
I_D	Drain current	Internally limited				A
I_R	Reverse DC output current	-15				A
V_{ESD1}	Electrostatic discharge (R=1.5 KΩ, C=100 pF)	4000				V
V_{ESD2}	Electrostatic discharge on output pin only (R=330 Ω, C=150 pF)	16500				V
P_{tot}	Total dissipation at T_c=25 °C	4.6	74	74	74	W
E_{MAX}	Maximum switching energy (L=0.4 mH; R_L=0 Ω; V_{bat}=13.5 V; T_{jstart}=150 °C; I_L=18 A)		93		93	mJ
T_j	Operating junction temperature	Internally limited				°C
T_c	Case operating temperature	Internally limited				°C
T_{stg}	Storage temperature	-55 to 150				°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		SO-8	DPAK	IPAK	D^2PAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case max		1.7	1.7	1.7	°C/W
$R_{thj\text{-}lead}$	Thermal resistance junction-lead max	27				°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	90(1)	65(1)	102	52(1)	°C/W

1. When mounted on a standard single-sided FR4 board with 0.5 cm^2 of Cu (at least 35 µm thick) connected to all DRAIN pins. Horizontal mounting and no artificial air flow.

2.3 Electrical characteristics

-40 < Tj < 150 °C unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off						
V_{CLAMP}	Drain-source clamp voltage	V_{IN}=0 V; I_D=7 A	40	45	55	V
V_{CLTH}	Drain-source clamp threshold voltage	V_{IN}=0 V; I_D=2 mA	36			V
V_{INTH}	Input threshold voltage	V_{DS}=V_{IN}; I_D=1 mA	0.5		2.5	V
I_{ISS}	Supply current from input pin	V_{DS}=0 V; V_{IN}=5 V		100	150	µA
V_{INCL}	Input-source clamp voltage	I_{IN}=1 mA I_{IN}=-1 mA	6 -1.0	6.8	8 -0.3	V
I_{DSS}	Zero input voltage drain current (V_{IN}=0 V)	V_{DS}=13 V; V_{IN}=0 V; T_j=25 °C V_{DS}=25 V; V_{IN}=0 V			30 75	µA
On						
$R_{DS(on)}$	Static drain-source on resistance	V_{in} = 5 V I_D = 7 A T_j = 25 °C V_{in} = 5 V I_D = 7 A			35 70	mΩ
Dynamic (Tj=25°C, unless otherwise specified)						
g_{fs} (1)	Forward transconductance	V_{DD} = 13 V I_D = 7 A		18		S
C_{oss}	Output capacitance	V_{DS} = 13 V f = 1 MHz V_{IN} = 0 V		400		pF
Switching						
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V I_D = 7 A V_{gen} = 5 V R_{gen} = $R_{IN\ MIN}$ =10 Ω (see *Figure 3*)		80	250	ns
t_r	Rise time			350	1000	ns
$t_{d(off)}$	Turn-off delay time			450	1350	ns
t_f	Fall time			150	500	ns

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V I_d = 7 A V_{gen} = 5 V R_{gen} = 2.2 KΩ (see *Figure 3*)		1.5	4.5	µs
t_r	Rise time			9.7	30.0	µs
$t_{d(off)}$	Turn-off delay time				25.0	µs
t_f	Fall time			10.2	30.0	µs
$(di/dt)_{on}$	Turn-on current slope	V_{DD} = 15 V I_D = 7 A V_{gen} = 5 V R_{gen} = $R_{IN\ MIN}$ =10 Ω		16		A/µs
Q_i	Total input charge	V_{DD} = 12 V I_D = 7 A V_{in} = 5 V; I_{gen} = 2.13 mA (see *Figure 7*)		36.8		nC
Source drain diode						
V_{SD} (1)	Forward on voltage	I_{SD} = 7 A V_{in} = 0 V		0.8		V
t_{rr}	Reverse recovery time	I_{SD} = 7 A; di/dt = 40 A/µs V_{DD} = 30 V L = 200 µH (see test circuit, *Figure 4*)		300		ns
Q_{rr}	Reverse recovery charge			0.8		µC
I_{RRM}	Reverse recovery current			5		A
Protection						
I_{lim}	Drain current limit	V_{IN} = 5 V; V_{DS} = 13 V	12	18	24	A
t_{dlim}	Step response current limit	V_{IN} = 5 V; V_{DS} = 13 V		45		µs
T_{jsh}	Over temperature shutdown		150	175	200	°C
T_{jrs}	Over temperature reset		135			°C
I_{gf}	Fault sink current	V_{IN} = 5 V; V_{DS} = 13 V; T_j = T_{jsh}	10	15	20	mA
E_{as}	Single pulse avalanche energy	starting T_j = 25 °C; V_{DD} = 24 V V_{IN} = 5 V; R_{gen} = $R_{IN\ MIN}$ = 10 Ω; L = 24 mH (see *Figure 5* and *Figure 6*)	400			mJ

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

3 Protection features

During normal operation, the input pin is electrically connected to the gate of the internal power MOSFET through a low impedance path.

The device then behaves like a standard power MOSFET and can be used as a switch from DC up to 50 KHz. The only difference from the user's standpoint is that a small DC current I_{ISS} (typ. 100 µA) flows into the input pin in order to supply the internal circuitry.

The device integrates:

- Overvoltage clamp protection: internally set at 45 V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- Linear current limiter circuit: limits the drain current I_D to I_{lim} whatever the input pin voltages. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the over temperature threshold T_{jsh}.
- Over temperature and short circuit protection: these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Over temperature cutout occurs in the range 150 to 190 °C, a typical value being 170 °C. The device is automatically restarted when the chip temperature falls of about 15 °C below shutdown temperature.
- Status feedback: in the case of an over temperature fault condition ($T_j > T_{jsh}$), the device tries to sink a diagnostic current Igf through the input pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the input pin driver is not able to supply the current I_{gf}, the input pin will fall to 0 V. This will not however affect the device operation: no requirement is put on the current capability of the input pin driver except to be able to supply the normal operation drive current I_{ISS}.

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit.

Figure 3. Switching time test circuit for resistive load

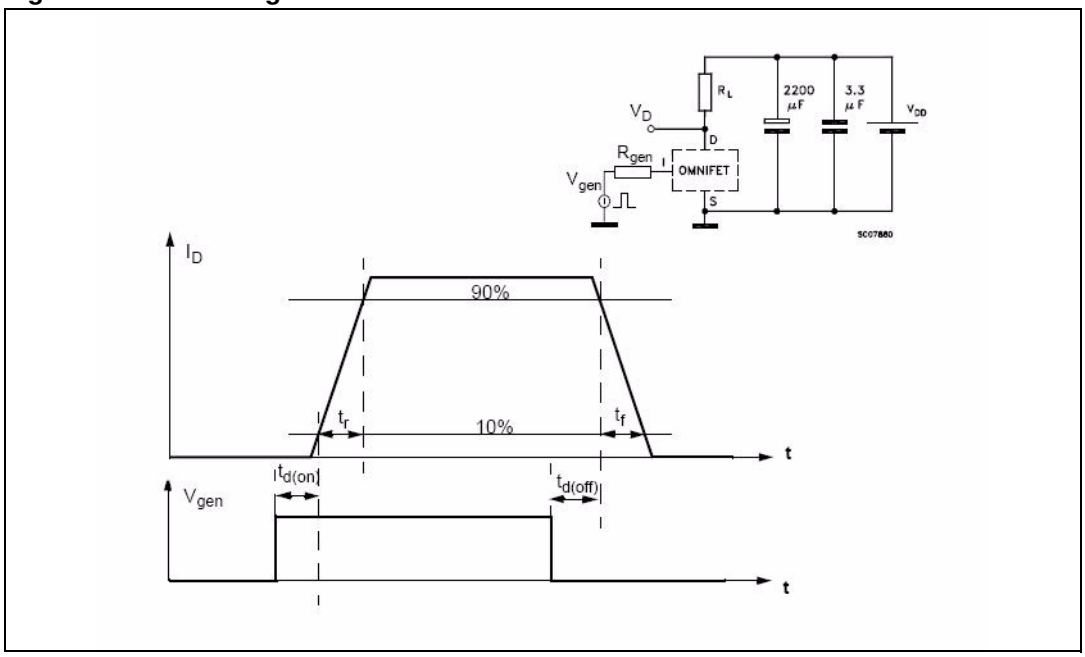


Figure 4. Test circuit for diode recovery times

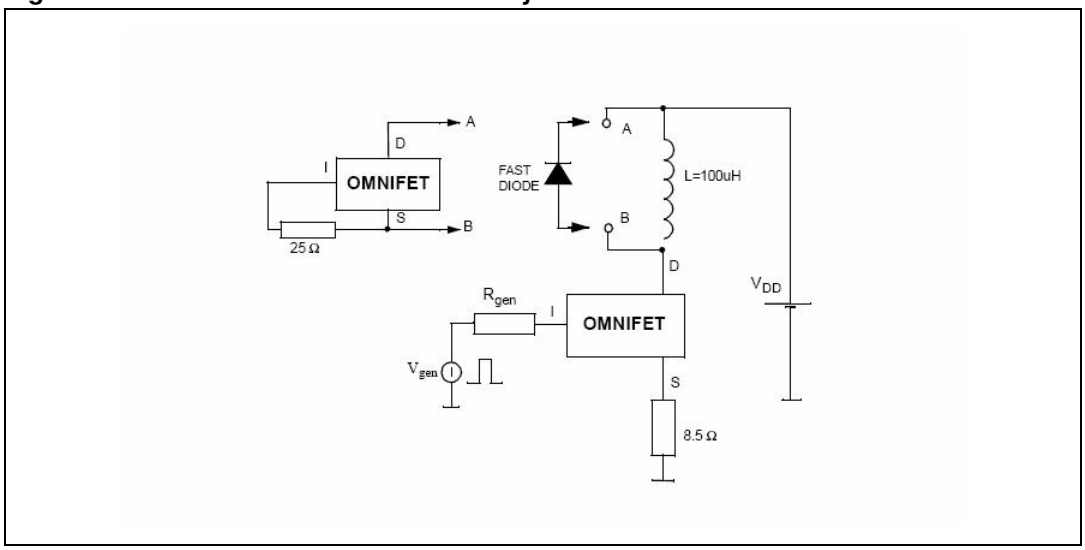


Figure 5. Unclamped inductive load test circuits

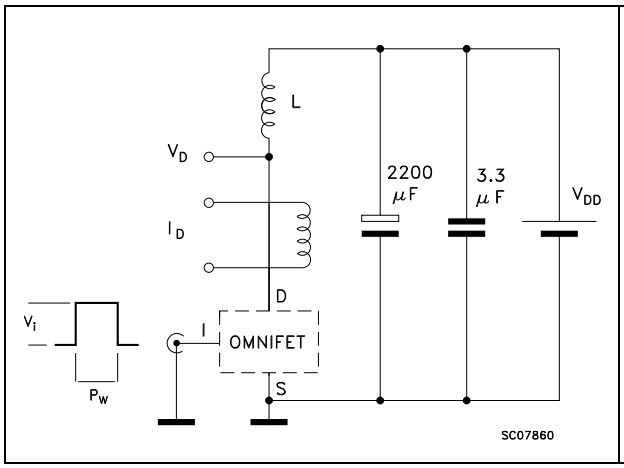


Figure 6. Unclamped inductive waveforms

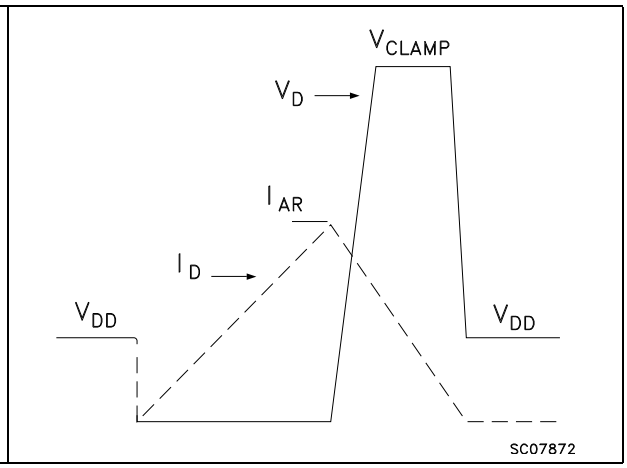


Figure 7. Input charge test circuit

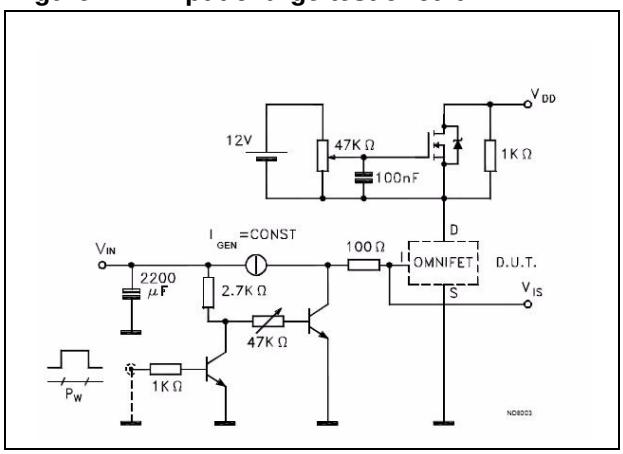


Figure 8. Source-drain diode forward characteristics

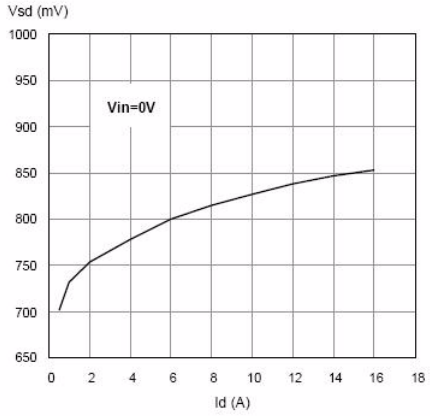


Figure 9. Static drain source on resistance

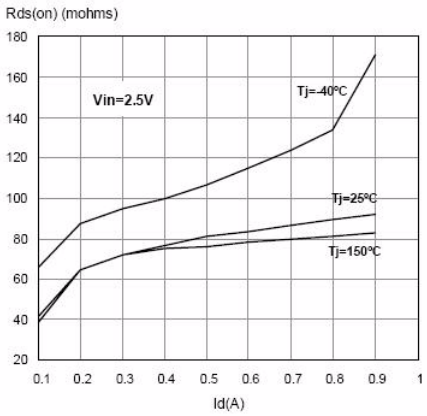


Figure 10. Derating curve

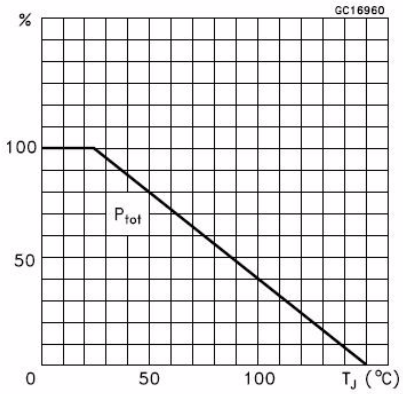


Figure 11. Static drain-source on resistance vs. input voltage (part 1/2)

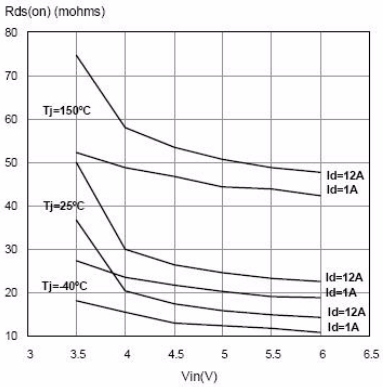


Figure 12. Static drain-source on resistance vs. input voltage (part 2/2)

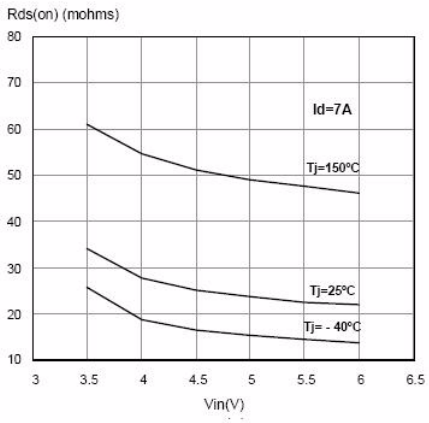


Figure 13. Transconductance

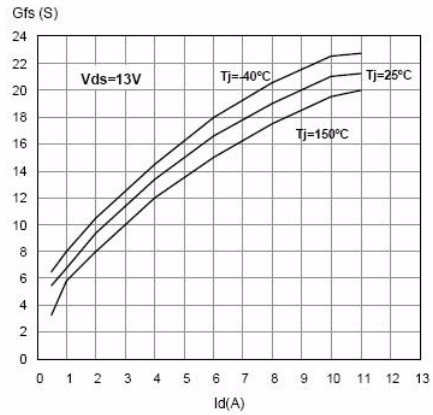


Figure 14. Static drain-source on resistance vs. id

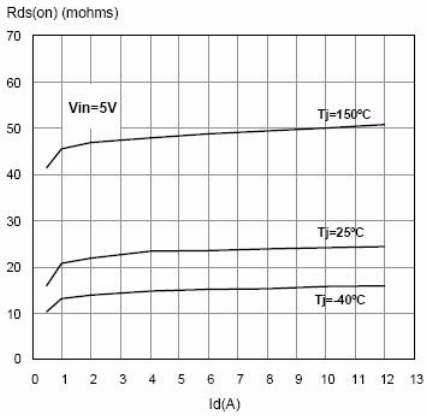


Figure 15. Transfer characteristics

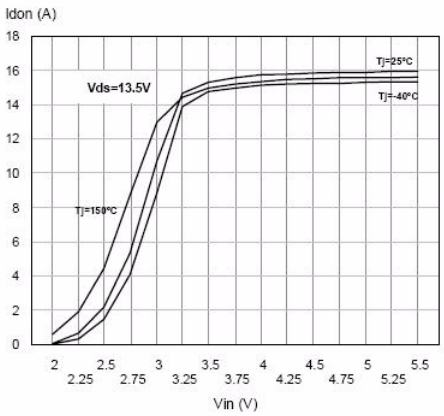


Figure 16. Turn-on current slope (part 1/2)

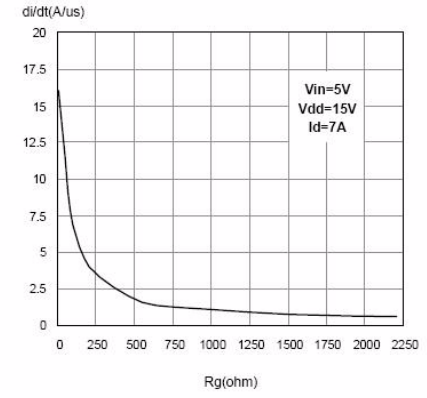


Figure 17. Turn-on current slope (part 2/2)

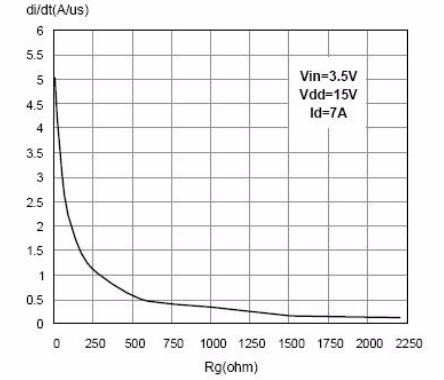


Figure 18. Input voltage vs. input charge

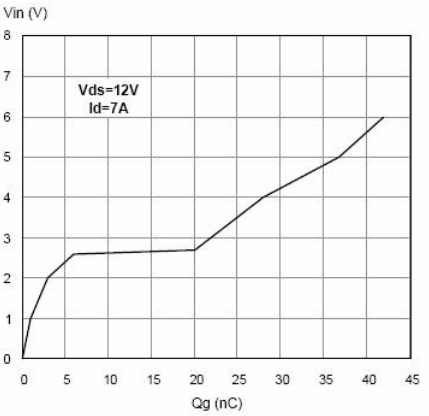


Figure 19. Turn-off drain source voltage slope (part 1/2)

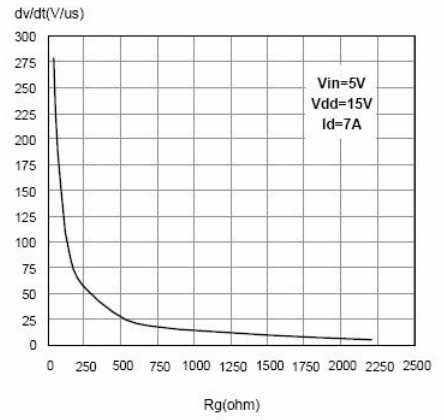


Figure 20. Turn-off drain source voltage slope (part 2/2)

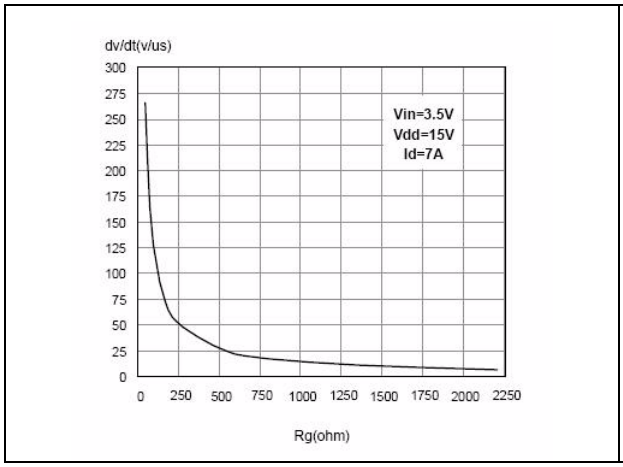


Figure 21. Capacitance variations

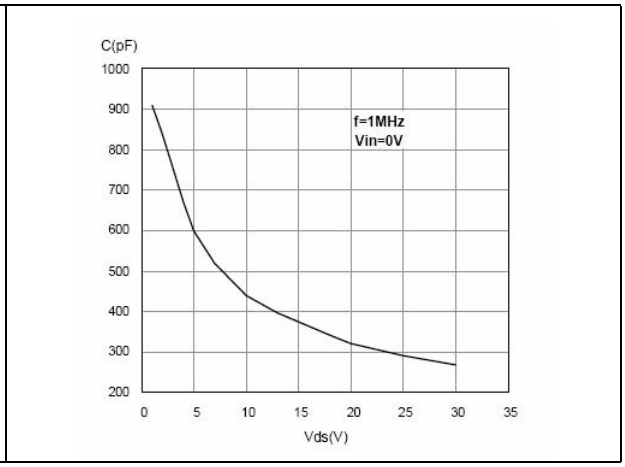


Figure 22. Switching time resistive load (part 1/2)

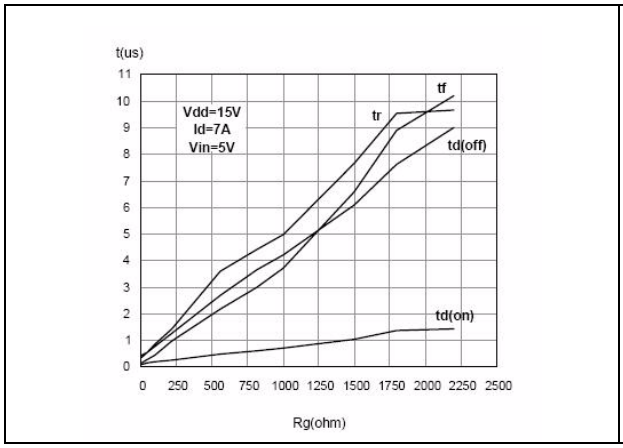


Figure 23. Switching time resistive load (part 2/2)

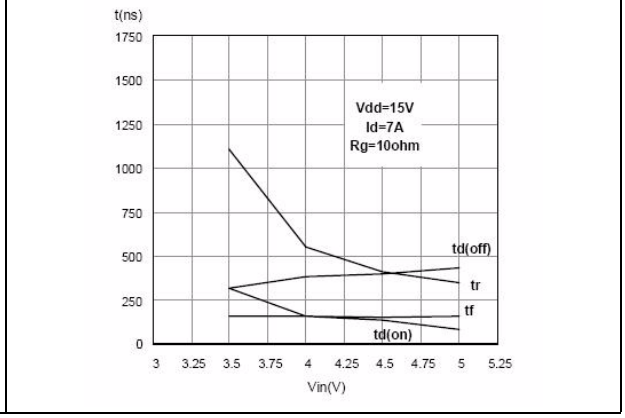
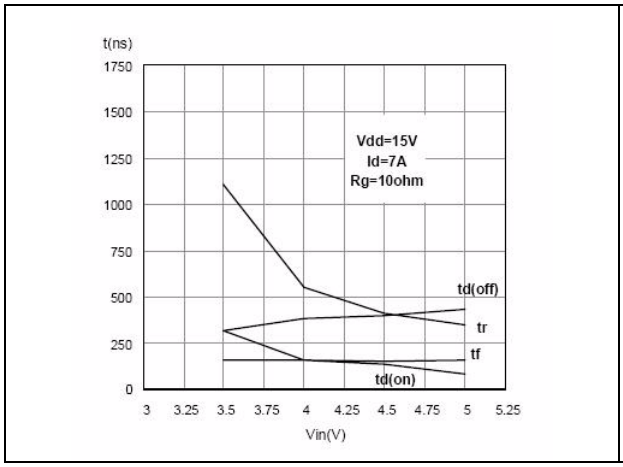


Figure 24. Output characteristics

Figure 25. Normalized on resistance vs. temperature



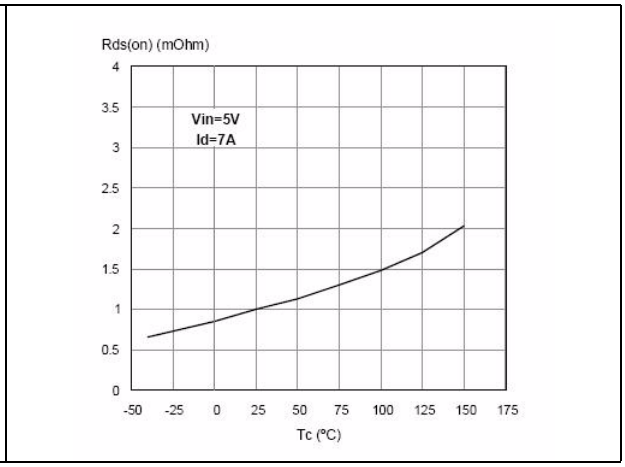


Figure 26. Normalized input threshold voltage vs. temperature

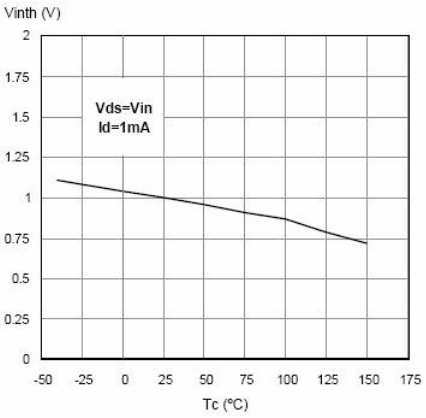


Figure 27. Current limit vs. junction temperatures

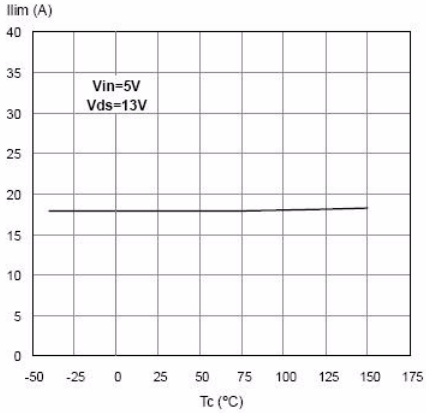


Figure 28. Step response current limit

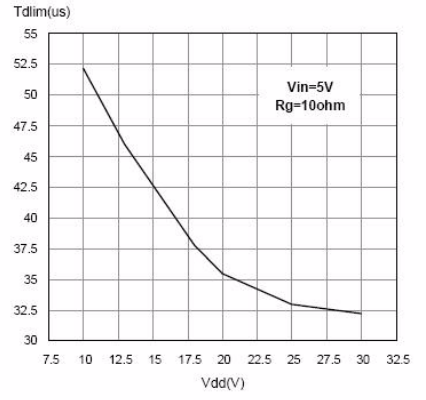
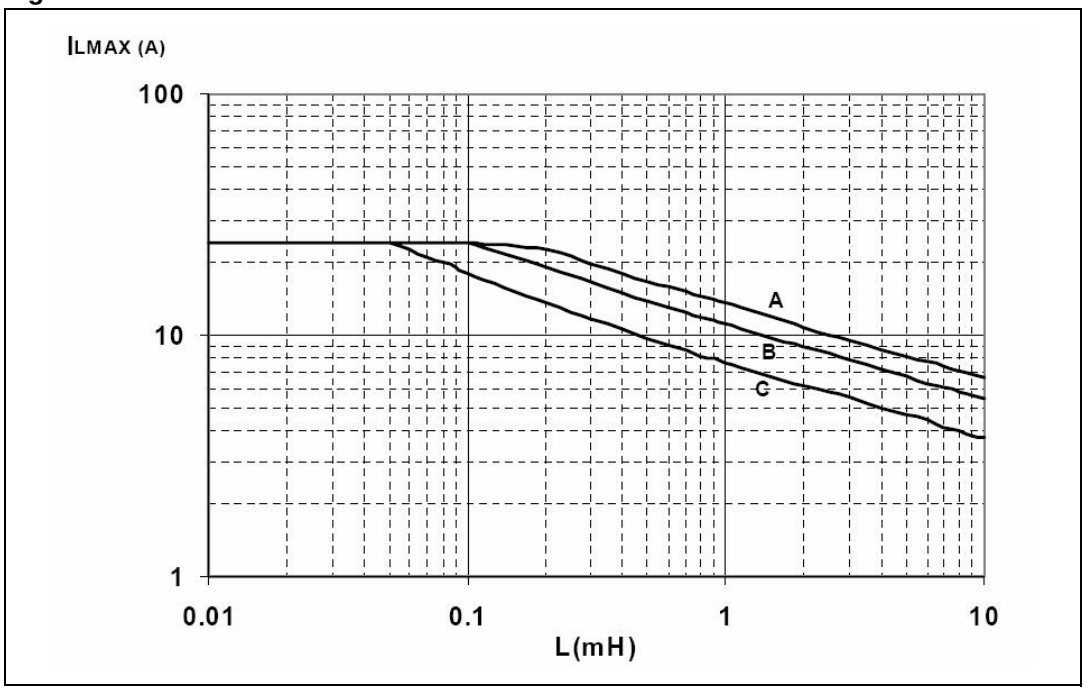


Figure 29. DPAK maximum turn-off current versus load inductance



Legend:

A= Single pulse at T_{Jstart}=150ºC

B= Repetitive pulse at T_{Jstart}=100ºC

C= Repetitive pulse at T_{Jstart}=125ºC

Conditions:

V_{CC}=13.5 V

Values are generated with R_L=0Ω

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

Figure 30. DPAK demagnetization

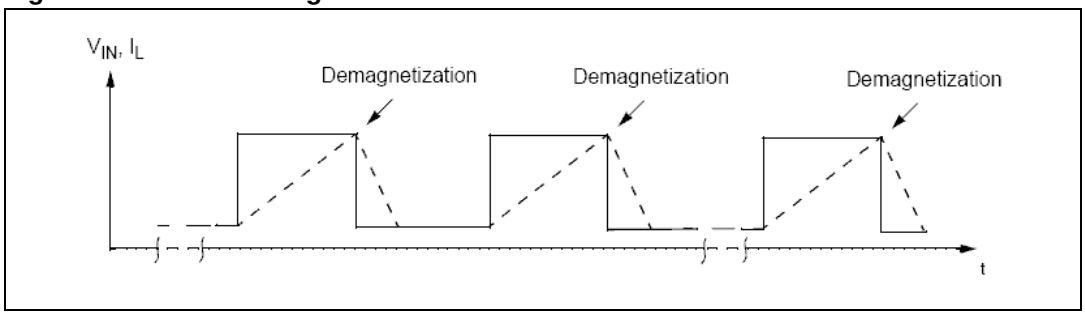
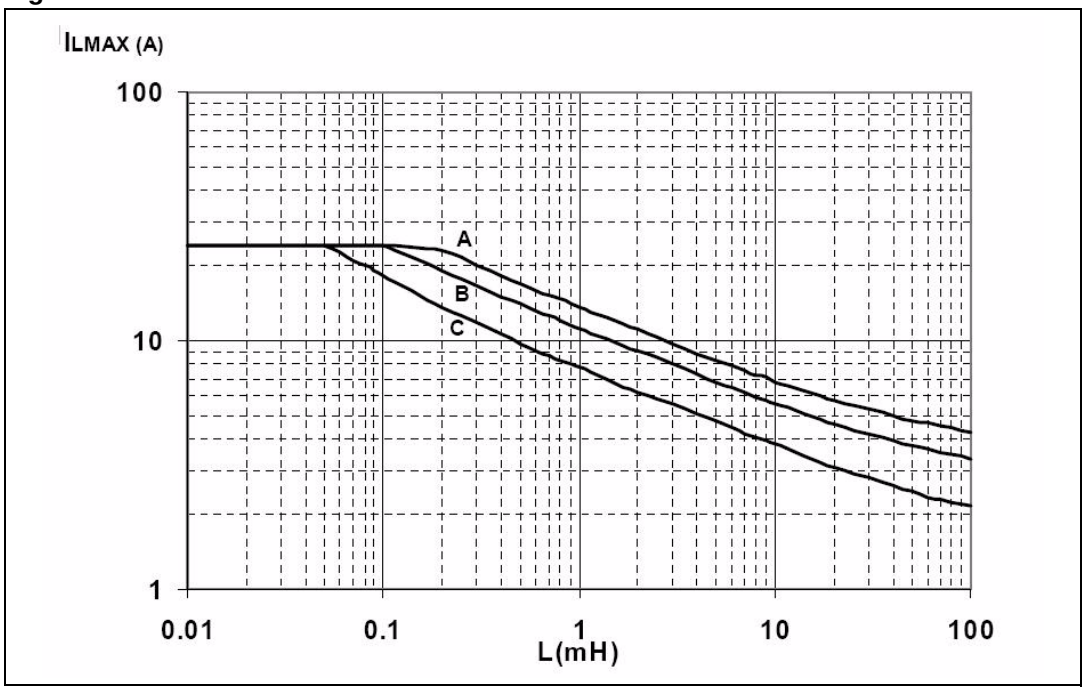


Figure 31. D²PAK maximum turn-off current versus load inductance



Legend:

A= Single pulse at T_{Jstart}=150ºC

B= Repetitive pulse at T_{Jstart}=100ºC

C= Repetitive pulse at T_{Jstart}=125ºC

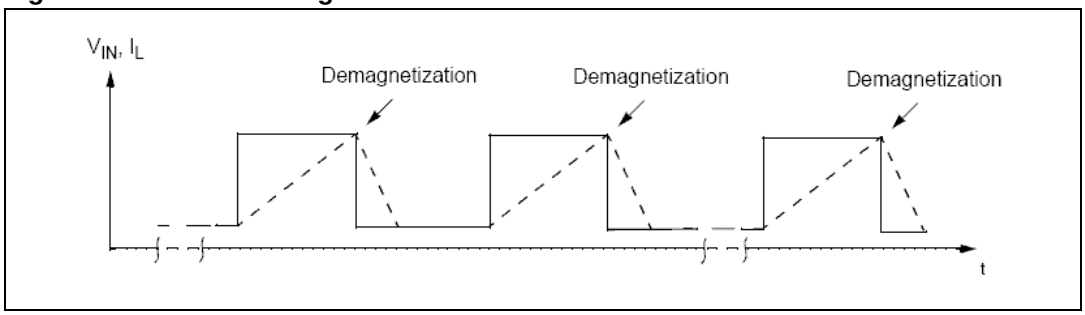
Conditions:

V_{CC}=13.5 V

Values are generated with R_L=0Ω

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

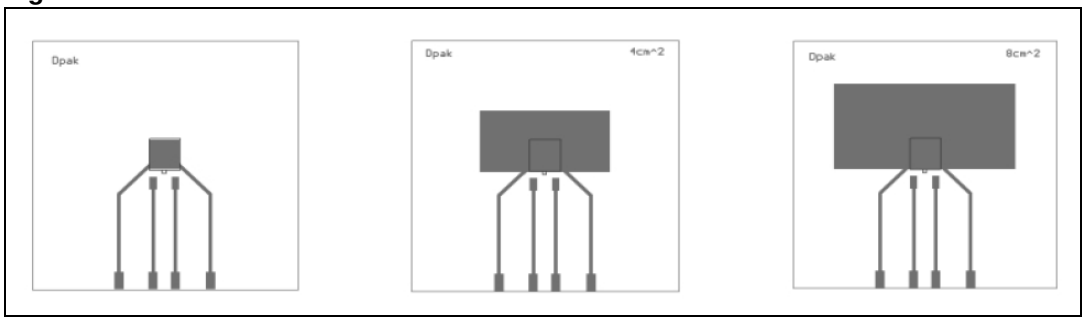
Figure 32. D²PAK demagnetization



4 Package thermal data

4.1 DPAK thermal data

Figure 33. DPAK PC board(1)



1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 60 mm x 60 mm, PCB thickness=2 mm, Cu thickness=35 µm, Copper areas: from minimum pad lay-out to 8 cm^2).

Figure 34. DPAK $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition

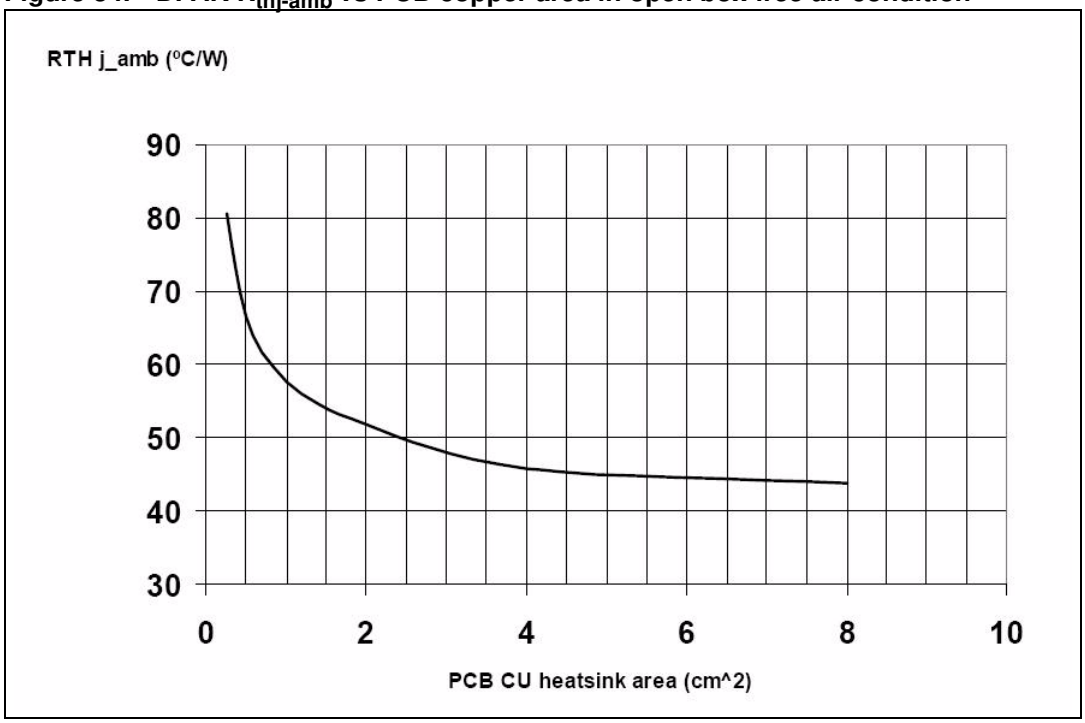


Figure 35. DPAK thermal impedance junction ambient single pulse

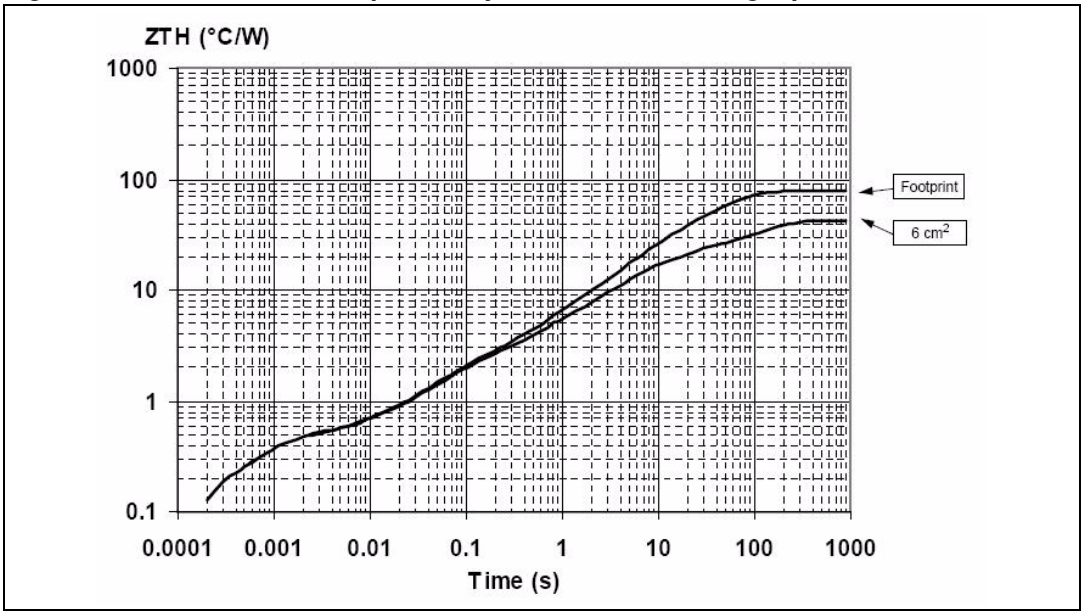
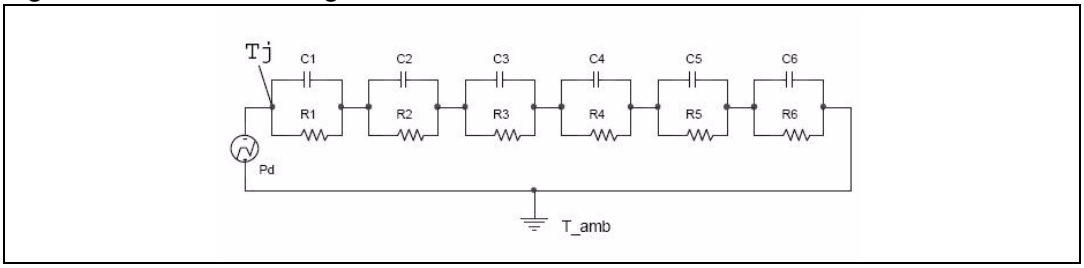


Figure 36. Thermal fitting model of an OMNIFET II in DPAK



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Table 5. DPAK thermal parameter

Area/island(cm²)	Footprint	6
R1 (°C/W)	0.1	
R2 (°C/W)	0.35	
R3 (°C/W)	1.20	
R4 (°C/W)	2	
R5 (°C/W)	15	
R6 (°C/W)	61	24
C1 (W.s/°C)	0.0006	
C2 (W.s/°C)	0.0021	
C3 (W.s/°C)	0.05	

Table 5. DPAK thermal parameter (continued)

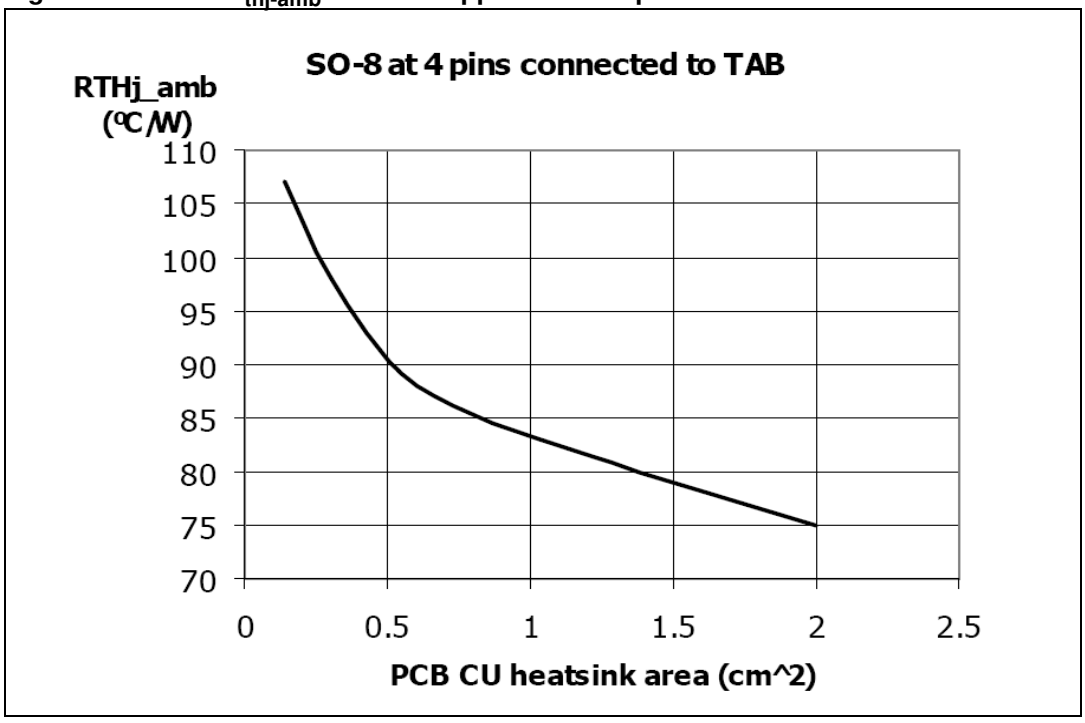
Area/island(cm^2)	Footprint	6
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.45	
C6 (W.s/°C)	0.8	5

4.2 SO-8 thermal data

Figure 37. SO-8 PC board(1)

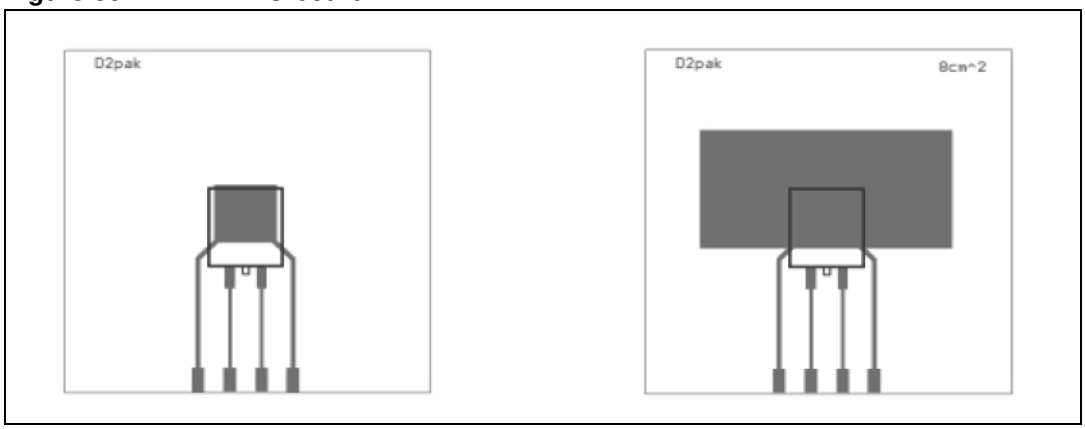
1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness=2 mm, Cu thickness=35 µm, Copper areas: 0.14 cm^2, 0.6 cm^2, 1.6 cm^2).

Figure 38. SO-8 $R_{thj-amb}$ vs PCB copper area in open box free air condition



4.3 D²PAK thermal data

Figure 39. D²PAK PC board(1)



1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 60 mm x 60 mm, PCB thickness=2 mm, Cu thickness=35 µm, Copper areas: from minimum pad lay-out to 8 cm^2).

Figure 40. D²PAK $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition

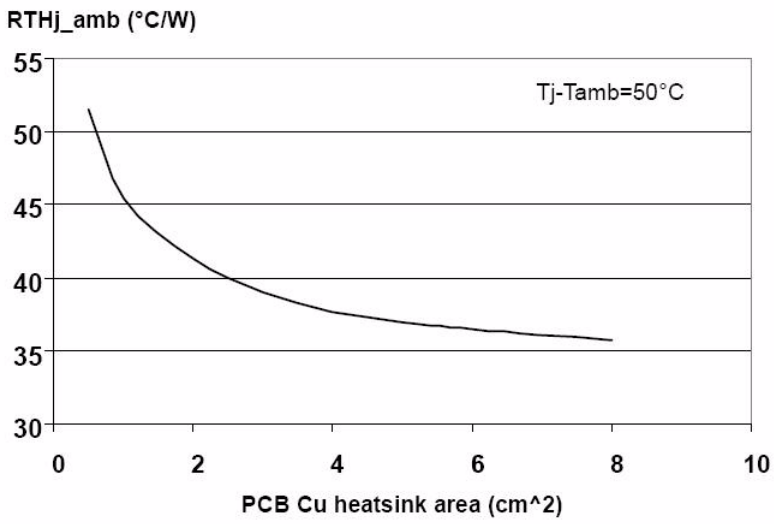


Figure 41. D²PAK thermal impedance junction ambient single pulse

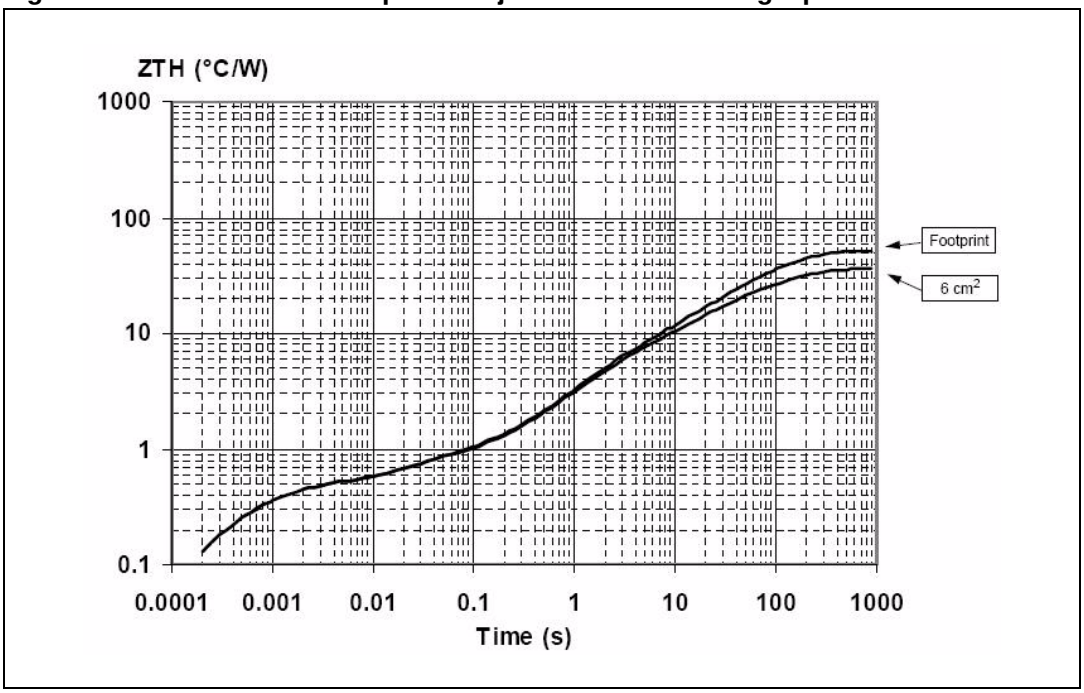
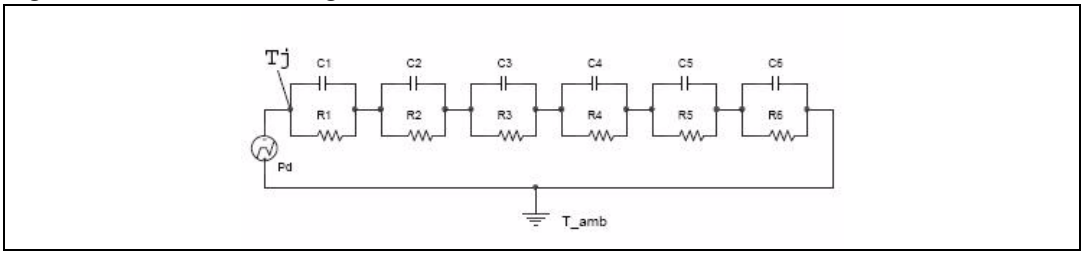


Figure 42. Thermal fitting model of an OMNIFET II in D²PAK



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Table 6. D²PAK thermal parameter

Area/island(cm²)	Footprint	6
R1 (°C/W)	0.1	
R2 (°C/W)	0.35	
R3 (°C/W)	0.3	
R4 (°C/W)	4	
R5 (°C/W)	9	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0006	
C2 (W.s/°C)	2.10E-03	

Table 6. D²PAK thermal parameter (continued)

Area/island(cm²)	Footprint	6
C3 (W.s/°C)	8.00E-02	
C4 (W.s/°C)	0.45	
C5 (W.s/°C)	2	
C6 (W.s/°C)	3	5

5 Package information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

5.2 TO-251 (IPAK) mechanical data

Figure 43. TO-251 (IPAK) package dimension

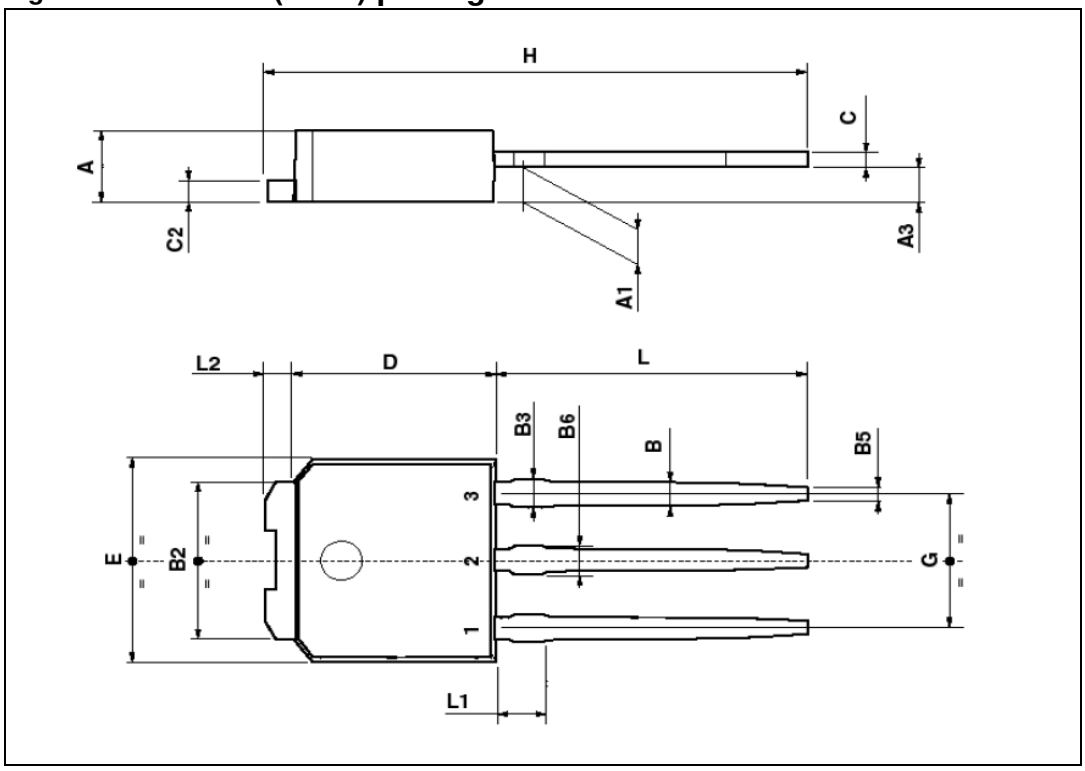


Table 7. TO-251 (IPAK) mechanical data

Dim.	Millimeters		
	Min.	Typ.	Max.
A	2.2		2.4
A1	0.9		1.1
A3	0.7		1.3
B	0.64		0.9
B2	5.2		5.4

Table 7. TO-251 (IPAK) mechanical data (continued)

Dim.	Millimeters		
	Min.	Typ.	Max.
B3			0.85
B5		0.3	
B6			0.95
C	0.45		0.6
C2	0.48		0.6
D	6		6.2
E	6.4		6.6
G	4.4		4.6
H	15.9		16.3
L	9		9.4
L1	0.8		1.2
L2		0.8	1

5.3 D²PAK mechanical data

Figure 44. D²PAK package dimension