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VND5E008AY-E

Double channel high-side driver with analog current sense for automotive applications

Datasheet - production data

PowerSSO-36

Features

Max transient supply voltage	V_{CC}	41 V
Operating voltage range	V_{CC}	4.5 to 28V
Typ on-state resistance (per ch.)	R_{ON}	8 mΩ
Current limitation (typ)	I_{LIMH}	76 A
Off-state supply current	I_S	2 µA(1)

1. Typical value with all loads connected.

- General:
  - Inrush current active management by power limitation
  - Very low standby current
  - 3.0V CMOS compatible input
  - Optimized electromagnetic emission
  - Very low electromagnetic susceptibility
  - Compliant with European directive 2002/95/EC
  - Proportional load current sense
  - High current sense precision for wide range current
  - Very low current sense leakage
- Diagnostic functions:
  - Off-state open-load detection
  - Current sense disable
  - Thermal shutdown indication
  - Output short to V_{CC} detection
  - Overload and short to ground (power limitation) indication
- Protection:
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of V_{CC}
  - Thermal shut down
  - Reverse battery protection with self switch of the Power MOS

Applications

- All types of resistive, inductive and capacitive loads

Description

The VND5E008AY-E is a device made using STMicroelectronics® VIPower® MO-5 technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes.

This device integrates an analog current sense which delivers a current proportional to the load current when CS_DIS high leads the current sense pin in high impedance.

Fault conditions such as overload, overtemperature or open-load are reported via the current sense pin

Output current limitation protects the device in overload condition. In case of long overload duration, the device limits the dissipated power to safe level up to thermal shutdown intervention. Thermal shutdown with automatic restart allows the device to recover normal operation as soon as fault condition disappears.

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1 Block diagram and pin description

Figure 1. Block diagram

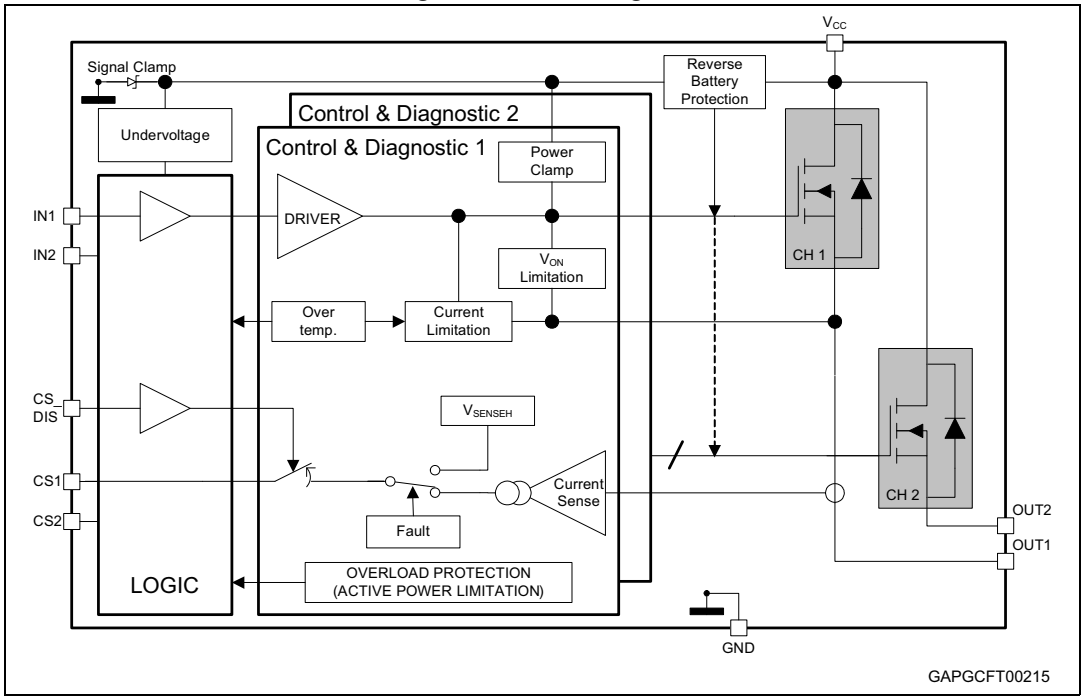


Table 1. Pin function

Name	Function
V_{CC}	Battery connection
$OUT_{1,2}$	Power output
GND	Ground connection
$IN_{1,2}$	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state
$CS_{1,2}$	Analog current sense pin, delivers a current proportional to the load current
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin

Figure 2. Configuration diagram (top view)

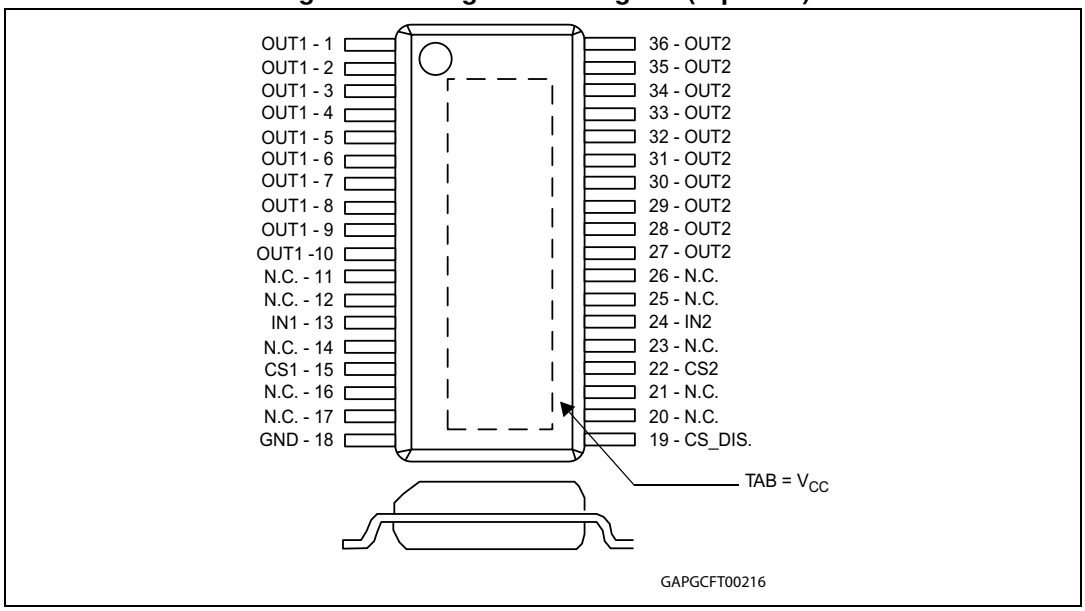
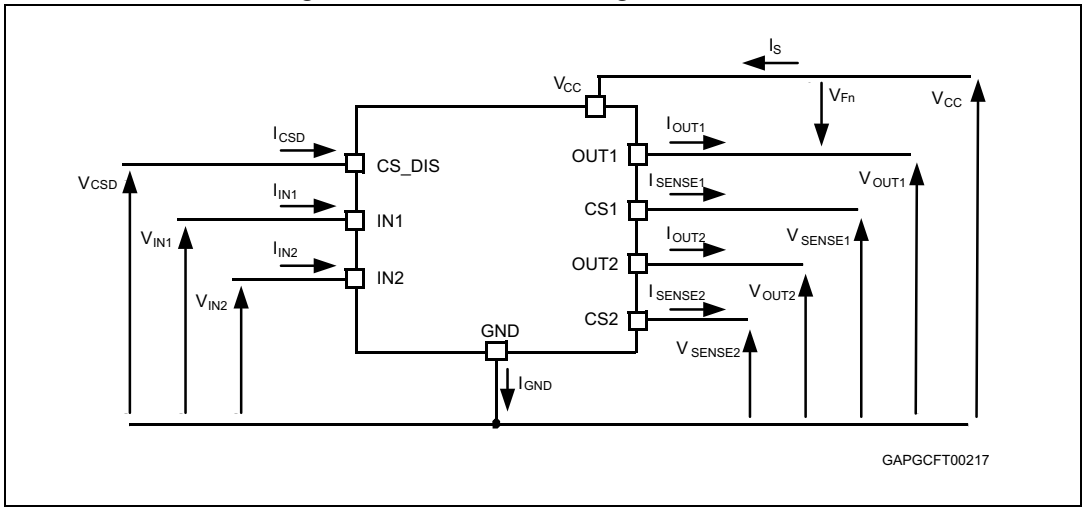


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input	CS_DIS
Floating	Not allowed	X	X	X	X
To ground	Through 1 KΩ resistor	X	Not allowed	Through 10 KΩ resistor	Through 10 KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	28	V
V_{CCPK}	Transient supply voltage (T < 400 ms, R_{LOAD} > 1 Ω)	41	V
$-V_{CC}$	Reverse DC supply voltage	16	V
V_{CC_LSC}	Maximum supply voltage for full protection to short-circuit (acc. AEC-Q100-012)	18	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	50	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
V_{CSENSE}	Current sense maximum voltage	V_{CC} - 41 $+V_{CC}$	V V
E_{MAX}	Maximum switching energy (single pulse) (L = 0.85 mH; R_L = 0 Ω; V_{bat} = 13.5 V; T_{jstart} = 150 °C; I_{OUT} = I_{limL}*(Typ.)*)	260	mJ
V_{ESD}	Electrostatic Discharge (Human Body Model: R = 1.5 KΩ; C = 100 pF) – V_{CC}, OUTPUT – INPUT, CS_DIS – CURRENT SENSE	 5000 4000 2000	V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case (MAX) (with one channel ON)	0.85	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (MAX)	See *Figure 36* in the Thermal section	°C/W

2.3 Electrical characteristics

8 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C, unless otherwise specified

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	ON-state resistance	I_{OUT} = 6 A; T_j = 25 °C		8		mΩ
		I_{OUT} = 6 A; T_j = 150 °C			15	mΩ
		I_{OUT} = 6 A; V_{CC} = 5 V; T_j = 25 °C			11	mΩ
$R_{ON\ REV}$	Reverse battery ON-state resistance	V_{CC} = -13 V; I_{OUT} = -6 A; T_j = 25 °C		8		mΩ
V_{clamp}	Clamp Voltage	I_S = 20 mA	41	46	52	V
I_S	Supply current	Off-state; V_{CC} = 13 V; T_j = 25 °C; V_{IN} = V_{OUT} = V_{SENSE} = V_{CSD} = 0 V		2 (1)	5(1)	µA
		On-state; V_{CC} = 13 V; V_{IN} = 5 V; I_{OUT} = 0 A		3.5	6.5	mA
$I_{L(off)}$	Off-state output current (2)	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 25 °C	0	0.01	3	µA
		V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 125 °C			5	µA

1. PowerMOS leakage included.
2. For each channel.

Table 6. Switching (V_{CC} = 13V; T_j = 25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 2.2 Ω (see *Figure 8*)	—	30	—	µs
$t_{d(off)}$	Turn-off delay time	R_L = 2.2 Ω (see *Figure 8*)	—	15	—	µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	R_L = 2.2 Ω	—	See *Figure 23*	—	V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	R_L = 2.2 Ω	—	See *Figure 24*	—	V/µs
W_{ON}	Switching energy losses during t_{won}	R_L = 2.2 Ω (see *Figure 8*)	—	1.2	—	mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L = 2.2 Ω (see *Figure 8*)	—	0.43	—	mJ

Table 7. Current sense (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.25 A; V_{SENSE} = 0.5 V T_j = -40 °C...150 °C	3658	6000	8926	
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 6 A; V_{SENSE} = 0.5 V T_j = -40 °C...150 °C T_j = 25 °C...150 °C	3910 4336	6000 6000	8928 8044	
dK_1/K_1 (1)	Current sense ratio drift	I_{OUT} = 6 A; V_{SENSE} = 0.5 V V_{CSD} = 0 V; T_J= -40 °C to 150 °C	-12		12	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 10 A; V_{SENSE} = 4 V T_j = -40 °C...150 °C T_j = 25 °C...150 °C	4948 5298	6000 6000	7372 6762	
dK_2/K_2 (1)	Current sense ratio drift	I_{OUT} = 10 A; V_{SENSE} = 4 V; V_{CSD} = 0 V; T_j = -40 °C to 150 °C	-7		7	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 25 A; V_{SENSE} = 4 V T_j = -40 °C...150 °C T_j = 25 °C...150 °C	5455 5535	6000 6000	6762 6282	
dK_3/K_3 (1)	Current sense ratio drift	I_{OUT} = 25 A; V_{SENSE} = 4 V; V_{CSD}= 0V; T_j = -40 °C to 150 °C	-5		5	%
I_{SENSE0}	Analog sense leakage current	I_{OUT} = 0 A; V_{SENSE} = 0 V; V_{CSD} = 5 V; V_{IN} = 0 V; T_j = -40 °C...150 °C	0		1	µA
		V_{CSD} = 0 V; V_{IN} = 5 V; T_j = -40 °C...150 °C	0		2	µA
		I_{OUT} = 6 A; V_{SENSE} = 0 V; V_{CSD} = V_{IN} = 5 V;	0		1	µA
V_{SENSE}	Max analog sense output voltage	I_{OUT} = 15 A; V_{CSD} = 0 V	5			V
V_{SENSEH}	Analog sense output voltage in overtemperature condition (2)	V_{CC} = 13 V; R_{SENSE} = 10 KΩ		8		V
I_{SENSEH}	Analog sense output current in overtemperature condition (2)	V_{CC} = 13 V; V_{SENSE} = 5 V		9		mA
$t_{DSENSE1H}$	Delay Response time from falling edge of CS_DIS pin	V_{SENSE} < 4 V, 1.5 A < I_{OUT} < 25 A I_{SENSE} = 90 % of $I_{SENSE\ max}$ (see *Figure 4*)		50	100	µs

Table 7. Current sense (8 V < V_{CC} < 18 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{DSENSE1L}$	Delay Response time from rising edge of CS_DIS pin	V_{SENSE} < 4 V, 1.5 A < I_{OUT} < 25 A I_{SENSE} = 10 % of $I_{SENSE\ max}$ (see *Figure 4*)		5	20	µs
$t_{DSENSE2H}$	Delay Response time from rising edge of INPUT pin	V_{SENSE} < 4 V, 1.5 A < I_{OUT} < 25 A I_{SENSE} = 90 % of $I_{SENSE\ max}$ (see *Figure 4*)		70	300	µs
$\Delta t_{DSENSE2H}$	Delay response time between rising edge of output current and rising edge of current sense	V_{SENSE} < 4 V, I_{SENSE} = 90 % of $I_{SENSEMAX}$, I_{OUT} = 90 % of I_{OUTMAX} I_{OUTMAX} = 5 A (see *Figure 11*)			300	µs
$t_{DSENSE2L}$	Delay Response time from falling edge of INPUT pin	V_{SENSE} < 4 V, 1.5 A < I_{OUT} < 25 A I_{SENSE} = 10 % of $I_{SENSE\ max}$ (see *Figure 4*)		100	250	µs

1. Parameter guaranteed by design; it is not tested.
2. Fault condition includes: power limitation, overtemperature and open load OFF-state detection.

Table 8. Open-load detection (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{OL}	Open-load off-state voltage detection threshold	V_{IN} = 0 V	2	—	4	V
t_{DSTKON}	Output short circuit to V_{CC} detection delay at turn-off	See *Figure 5*	180	—	1200	µs
$I_{L(off2)r}$	Off-state output current at V_{OUT} = 4 V	V_{IN} = 0V; V_{SENSE} = 0 V; V_{OUT} rising from 0 V to 4 V	-120	—	90	µA
$I_{L(off2)f}$	Off-state output current at V_{OUT} = 2 V	V_{IN} = 0V; V_{SENSE} = V_{SENSEH}; V_{OUT} falling from V_{CC} to 2 V	-50	—	90	µA

Table 9. Protections (1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	V_{CC} = 13 V	53	76	106	A
		5 V < V_{CC} < 18 V			106	A
I_{limL}	Short circuit current during thermal cycling	V_{CC} = 13 V; T_R < T_j < T_{TSD}		21		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} +1	T_{RS} +5		°C
T_{RS}	Thermal reset of STATUS		135			°C

Table 9. Protections (1) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 2 A; V_{IN} = 0; L = 6 mH	V_{CC}-29	V_{CC}-32	V_{CC}-36	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 0.4 A; T_j = -40 °C...150 °C (see *Figure 10*)		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 10. Logic input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.5		7	V
		I_{IN} = -1 mA		-0.7		V
V_{CSDL}	CS_DIS low level voltage				0.9	V
I_{CSDL}	Low level CS_DIS current	V_{CSD} = 0.9 V	1			µA
V_{CSDH}	CS_DIS high level voltage		2.1			V
I_{CSDH}	High level CS_DIS current	V_{CSD} = 2.1 V			10	µA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	I_{CSD} = 1 mA	5.5		7	V
		I_{CSD} = -1 mA		-0.7		V

Figure 4. Current sense delay characteristics

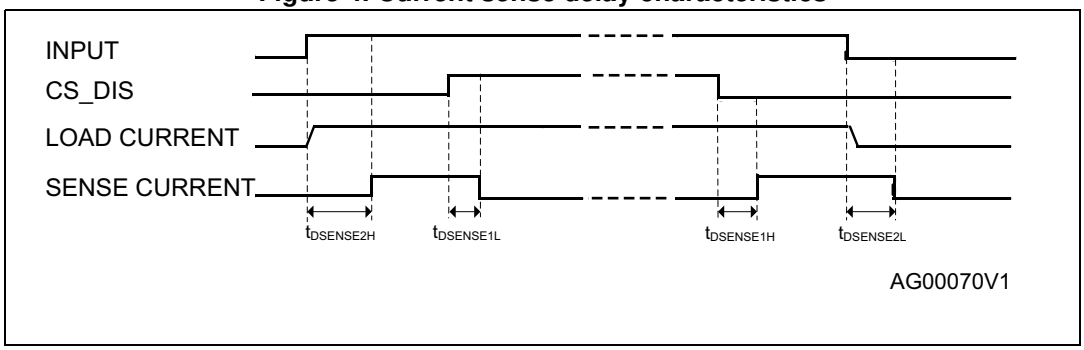


Figure 5. Open-load off-state delay timing

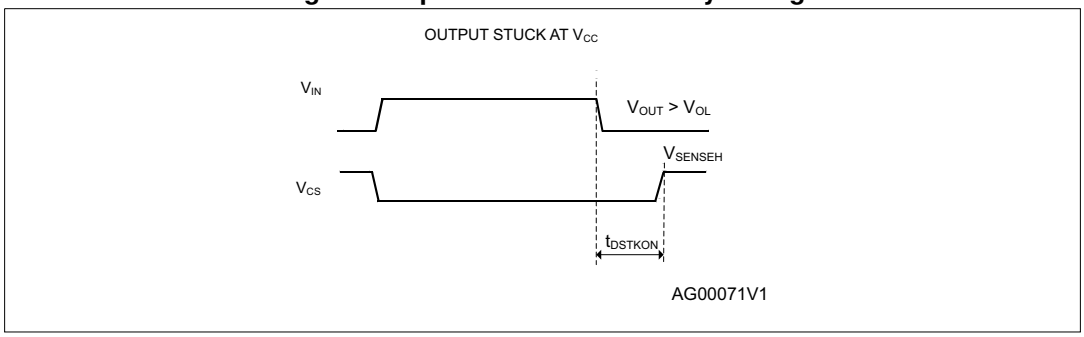


Figure 6. I_{OUT}/I_{SENSE} vs I_{OUT}

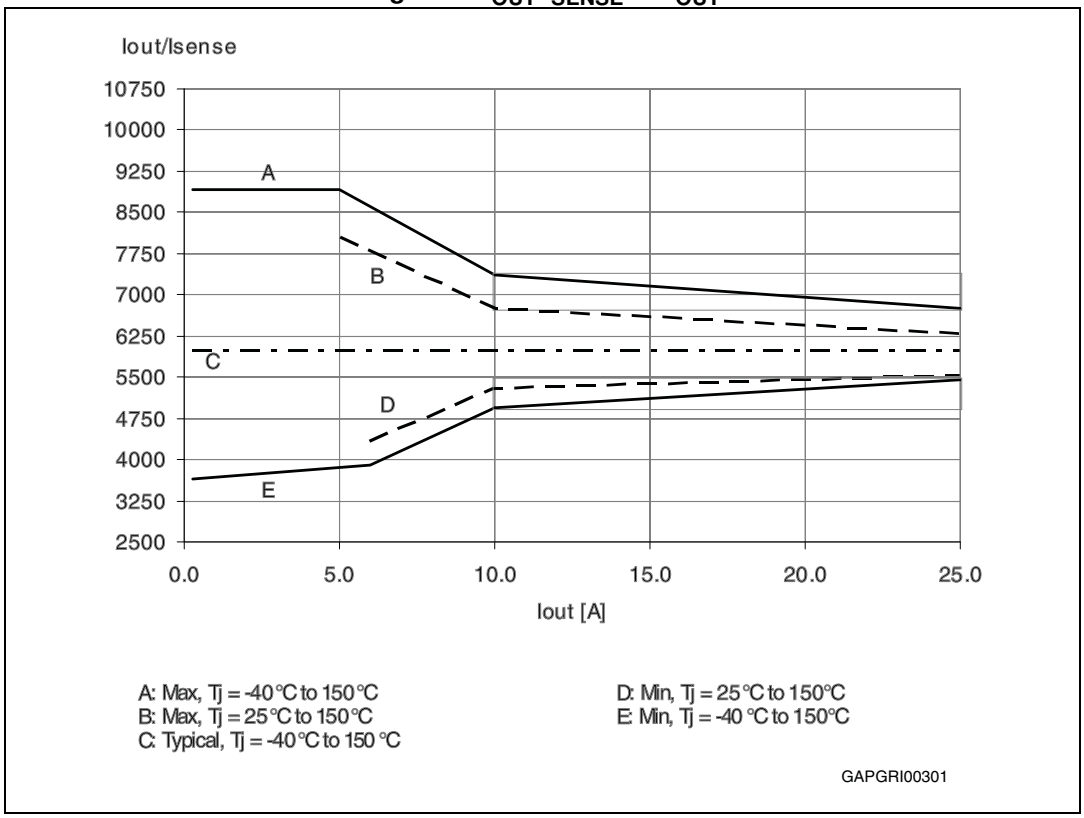


Figure 7. Maximum current sense ratio drift vs load current

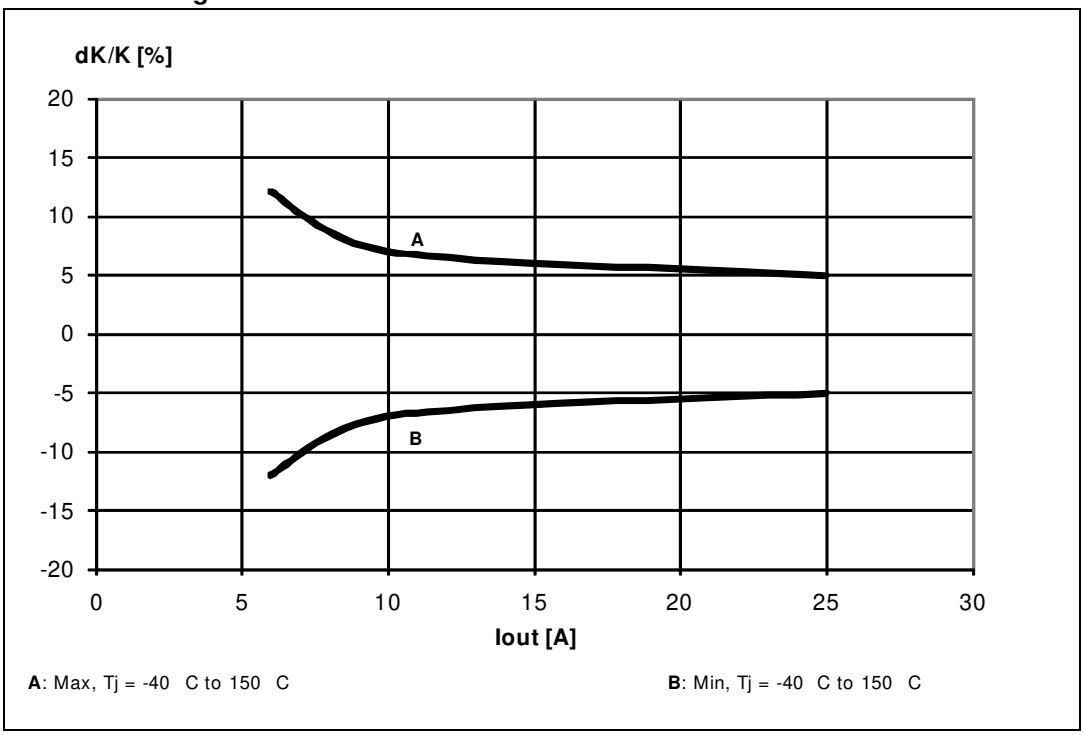


Table 11. Truth table

Conditions	Input	Output	Sense (V_{CSD} = 0 V)(1)
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overload	H H	X (no power limitation) Cycling (power limitation)	Nominal V_{SENSEH}
Short circuit to GND (Power limitation)	L H	L L	0 V_{SENSEH}
Open-load off-state (with external pull up)	L	H	V_{SENSEH}
Short circuit to V_{CC} (external pull up disconnected)	L H	H H	V_{SENSEH} < Nominal
Negative output voltage clamp	L	L	0

1. If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Figure 8. Switching characteristics

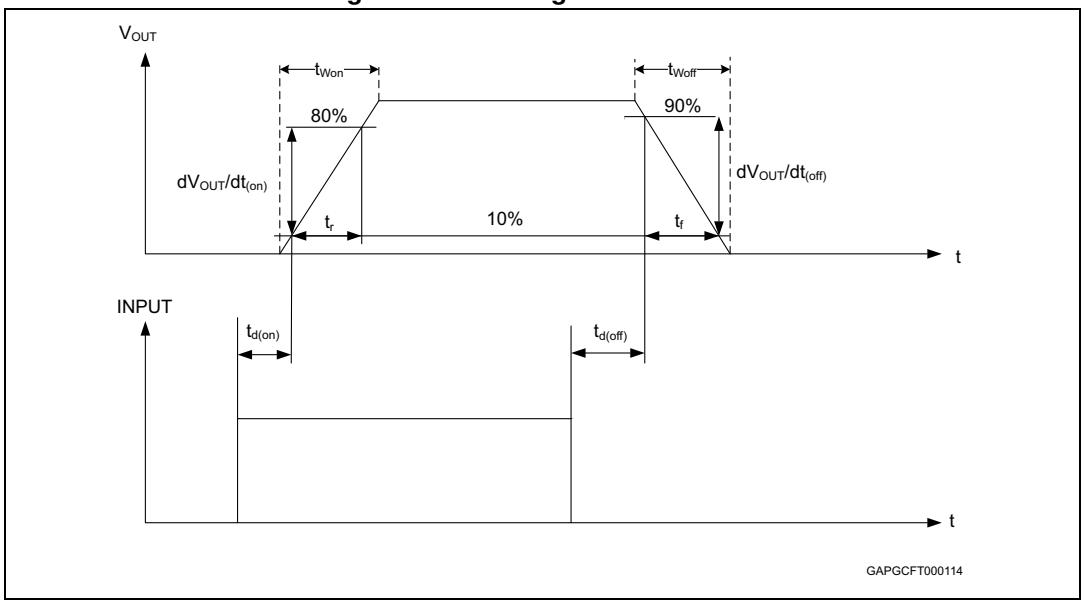


Figure 9. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

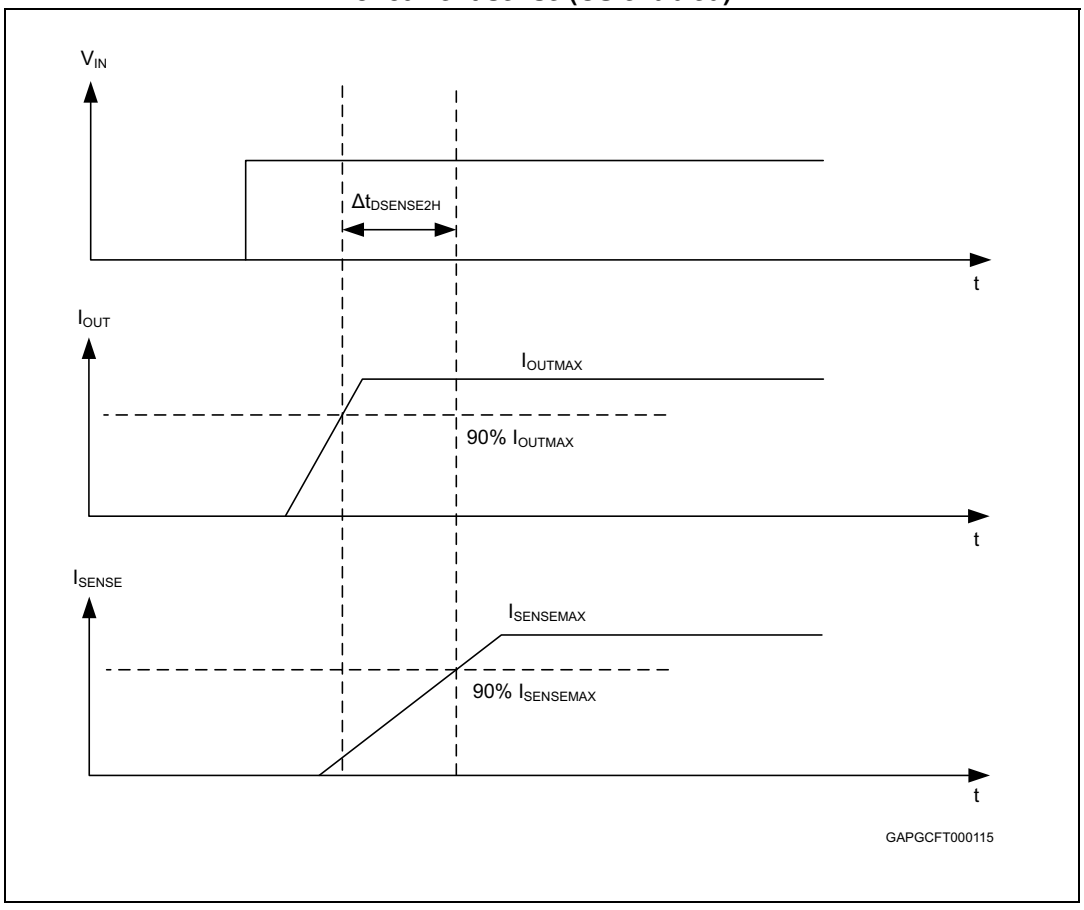


Figure 10. Output voltage drop limitation

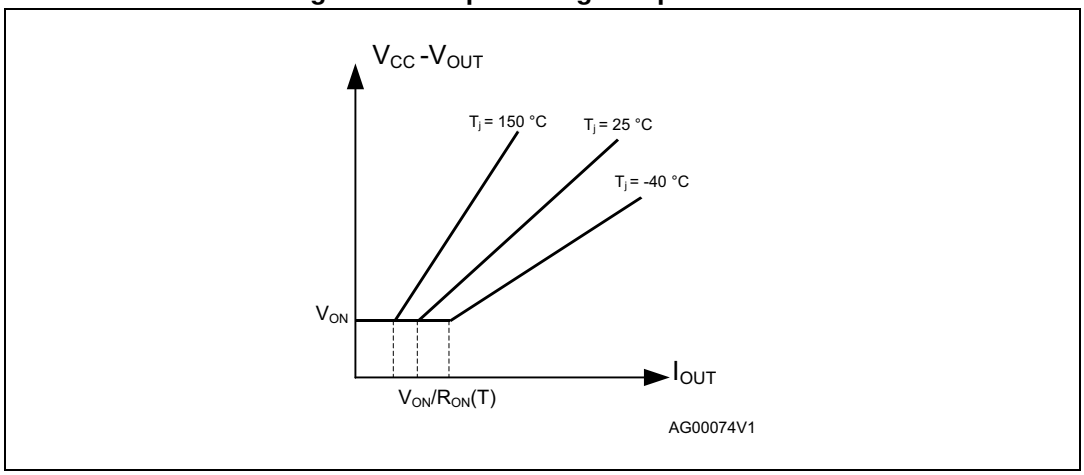


Table 12. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test pulse	Test levels(1)		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01 Ω
5b(2)	+65 V	+87 V	1 pulse			400 ms, 2 Ω

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.

Table 13. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) Test pulse	Test level results(1)	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b (2)(3)	C	C

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground. The protection strategy allows PowerMOS to be cyclically switched on during load dump, so distributing the load dump energy along the time and to transfer a part of it to the load.
3. Suppressed load dump (pulse 5b) is withstood with a minimum load connected as specified in *Table 3: Absolute maximum ratings*.

Table 14. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the

2.4 Waveforms

Figure 11. Normal operation

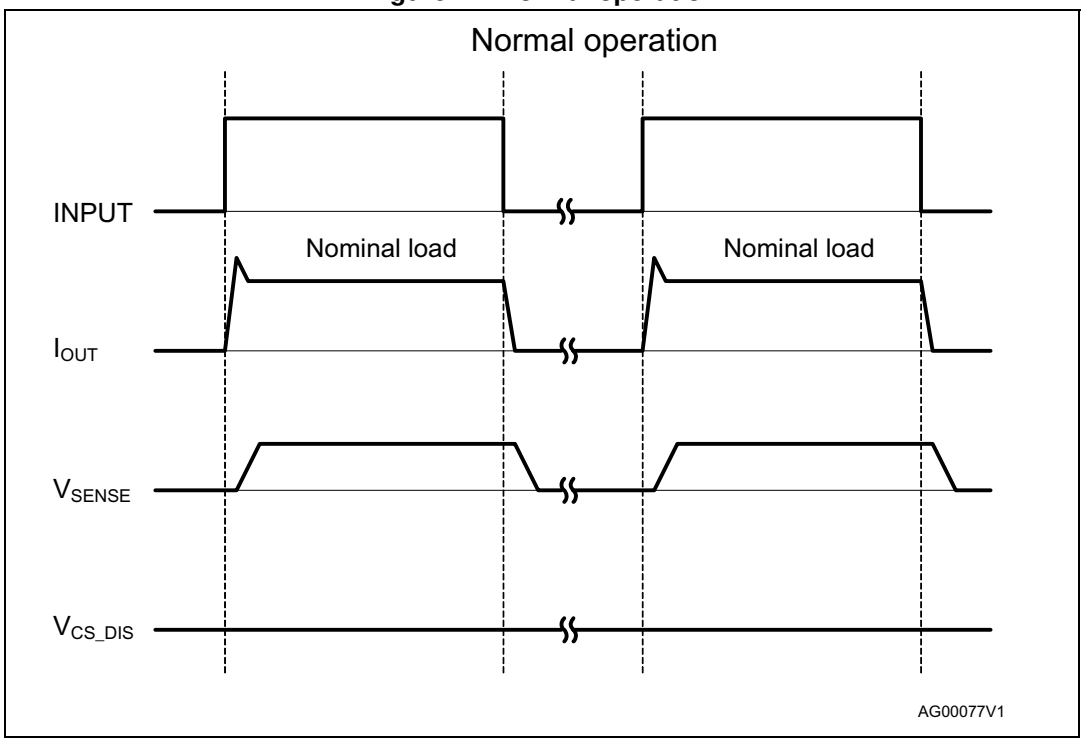


Figure 12. Overload or short to GND

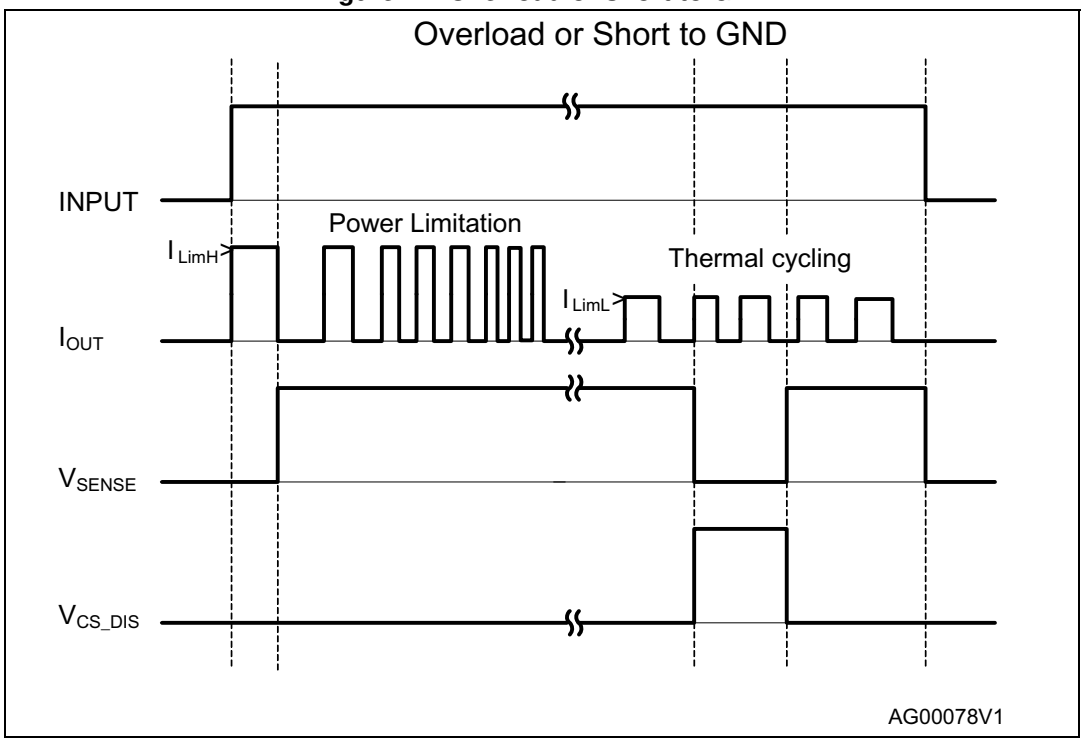


Figure 13. Intermittent overload

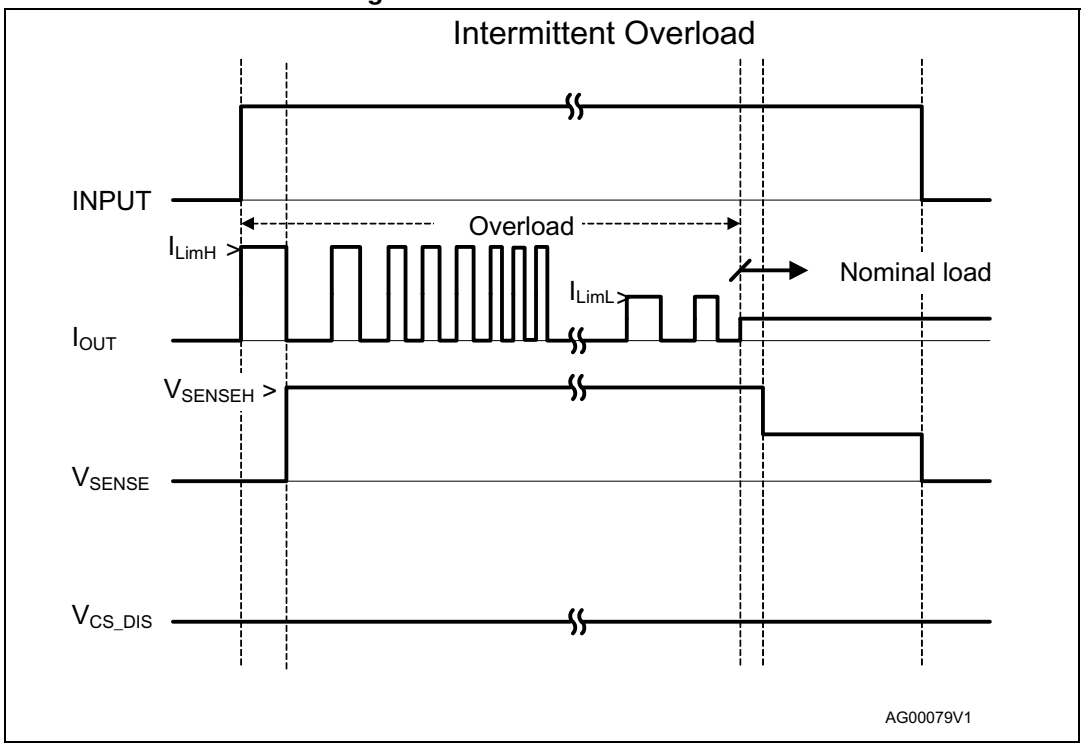


Figure 14. Off-state open-load with external circuitry

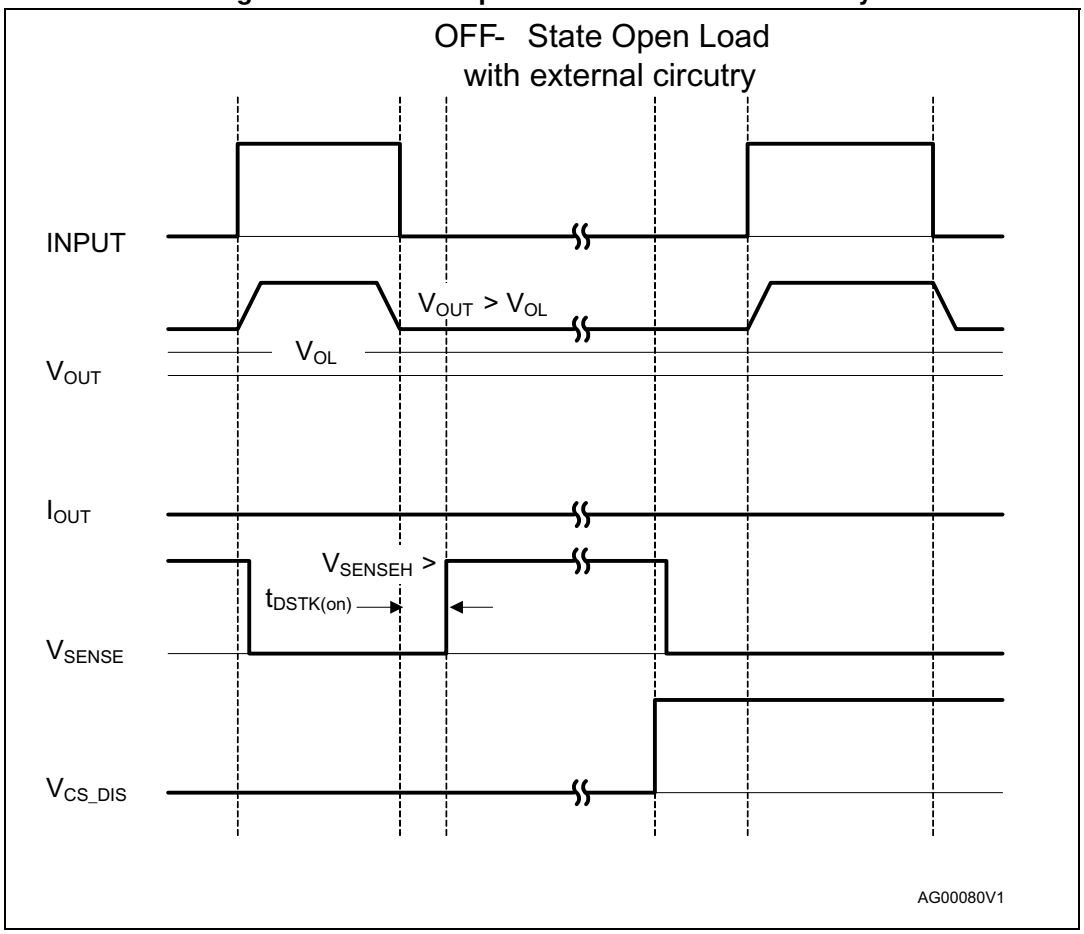


Figure 15. Short to V_{CC}

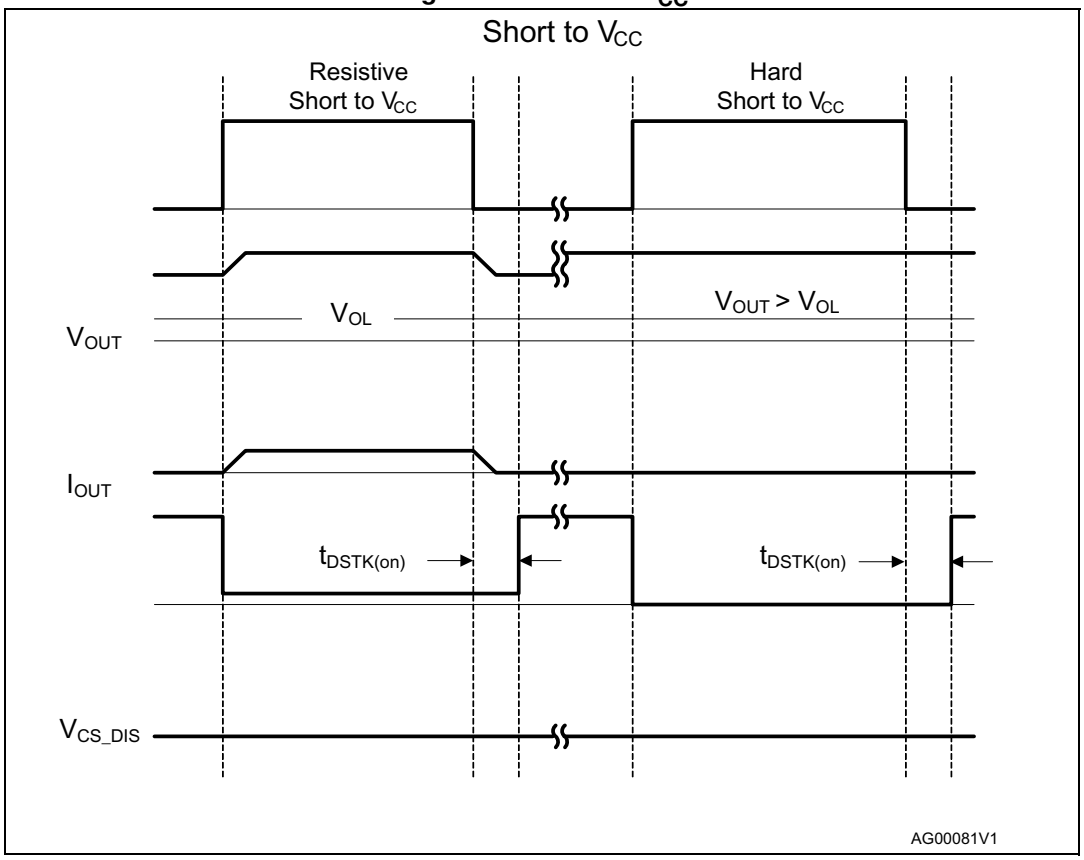
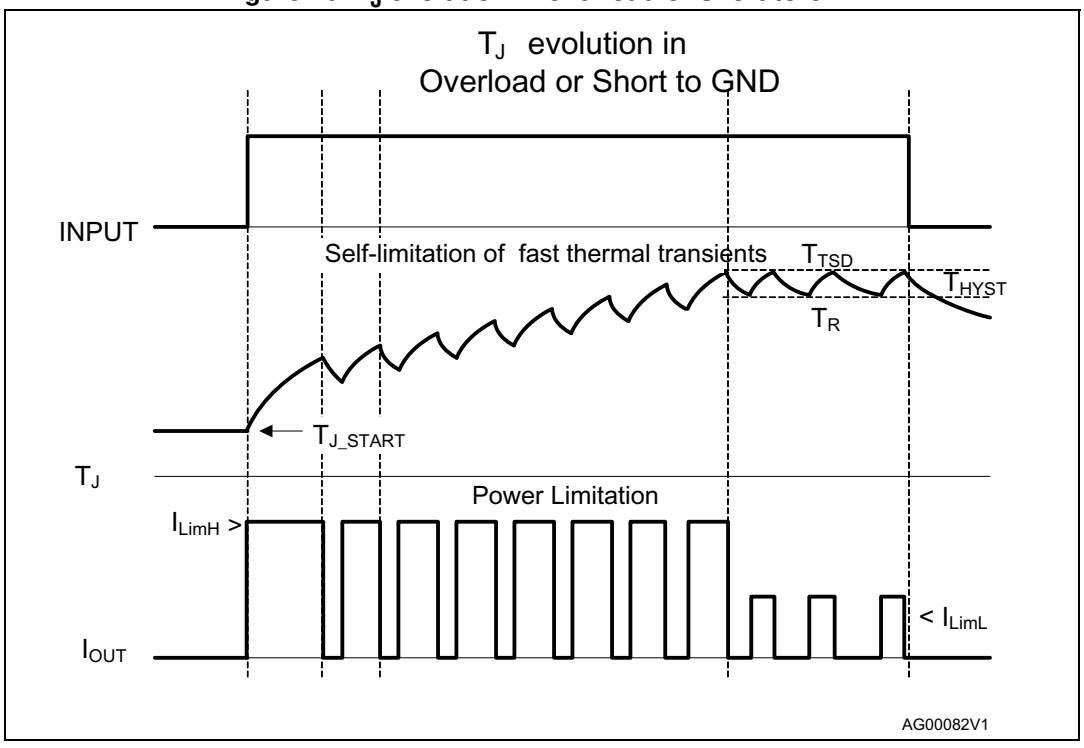


Figure 16. T_J evolution in overload or short to GND



2.5 Electrical characteristics curves

Figure 17. Off-state output current

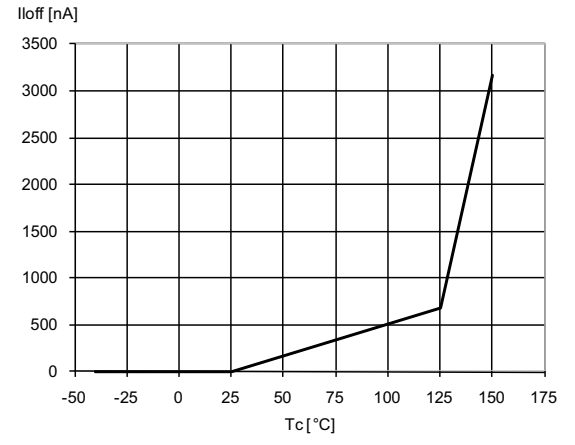


Figure 18. High level input current

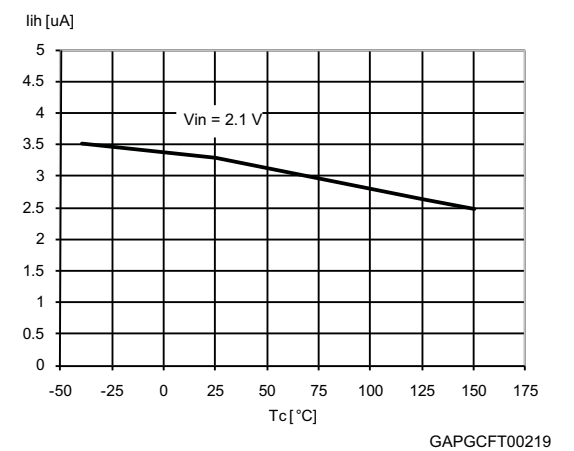


Figure 19. Input clamp voltage

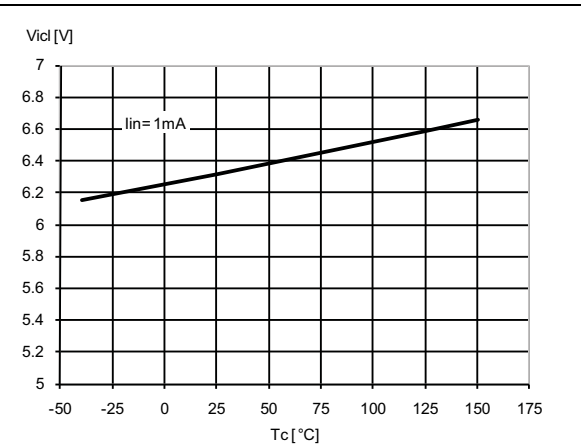


Figure 20. Input high level

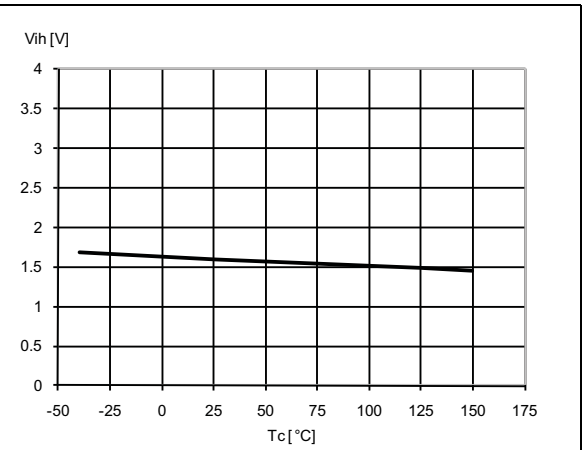


Figure 21. Input low level

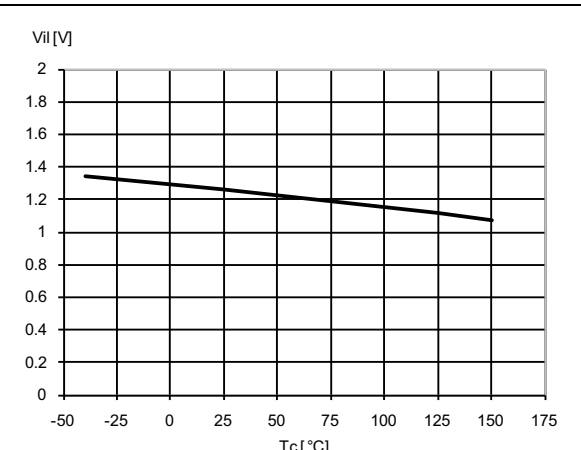


Figure 22. Input hysteresis voltage

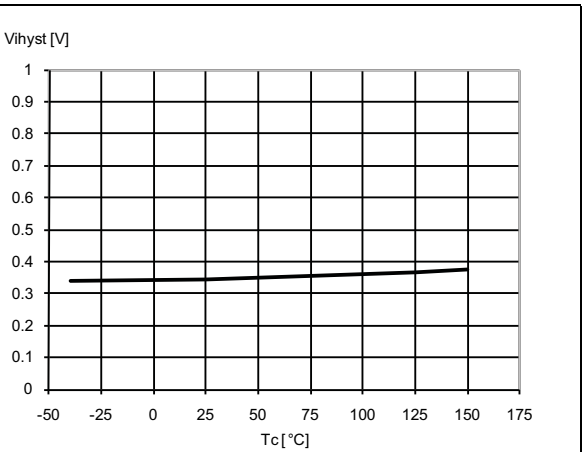


Figure 23. On-state resistance vs T_{case}

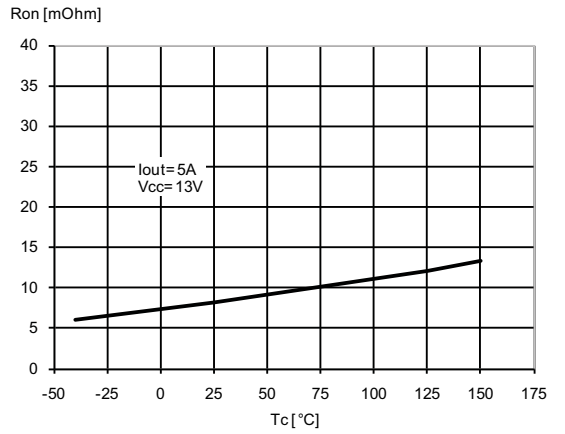


Figure 24. On-state resistance vs V_{CC}

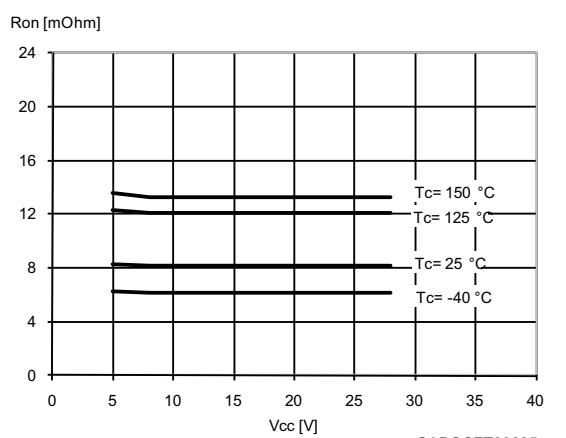


Figure 25. Undervoltage shutdown

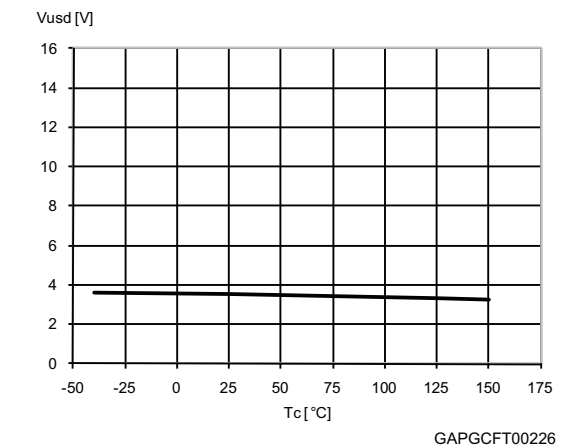


Figure 26. I_{LIMH} vs T_{case}

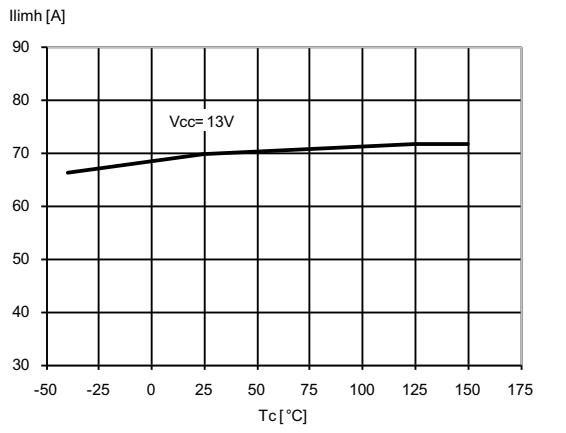


Figure 27. Turn-on voltage slope

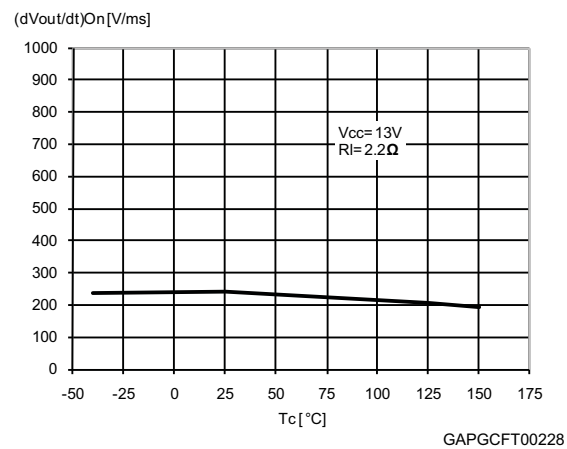


Figure 28. Turn-off voltage slope

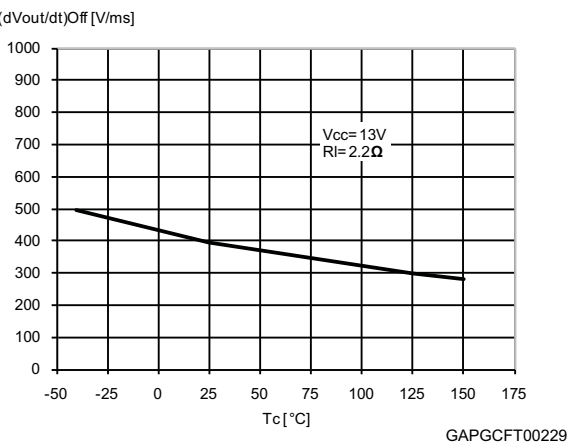


Figure 29. CS_DIS clamp voltage

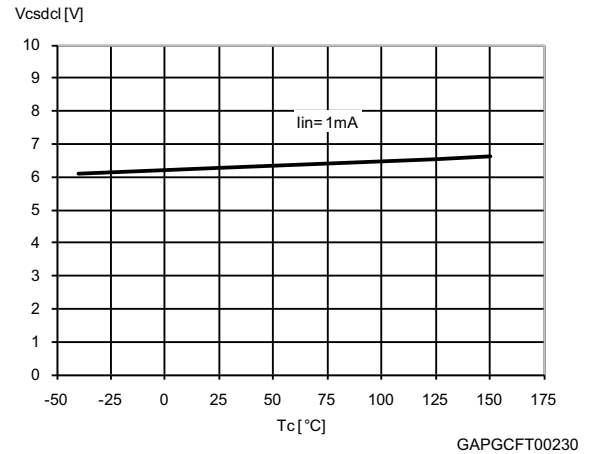


Figure 30. Low level CS_DIS voltage

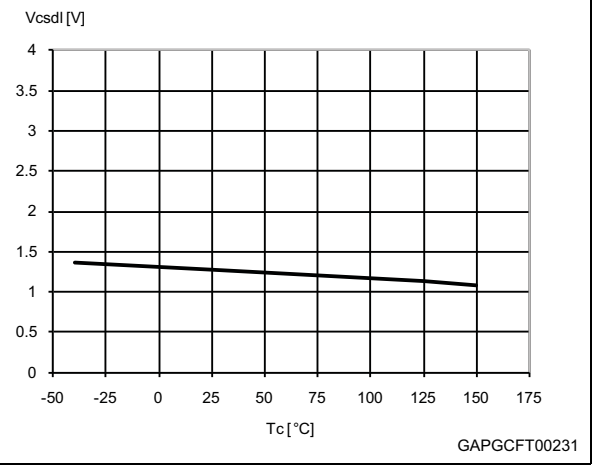
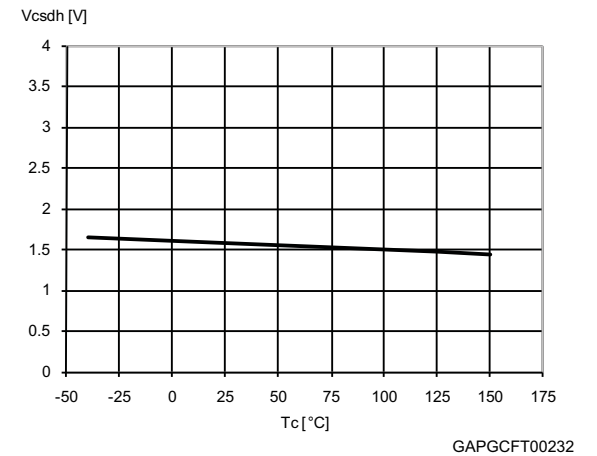
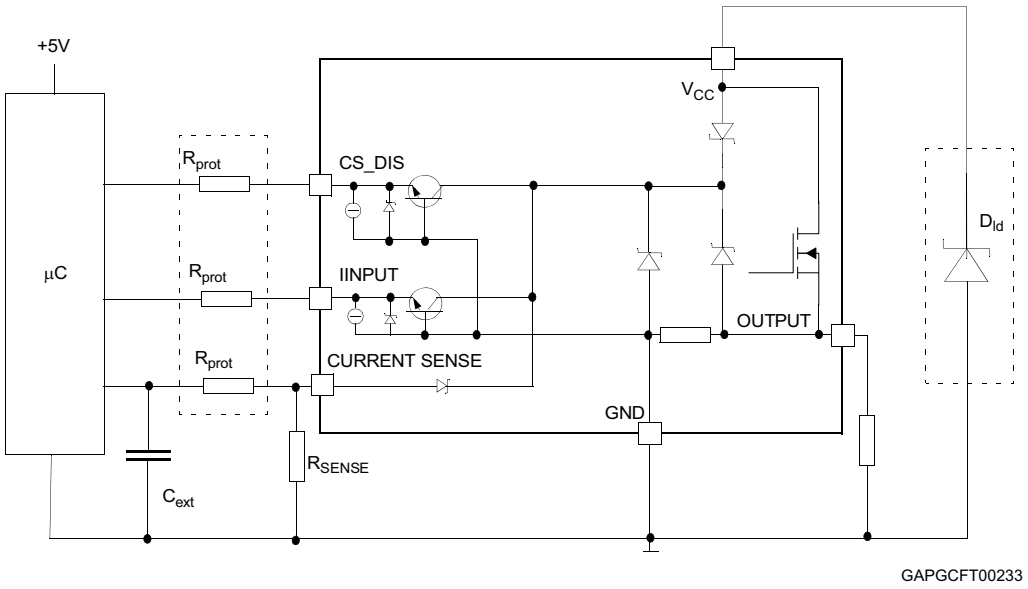


Figure 31. High level CS_DIS voltage



3 Application information

Figure 32. Application schematic



Note: Channel 2 has the same internal circuit as channel 1.

3.1 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CCPK} max rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

3.2 MCU I/Os protection

When negative transients are present on the V_{CC} line, the control pin is pulled negative to approximately -1.5 V. ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/O pins from latching-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation 1:

$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH}) / I_{IHmax}$

Calculation example:

For V_{CCpeak} = - 1.5 V; $I_{latchup} \geq$ 20 mA; $V_{OH\mu C} \geq$ 4.5 V

$75\ \Omega \leq R_{prot} \leq 240\ k\Omega$.

Recommended values: R_{prot} =10 kΩ, C_{EXT} =10 nF.