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VND5E050AJ-E
VND5E050AK-E

Double channel high side driver with analog current sense for automotive applications

Features

Max transient supply voltage	V_{CC}	41 V
Operating voltage range	V_{CC}	4.5 to 28 V
Max On-state resistance (per ch.)	R_{ON}	50 mΩ
Current limitation (typ)	I_{LIMH}	27 A
Off-state supply current	I_S	2 µA(1)

1. Typical value with all loads connected.

- General
  - Inrush current active management by power limitation
  - Very low standby current
  - 3.0 V CMOS compatible inputs
  - Optimized electromagnetic emissions
  - Very low electromagnetic susceptibility
  - In compliance with the 2002/95/EC european directive
  - Very low current sense leakage
- Diagnostic functions
  - Proportional load current sense
  - High current sense precision for wide currents range
  - Current sense disable
  - Off-state open load detection
  - Output short to V_{CC} detection
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of V_{CC}
  - Over temperature shutdown with auto restart (thermal shutdown)

PowerSSO-12 PowerSSO-24

  - Reverse battery protected (see *Figure 32*)
  - Electrostatic discharge protection

Applications

- All types of resistive, inductive and capacitive loads
- Suitable as LED driver

Description

The VND5E050AJ-E and VND5E050AK-E are double channel high-side drivers manufactured in the ST proprietary VIPower M0-5 technology and housed in the tiny PowerSSO-12 and PowerSSO-24 packages. The VND5E050AJ-E and VND5E050AK-E are designed to drive 12V automotive grounded loads delivering protection, diagnostics and easy 3V and 5V CMOS compatible interface with any microcontroller.

The devices integrate advanced protective functions such as load current limitation, inrush and overload active management by power limitation, over-temperature shut-off with auto-restart and over-voltage active clamp. A dedicated analog current sense pin is associated with every output channel in order to provide *Enhanced* diagnostic functions including fast detection of overload and short-circuit to ground through power limitation indication, over-temperature indication, short-circuit to Vcc diagnosis and on & off state open load detection.

The current sensing and diagnostic feedback of the whole device can be disabled by pulling the CS_DIS pin high to allow sharing of the external sense resistor with other similar devices.

Contents

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List of figures

1 Block diagram and pin description

Figure 1. Block diagram

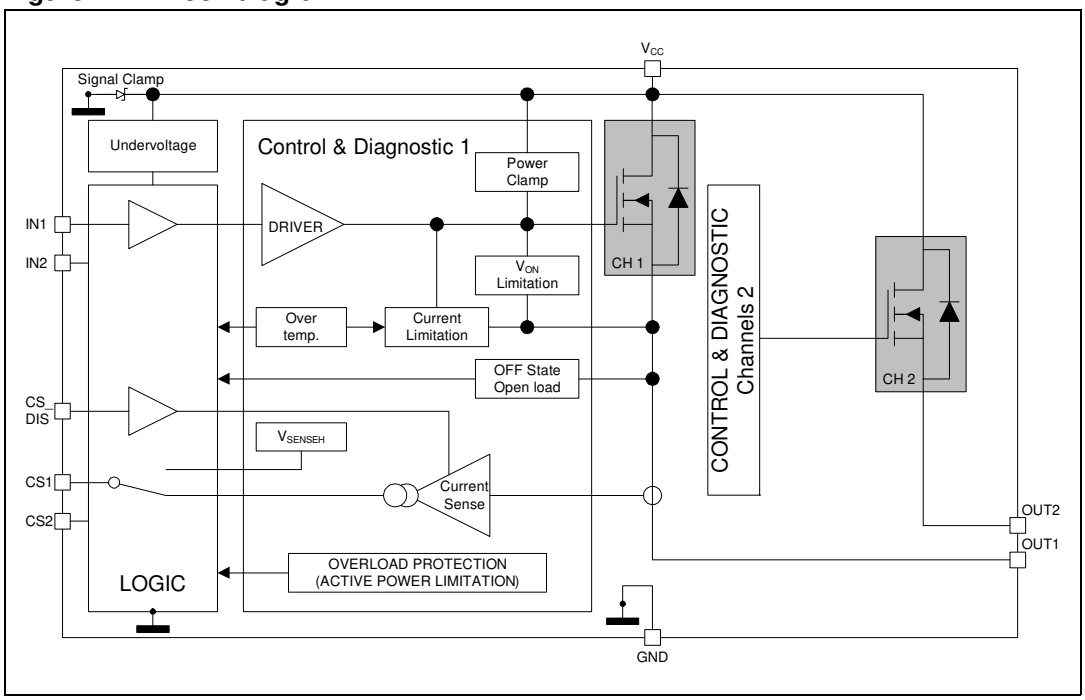


Table 1. Pin function

Name	Function
V_{CC}	Battery connection.
$OUTPUT_{1,2}$	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network.
$INPUT_{1,2}$	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state.
CURRENT $SENSE_{1,2}$	Analog current sense pin, delivers a current proportional to the load current.
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin.

Figure 2. Configuration diagram (top view)

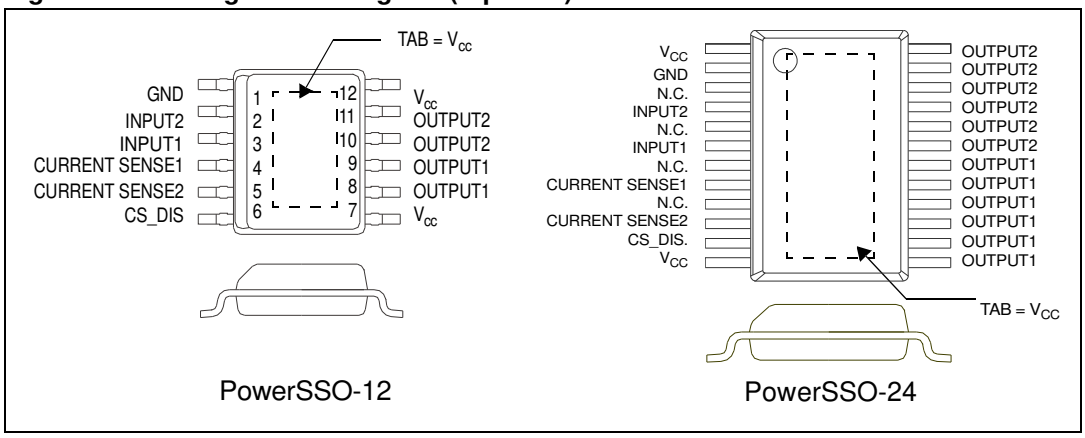
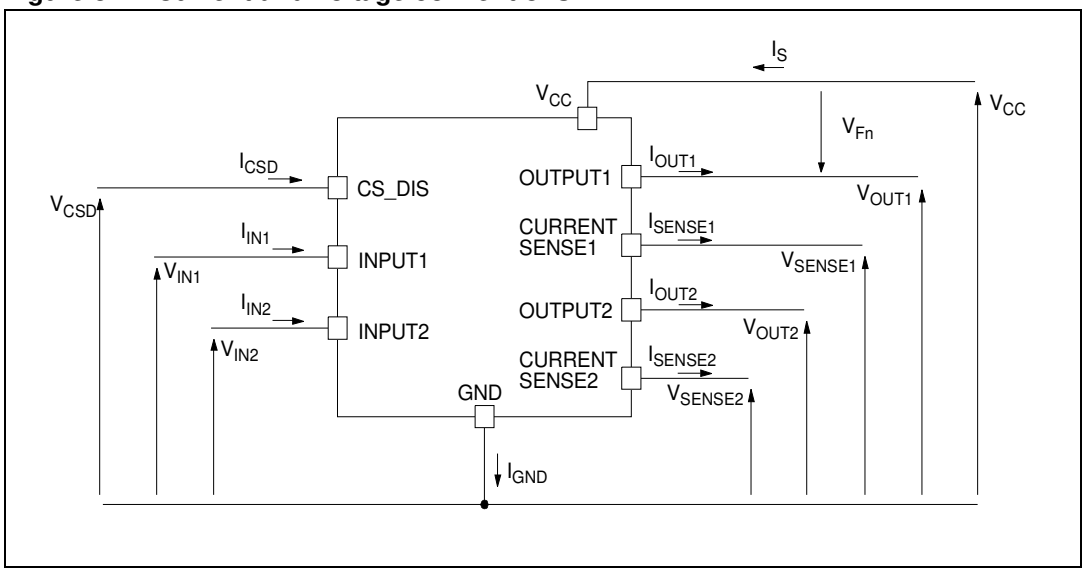


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input	CS_DIS
Floating	Not allowed	X	X	X	X
To ground	Through 1 KΩ resistor	X	Through 22 KΩ resistor	Through 10 KΩ resistor	Through 10 KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



Note: $V_{Fn} = V_{OUTn} - V_{CC}$ *during reverse battery condition.*

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	20	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
$-I_{CSENSE}$	DC reverse CS pin current	200	mA
V_{CSENSE}	Current sense maximum voltage	V_{CC} - 41 to $+V_{CC}$	V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
E_{MAX}	Maximum switching energy (single pulse) (L= 3mH; R_L=0Ω; V_{bat}=13.5V; T_{jstart}=150°C; I_{OUT} = I_{limL}(*Typ.*))	104	mJ
V_{ESD}	Electrostatic discharge (human body model: R=1.5KΩ; C=100pF) – Input – Current sense – CS_DIS – Output – V_{CC}	 4000 2000 4000 5000 5000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	- 40 to 150	°C
T_{stg}	Storage temperature	- 55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max value		Unit
		PowerSSO-12	PowerSSO-24	
$R_{thj-case}$	Thermal resistance junction-case (with one channel ON)	2.7	2.7	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	See *Figure 36*	See *Figure 40*	°C/W

2.3 Electrical characteristics

Values specified in this section are for 8 V<V_{CC}<28 V; -40 °C<T_j<150 °C, unless otherwise stated.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance(1)	I_{OUT}= 2A; T_j= 25°C			50	mΩ
		I_{OUT}= 2A; T_j= 150°C			100	
		I_{OUT}= 2A; V_{CC}= 5V; T_j= 25°C			65	
V_{clamp}	Clamp voltage	I_S= 20mA	41	46	52	V

Table 5. Power section (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Supply current	Off-state; V_{CC}= 13V; T_j= 25°C; V_{IN}=V_{OUT}=V_{SENSE}=V_{CSD}=0V		2(2)	5(2)	µA
		On-state; V_{CC}= 13V; V_{IN}= 5V; I_{OUT}=0A		3	6	mA
$I_{L(off1)}$	Off-state output current (1)	V_{IN}=V_{OUT}= 0V; V_{CC}= 13V; T_j=25°C	0	0.01	3	µA
		V_{IN}=V_{OUT}= 0V; V_{CC}= 13V; T_j=125°C	0		5	
V_F	Output - V_{CC} diode voltage(1)	-I_{OUT}= 4A; T_j= 150°C			0.7	V

1. For each channel.
2. PowerMOS leakage included.

Table 6. Switching (V_{CC} = 13V; T_j = 25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L= 6.5Ω (see *Figure 6*)		20		µs
$t_{d(off)}$	Turn-off delay time	R_L= 6.5Ω (see *Figure 6*)		45		µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L= 6.5Ω		See *Figure 26*		V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L= 6.5Ω		See *Figure 28*		V/µs
W_{ON}	Switching energy losses during t_{won}	R_L= 6.5Ω (see *Figure 6*)		0.15		mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L= 6.5Ω (see *Figure 6*)		0.3		mJ

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN}=0.9V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN}=2.1V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN}=1mA	5.5		7	V
		I_{IN}=-1mA		-0.7		
V_{CSDL}	CS_DIS low level voltage				0.9	V
I_{CSDL}	Low level CS_DIS current	V_{CSD}=0.9V	1			µA

Table 7. Logic inputs (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CSDH}	CS_DIS high level voltage		2.1			V
I_{CSDH}	High level CS_DIS current	V_{CSD}=2.1V			10	µA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	I_{CSD}=1mA	5.5		7	V
		I_{CSD}=-1mA		-0.7		

Table 8. Protections and diagnostics (1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	V_{CC}=13V 5V<V_{CC}< 28V	19	27	38 38	A A
I_{limL}	Short circuit current during thermal cycling	V_{CC}= 13V T_R<T_j<T_{TSD}		7		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS}+1	T_{RS}+5		°C
T_{RS}	Thermal reset of status		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD} -T_R)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT}= 2A; V_{IN}=0; L=6mH	V_{CC}-41	V_{CC}-46	V_{CC}-52	V
V_{ON}	Output voltage drop limitation	I_{OUT}= 0.1A; T_j= -40°C...+150°C (see *Figure 8*)		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 9. Current sense (8V<V_{CC}<18V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT}= 0.05A; V_{SENSE}=0.5V;V_{CSD}=0V; T_j= -40°C...150°C	1440	2250	3630	
K_1	I_{OUT}/I_{SENSE}	I_{OUT}= 1A; V_{SENSE}=4V;V_{CSD}=0V; T_j= -40°C...150°C T_j= 25°C...150°C	1740 1750	2070 2070	2820 2562	
dK_1/K_1 (1)	Current sense ratio drift	I_{OUT}=1A; V_{SENSE}= 4V; V_{CSD}=0V; T_J= -40 °C to 150 °C	-15		15	%

Table 9. Current sense (8V<V_{CC}<18V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_2	I_{OUT}/I_{SENSE}	I_{OUT}= 2A; V_{SENSE}= 4V;V_{CSD}= 0V; T_j= -40°C...150°C T_j= 25°C...150°C	 1900 1899	 2000 2000	 2395 2282	
dK_2/K_2(1)	Current sense ratio drift	I_{OUT}= 2 A; V_{SENSE}= 4 V; V_{CSD}=0V; T_J= -40 °C to 150 °C	-9		9	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT}= 4A; V_{SENSE}= 4V;V_{CSD}= 0V; T_j= -40°C...150°C T_j= 25°C...150°C	 1969 1950	 1990 1990	 2210 2153	
dK_3/K_3(1)	Current sense ratio drift	I_{OUT}= 4 A; V_{SENSE}= 4 V; V_{CSD}= 0V; T_J= -40 °C to 150 °C	-6		6	%
I_{SENSE0}	Analog sense leakage current	I_{OUT}= 0A; V_{SENSE}=0V; V_{CSD}=5V; V_{IN}=0V; T_j= -40°C...150°C V_{CSD}= 0V; V_{IN}=5V; T_j= -40°C...150°C	 0 0		 1 2	µA
		I_{OUT}= 2A; V_{SENSE}= 0V; V_{CSD}= 5V; V_{IN}= 5V; T_j= -40°C...150°C	0		1	
I_{OL}	Open load on-state current detection threshold	V_{IN} = 5V, 8V<V_{CC}<18V I_{SENSE}= 5 µA	4		20	mA
V_{SENSE}	Max analog sense output voltage	I_{OUT}= 4A; V_{CSD}= 0V	5			V
V_{SENSEH}	Analog sense output voltage in fault condition(2)	V_{CC}= 13V; R_{SENSE}= 3.9 KΩ		8		V
I_{SENSEH}	Analog sense output current in fault condition(2)	V_{CC}= 13V; V_{SENSE}= 5V		9		mA
$t_{DSENSE1H}$	Delay response time from falling edge of CS_DIS pin	V_{SENSE}<4V, 0.5A<Iout<4A I_{SENSE}= 90% of $I_{SENSEMAX}$ (see *Figure 4*)		40	100	µs
$t_{DSENSE1L}$	Delay response time from rising edge of CS_DIS pin	V_{SENSE}<4V, 0.5A<Iout<4A I_{SENSE}=10% of $I_{SENSEMAX}$ (see *Figure 4*)		5	20	µs
$t_{DSENSE2H}$	Delay response time from rising edge of INPUT pin	V_{SENSE}<4V, 0.5A<Iout<4A I_{SENSE}=90% of $I_{SENSEMAX}$ (see *Figure 4*)		80	250	µs

Table 9. Current sense (8V<V_{CC}<18V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$\Delta t_{DSENSE2H}$	Delay response time between rising edge of output current and rising edge of current sense	V_{SENSE} < 4V, I_{SENSE} = 90% of $I_{SENSEMAX}$, I_{OUT} = 90% of I_{OUTMAX} I_{OUTMAX}= 2A (see *Figure 7*)			40	µs
$t_{DSENSE2L}$	Delay response time from falling edge of INPUT pin	V_{SENSE}<4V, 0.5A<Iout<4A I_{SENSE}=10% of $I_{SENSEMAX}$ (see *Figure 4*)		80	250	µs

1. Parameter guaranteed by design; it is not tested.
2. Fault condition includes: power limitation, over temperature and open load off-state detection.

Table 10. Open load detection (8V<V_{CC}<18V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Open load off-state voltage detection threshold	V_{IN} = 0 V	2	See *Figure 5*	4	V
t_{DSTKON}	Output short circuit to V_{CC} detection delay at turn-off	See *Figure 5*	180		1200	µs
$I_{L(off2)r}$	Off-state output current at V_{OUT} = 4V	V_{IN}=0V; V_{SENSE}=0V V_{OUT} rising from 0V to 4V	-120		0	µA
$I_{L(off2)f}$	Off-state output current at V_{OUT} = 2V	V_{IN}=0V; V_{SENSE}=V_{SENSEH} V_{OUT} falling from V_{CC} to 2V	-50		90	µA
td_vol	Delay response from output rising edge to V_{SENSE} rising edge in open load	V_{OUT}= 4 V; V_{IN}= 0V V_{SENSE}= 90% of V_{SENSEH}			20	µs

Figure 4. Current sense delay characteristics

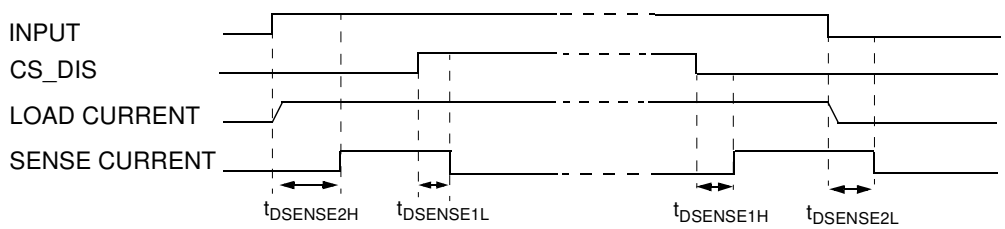


Figure 5. Open load off-state delay timing

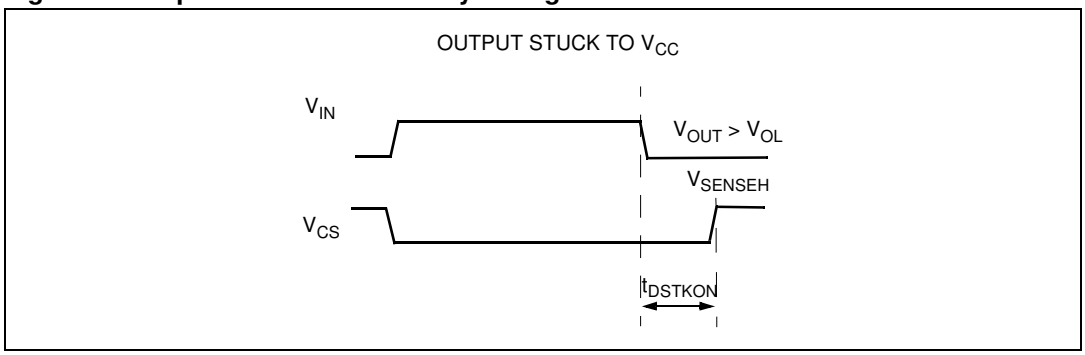


Figure 6. Switching characteristics

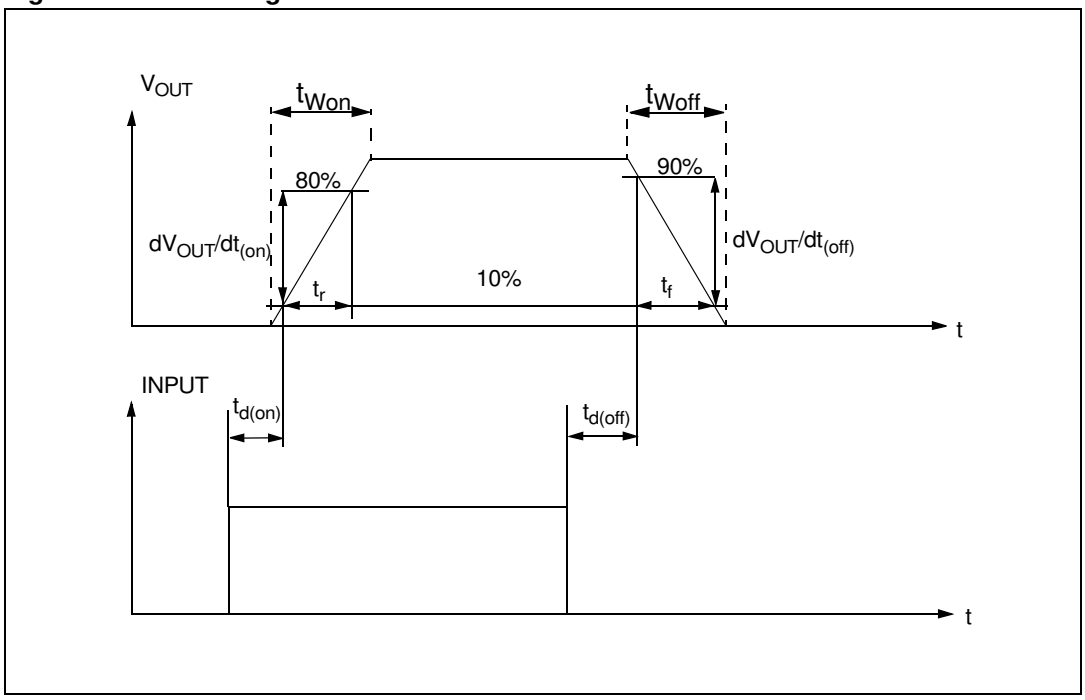


Figure 7. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

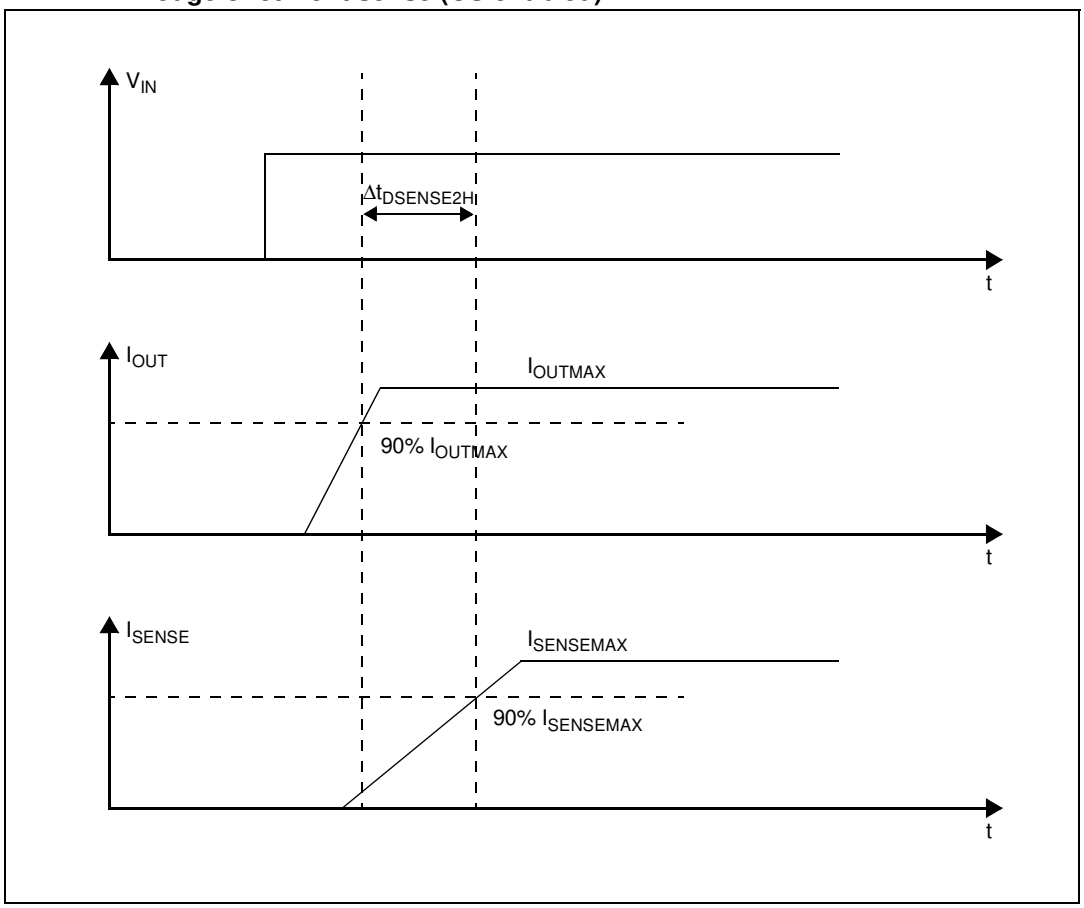


Figure 8. Output voltage drop limitation

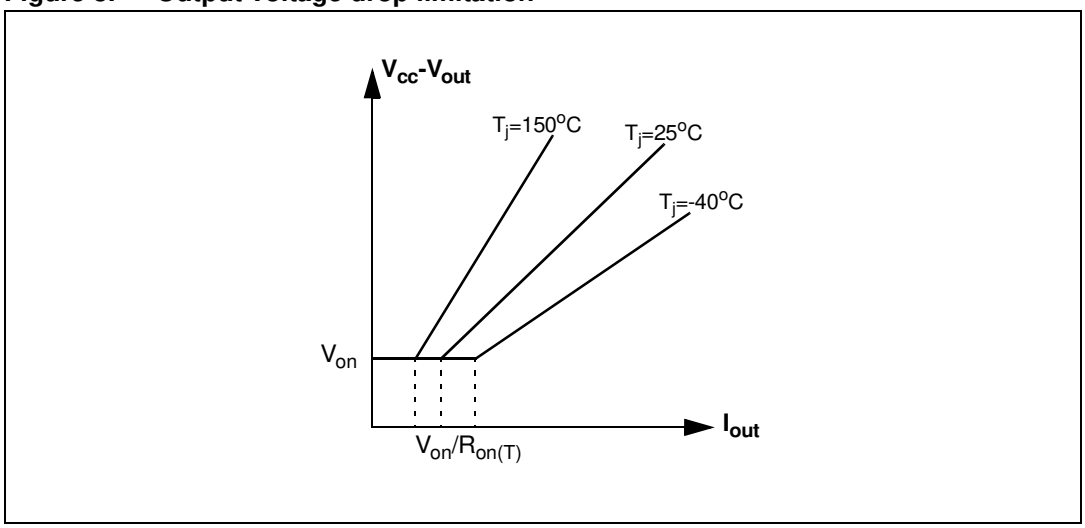


Figure 9. I_{OUT}/I_{SENSE} vs I_{OUT}

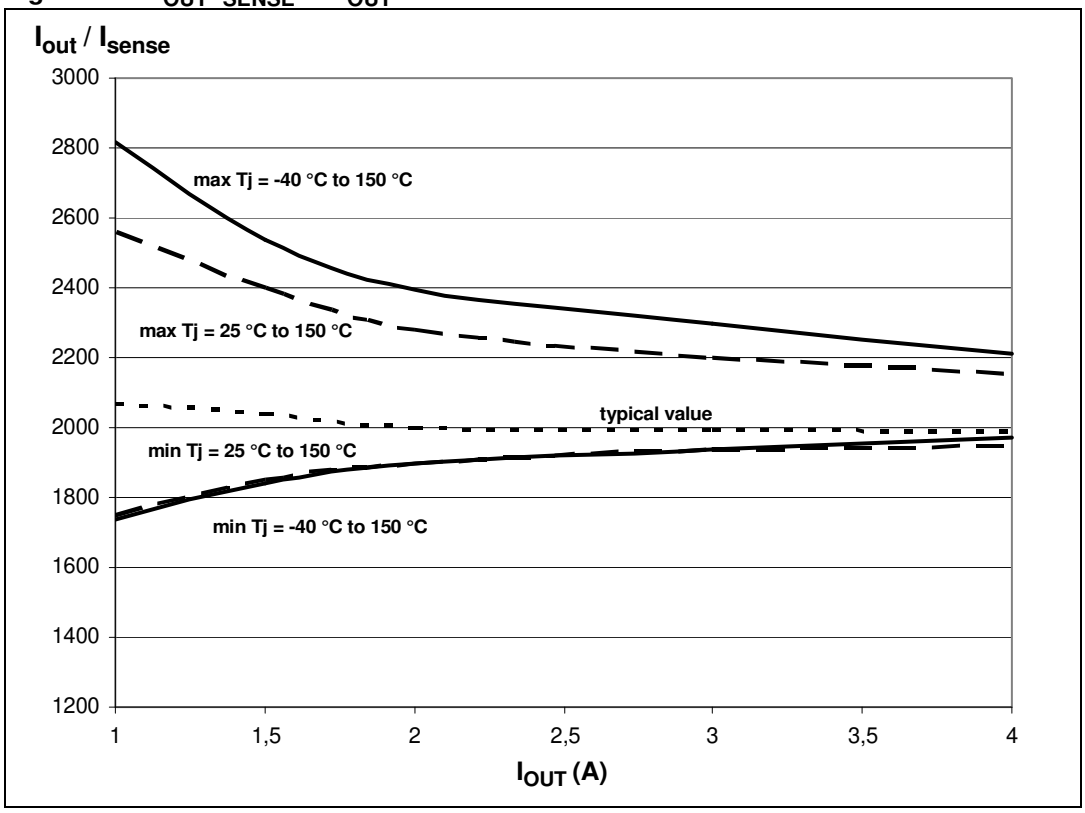
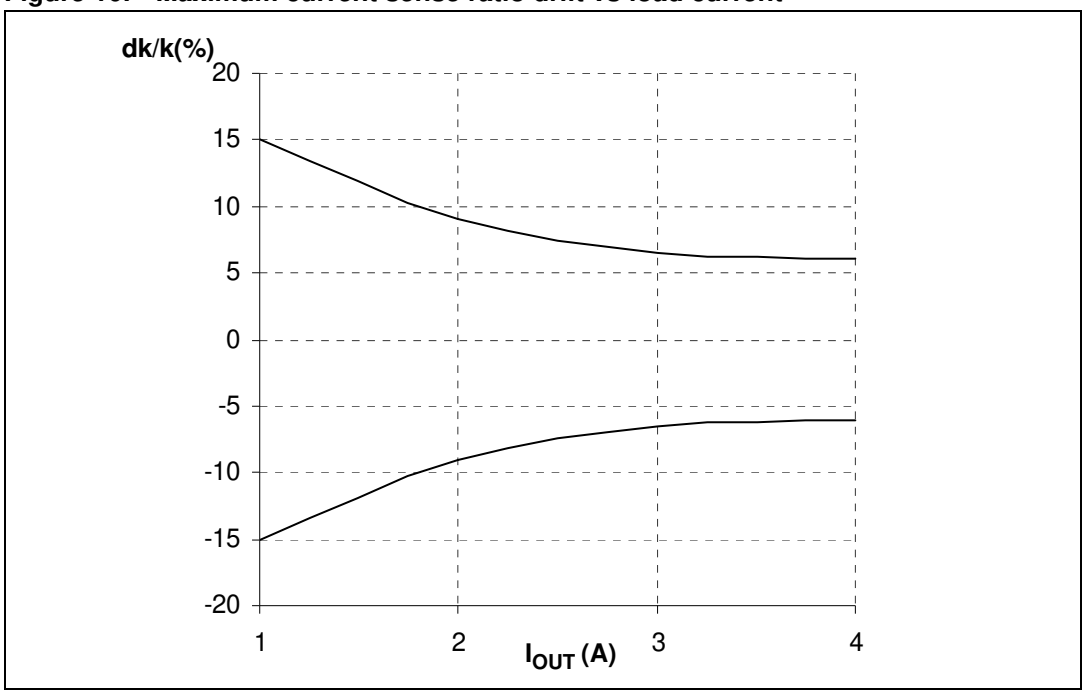


Figure 10. Maximum current sense ratio drift vs load current



Note: Parameter guaranteed by design; it is not tested.

Table 11. Truth table

Conditions	Input	Output	Sense (V_{CSD}=0V)(1)
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overload	H H	X (no power limitation) Cycling (power limitation)	Nominal V_{SENSEH}
Short circuit to GND (power limitation)	L H	L L	0 V_{SENSEH}
Open load off-state (with external pull-up)	L	H	V_{SENSEH}
Short circuit to V_{CC} (external pull-up disconnected)	L H	H H	V_{SENSEH} < Nominal
Negative output voltage clamp	L	L	0

1. If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Table 12. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) test pulse	Test levels(1)		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and Impedance
	III	IV		Min.	Max.	
1	-75V	-100V	5000 pulses	0.5s	5s	2 ms, 10Ω
2a	+37V	+50V	5000 pulses	0.2s	5s	50µs, 2Ω
3a	-100V	-150V	1h	90ms	100ms	0.1µs, 50Ω
3b	+75V	+100V	1h	90ms	100ms	0.1µs, 50Ω
4	-6V	-7V	1 pulse			100ms, 0.01Ω
5b(2)	+65V	+87V	1 pulse			400ms, 2Ω

1. The above test levels must be considered referred to V_{CC} = 13.5V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 13. Electrical transient requirements (part 2)

ISO 7637-2: 2004E test pulse	Test level results	
	III	VI
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b(1)	C	C

1. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 14. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device performed as designed after exposure to disturbance.
E	One or more functions of the device did not perform as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Waveforms

Figure 11. Normal operation

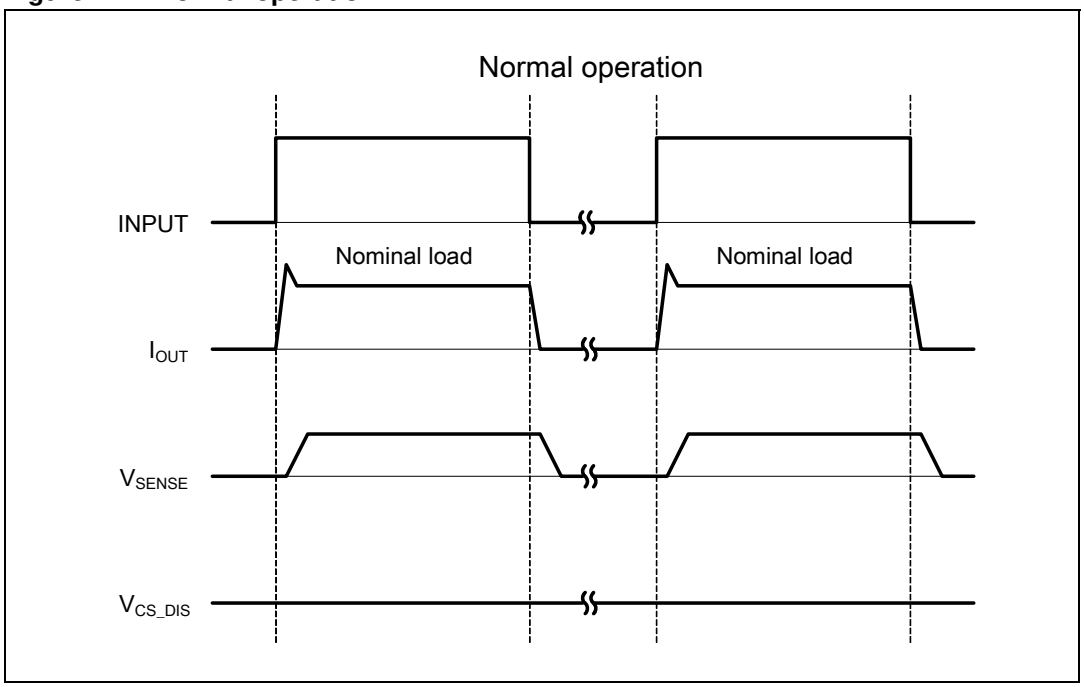


Figure 12. Overload or short to GND

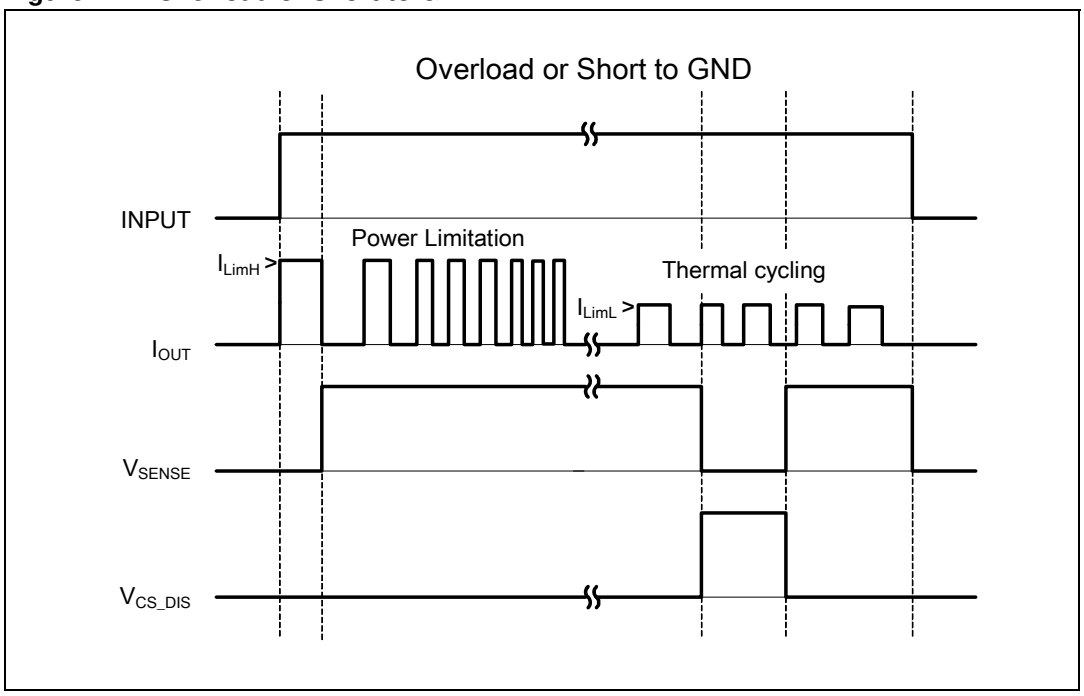


Figure 13. Intermittent overload

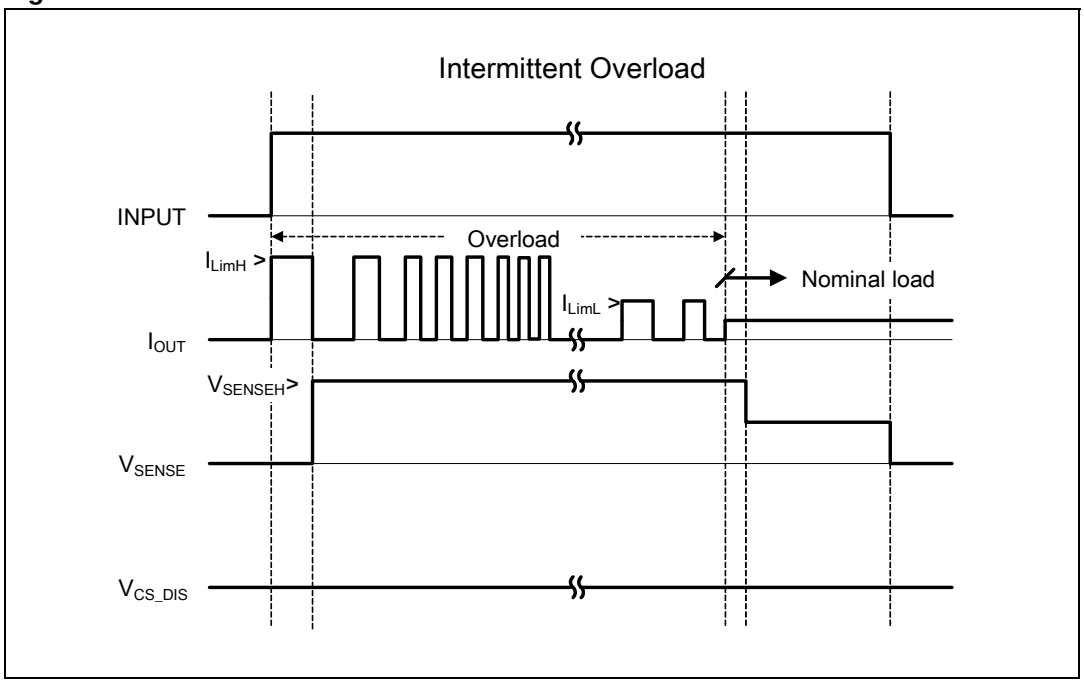


Figure 14. Off-state open load with external circuitry

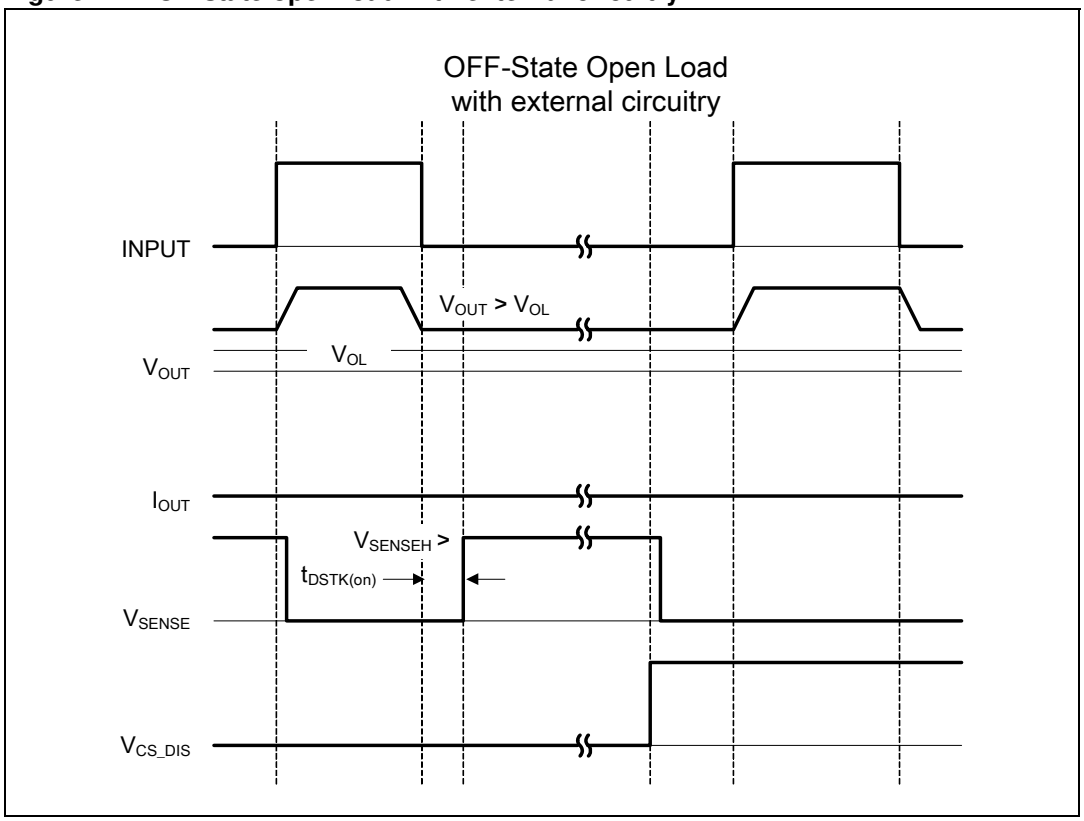


Figure 15. Short to V_{CC}

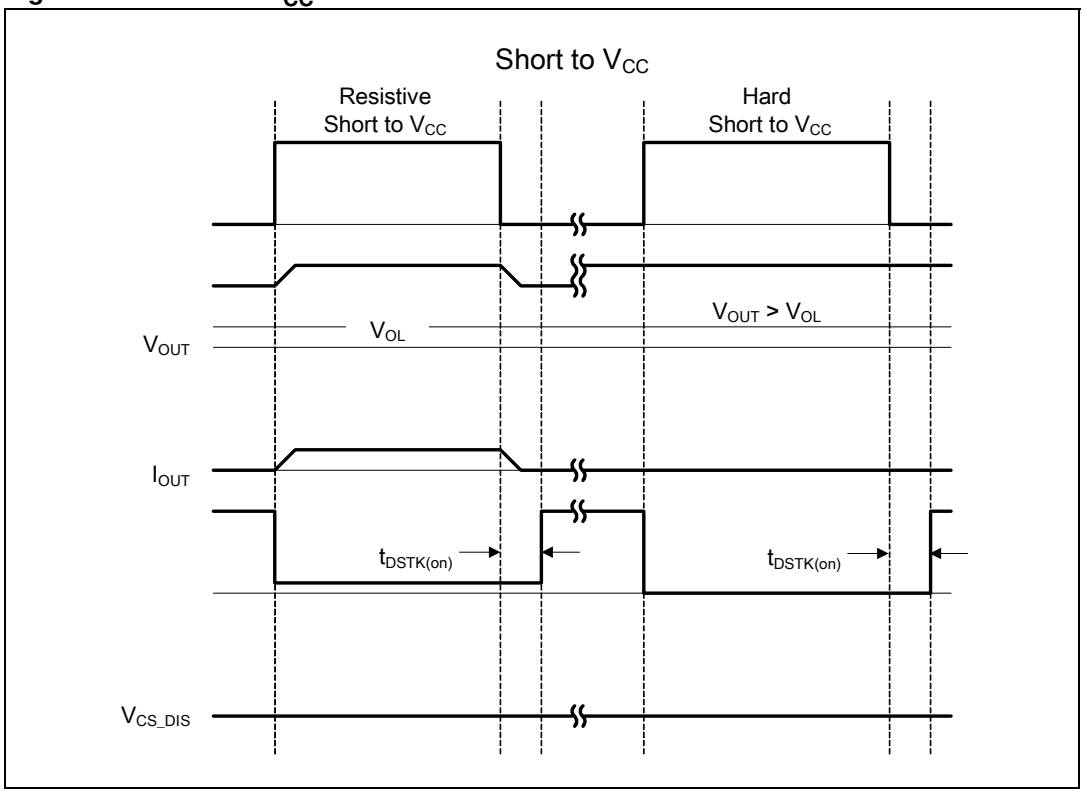
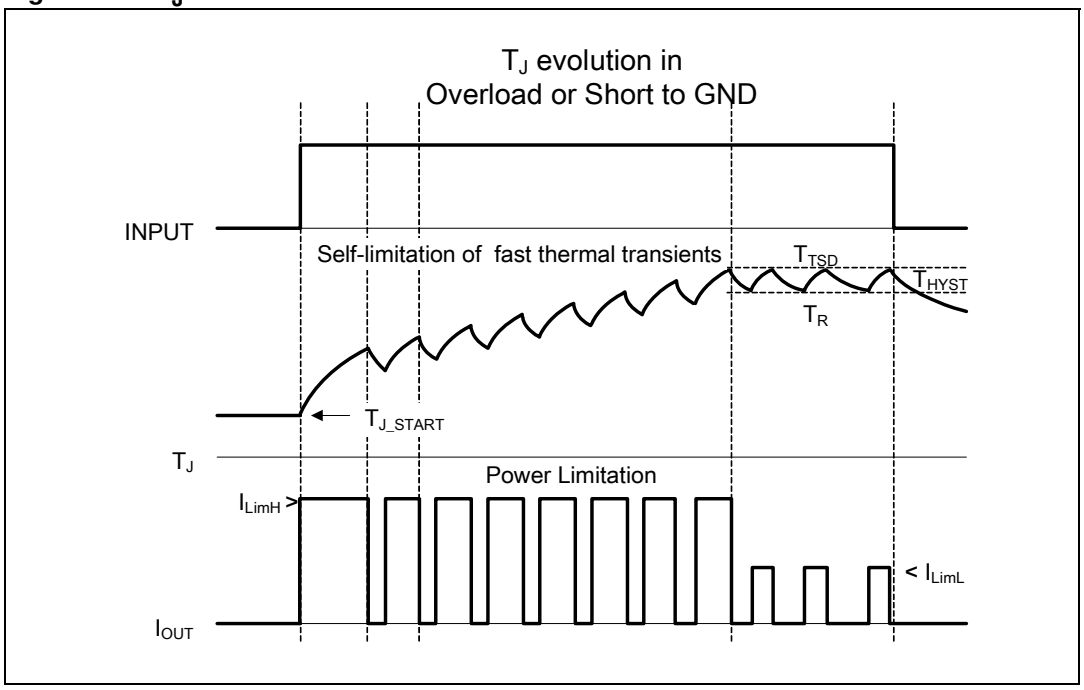


Figure 16. T_J evolution in overload or short to GND



2.5 Electrical characteristics curves

Figure 17. Off-state output current

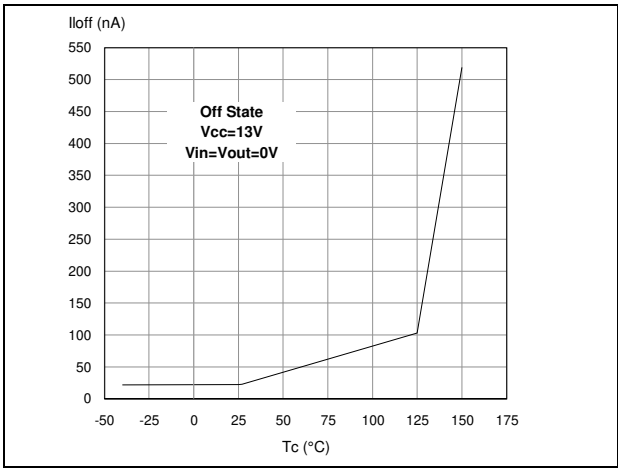


Figure 18. High level input current

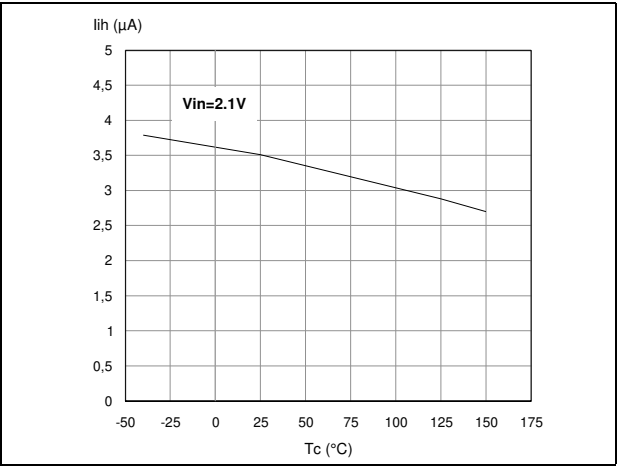


Figure 19. Input clamp voltage

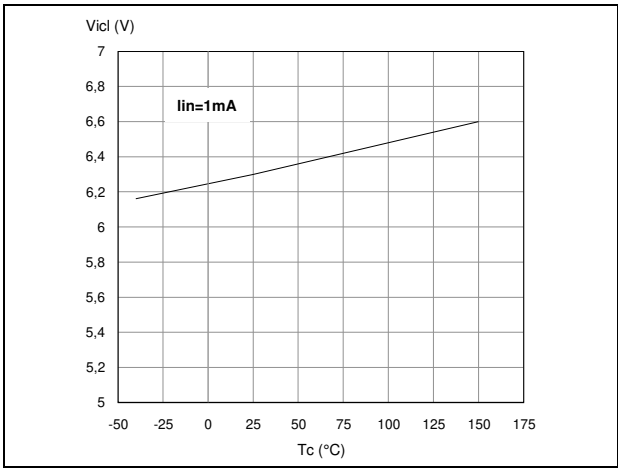


Figure 20. Input low level

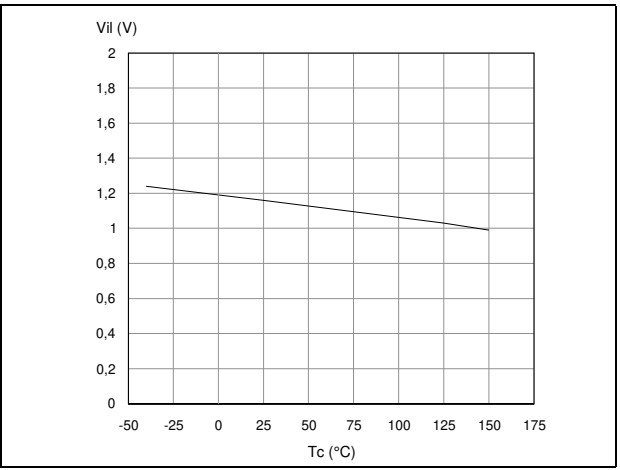


Figure 21. Input high level

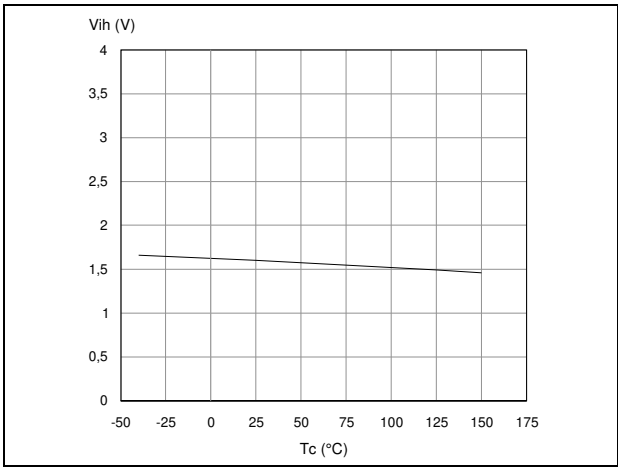


Figure 22. Input hysteresis voltage

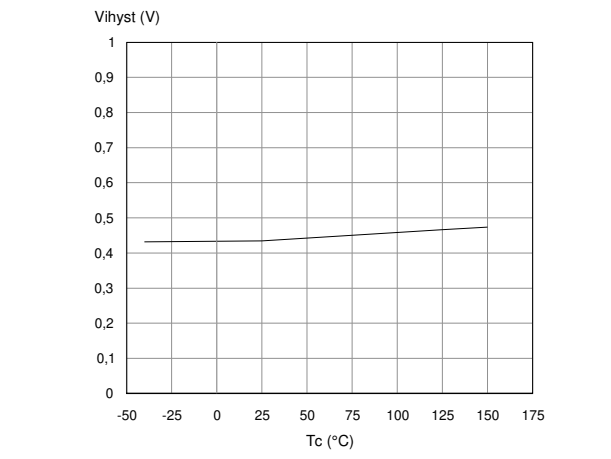


Figure 23. On-state resistance vs T_{case}

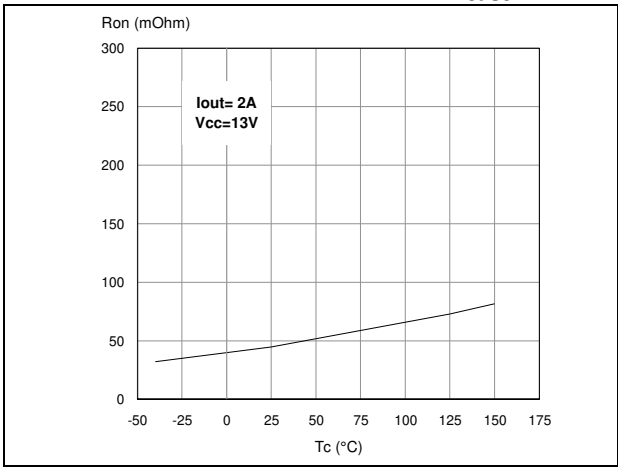


Figure 24. On-state resistance vs V_{CC}

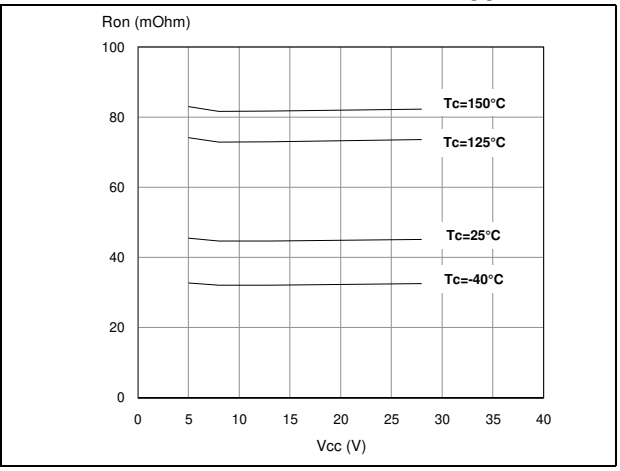


Figure 25. Undervoltage shutdown

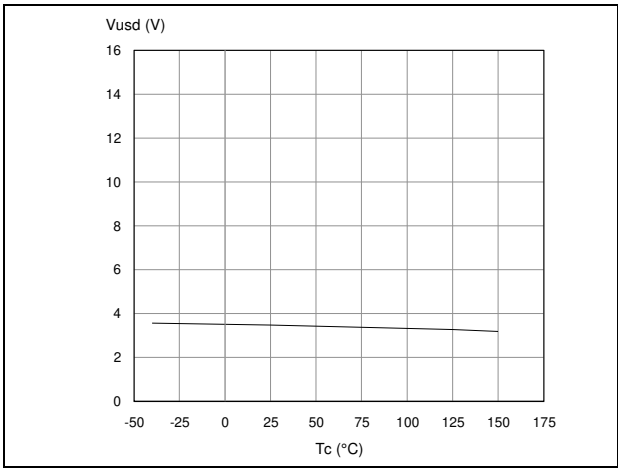


Figure 26. Turn-on voltage slope

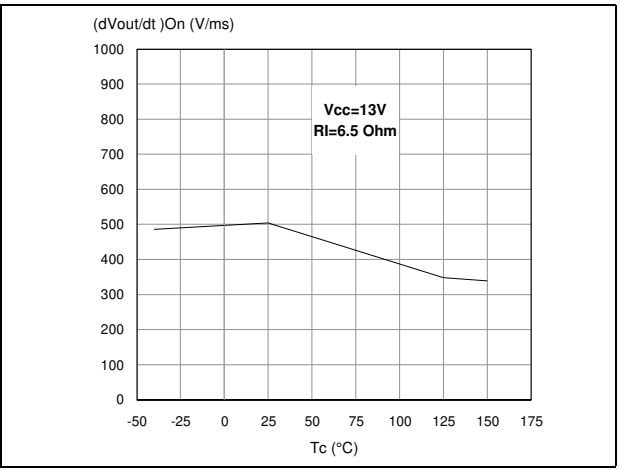


Figure 27. I_{LIMH} vs T_{case}

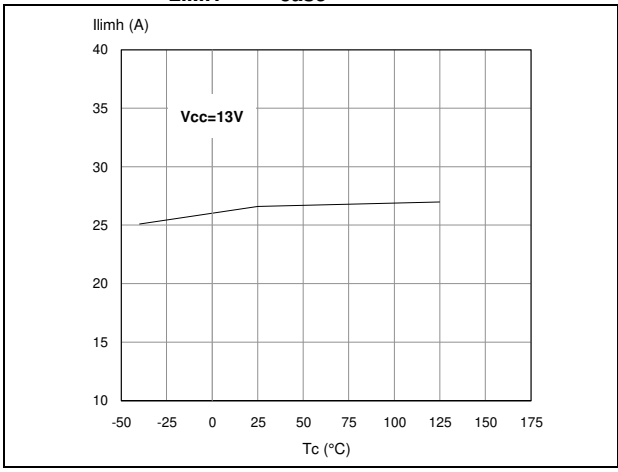


Figure 28. Turn-off voltage slope

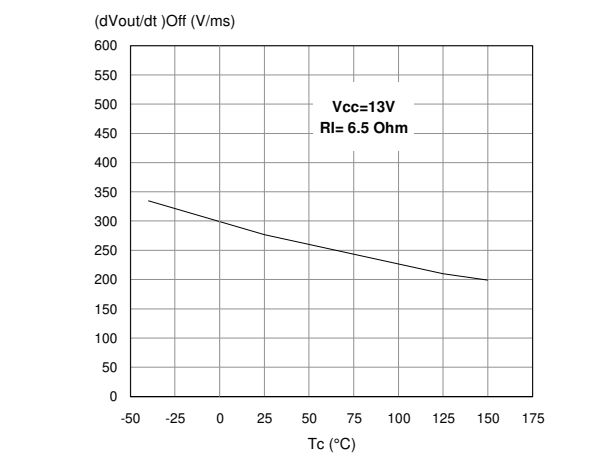


Figure 29. CS_DIS high level voltage

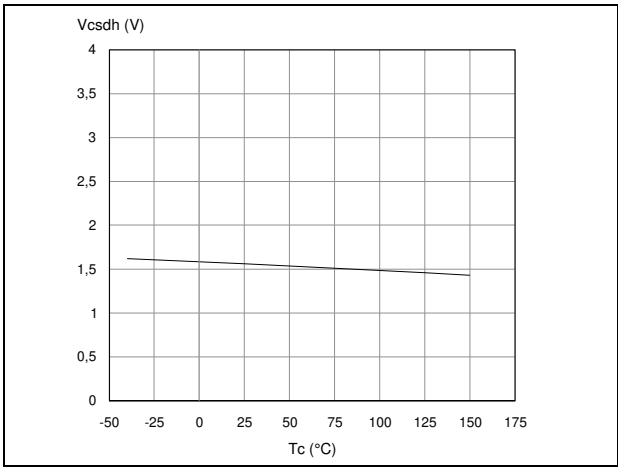


Figure 30. CS_DIS clamp voltage

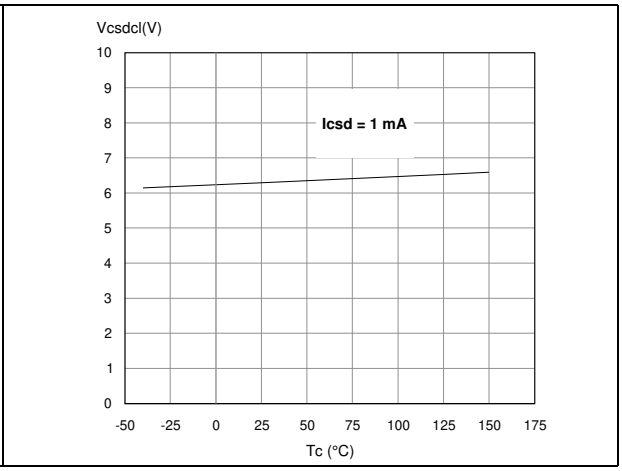
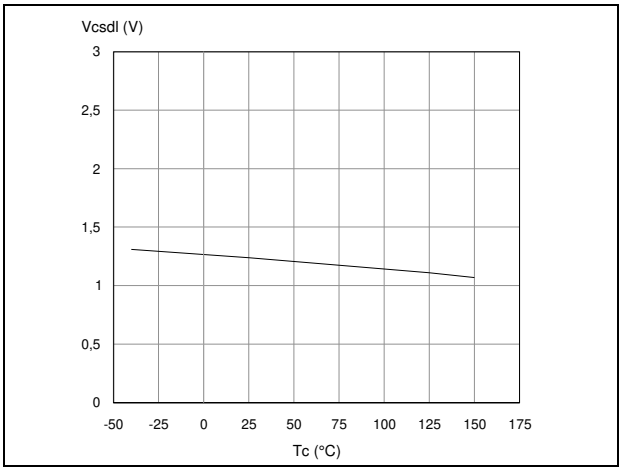
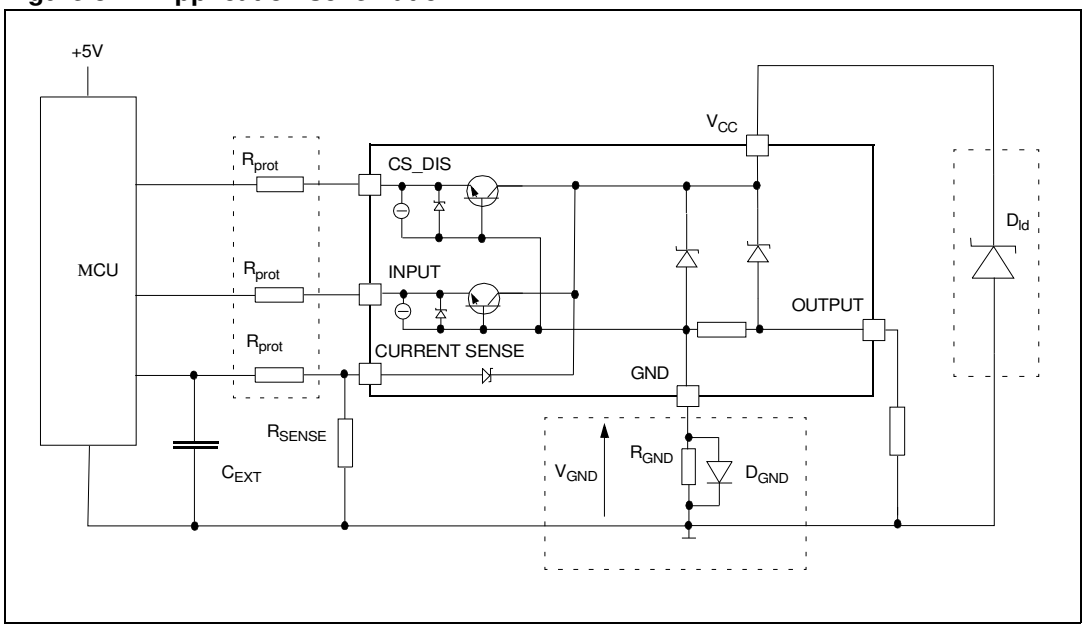


Figure 31. CS_DIS low level voltage



3 Application information

Figure 32. Application schematic



Note: Channel 2 has the same internal circuit as channel 1.

3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600mV / (I_{S(on)max})$
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when V_{CC}<0: during reverse battery situations) is:

$P_D = (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift ($I_{S(on)max}$ * R_{GND}) in the input thresholds and the status output values. This shift will vary depending on how many devices are on in the case of several high side drivers sharing the same R_{GND}.