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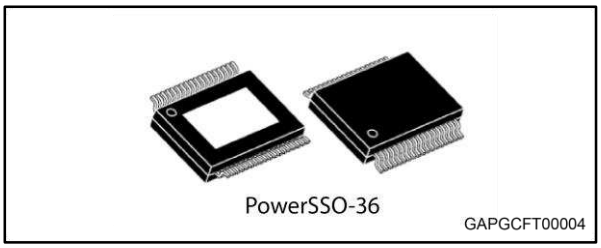
VND7012AY

Double channel high-side driver with MultiSense analog feedback for automotive applications

Datasheet - production data



Features

Max transient supply voltage	V_{CC}	41 V
Operating voltage range	V_{CC}	4 to 28 V
Typ. on-state resistance (per Ch)	R_{ON}	12 mΩ
Current limitation (typ)	I_{LIMH}	75 A
Standby current (max)	I_{STBY}	0.5 µA

- AEC-Q100 qualified
- General
  - Double channel smart high side driver with MultiSense analog feedback
  - Very low standby current
  - Compatible with 3 V and 5 V CMOS outputs
- MultiSense diagnostic functions
  - Multiplexed analog feedback of: load current with high precision proportional current mirror, V_{CC} supply voltage and T_{CHIP} device temperature
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
  - Off-state open-load detection
  - Output short to V_{CC} detection
  - Sense enable/ disable
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Configurable latch-off on overtemperature or power limitation with dedicated fault reset pin
  - Loss of ground and loss of V_{CC}
  - Reverse battery through self turn-on
  - Electrostatic discharge protection

Applications

- All types of Automotive resistive, inductive and capacitive loads
- Specially intended for Automotive Turn Indicators (up to 3 x P27W or SAE1156 and 2 x R5W paralleled or Automotive Headlamps)

Description

The device is a double channel high-side driver manufactured using ST proprietary VIPower® M0-7 technology and housed in PowerSSO-36 package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, providing protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off.

A $\overline{\text{FaultRST}}$ pin unlatches the output in case of fault or disables the latch-off functionality.

A dedicated multifunction multiplexed analog output pin delivers sophisticated diagnostic functions including high precision proportional load current sense, supply voltage feedback and chip temperature sense, in addition to the detection of overload and short circuit to ground, short to V_{CC} and OFF-state open-load.

A sense enable pin allows OFF-state diagnosis to be disabled during the module low-power mode as well as external sense resistor sharing among similar devices.

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1 Block diagram and pin description

Figure 1: Block diagram

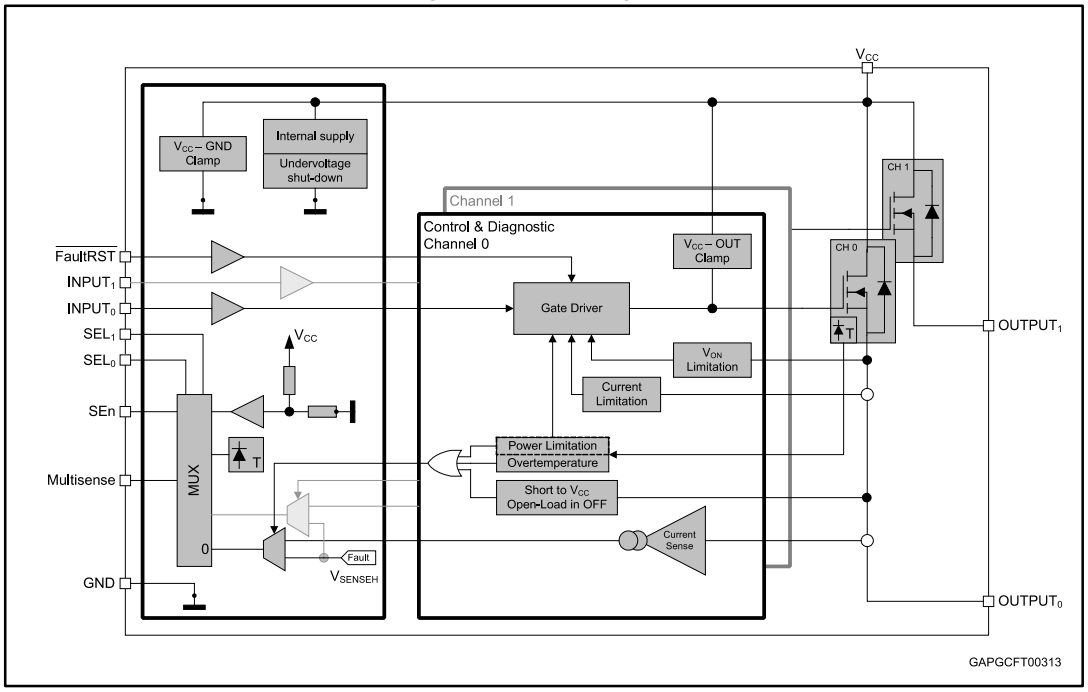


Table 1: Pin functions

Name	Function
V_{CC}	Battery connection.
$OUTPUT_{0,1}$	Power output.
GND	Ground connection.
$INPUT_{0,1}$	Voltage controlled input pin with hysteresis, compatible with 3V and 5V CMOS outputs. They control output switch state.
MultiSense	Multiplexed analog sense output pin; delivers a current proportional to the selected diagnostic: load current, supply voltage or chip temperature.
SEn	Active high compatible with 3V and 5V CMOS outputs; it enables the MultiSense diagnostic pin.
$SEL_{0,1}$	Active high compatible with 3V and 5V CMOS outputs; they address the MultiSense multiplexer.
$\overline{FaultRST}$	Active low compatible with 3V and 5V CMOS outputs; unlatches the output in case of fault; if kept low, sets the outputs in auto-restart mode.

Figure 2: Configuration diagram (top view)

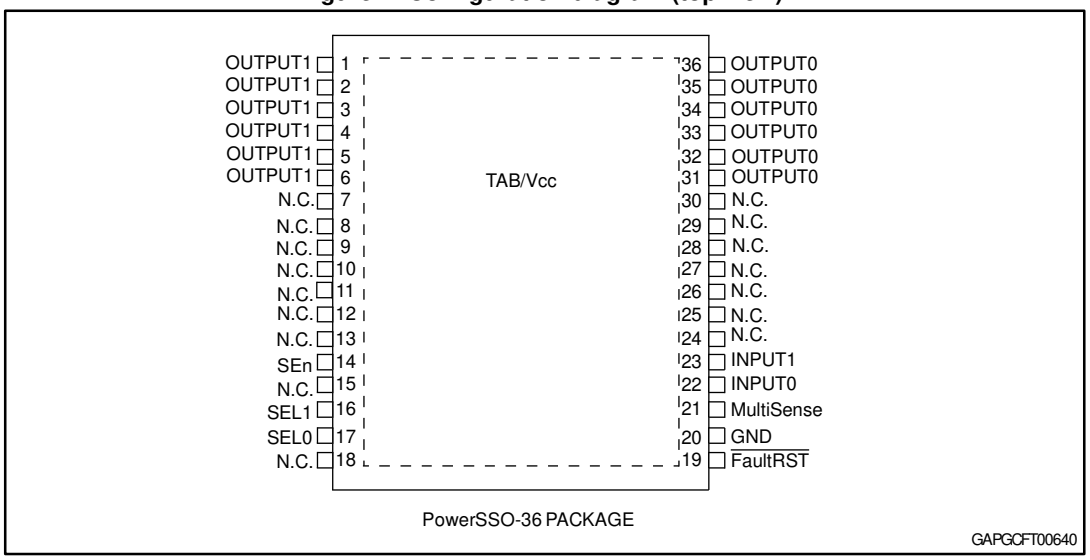


Table 2: Suggested connections for unused and not connected pins

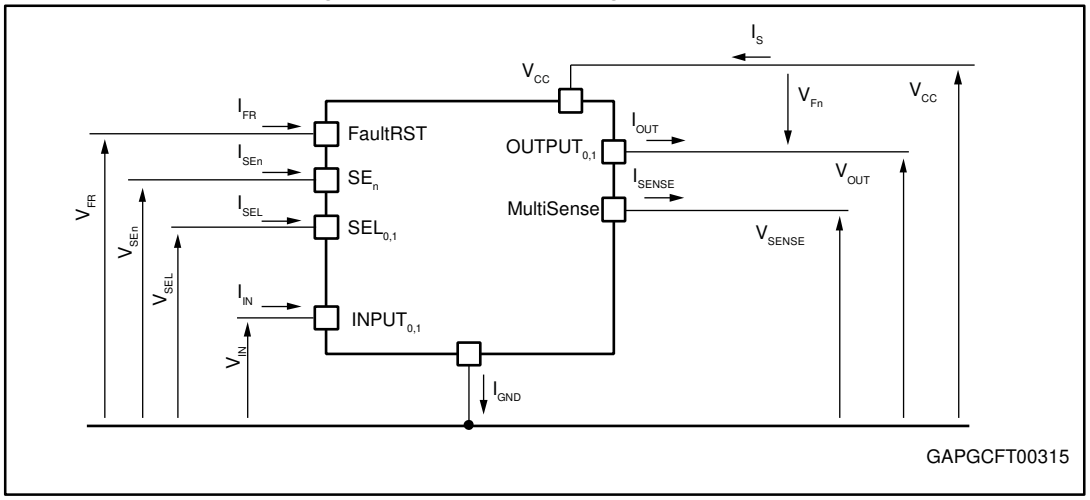
Connection/pin	MultiSense	N.C.	Output	Input	SEn, SELx, $\overline{\text{FaultRST}}$
Floating	Not allowed	X (1)	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 15 kΩ resistor	Through 15 kΩ resistor

Notes:

(1)X: do not care.

2 Electrical specification

Figure 3: Current and voltage conventions



$V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 3: "Absolute maximum ratings"* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	38	V
$-V_{CC}$	Reverse DC supply voltage	16	
V_{CCPK}	Maximum transient supply voltage (ISO7637-2:2004 Pulse 5b level IV clamped to 40 V; R_L = 4 Ω)	40	
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	$OUTPUT_{0,1}$ DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	22	
I_{IN}	$INPUT_{0,1}$ DC input current	-1 to 10	mA
I_{SEn}	SEn DC input current		
I_{SEL}	$SEL_{0,1}$ DC input current		
I_{FR}	FaultRST DC input current		
V_{FR}	FaultRST DC input voltage	7.5	V

Symbol	Parameter	Value	Unit
I_{SENSE}	MultiSense pin DC output current (V_{GND} = V_{CC} and V_{SENSE} < 0 V)	10	mA
	MultiSense pin DC output current in reverse (V_{CC} < 0 V)	-20	
E_{MAX}	Maximum switching energy (single pulse) (T_{DEMAG} = 0.4 ms; T_{jstart} = 150°C)	144	mJ
V_{ESD}	Electrostatic discharge (JDEC 22 A-114 F) • $INPUT_{0,1}$ • MultiSense • SEn, $SEL_{0,1}$, FaultRST • $OUTPUT_{0,1}$ • V_{CC}	 4000 2000 4000 4000 4000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	

2.2 Thermal data

Table 4: Thermal data

Symbol	Parameter	Typ. value	Unit
$R_{thj\text{-}board}$	Thermal resistance junction-board (JEDEC JESD 51-5 / 51-8) (1)(2)	4	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-5)(1)(3)	50.6	
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-7)(1)(2)	16.6	

Notes:

(1)One channel ON.

(2)Device mounted on four-layers 2s2p PCB

(3)Device mounted on two-layers 2s0p PCB with 2 cm^2 heatsink copper trace

2.3 Main electrical characteristics

7 V < V_{CC} < 28 V; -40°C < T_j < 150°C, unless otherwise specified.

All typical values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.

Table 5: Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4	13	28	V
V_{USD}	Undervoltage shutdown				4	
$V_{USDReset}$	Undervoltage shutdown reset				5	
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.3		
R_{ON}	On-state resistance (1)	I_{OUT} = 7 A; T_j = 25°C		12		mΩ
		I_{OUT} = 7 A; T_j = 150°C			24	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
		I_{OUT} = 7 A; V_{CC} = 4 V; T_j = 25°C			18	
R_{ON_REV}	On-state resistance in reverse battery	I_{OUT} = -7 A; V_{CC} = -13 V; T_j = 25°C		12		mΩ
V_{clamp}	Clamp voltage	I_S = 20 mA; 25°C < T_j < 150°C	41	46	52	V
		I_S = 20 mA; T_j = -40 °C	38			V
I_{STBY}	Supply current in standby at V_{CC} = 13 V (2)	V_{CC} = 13 V; $V_{IN0,1}$ = $V_{OUT0,1}$ = V_{FR} = V_{SEn} 0 V; $V_{SEL0,1}$ = 0 V; T_j = 25°C			0.5	µA
		V_{CC} = 13 V; $V_{IN0,1}$ = $V_{OUT0,1}$ = V_{FR} = V_{SEn} 0 V; $V_{SEL0,1}$ = 0 V; T_j = 85°C (3)			0.5	µA
		V_{CC} = 13 V; $V_{IN0,1}$ = $V_{OUT0,1}$ = V_{FR} = V_{SEn} 0 V; $V_{SEL0,1}$ = 0 V; T_j = 125°C			3	µA
t_{D_STBY}	Standby mode blanking time	V_{CC} = 13 V; $V_{IN0,1}$ = $V_{OUT0,1}$ = 0 V; V_{FR} = $V_{SEL0,1}$ = 0 V; V_{SEn} = 5 V to 0 V	60	300	550	µs
$I_{S(ON)}$	Supply current	V_{CC} = 13 V; V_{SEn} = V_{FR} = $V_{SEL0,1}$ = 0 V; $V_{IN0,1}$ = 5 V; I_{OUT0} = 0 A; I_{OUT1} = 0 A		5	8	mA
$I_{GND(ON)}$	Control stage current consumption in ON state. All channels active.	V_{CC} = 13 V; V_{SEn} = 5 V; V_{FR} = $V_{SEL0,1}$ = 0 V; $V_{IN0,1}$ = 5 V; I_{OUT0} = 7 A; I_{OUT1} = 7 A			10	mA
$I_{L(off)}$	Off-state output current at V_{CC} = 13 V (1)	$V_{IN0,1}$ = $V_{OUT0,1}$ = 0 V; V_{CC} = 13 V; T_j = 25°C	0	0.01	0.5	µA
		$V_{IN0,1}$ = $V_{OUT0,1}$ = 0 V; V_{CC} = 13 V; T_j = 125°C	0		3	
V_F	Output - V_{CC} diode voltage (1)	I_{OUT} = -7 A; T_j = 150 °C			0.7	V

Notes:

(1) For each channel.

(2) PowerMOS leakage included.

(3) Parameter specified by design; not subjected to production test.

Table 6: Switching (VCC = 13 V; -40 °C < Tj < 150 °C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ (1)	Turn-on delay time at T_j = 25 °C	R_L = 1.84 Ω	10	50	120	µs
$t_{d(off)}$ (1)	Turn-off delay time at T_j = 25 °C		10	45	100	
$(dV_{OUT}/dt)_{on}$ (1)	Turn-on voltage slope at T_j = 25 °C	R_L = 1.84 Ω	0.1	0.45	0.7	V/µs
$(dV_{OUT}/dt)_{off}$ (1)	Turn-off voltage slope at T_j = 25 °C		0.2	0.5	0.8	
W_{ON}	Switching energy losses at turn-on (t_{won})	R_L = 1.84 Ω	—	0.6	1.4 (2)	mJ
W_{OFF}	Switching energy losses at turn-off (t_{woff})	R_L = 1.84 Ω	—	0.6	1.3 (2)	mJ

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{SKEW} (1)	Differential pulse skew (t_{PHL} - t_{PLH})	R_L = 1.84 Ω	-60	-10	40	µs

Notes:

(1)See *Figure 6: "Switching times and Pulse skew"*

(2)Parameter guaranteed by design and characterization, not subjected to production test.

Table 7: Logic Inputs (7 V < VCC < 28 V; -40°C < Tj < 150°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$INPUT_{0,1}$ characteristics						
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.2			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
FaultRST characteristics						
V_{FRL}	Input low level voltage				0.9	V
I_{FRL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{FRH}	Input high level voltage		2.1			V
I_{FRH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{FR(hyst)}$	Input hysteresis voltage		0.2			V
V_{FRCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.5	V
		I_{IN} = -1 mA		-0.7		
$SEL_{0,1}$ characteristics (7 V < V_{CC} < 18 V)						
V_{SELL}	Input low level voltage				0.9	V
I_{SELL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SELH}	Input high level voltage		2.1			V
I_{SELH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEL(hyst)}$	Input hysteresis voltage		0.2			V
V_{SELCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
SEn characteristics (7 V < V_{CC} < 18 V)						
V_{SEnL}	Input low level voltage				0.9	V
I_{SEnL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SEnH}	Input high level voltage		2.1			V
I_{SEnH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEn(hyst)}$	Input hysteresis voltage		0.2			V
V_{SEnCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
		I_{IN} = -1 mA		-0.7		

Table 8: Protections (7 V < VCC < 18 V; -40°C < Tj < 150°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{LIMH}(1)	DC short circuit current	V_{CC} = 13 V	60	75	96	A
		4 V < V_{CC} < 18 V (2)			96	
I_{LIML}	Short circuit current during thermal cycling	V_{CC} = 13 V; T_R < T_j < T_{TSD}		25		
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature(2)		T_{RS} + 1	T_{RS} + 5		
T_{RS}	Thermal reset of fault diagnostic indication	V_{FR} = 0 V; V_{SEn} = 5 V	135			
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)(2)			5		
ΔT_{J_SD}	Dynamic temperature			60		K
t_{LATCH_RST}	Fault reset time for output unlatch(2)	V_{FR} = 5 V to 0 V; V_{SEn} = 5 V; $V_{IN0,1}$ = 5 V; $V_{SEL0,1}$ = 0 V	3	10	20	µs
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 2 A; L = 6 mH; T_j = -40 °C	V_{CC} - 38			V
		I_{OUT} = 2 A; L = 6 mH; T_j = 25°C to 150°C	V_{CC} - 41	V_{CC} - 46	V_{CC} - 52	
V_{ON}	Output voltage drop limitation	I_{OUT} = 0.7 A		20		mV

Notes:

(1)Parameter guaranteed by an indirect test sequence.

(2)Parameter guaranteed by design and characterization; not subjected to production test.

Table 9: MultiSense (7 V < VCC < 18 V; -40°C < Tj < 150°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SENSE_CL}	MultiSense clamp voltage	V_{SEn} = 0 V; I_{SENSE} = 1 mA	-17		-12	V
		V_{SEn} = 0 V; I_{SENSE} = -1 mA		7		V
Current Sense characteristics						
K_{OL}	I_{OUT}/I_{SENSE}	I_{OUT} = 10 mA; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	1400			
dK_{cal}/K_{cal}(1)(2)	Current sense ratio drift at calibration point	I_{CAL} = 130 mA; I_{OUT} = 10 mA to 250 mA; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-35		35	%

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_{LED}	I_{OUT}/I_{SENSE}	I_{OUT} = 250 mA; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	2490	5100	8000	
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.7 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	2560	5120	7680	
dK_0/K_0 (1)(2)	Current sense ratio drift	I_{OUT} = 0.7 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-25		25	%
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 1.4 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	3480	4900	6470	
dK_1/K_1 (1)(2)	Current sense ratio drift	I_{OUT} = 1.4 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-20		20	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 7 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	3410	4280	5120	
dK_2/K_2 (1)(2)	Current sense ratio drift	I_{OUT} = 7 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-10		10	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 21 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	3810	4300	4660	
dK_3/K_3 (1)(2)	Current sense ratio drift	I_{OUT} = 21 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-5		5	%
I_{SENSE0}	MultiSense leakage current	MultiSense disabled: V_{SEn} = 0 V;	0		0.5	µA
		MultiSense disabled: -1 V < V_{SENSE} < 5 V (1)	-0.5		0.5	µA
		MultiSense enabled: V_{SEn} = 5 V; All channel ON; I_{OUTX} = 0 A; Ch_X diagnostic selected; • E.g. Ch_0: V_{IN0} = 5 V; V_{IN1} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT0} = 0 A; I_{OUT1} = 7 A	0		2	µA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
		MultiSense enabled: V_{SEn} = 5 V; Ch_X channel OFF; Ch_X diagnostic selected; • E.g. Ch_0: V_{IN0} = 0 V; V_{IN1} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT1} = 7 A	0		2	µA
V_{OUT_MSD}(1)	Output Voltage for MultiSense shutdown	V_{SEn} = 5 V; R_{SENSE} = 2.7 kΩ • E.g. Ch_0: V_{IN0} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT0} = 7 A		5		V
V_{SENSE_SAT}	Multisense saturation voltage	V_{CC} = 7 V; R_{SENSE} = 2.7 kΩ; V_{SEn} = 5 V; V_{IN0} = 5 V; $V_{SEL0,1}$ = 0 V; I_{OUT0} = 21 A; T_j = 150°C	5			V
I_{SENSE_SAT}(1)	CS saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{SEn} = 5 V; V_{IN0} = 5 V; $V_{SEL0,1}$ = 0 V; T_j = 150°C	4			mA
I_{OUT_SAT}(1)	Output saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN0} = 5 V; V_{SEn} = 5 V; $V_{SEL0,1}$ = 0 V; T_j = 150°C	23			A
Off-state diagnostic						
V_{OL}	Off-state open-load voltage detection threshold	V_{SEn} = 5 V; Ch_X OFF; Ch_X diagnostic selected • E.g: Ch_0 V_{IN0} = 0 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V	2	3	4	V
$I_{L(off2)}$	OFF state output sink current	V_{IN} = 0 V; V_{OUT} = V_{OL}; T_j = -40°C to 125°C	-100		-15	µA
t_{DSTKON}	Off-state diagnostic delay time from falling edge of INPUT (see *Figure 9: "TDSKON"*)	V_{SEn} = 5 V; Ch_X ON to OFF transition Ch_X diagnostic selected • E.g: Ch_0 V_{IN0} = 5 V to 0 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT0} = 0 A; V_{OUT} = 4 V	100	350	700	µs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{D\_OL\_V}$	Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn	V_{IN0} = 0 V; V_{IN1} = 0 V; V_{FR} = 0 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; V_{OUT0} = 4 V; V_{SEn} = 0 V to 5 V			60	µs
t_{D_VOL}	Off-state diagnostic delay time from rising edge of V_{OUT}	V_{SEn} = 5 V; Ch_X OFF Ch_X diagnostic selected • E.g: Ch_0 V_{IN0} = 0 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; V_{OUT} = 0 V to 4 V		5	30	µs
Chip temperature analog feedback						
V_{SENSE_TC}	MultiSense output voltage proportional to chip temperature	V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; $V_{IN0,1}$ = 0 V; R_{SENSE} = 1 KΩ; T_j = -40°C	2.325	2.41	2.495	V
		V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; $V_{IN0,1}$ = 0 V; R_{SENSE} = 1 kΩ; T_j = 25°C	1.985	2.07	2.155	V
		V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; $V_{IN0,1}$ = 0 V; R_{SENSE} = 1 kΩ; T_j = 125°C	1.435	1.52	1.605	V
dV_{SENSE_TC}/dT (1)	Temperature coefficient	T_j = -40°C to 150°C		-5.5		mV/K
Transfer function		$V_{SENSE\_TC}(T) = V_{SENSE\_TC}(T_0) + dV_{SENSE\_TC} / dT * (T - T_0)$				
V_{CC} supply voltage analog feedback						
V_{SENSE_VCC}	MultiSense output voltage proportional to V_{CC} supply voltage	V_{CC} = 13 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; $V_{IN0,1}$ = 0 V; R_{SENSE} = 1 kΩ	3.16	3.23	3.3	V
Transfer function (3)		$V_{SENSE\_VCC} = V_{CC} / 4$				
Fault diagnostic feedback (see *Table 10: "Truth table"*)						
V_{SENSEH}	MultiSense output voltage in fault condition	V_{CC} = 13 V; R_{SENSE} = 1 kΩ; • E.g: Ch_0 in open load V_{IN0} = 0 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT0} = 0 A; V_{OUT} = 4 V	5		6.6	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SENSEH}	MultiSense output current in fault condition	V_{CC} = 13 V; V_{SENSE} = 5 V	7	20	30	mA
MultiSense timings (current sense mode - see *Figure 7: "MultiSense timings (current sense mode)"*)(4)						
$t_{DSENSE1H}$	Current sense settling time from rising edge of SEn	V_{IN} = 5 V; V_{SEn} = 0 V to 5 V; R_{SENSE} = 1 kΩ; R_L = 1.84 Ω			60	µs
$t_{DSENSE1L}$	Current sense disable delay time from falling edge of SEn	V_{IN} = 5 V; V_{SEn} = 5 V to 0 V; R_{SENSE} = 1 kΩ; R_L = 1.84 Ω		5	20	µs
$t_{DSENSE2H}$	Current sense settling time from rising edge of INPUT	V_{IN} = 0 V to 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 1.84 Ω		100	250	µs
$\Delta t_{DSENSE2H}$	Current sense settling time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	V_{IN} = 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 1.84 Ω			100	µs
$t_{DSENSE2L}$	Current sense turn-off delay time from falling edge of INPUT	V_{IN} = 5 V to 0 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 1.84 Ω		50	250	µs
MultiSense timings (chip temperature sense mode - see *Figure 8: "MultiSense timings (chip temperature and VCC sense mode)"*)(4)						
$t_{DSENSE3H}$	V_{SENSE_TC} settling time from rising edge of SEn	V_{SEn} = 0 V to 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			60	µs
$t_{DSENSE3L}$	V_{SENSE_TC} disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
MultiSense timings (V_{CC} voltage sense mode - see *Figure 8: "MultiSense timings (chip temperature and VCC sense mode)"*)(4)						
$t_{DSENSE4H}$	V_{SENSE_VCC} settling time from rising edge of SEn	V_{SEn} = 0 V to 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			60	µs
$t_{DSENSE4L}$	V_{SENSE_VCC} disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
MultiSense timings (Multiplexer transition times) (4)						

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{D_XtoY}	MultiSensetransition delay from Ch_X to Ch_Y	V_{IN0} = 5 V; V_{IN1} = 5 V; V_{SEn} = 5 V; V_{SEL1} = 0 V; V_{SEL0} = 0 V to 5 V; I_{OUT0} = 0 A; I_{OUT1} = 3 A; R_{SENSE} = 1 kΩ			20	µs
t_{D_CStoTC}	MultiSensetransition delay from current sense to T_C sense	V_{IN0} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V to 5 V; I_{OUT0} = 3.5 A; R_{SENSE} = 1 kΩ			60	µs
t_{D_TCtoCS}	MultiSensetransition delay from T_C sense to current sense	V_{IN0} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 5 V to 0 V; I_{OUT0} = 3.5 A; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_CStoVCC}$	MultiSensetransition delay from current sense to V_{CC} sense	V_{IN1} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 0 V to 5 V; I_{OUT1} = 3.5A; R_{SENSE} = 1 kΩ			60	µs
$t_{D\_VCCtoCS}$	MultiSensetransition delay from V_{CC} sense to current sense	V_{IN1} = 5 V; V_{SEn} = 5 V; V_{SEL0} = 5 V; V_{SEL1} = 5 V to 0 V; I_{OUT1} = 3.5 A; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_TCtoVCC}$	MultiSensetransition delay from T_C sense to V_{CC} sense	V_{CC} = 13 V; T_j = 125°C; V_{SEn} = 5 V; V_{SEL0} = 0 V to 5 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_VCCtoTC}$	MultiSensetransition delay from V_{CC} sense to T_C sense	V_{CC} = 13 V; T_j = 125°C; V_{SEn} = 5 V; V_{SEL0} = 5 V to 0 V; V_{SEL1} = 5 V; R_{SENSE} = 1 kΩ			20	µs
$t_{D\_CStoVSENSEH}$	MultiSensetransition delay from stable current sense on Ch_X to V_{SENSEH} on Ch_Y	V_{IN0} = 5 V; V_{IN1} = 0 V; V_{SEn} = 5 V; V_{SEL1} = 0 V; V_{SEL0} = 0 V to 5 V; I_{OUT0} = 7 A; V_{OUT1} = 4 V; R_{SENSE} = 1 kΩ			20	µs

Notes:

(1)Parameter specified by design; not subjected to production test.

(2)All values refer to V_{CC} = 13 V; T_j = 25 °C, unless otherwise specified.

(3)V_{CC} sensing and T_C sensing are referred to GND potential.

(4)Transition delay are measured up to +/- 10% of final conditions.

Figure 4: IOUT/ISENSE vs. IOUT

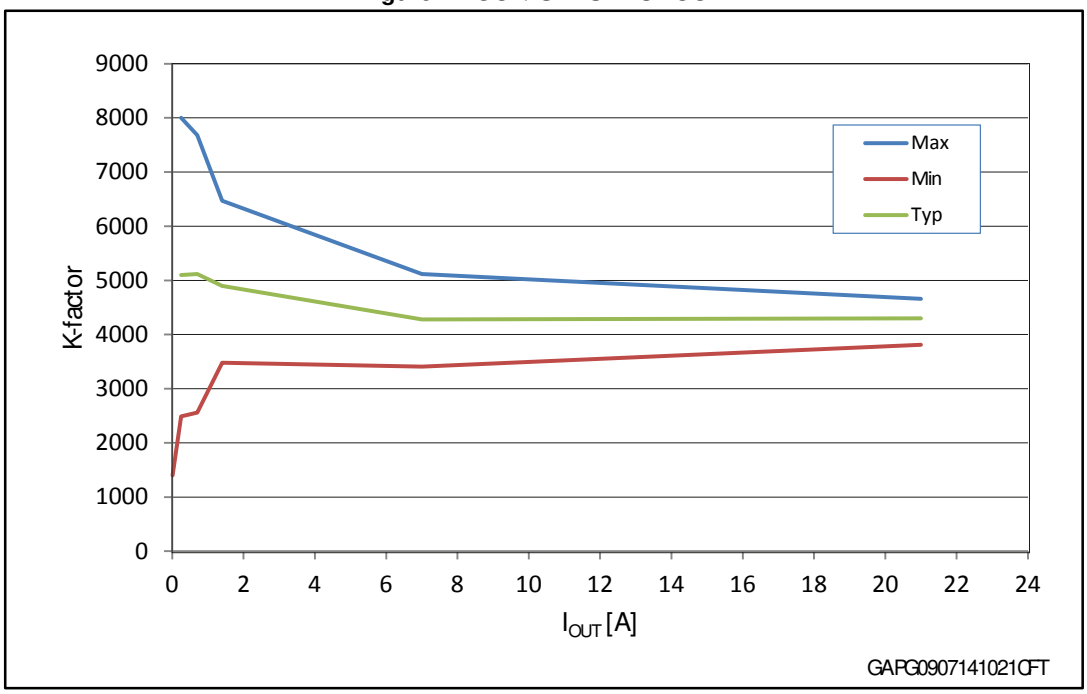


Figure 5: Current sense precision vs. IOUT

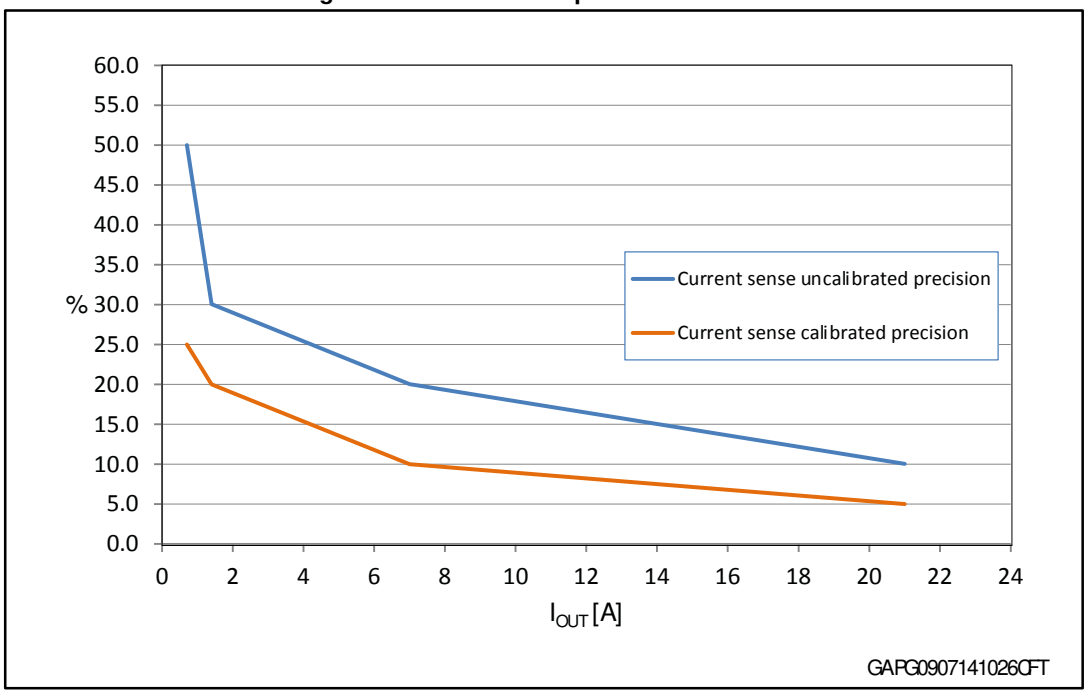


Figure 6: Switching times and Pulse skew

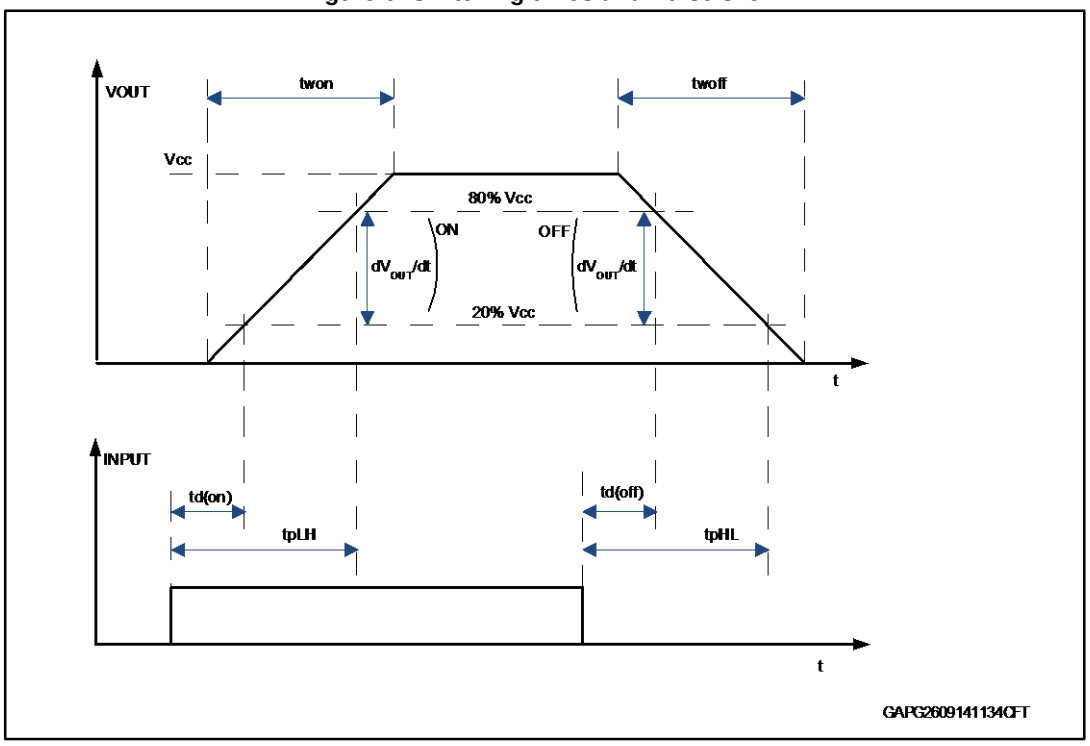


Figure 7: MultiSense timings (current sense mode)

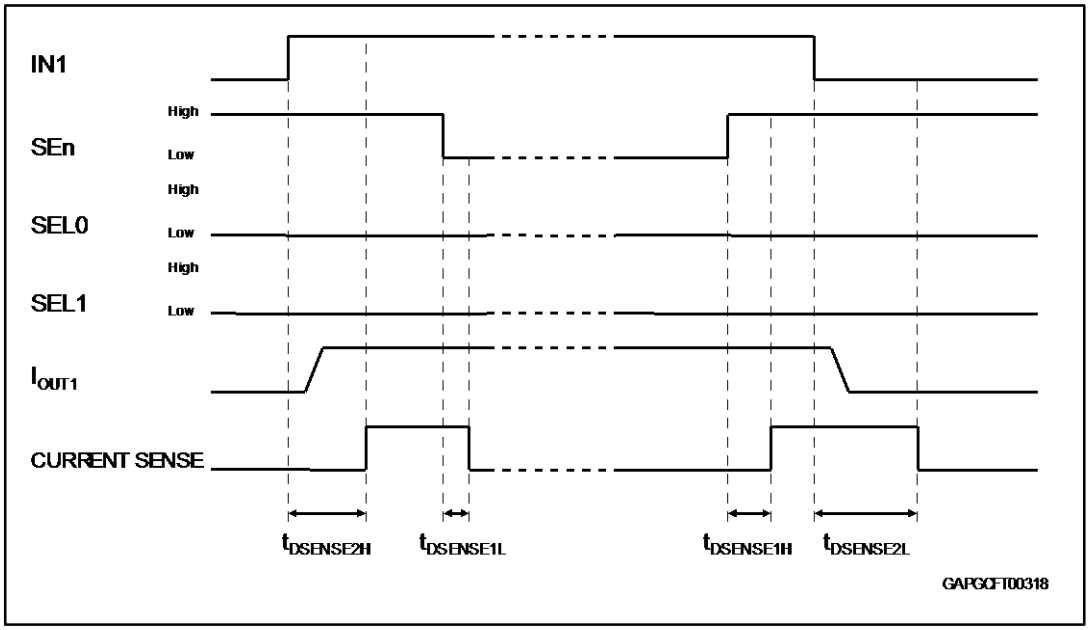


Figure 8: MultiSense timings (chip temperature and VCC sense mode)

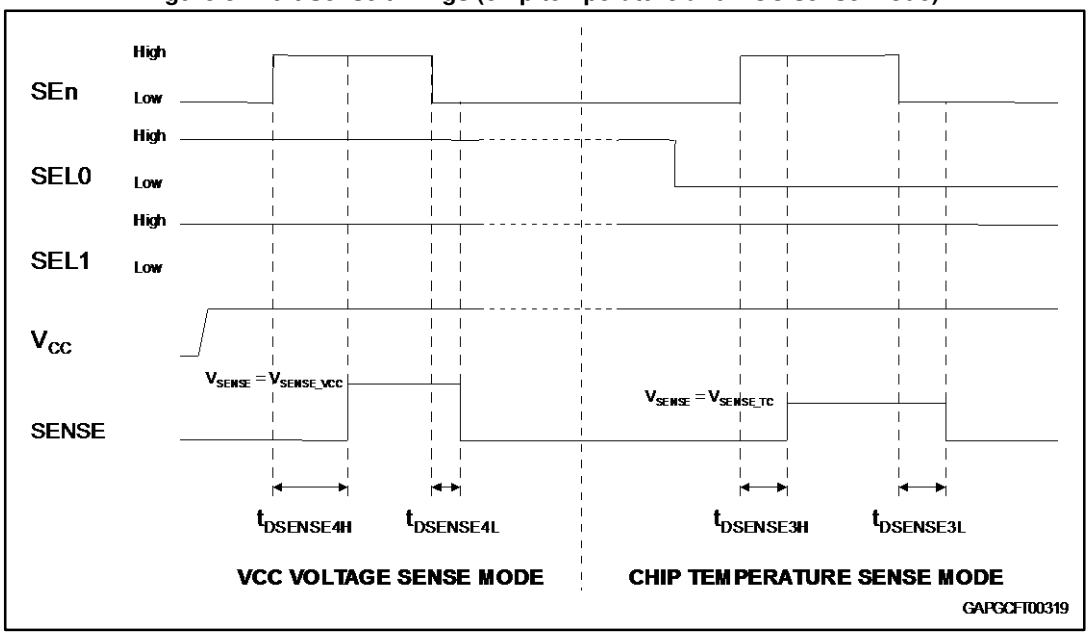


Figure 9: TDSKON

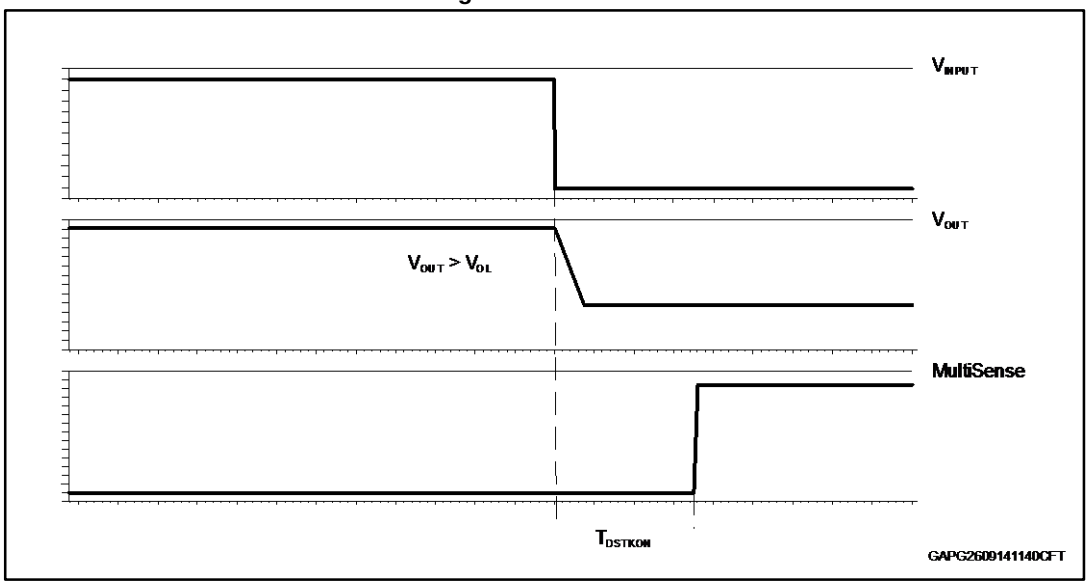


Table 10: Truth table

Mode	Conditions	INx	FR	SEn	SELx	OUTx	MultiSense	Comments
Standby	All logic inputs low	L	L	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; T_j < 150°C	L	X	See (1)		L	See (1)	
		H	L			H	See (1)	Outputs configured for auto-restart

Mode	Conditions	IN_X	FR	SEn	SEL_X	OUT_X	MultiSense	Comments
		H	H			H	See [(1)]	Outputs configured for latch off
Overload	Overload or short to GND causing: $T_j > T_{TSD}$ or $\Delta T_j > \Delta T_{j\_SD}$	L	X	See [(1)]		L	See [(1)]	
		H	L			H	See [(1)]	Output cycles with temperature hysteresis
		H	H			L	See [(1)]	Output latches off
Under-voltage	$V_{CC} < V_{USD}$ (falling)	X	X	X	X	L L	Hi-Z Hi-Z	Re-start when $V_{CC} > V_{USD} + V_{USDhyst}$ (rising)
Off-state diagnostics	Short to V_{CC}	L	X	See [(1)]		H	See [(1)]	
	Open-load	L	X			H	See [(1)]	External pull up
Negative output voltage	Inductive loads turn-off	L	X	See [(1)]		< 0 V	See [(1)]	

Notes:

[(1)]Refer to *Table 11: "MultiSense multiplexer addressing"*

Table 11: MultiSense multiplexer addressing

SEn	SEL_1	SEL_0	MUXchannel	MultiSense output			
				Normal mode	Overload	Off-state diag. [(1)]	Negative output
L	X	X		Hi-Z			
H	L	L	Channel 0 diagnostic	$I_{SENSE} = 1/K * I_{OUT0}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	Hi-Z
H	L	H	Channel 1 diagnostic	$I_{SENSE} = 1/K * I_{OUT1}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	Hi-Z
H	H	L	T_{CHIP} Sense	$V_{SENSE} = V_{SENSE\_TC}$			
H	H	H	V_{CC} Sense	$V_{SENSE} = V_{SENSE\_VCC}$			

Notes:

[(1)]In case the output channel corresponding to the selected MUX channel is latched off while the relevant input is low, Multisense pin delivers feedback according to OFF-State diagnostic. Example 1: FR = 1; IN_0 = 0; OUT_0 = L (latched); MUX channel = channel 0 diagnostic; Mutisense = 0. Example 2: FR = 1; IN_0 = 0; OUT_0 = latched, $V_{OUT0} > V_{OL}$; MUX channel = channel 0 diagnostic; Mutisense = V_{SENSEH}

2.4 Electrical characteristics curves

Figure 10: OFF-state output current

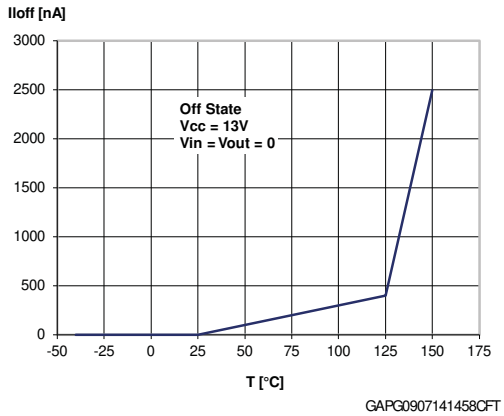


Figure 11: Standby current

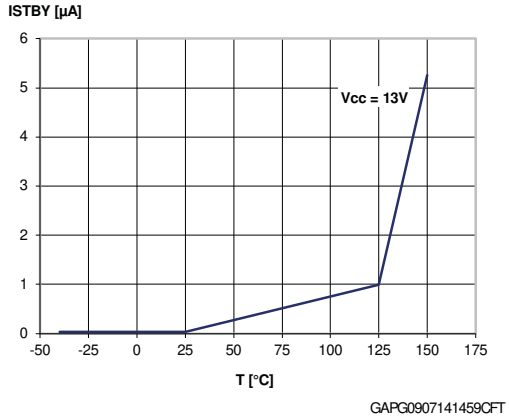


Figure 12: IGND(ON) vs. Iout

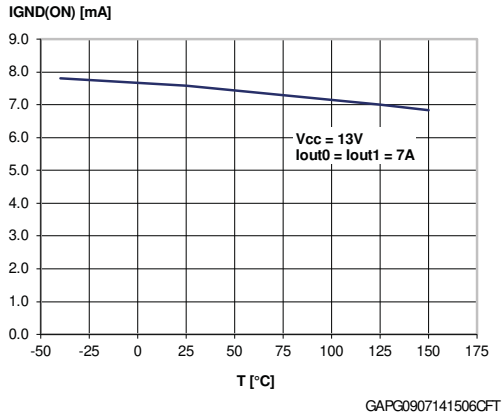


Figure 13: Logic Input high level voltage

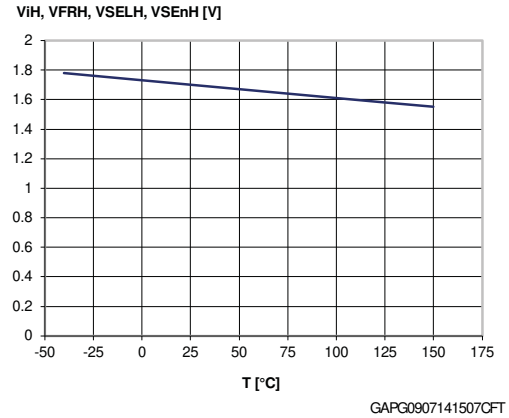


Figure 14: Logic Input low level voltage

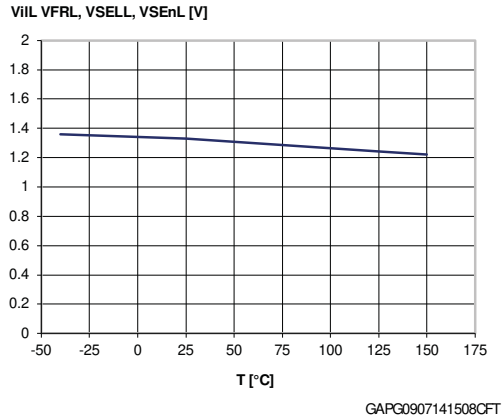


Figure 15: High level logic input current

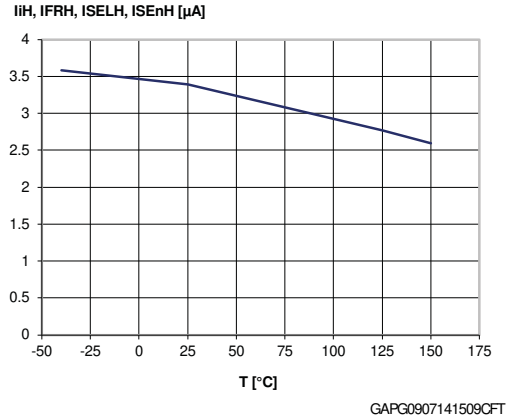


Figure 16: Low level logic input current

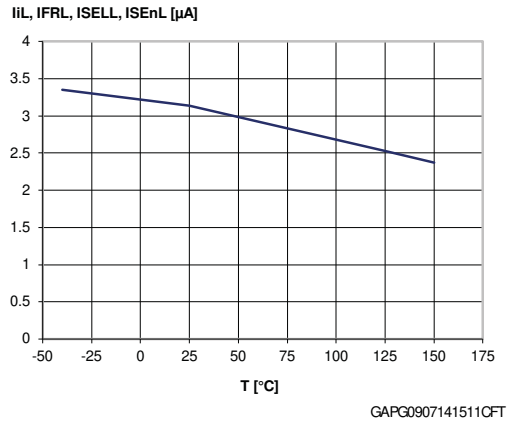


Figure 17: Logic Input hysteresis voltage

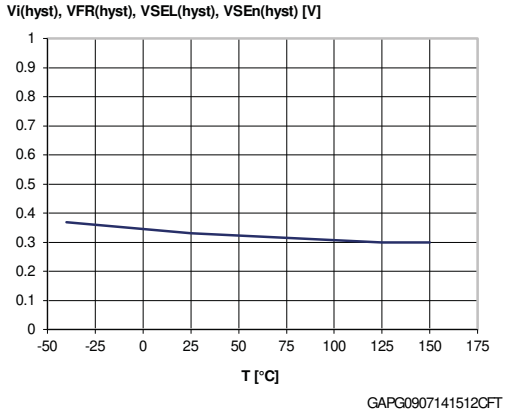


Figure 18: FaultRST Input clamp voltage

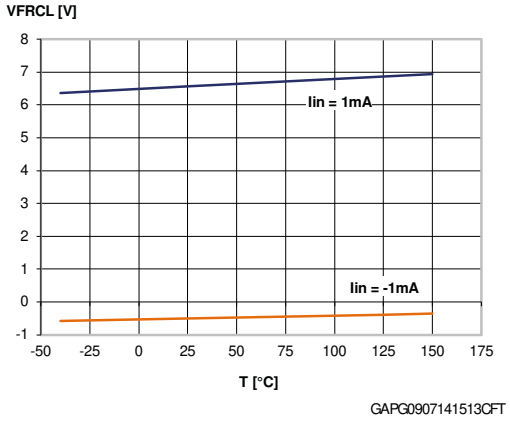


Figure 19: Undervoltage shutdown

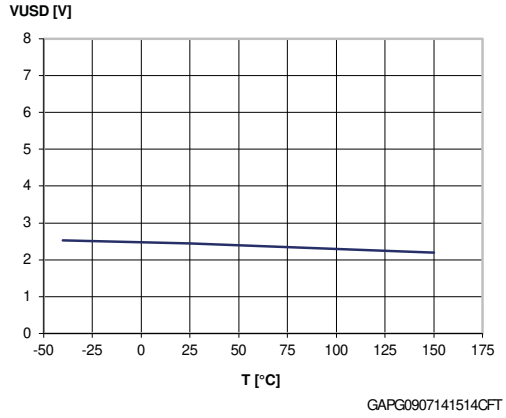


Figure 20: On-state resistance vs. Tcase

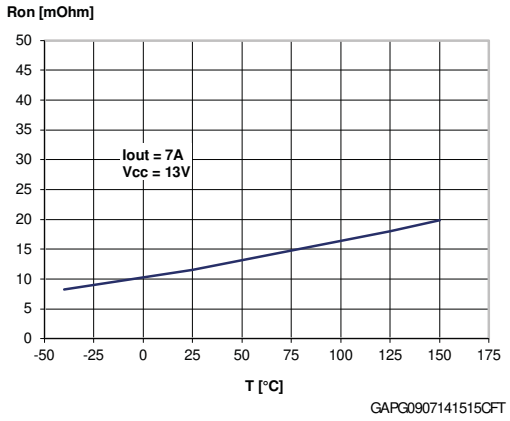


Figure 21: On-state resistance vs. VCC

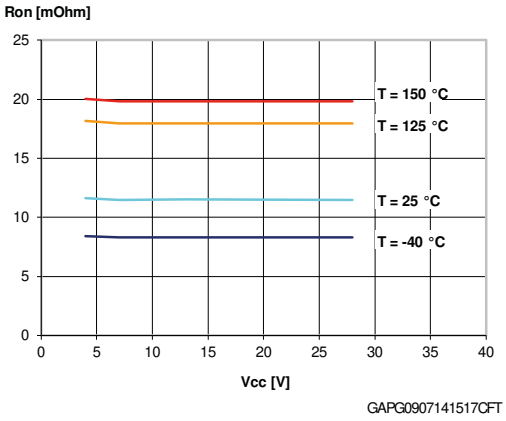


Figure 22: Turn-on voltage slope

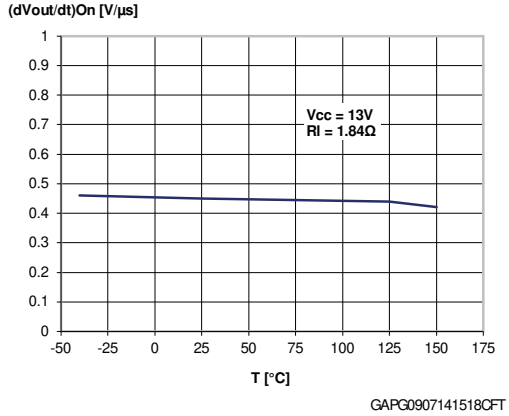


Figure 23: Turn-off voltage slope

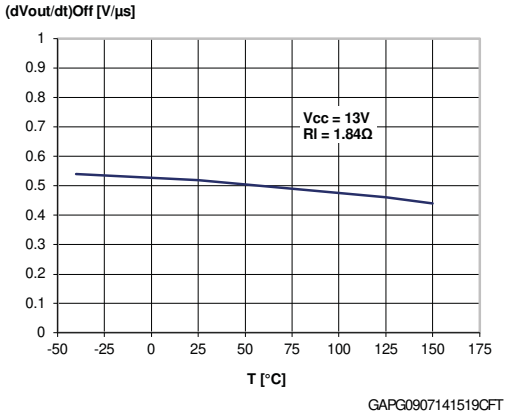


Figure 24: Won vs. Tcase

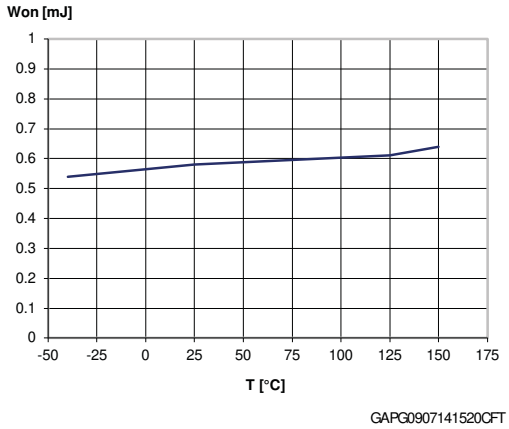


Figure 25: Woff vs. Tcase

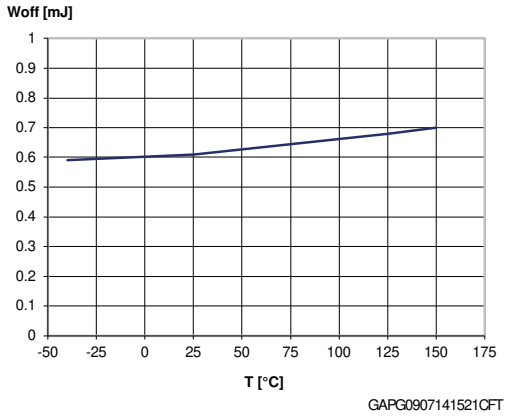


Figure 26: ILIMH vs. Tcase

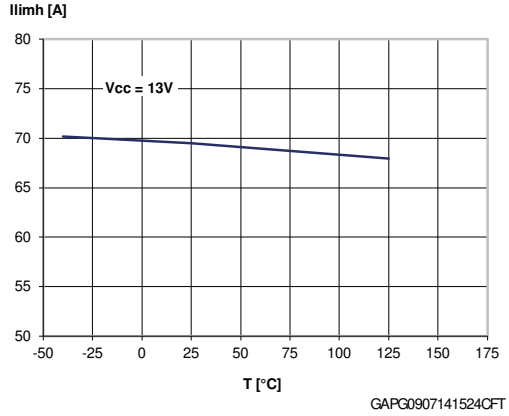


Figure 27: OFF-state open-load voltage detection threshold

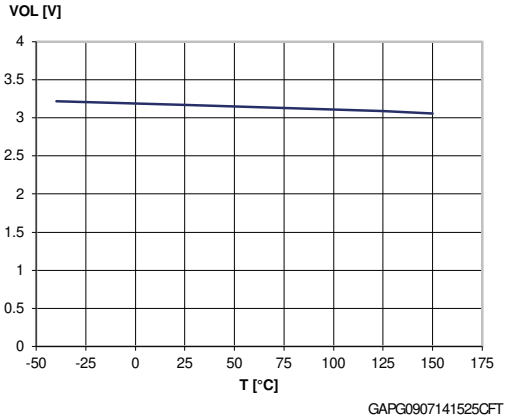


Figure 28: Vsense clamp vs. Tcase

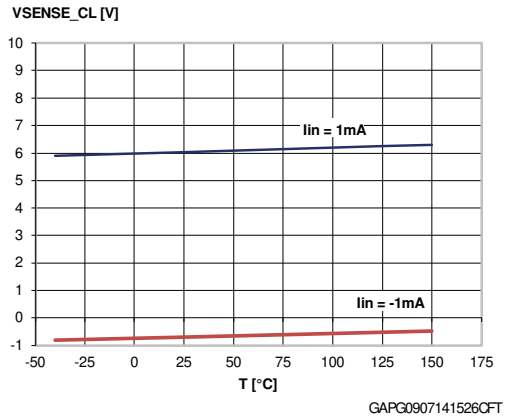
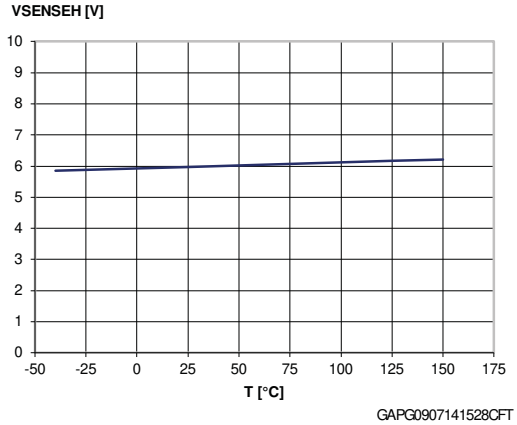


Figure 29: Vsenseh vs. Tcase



3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_j through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_j exceeds the safety level of ΔT_{j_SD}. According to the voltage level on the FaultRST pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled (FaultRST = Low) or remains off (FaultRST = High). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the FaultRST pin, the device switches on again as soon as its junction temperature drops to T_R (FaultRST = Low) or remains off (FaultRST = High).

3.3 Current limitation

The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH}, by operating the output power MOSFET in the active region.

3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches a negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG}, allowing the inductor energy to be dissipated without damaging the device.