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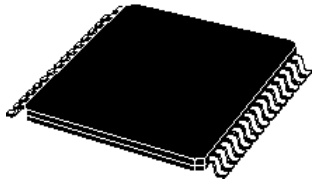
VNH2SP30-E

Automotive fully integrated H-bridge motor driver

Datasheet - production data



MultiPowerSO-30™

Features

Type	$R_{DS(on)}$	I_{out}	V_{ccmax}
VNH2SP30-E	19 mΩ max (per leg)	30 A	41 V

- AEC-Q100 qualified
- 5 V logic level compatible inputs
- Undervoltage and overvoltage shutdown
- Overvoltage clamp
- Thermal shutdown
- Cross-conduction protection
- Linear current limiter
- Very low standby power consumption
- PWM operation up to 20 kHz
- Protection against loss of ground and loss of V_{CC}
- Current sense output proportional to motor current
- Package: ECOPACK®

Description

The VNH2SP30-E is a full bridge motor driver intended for a wide range of automotive applications. The device incorporates a dual monolithic high side driver and two low side switches. The high side driver switch is designed using STMicroelectronics well known and proven proprietary VIPower™ M0 technology which permits efficient integration on the same die of a true power MOSFET with intelligent signal/protection circuitry.

The low side switches are vertical MOSFETs manufactured using STMicroelectronics proprietary EHD (STripFET™) process. The three die are assembled in a MultiPowerSO-30 package on electrically isolated leadframes. This package, specifically designed for the harsh automotive environments, offers improved thermal performance thanks to exposed die pads. Moreover, its fully symmetrical mechanical design allows superior manufacturability at board level. The input signals IN_A and IN_B can directly interface with the microcontroller to select the motor direction and brake condition. The $DIAG_A/EN_A$ or $DIAG_B/EN_B$, when connected to an external pull-up resistor, enable one leg of the bridge. They also provide a feedback digital diagnostic signal. The normal operating condition is explained in the truth table. The motor current can be monitored with the CS pin by delivering a current proportional to its value. The speed of the motor can be controlled in all possible conditions by the PWM up to 20 kHz. In all cases, a low level state on the PWM pin will turn off both the LS_A and LS_B switches. When PWM rises to a high level, LS_A or LS_B turn on again depending on the input pin state.

Table 1. Device summary

Package	Order code
	Tape and reel
MultiPowerSO-30	VNH2SP30TR-E

Contents

List of tables

List of figures

1 Block diagram and pin description

Figure 1. Block diagram

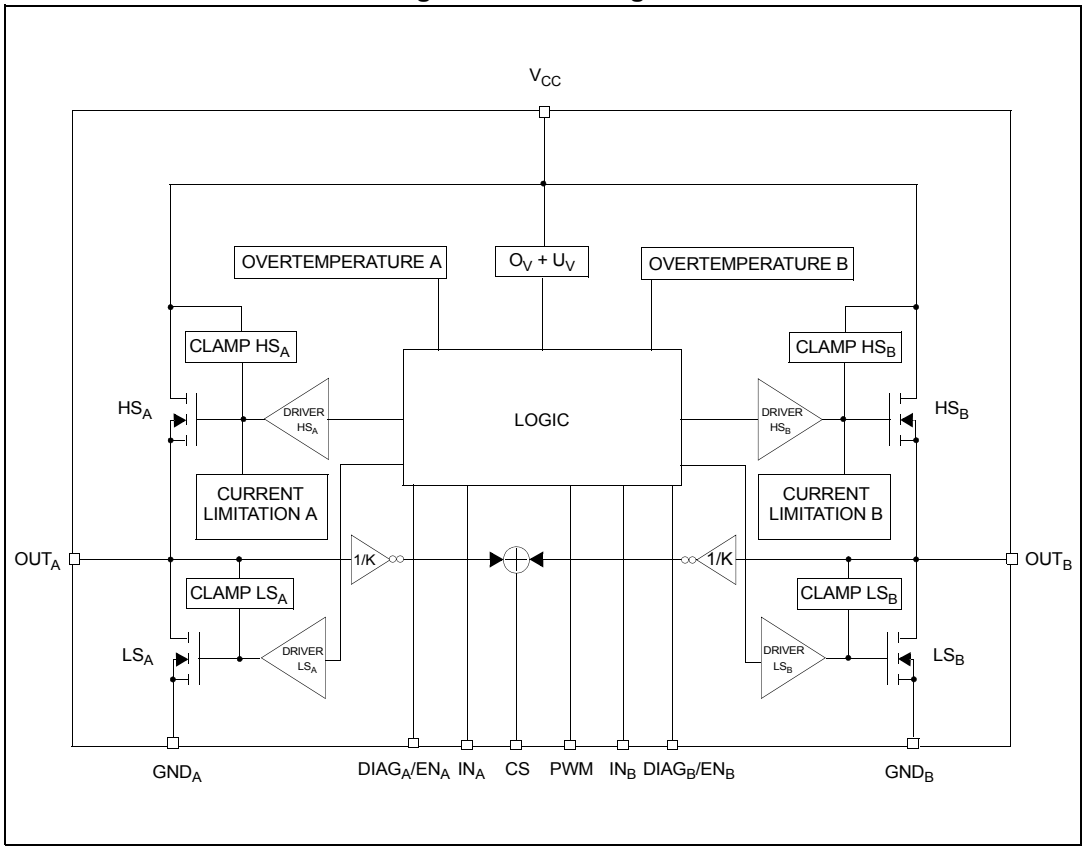


Table 2. Block description

Name	Description
Logic control	Allows the turn-on and the turn-off of the high side and the low side switches according to the truth table
Overvoltage + undervoltage	Shuts down the device outside the range [5.5V..16V] for the battery voltage
High side and low side clamp voltage	Protects the high side and the low side switches from the high voltage on the battery line in all configurations for the motor
High side and low side driver	Drives the gate of the concerned switch to allow a proper $R_{DS(on)}$ for the leg of the bridge
Linear current limiter	Limits the motor current by reducing the high side switch gate-source voltage when short-circuit to ground occurs
Overtemperature protection	In case of short-circuit with the increase of the junction's temperature, shuts down the concerned high side to prevent its degradation and to protect the die
Fault detection	Signals an abnormal behavior of the switches in the half-bridge A or B by pulling low the concerned $EN_x/DIAG_x$ pin

Figure 2. Configuration diagram (top view)

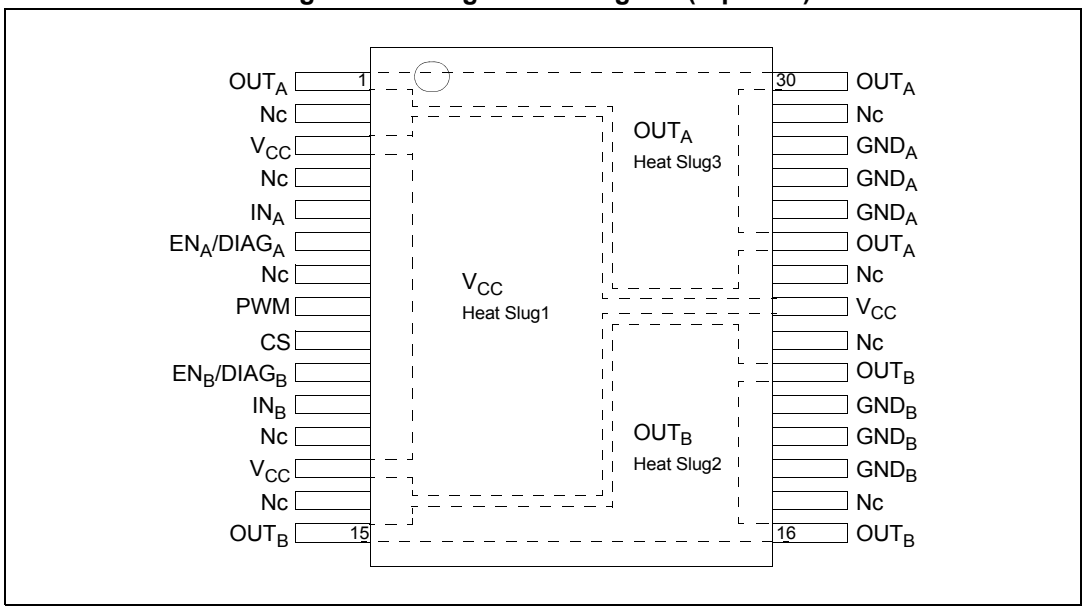


Table 3. Pin definitions and functions

Pin no.	Symbol	Function
1, 25, 30	OUT_A, Heat Slug3	Source of high side switch A / Drain of low side switch A
2, 4, 7, 12, 14, 17, 22, 24, 29	NC	Not connected
3, 13, 23	V_{CC}, Heat Slug1	Drain of high side switches and power supply voltage
6	$EN_A/DIAG_A$	Status of high side and low side switches A; open drain output
5	IN_A	Clockwise input
8	PWM	PWM input
9	CS	Output of current sense
11	IN_B	Counter clockwise input
10	$EN_B/DIAG_B$	Status of high side and low side switches B; open drain output
15, 16, 21	OUT_B, Heat Slug2	Source of high side switch B / Drain of low side switch B
26, 27, 28	GND_A	Source of low side switch A(1)
18, 19, 20	GND_B	Source of low side switch B(1)

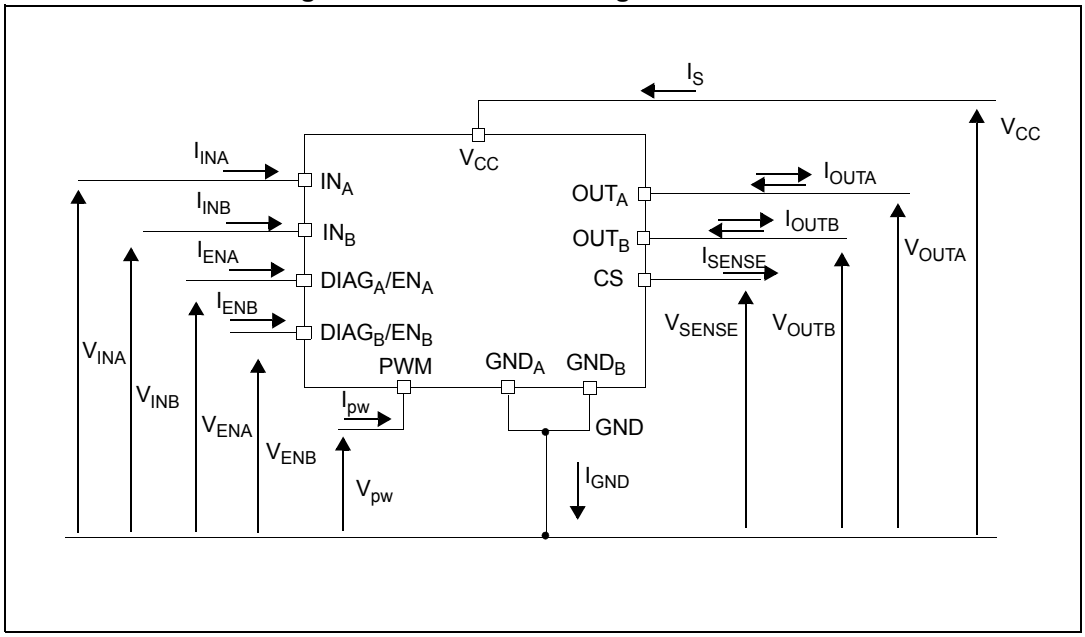
1. GND_A and GND_B must be externally connected together.

Table 4. Pin functions description

Name	Description
V_{CC}	Battery connection
GND_A, GND_B	Power grounds; must always be externally connected together
OUT_A, OUT_B	Power connections to the motor
IN_A, IN_B	Voltage controlled input pins with hysteresis, CMOS compatible. These two pins control the state of the bridge in normal operation according to the truth table (brake to V_{CC}, brake to GND, clockwise and counterclockwise).
PWM	Voltage controlled input pin with hysteresis, CMOS compatible. Gates of low side FETs are modulated by the PWM signal during their ON phase allowing speed control of the motor.
$EN_A/DIAG_A$, $EN_B/DIAG_B$	Open drain bidirectional logic pins. These pins must be connected to an external pull up resistor. When externally pulled low, they disable half-bridge A or B. In case of fault detection (thermal shutdown of a high side FET or excessive ON state voltage drop across a low side FET), these pins are pulled low by the device (see truth table in fault condition).
CS	Analog current sense output. This output sources a current proportional to the motor current. The information can be read back as an analog voltage across an external resistor.

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	+41	V
I_{max}	Maximum output current (continuous)	30	A
I_R	Reverse output current (continuous)	-30	
I_{IN}	Input current (IN_A and IN_B pins)	±10	mA
I_{EN}	Enable input current ($DIAG_A/EN_A$ and $DIAG_B/EN_B$ pins)	±10	
I_{pw}	PWM input current	±10	
V_{CS}	Current sense maximum voltage	-3/+15	V
V_{ESD}	Electrostatic discharge (R = 1.5kΩ, C = 100pF) – CS pin – logic pins – output pins: OUT_A, OUT_B, V_{CC}	 2 4 5	 kV kV kV
T_j	Junction operating temperature	Internally limited	°C
T_c	Case operating temperature	-40 to 150	
T_{STG}	Storage temperature	-55 to 150	

2.2 Electrical characteristics

V_{CC} = 9V up to 16 V; -40°C < T_J < 150°C, unless otherwise specified.

Table 6. Power section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CC}	Operating supply voltage		5.5		16	V
I_S	Supply current	Off state with all Fault Cleared & ENx=0 IN_A = IN_B = PWM = 0; T_j = 25°C; V_{CC} = 13V IN_A = IN_B = PWM = 0 Off state: IN_A = IN_B = PWM = 0		12 2	30 60	µA µA mA
		On state: IN_A or IN_B = 5V, no PWM			10	mA
R_{ONHS}	Static high side resistance	I_{OUT} = 15A; T_j = 25°C			14	mΩ
		I_{OUT} = 15A; T_j = -40 to 150°C			28	
R_{ONLS}	Static low side resistance	I_{OUT} = 15A; T_j = 25°C			5	
		I_{OUT} = 15A; T_j = -40 to 150°C			10	
V_f	High side free-wheeling diode forward voltage	I_f = 15A		0.8	1.1	V
$I_{L(off)}$	High side off state output current (per channel)	T_j = 25°C; V_{OUTX} = EN_X = 0V; V_{CC} = 13V			3	µA
		T_j = 125°C; V_{OUTX} = EN_X = 0V; V_{CC} = 13V			5	
I_{RM}	Dynamic cross-conduction current	I_{OUT} = 15A (see *Figure 7*)		0.7		A

Table 7. Logic inputs (IN_A, IN_B, EN_A, EN_B)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	Normal operation ($DIAG_X$/EN_X pin acts as an input pin)			1.25	V
V_{IH}	Input high level voltage		3.25			
V_{IHYST}	Input hysteresis voltage		0.5			
V_{ICL}	Input clamp voltage	I_{IN} = 1mA	5.5	6.3	7.5	
		I_{IN} = -1mA	-1.0	-0.7	-0.3	
I_{INL}	Input low current	V_{IN} = 1.25V	1			µA
I_{INH}	Input high current	V_{IN} = 3.25V			10	
V_{DIAG}	Enable output low level voltage	Fault operation ($DIAG_X$/EN_X pin acts as an output pin); I_{EN} = 1mA			0.4	V

Table 8. PWM

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{pwl}	PWM low level voltage				1.25	V
I_{pwl}	PWM pin current	V_{pw} = 1.25V	1			µA
V_{pwh}	PWM high level voltage		3.25			V
I_{pwh}	PWM pin current	V_{pw} = 3.25V			10	µA
$V_{pwhhyst}$	PWM hysteresis voltage		0.5			V
V_{pwcl}	PWM clamp voltage	I_{pw} = 1mA	V_{CC} + 0.3	V_{CC} + 0.7	V_{CC} + 1.0	
		I_{pw} = -1mA	-6.0	-4.5	-3.0	
C_{INPWM}	PWM pin input capacitance	V_{IN} = 2.5V			25	pF

Table 9. Switching (V_{CC} = 13 V, R_{LOAD} = 0.87 Ω , unless otherwise specified)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
f	PWM frequency		0		20	kHz
$t_{d(on)}$	Turn-on delay time	Input rise time < 1µs (see *Figure 6*)			250	µs
$t_{d(off)}$	Turn-off delay time	Input rise time < 1µs (see *Figure 6*)			250	
t_r	Rise time	(see *Figure 5*)		1	1.6	
t_f	Fall time	(see *Figure 5*)		1.2	2.4	
t_{DEL}	Delay time during change of operating mode	(see *Figure 4*)	300	600	1800	
t_{rr}	High side free wheeling diode reverse recovery time	(see *Figure 7*)		110		ns
$t_{off(min)}$(1)	PWM minimum off time	9V < V_{CC} < 16V; T_j = 25°C; L = 250µH; I_{OUT} = 15A			6	µs

1. To avoid false short to battery detection during PWM operation, the PWM signal must be low for a time longer than 6 µs.

Table 10. Protection and diagnostic

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{USD}	Undervoltage shutdown				5.5	V
	Undervoltage reset			4.7		
V_{OV}	Overvoltage shutdown		16	19	22	
I_{LIM}	High side current limitation		30	50	70	A
V_{CLP}	Total clamp voltage (V_{CC} to GND)	I_{OUT} = 15A	43	48	54	V
T_{TSD}	Thermal shutdown temperature	V_{IN} = 3.25V	150	175	200	°C
T_{TR}	Thermal reset temperature		135			
T_{HYST}	Thermal hysteresis		7	15		

Table 11. Current sense (9 V < V_{CC} < 16 V)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 30A; R_{SENSE} = 1.5kΩ; T_j = -40 to 150°C	9665	11370	13075	
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 8A; R_{SENSE} = 1.5kΩ; T_j = -40 to 150°C	9096	11370	13644	
dK_1 / K_1 (1)	Analog sense current drift	I_{OUT} = 30A; R_{SENSE} = 1.5kΩ; T_j = -40 to 150°C	-8		+8	%
dK_2 / K_2 (1)	Analog sense current drift	I_{OUT} > 8A; R_{SENSE} = 1.5kΩ; T_j = -40 to 150°C	-10		+10	
I_{SENSEO}	Analog sense leakage current	I_{OUT} = 0A; V_{SENSE} = 0V; T_j = -40 to 150°C	0		65	µA

1. Analog sense current drift is deviation of factor K for a given device over (-40 °C to 150 °C and 9 V < V_{CC} < 16 V) with respect to its value measured at T_j = 25°C, V_{CC} = 13 V.

Figure 4. Definition of the delay times measurement

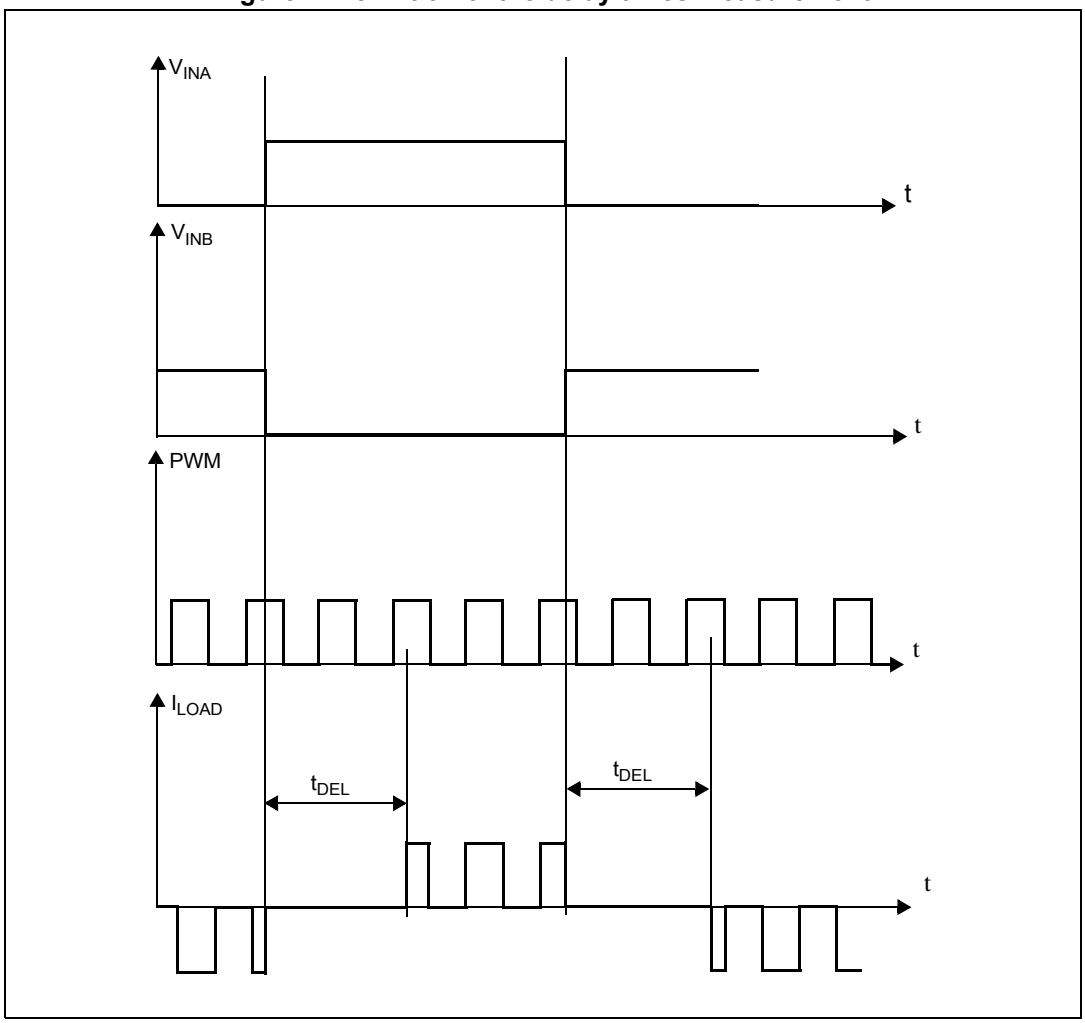


Figure 5. Definition of the low side switching times

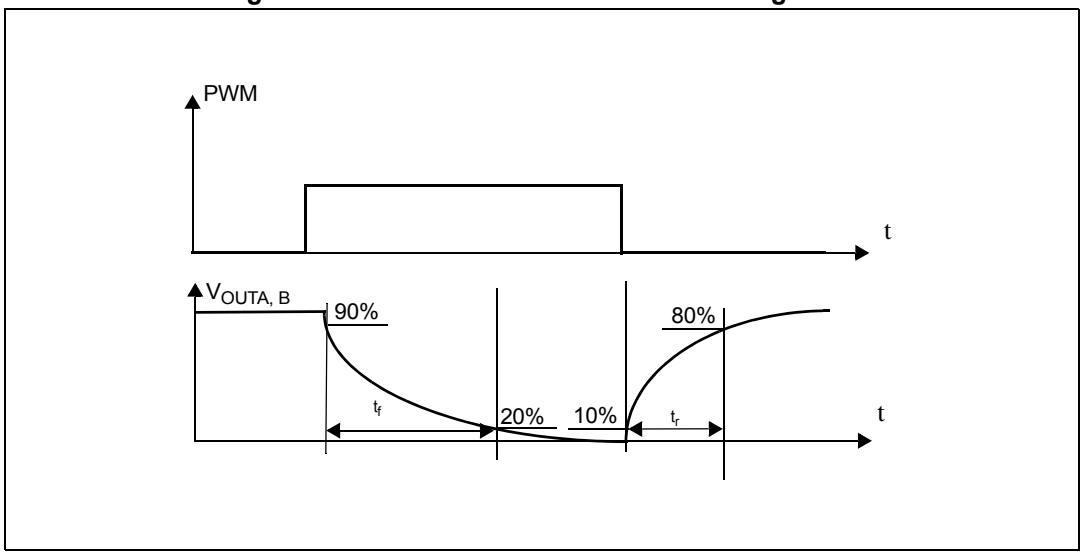


Figure 6. Definition of the high side switching times

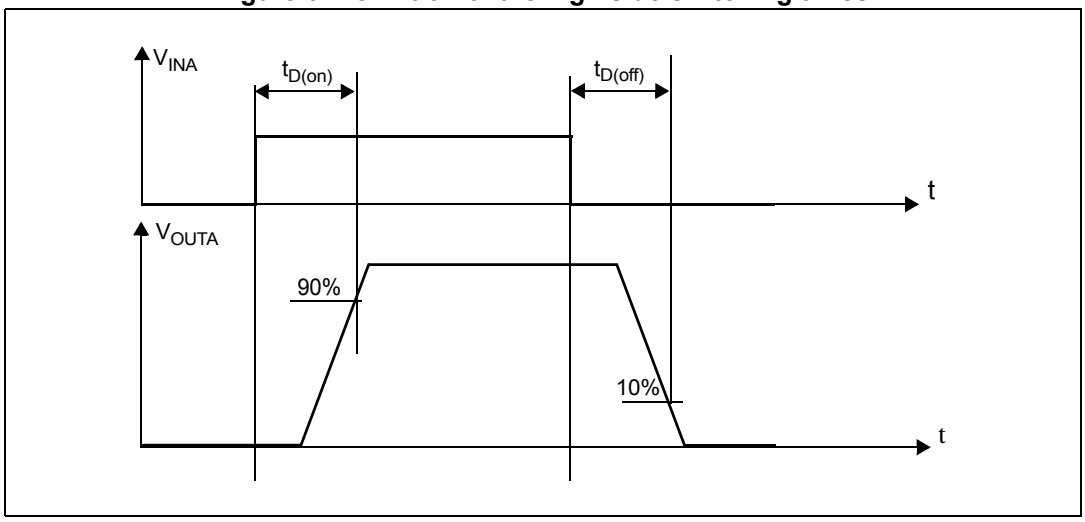


Figure 7. Definition of dynamic cross conduction current during a PWM operation

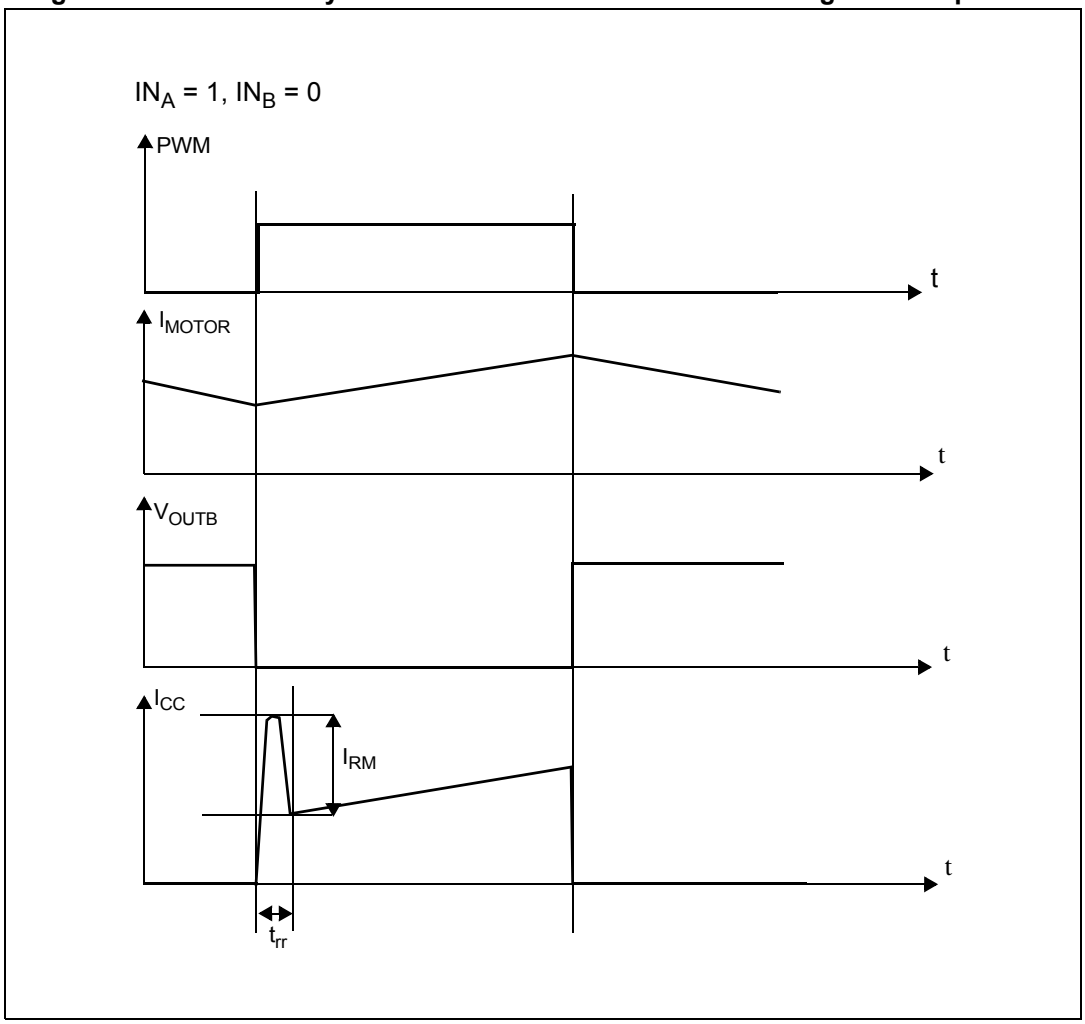


Table 12. Truth table in normal operating conditions

IN_A	IN_B	$DIAG_A/EN_A$	$DIAG_B/EN_B$	OUT_A	OUT_B	CS	Operating mode
1	1	1	1	H	H	High Imp.	Brake to V_{CC}
	0				L	$I_{SENSE} = I_{OUT}/K$	Clockwise (CW)
0	1			L	H		Counterclockwise (CCW)
	0				L	High imp.	Brake to GND

Table 13. Truth table in fault conditions (detected on OUT_A)

IN_A	IN_B	$DIAG_A/EN_A$	$DIAG_B/EN_B$	OUT_A	OUT_B	CS
1	1	0	1	OPEN	H	High Imp.
	0				L	
0	1				H	I_{OUTB}/K
	0				L	High Imp.
X	X		0		OPEN	
	1		1		H	I_{OUTB}/K
	0				L	High Imp.
		↑ Fault Information		↑ Protection Action		

Note: The saturation detection on the low side power MOSFET is possible only if the impedance of the short-circuit from the output to the battery is less than 100 mΩ when the device is supplied with a battery voltage of 13.5 V.

Table 14. Electrical transient requirements

ISO T/R - 7637/1 test pulse	Test level I	Test level II	Test level III	Test level IV	Test levels delays and impedance
1	-25V	-50V	-75V	-100V	2ms, 10Ω
2	+25V	+50V	+75V	+100V	0.2ms, 10Ω
3a	-25V	-50V	-100V	-150V	0.1µs, 50Ω
3b	+25V	+50V	+75V	+100V	
4	-4V	-5V	-6V	-7V	100ms, 0.01Ω
5	+26.5V	+46.5V	+66.5V	+86.5V	400ms, 2Ω

ISO T/R - 7637/1 test pulse	Test levels result I	Test levels result II	Test levels result III	Test levels result IV
1	C	C	C	C
2				
3a				
3b				
4				
5(1)		E	E	E

1. For load dump exceeding the above value a centralized suppressor must be adopted.

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.3 Electrical characteristics curves

Figure 8. On state supply current

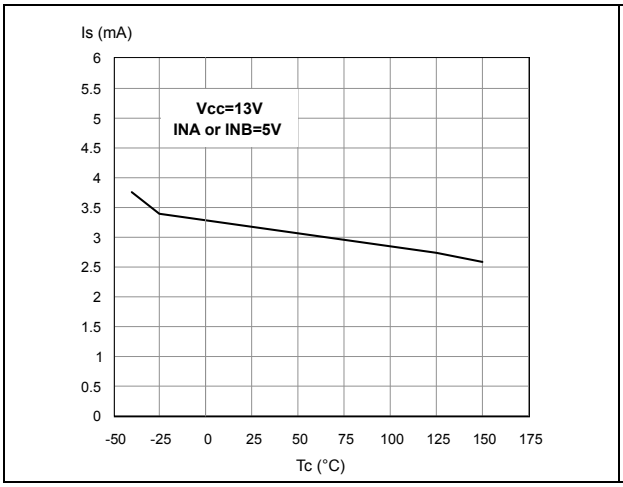


Figure 9. Off state supply current

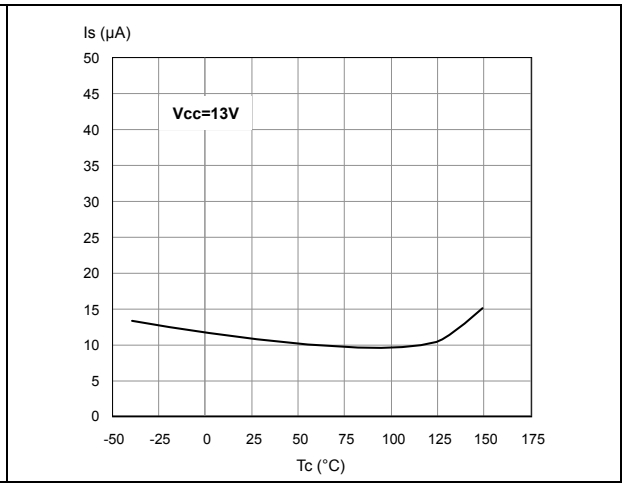


Figure 10. High level input current

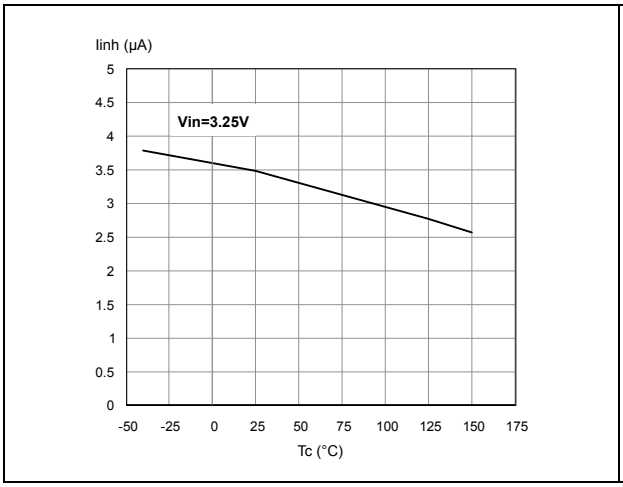


Figure 11. Input clamp voltage

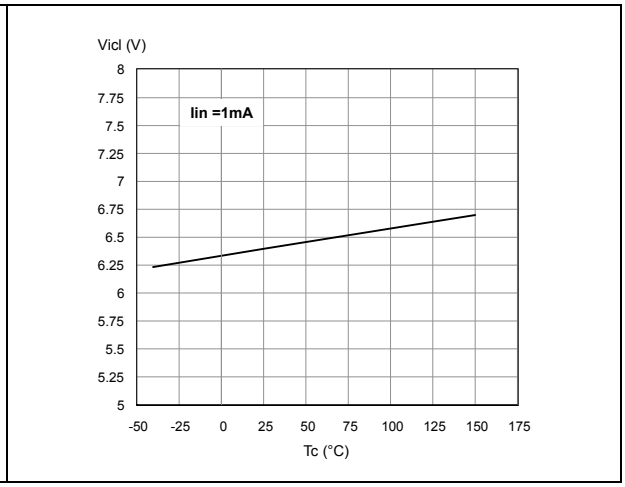


Figure 12. Input high level voltage

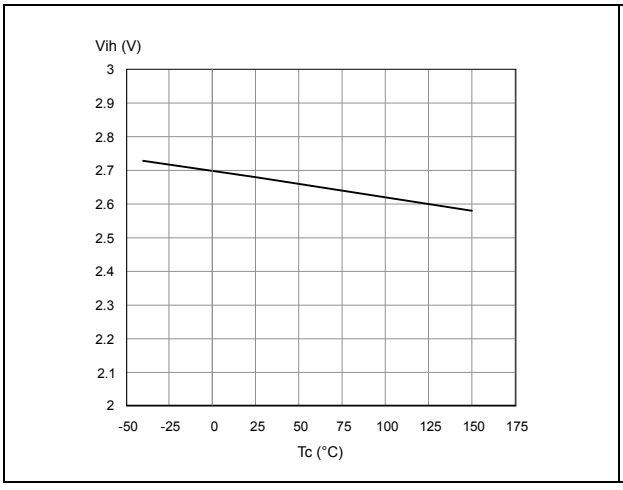


Figure 13. Input low level voltage

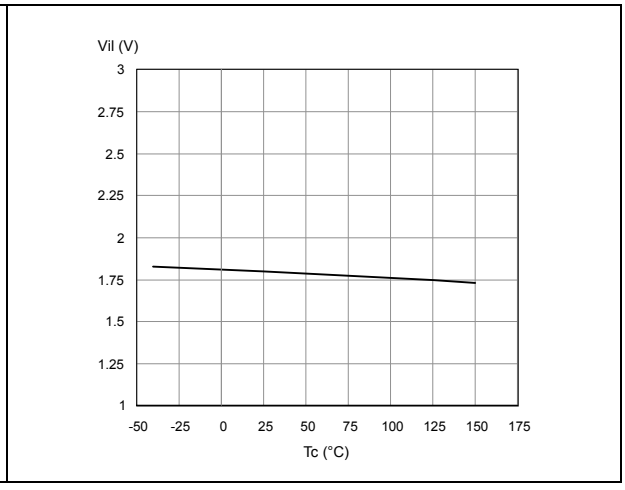


Figure 14. Input hysteresis voltage

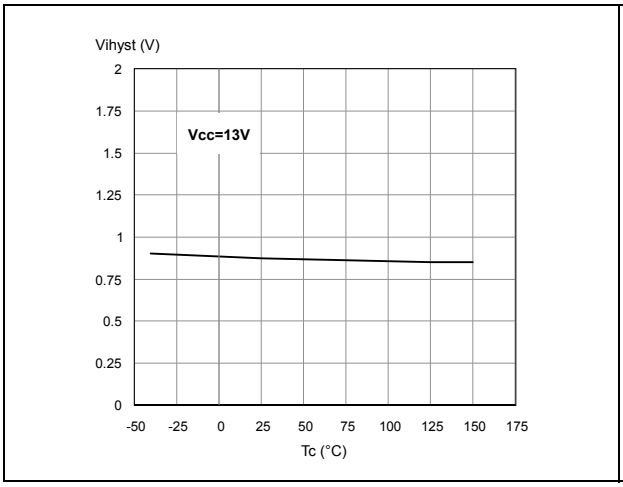


Figure 15. High level enable pin current

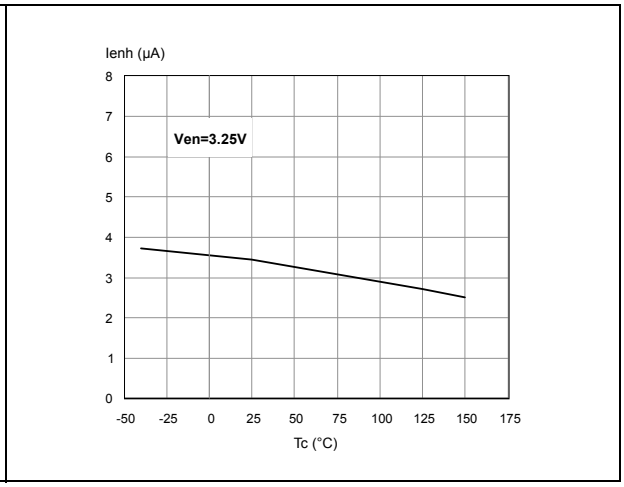


Figure 16. Delay time during change of operation mode

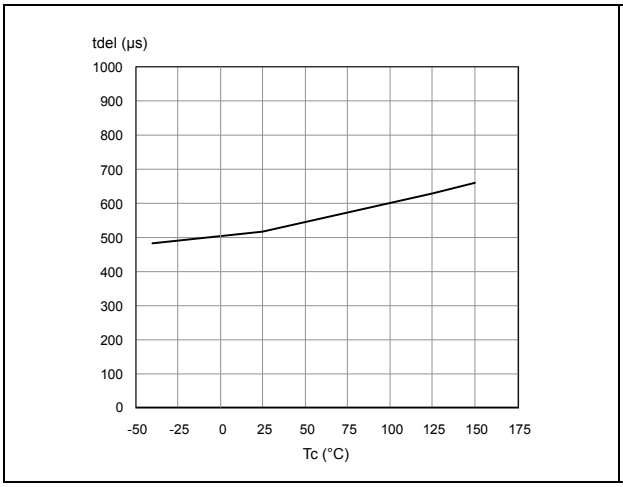


Figure 17. Enable clamp voltage

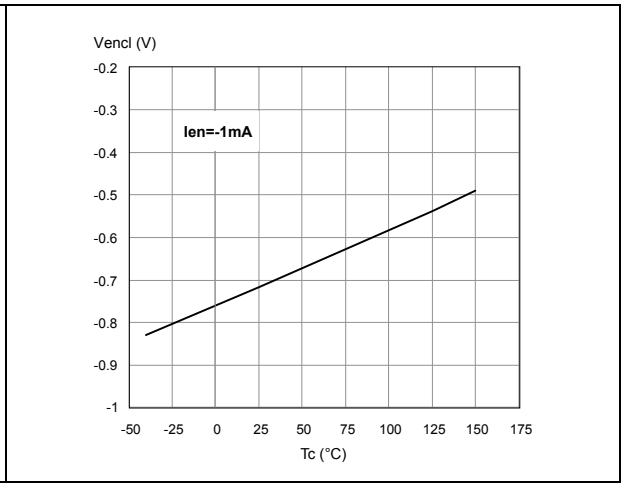


Figure 18. High level enable voltage

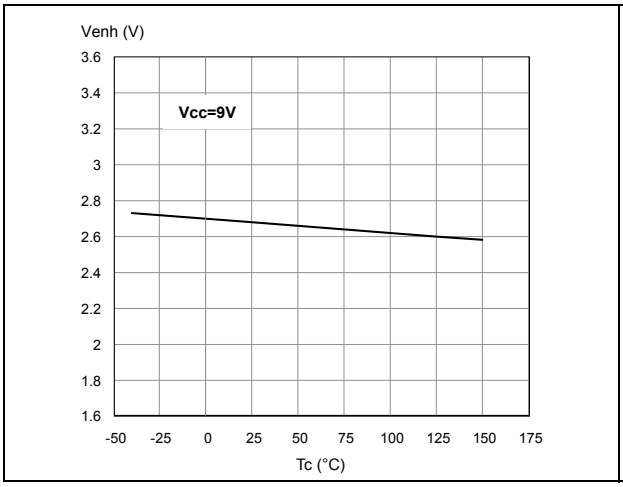


Figure 19. Low level enable voltage

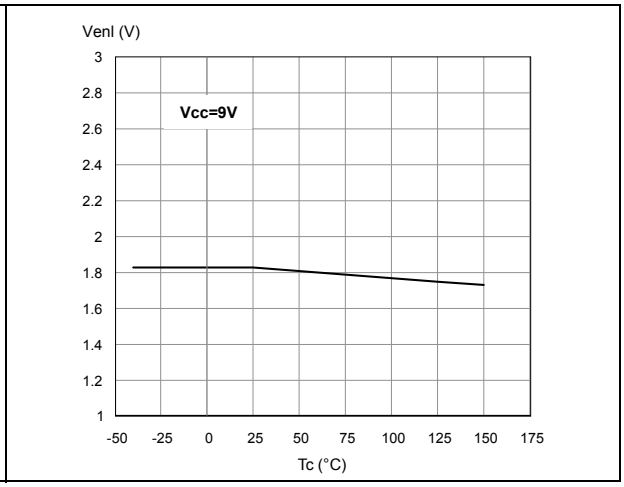


Figure 20. PWM high level voltage

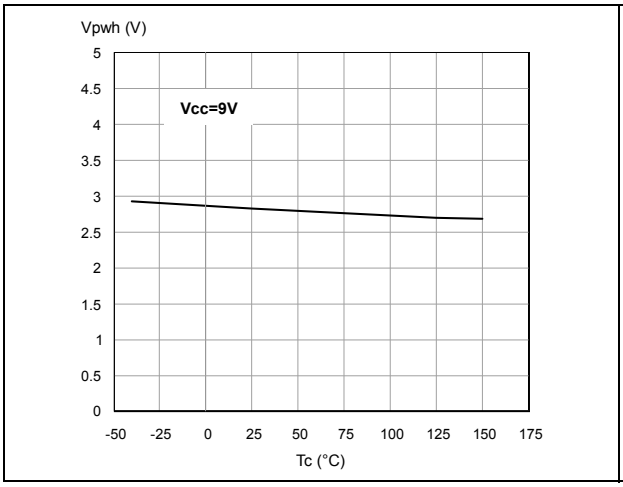


Figure 21. PWM low level voltage

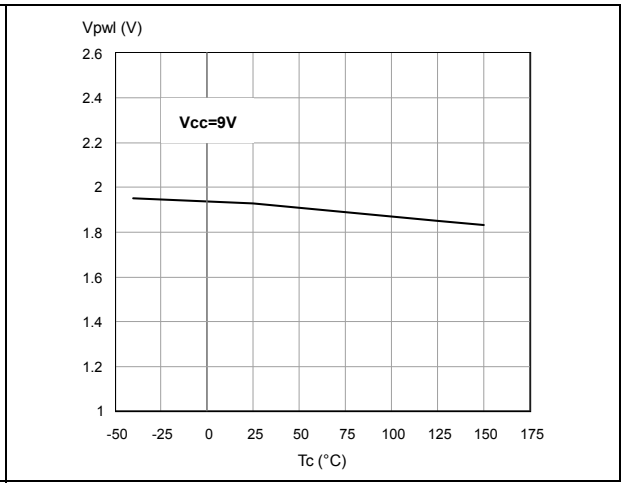


Figure 22. PWM high level current

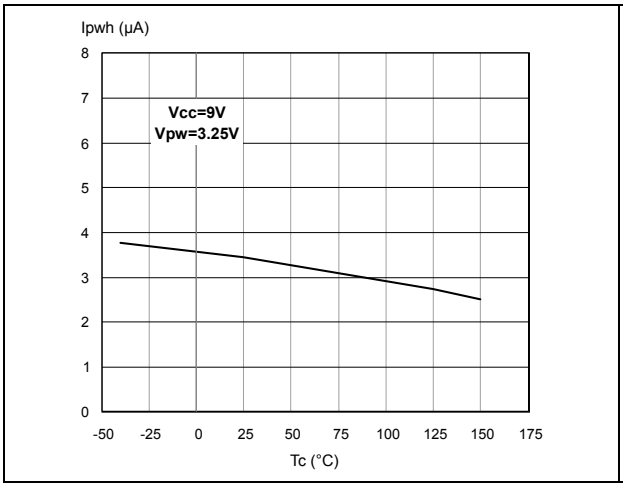


Figure 23. Overvoltage shutdown

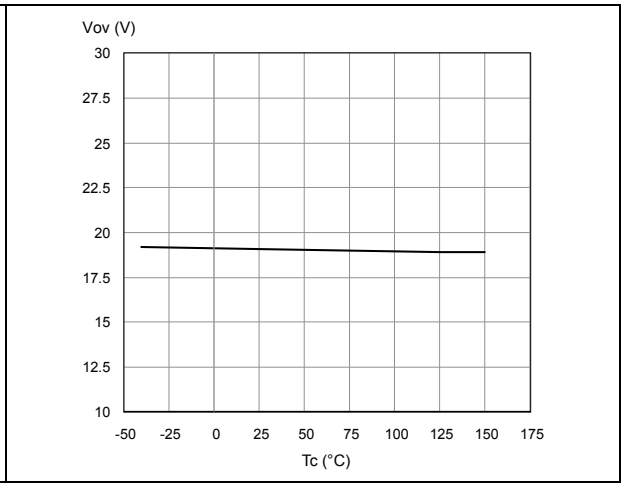


Figure 24. Undervoltage shutdown

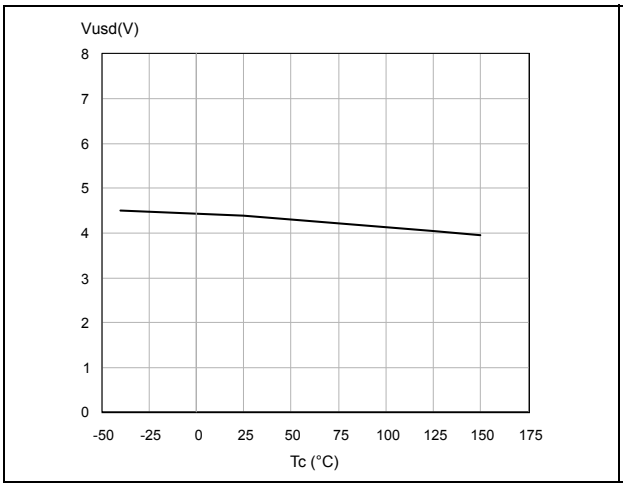


Figure 25. Current limitation

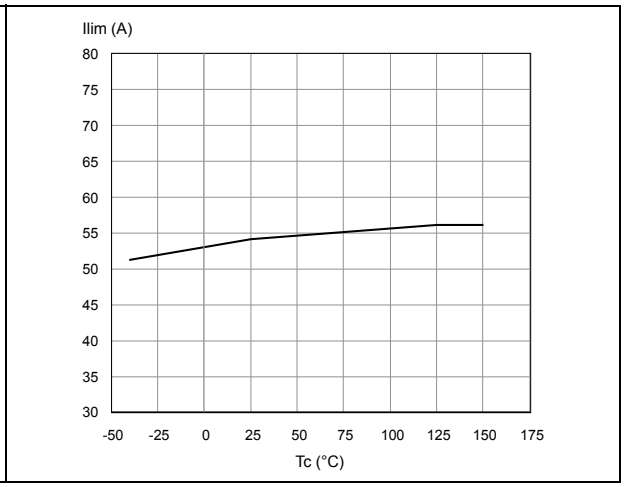


Figure 26. On state high side resistance vs T_{case}

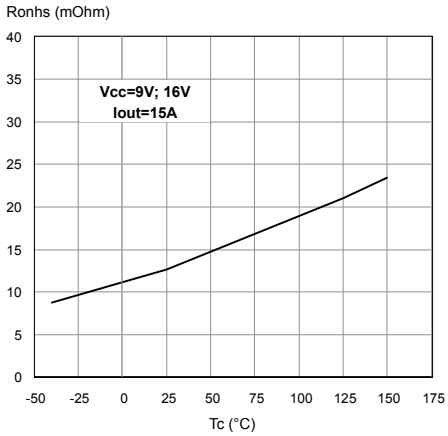


Figure 27. On state low side resistance vs T_{case}

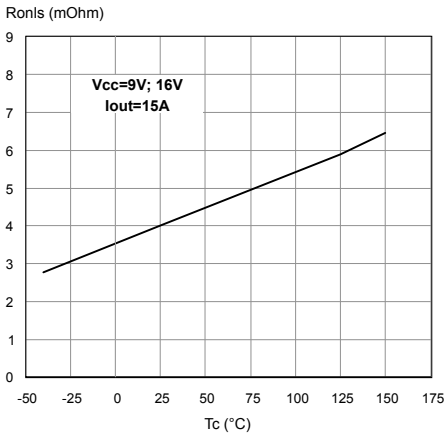


Figure 28. Turn-on delay time

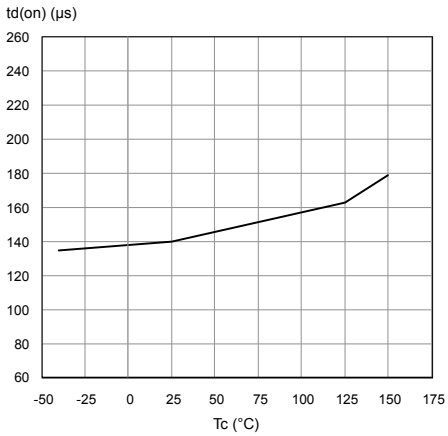


Figure 29. Turn-off delay time

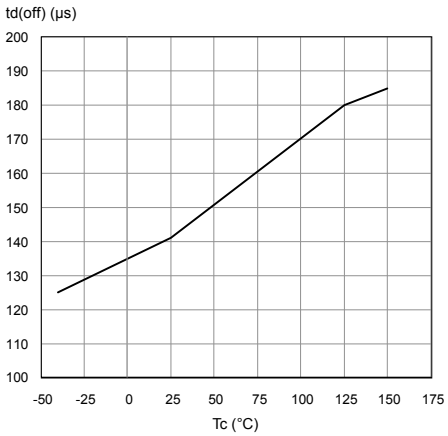


Figure 30. Output voltage rise time

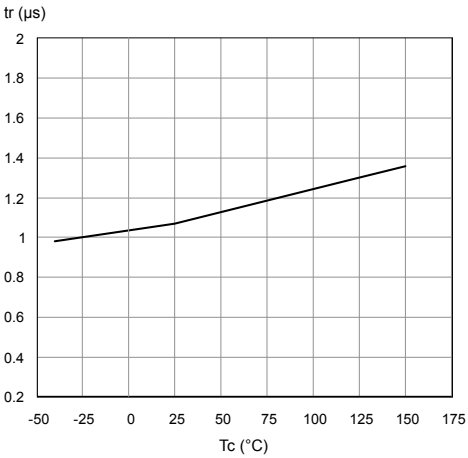
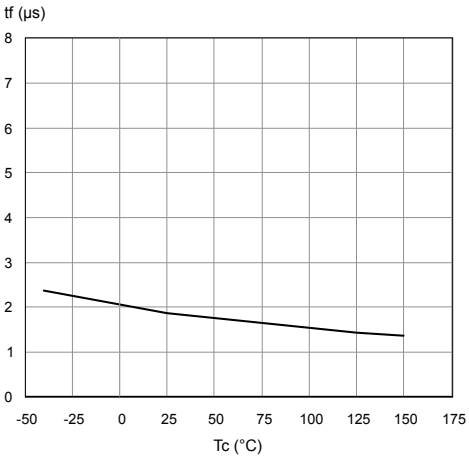


Figure 31. Output voltage fall time

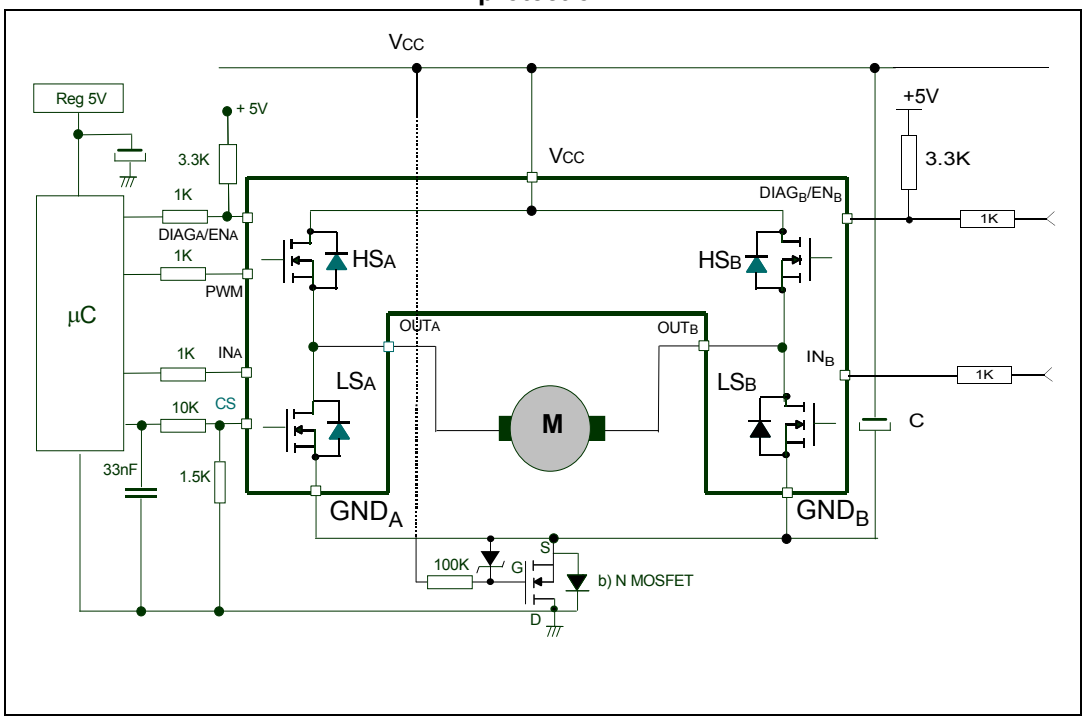


3 Application information

In normal operating conditions the $DIAG_X/EN_X$ pin is considered as an input pin by the device. This pin must be externally pulled high.

PWM pin usage: in all cases, a “0” on the PWM pin will turn off both LS_A and LS_B switches. When PWM rises back to “1”, LS_A or LS_B turn on again depending on the input pin state.

Figure 32. Typical application circuit for DC to 20 kHz PWM operation short-circuit protection



Note: The value of the blocking capacitor (C) depends on the application conditions and defines the voltage and current ripple on the supply line at PWM operation. Stored energy from the motor inductance may fly back into the blocking capacitor if the bridge driver goes into tri-state. This causes a hazardous overvoltage if the capacitor is not large enough. As a basic guideline, 500 µF per 10 A load current is recommended.

In case of a fault condition, the $DIAG_X/EN_X$ pin is considered an output pin by the device.The fault conditions are:

- overtemperature on one or both high sides
- short to battery condition on the output (saturation detection on the low side power MOSFET)

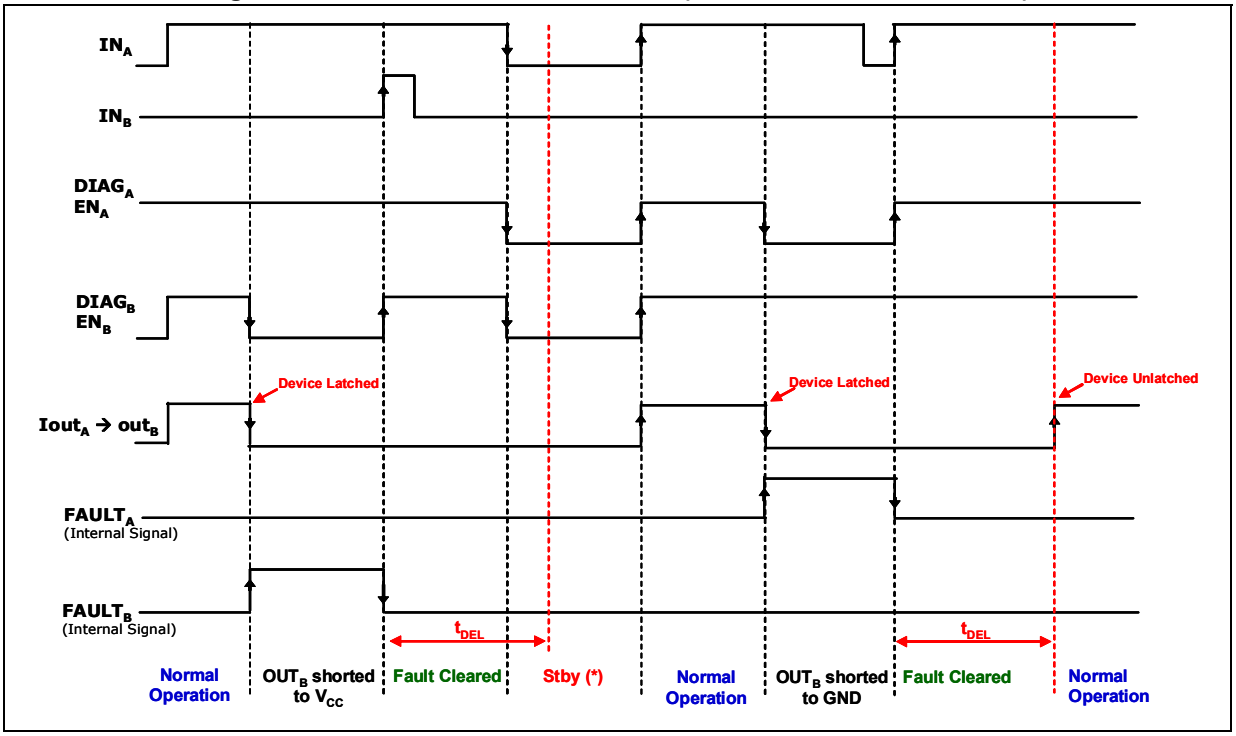
Possible origins of fault conditions may be:

- OUT_A is shorted to ground ⟶ overtemperature detection on high side A.
- OUT_A is shorted to V_{CC} ⟶ low side power MOSFET saturation detection.

When a fault condition is detected, the user can be informed of which power element is in fault by monitoring the IN_A, IN_B, $DIAG_A/EN_A$ and $DIAG_B/EN_B$ pins.

In any case, when a fault is detected, the faulty leg of the bridge is latched off. To turn on the respective output (OUT_X) again, the input signal must rise from low to high level.

Figure 33. Behavior in fault condition (how a fault can be cleared)



Note: In case of the fault condition is not removed, the procedure for unlatching and sending the device into Stby mode is:

- Clear the fault in the device (toggle : INA if ENA=0 or INB if ENB=0)

- Pull low all inputs, PWM and Diag/EN pins within tDEL.

If the Diag/En pins are already low, PWM=0, the fault can be cleared simply toggling the input. The device will enter Stby mode as soon as the fault is cleared.

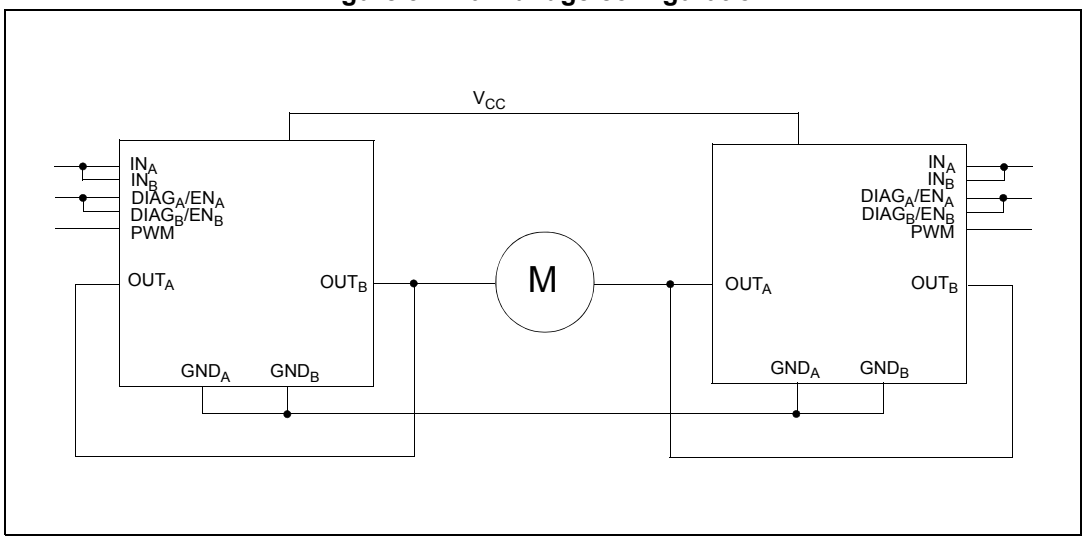
3.1 Reverse battery protection

Three possible solutions can be considered:

1. a Schottky diode D connected to V_{CC} pin
2. an N-channel MOSFET connected to the GND pin (see *Figure 32: Typical application circuit for DC to 20 kHz PWM operation short-circuit protection on page 21*)
3. a P-channel MOSFET connected to the V_{CC} pin

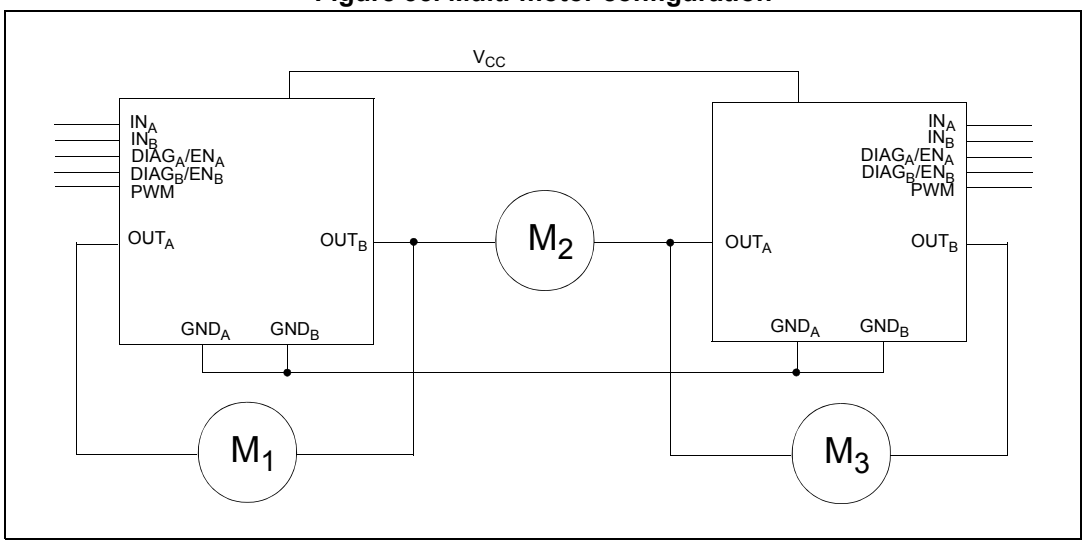
The device sustains no more than -30 A in reverse battery conditions because of the two body diodes of the power MOSFETs. Additionally, in reverse battery condition the I/Os of the VNH2SP30-E are pulled down to the V_{CC} line (approximately -1.5 V). A series resistor must be inserted to limit the current sunk from the microcontroller I/Os. If I_{Rmax} is the maximum target reverse current through µC I/Os, the series resistor is:

Figure 34. Half-bridge configuration



Note: The VNH2SP30-E can be used as a high power half-bridge driver achieving an On resistance per leg of 9.5 mΩ.

Figure 35. Multi-motor configuration



Note: The VNH2SP30-E can easily be designed in multi-motor driving applications such as seat positioning systems where only one motor must be driven at a time. The $DIAG_X/EN_X$ pins allow the unused half-bridges to be put into high impedance.

Figure 36. Waveforms in full bridge operation

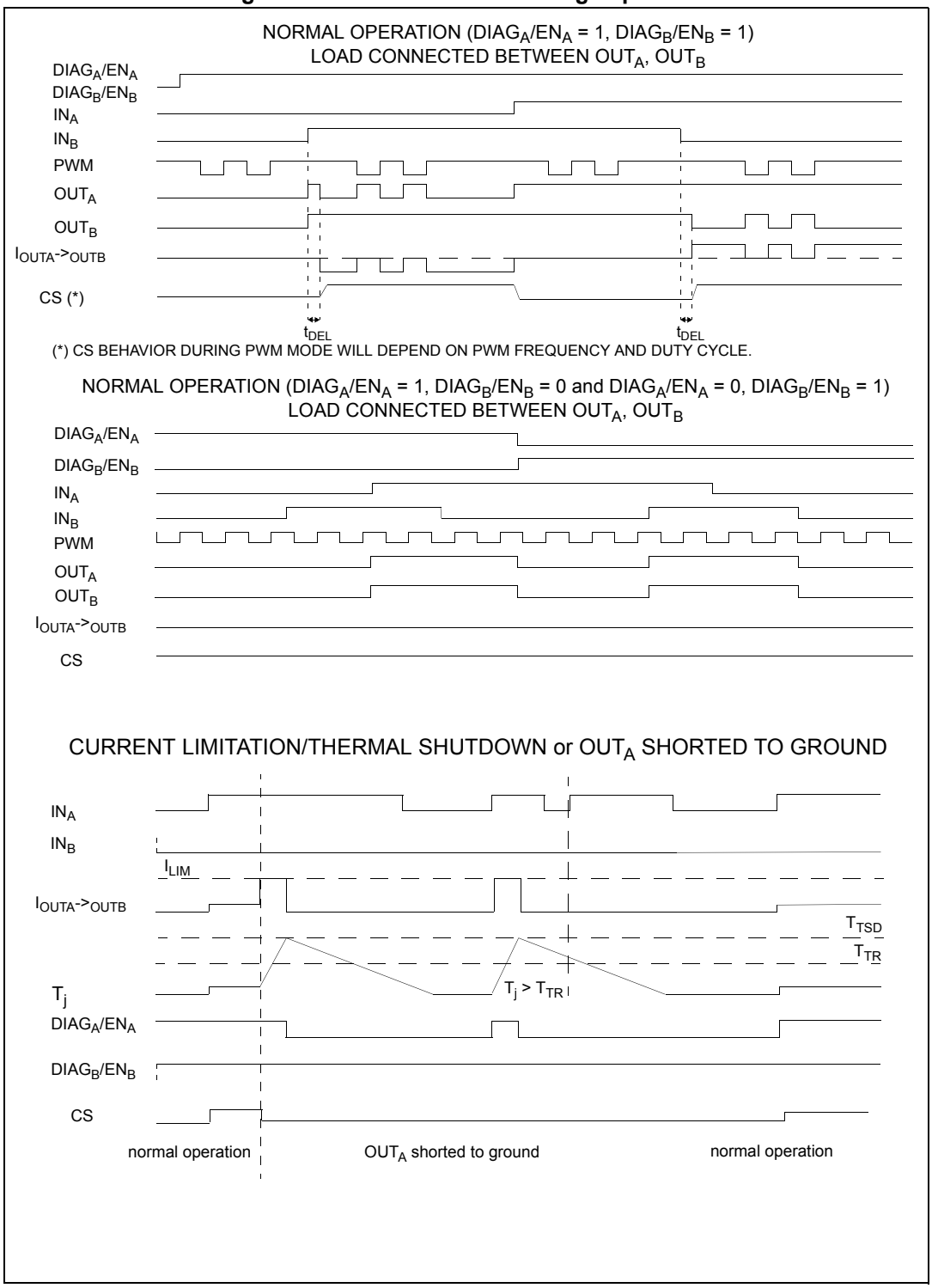


Figure 37. Waveforms in full bridge operation (continued)