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VNQ5050AK-E

Quad channel high side driver with analog current sense for automotive applications

Features

Parameters	Symbol	Value
Max supply voltage	V_{CC}	41 V
Operating voltage range	V_{CC}	4.5 to 36 V
Max on-state resistance (per ch.)	R_{ON}	50 mΩ
Current limitation (typ)	I_{LIMH}	19 A
Off-state supply current	I_S	2 µA(1)

1. Typical value with all loads connected.

- General features:
  - Inrush current active management by power limitation
  - Very low standby current
  - 3.0V CMOS compatible input
  - Optimized electromagnetic emission
  - Very low electromagnetic susceptibility
  - In compliance with the 2002/95/EC European directive
- Diagnostic functions:
  - Proportional load current sense
  - High current sense precision for wide current range
  - Current sense disable
  - Thermal shutdown indication
  - Very low current sense leakage
- Protection:
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of V_{CC}
  - Thermal shutdown


PowerSSO-24

  - Reverse battery protection (see *Figure 25*)
  - Electrostatic discharge protection

Application

- All types of resistive, inductive and capacitive loads.
- Suitable as LED driver.

Description

The VNQ5050AK-E is a monolithic device made using STMicroelectronics VIPower M0-5 technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

This device integrates an analog current sense which delivers a current proportional to the load current (according to a known ratio) when CS_DIS is driven low or left open. When CS_DIS is driven high, the CURRENT SENSE pin is in a high impedance condition.

Output current limitation protects the device in overload condition. In case of long overload duration, the device limits the dissipated power to a safe level up to thermal shutdown intervention. Thermal shutdown with automatic restart allows the device to recover normal operation as soon as the fault condition disappears.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and Reel
PowerSSO-24	VNQ5050AK-E	VNQ5050AKTR-E

Contents

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List of figures

1 Block diagram and pin configuration

Figure 1. Block diagram

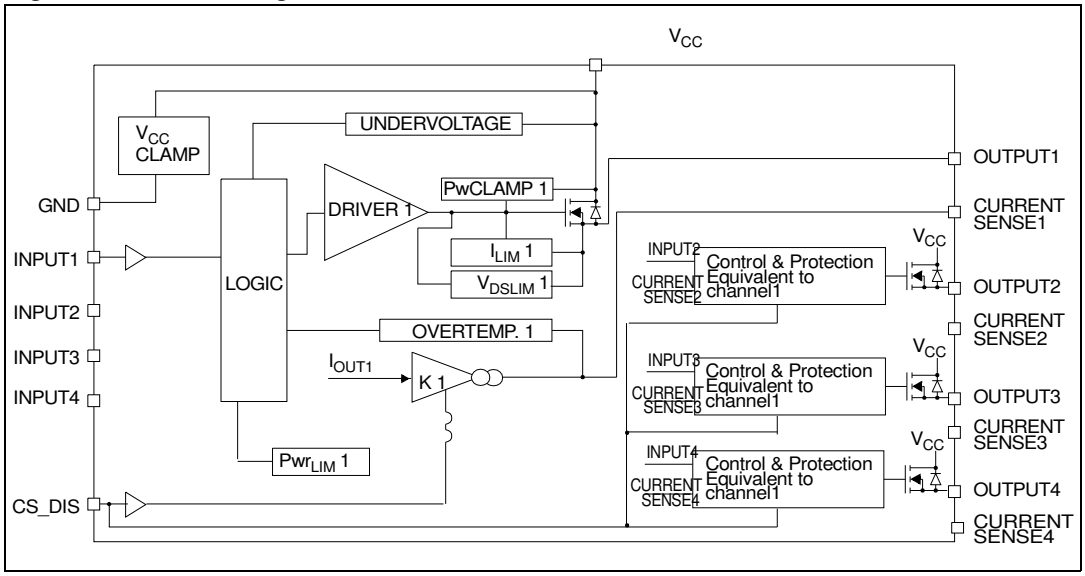


Table 2. Pin functions

Name	Function
V_{CC}	Battery connection
$OUTPUT_n$	Power output
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network
$INPUT_n$	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state
$CURRENT\ SENSE_n$	Analog current sense pin, delivers a current proportional to the load current
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin

Figure 2. Configuration diagram (top view)

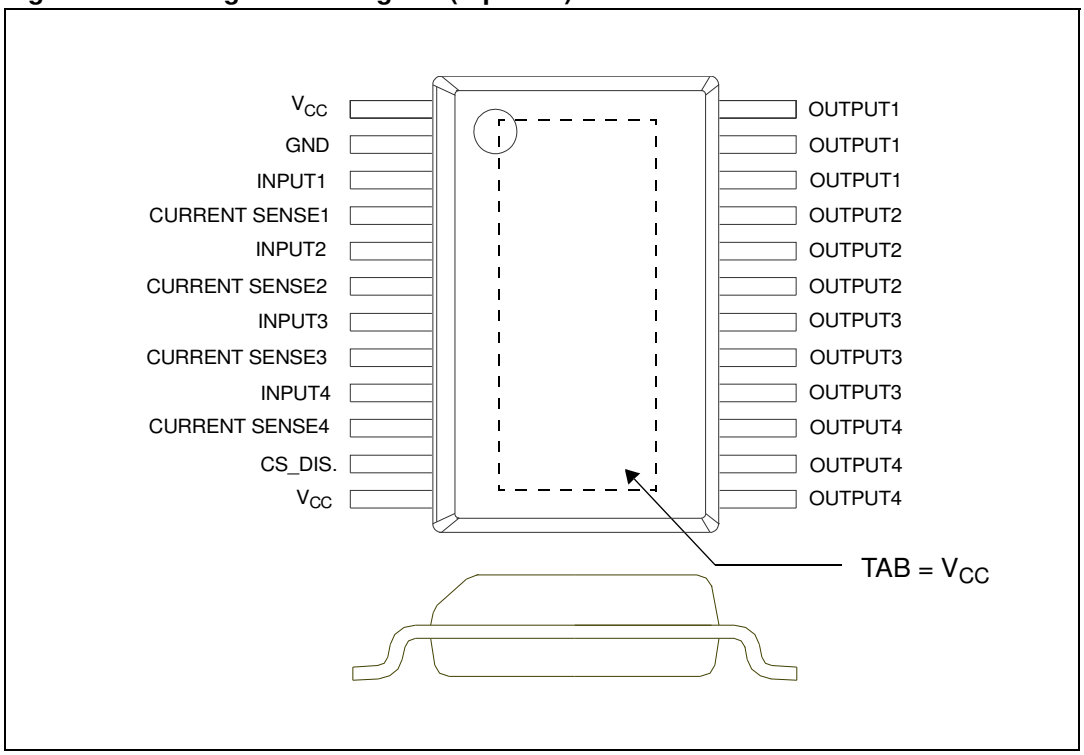


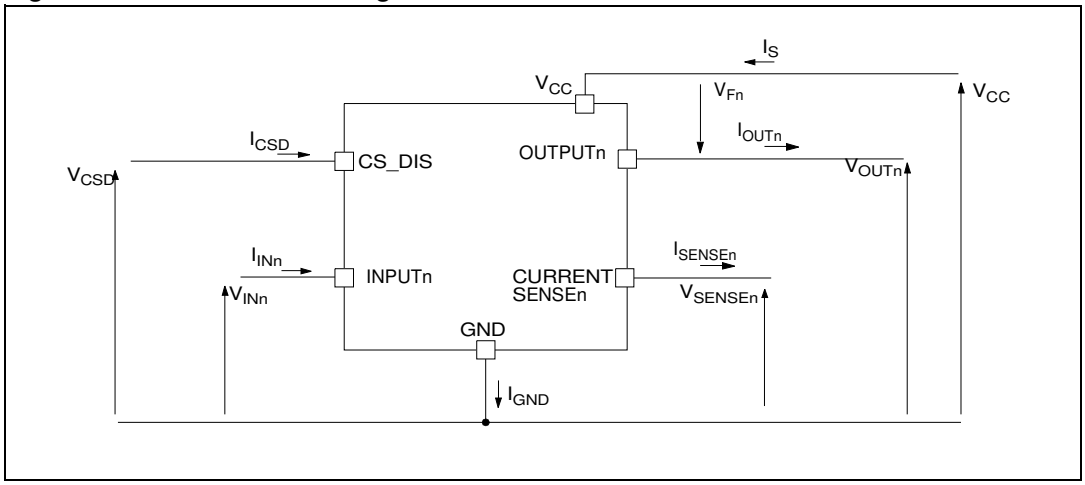
Table 3. Suggested connections for unused and not connected pins

Connection/pin	Current sense	N.C.	Output	Input	CS_DIS
Floating	N.R.(1)	X	X	X	X
To ground	Through 1 kΩ resistor	X	N.R.	Through 10 kΩ resistor	Through 10 kΩ resistor

1. Not recommended.

2 Electrical specifications

Figure 3. Current and voltage conventions



Note: $V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stress values that exceed those listed in the “Absolute maximum ratings” table can cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions greater than those, indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics sure program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$- I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$- I_{OUT}$	Reverse DC output current	20	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
$-I_{CSENSE}$	DC reverse CS pin current	200	mA
V_{CSENSE}	Current sense maximum voltage	V_{CC}-41 $+V_{CC}$	V V
E_{MAX}	Maximum switching energy (single pulse) (L=3 mH; R_L=0 Ω; V_{bat}=13.5 V; T_{jstart}=150 ºC; I_{OUT} = I_{limL}(Typ.))	104	mJ

Table 4. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{ESD}	Electrostatic discharge (human body model: R=1.5KΩ; C=100pF) – Input – Current sense – CS_DIS – Output – V_{CC}	 4000 2000 4000 5000 5000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Max value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case (With one channel ON)	2.8	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	See *Figure 29*	°C/W

2.3 Electrical characteristics

Values specified in this section are for 8 V<V_{CC}<36 V, -40 °C<T_j<150 °C, unless otherwise stated.

Table 6. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	36	V
V_{USD}	Undervoltage shutdown		-	3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis		-	0.5	-	V
R_{ON}	On-state resistance	I_{OUT}=2 A; T_j=25 °C I_{OUT}=2 A; T_j=150 °C I_{OUT}=2 A; V_{CC}=5 V; T_j=25 °C	-	-	50 100 65	mΩ mΩ mΩ
V_{clamp}	Clamp voltage	I_S=20 mA	41	46	52	V
I_S	Supply current	Off-State; V_{CC}=13 V; T_j=25 °C; V_{IN}=V_{OUT}=V_{SENSE}=V_{CSD}=0 V On-State; V_{CC}=13 V; V_{IN}=5 V; I_{OUT}=0 A	-	2(1) 8	5(1) 14	µA mA
$I_{L(off)}$	Off-state output current(2)	V_{IN}=V_{OUT}=0 V; V_{CC}=13 V; T_j=25 °C V_{IN}=V_{OUT}=0 V; V_{CC}=13 V; T_j=125 °C	0 0	0.01	3 5	µA
V_F	Output - V_{CC} diode voltage(2)	-I_{OUT}=2 A; T_j=150 °C	-	-	0.7	V

1. PowerMOS leakage included.
2. For each channel.

Table 7. Switching (V_{CC}=13V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L= 6.5 Ω (see *Figure 6*)	-	20	-	µs
$t_{d(off)}$	Turn-off delay time	R_L= 6.5 Ω (see *Figure 6*)	-	45	-	µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	R_L= 6.5 Ω	-	See *Figure 19*	-	V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	R_L= 6.5 Ω	-	See *Figure 21*	-	V/µs
W_{ON}	Switching energy losses during t_{won}	R_L= 6.5 Ω (see *Figure 6*)	-	0.15	-	mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L= 6.5 Ω (see *Figure 6*)	-	0.3	-	mJ

Table 8. Current sense (8V<V_{CC}<16V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT}= 0.05 A; V_{SENSE}= 0.5 V; V_{CSD}=0 V; T_j= -40 °C...150 °C	1340	2420	3460	
K_1	I_{OUT}/I_{SENSE}	I_{OUT}= 1 A; V_{SENSE}= 0.5 V; V_{CSD}=0 V; T_j= -40 °C...150 °C T_j= 25 °C...150 °C	1370 1510	1860 1860	2510 2210	
dK_1/K_1 (1)	Current sense ratio drift	I_{OUT}= 1 A; V_{SENSE}= 0.5 V; V_{CSD}= 0 V; T_J= -40 °C to 150 °C	-10	-	10	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT}= 2 A; V_{SENSE}= 4 V; V_{CSD}= 0 V; T_j= -40 °C...150 °C T_j= 25 °C...150 °C	1590 1600	1760 1760	2140 1930	
dK_2/K_2 (1)	Current sense ratio drift	I_{OUT}= 2 A; V_{SENSE}= 4 V; V_{CSD}= 0 V; T_J= -40 °C to 150 °C	-8	-	8	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT}= 4 A; V_{SENSE}= 4 V; V_{CSD}= 0 V; T_j= -40 °C...150 °C T_j= 25 °C...150 °C	1650 1650	1740 1740	1950 1830	-
dK_3/K_3 (1)	Current sense ratio drift	I_{OUT}= 4 A; V_{SENSE}= 4 V; V_{CSD}= 0 V; T_J= -40 °C to 150 °C	-5	-	5	%
I_{SENSE0}	Analog sense leakage current	I_{OUT}= 0 A; V_{SENSE}= 0 V; V_{CSD}= 5 V; V_{IN}= 0 V; T_j= -40 °C...150 °C V_{CSD}= 0 V; V_{IN}= 5 V; T_j= -40 °C...150 °C I_{OUT}= 2 A; V_{SENSE}= 0 V; V_{CSD}= 5 V; V_{IN}= 5 V; T_j= -40 °C...150 °C	0 0 0	- - -	1 2 1	µA µA µA
I_{OL}	Openload ON state current detection threshold	V_{IN} = 5 V, I_{SENSE}= 5 µA	4	-	20	mA
V_{SENSE}	Max analog sense output voltage	I_{OUT}= 4 A; V_{CSD}= 0 V	5	-	-	V
V_{SENSEH}	Analog sense output voltage in over temperature condition	V_{CC}= 13 V; R_{SENSE}= 10 KΩ	-	9	-	V

Table 8. Current sense (8V<V_{CC}<16V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SENSEH}	Analog sense output current in over temperature condition	V_{CC}= 13 V; V_{SENSE}= 5 V	-	8	-	mA
$t_{DSENSE1H}$	Delay response time from falling edge of CS_DIS pin	V_{SENSE}<4 V, 0.5 A<Iout<4 A I_{SENSE}= 90 % of $I_{SENSE\ max}$ (see *Figure 4*)	-	50	100	µs
$t_{DSENSE1L}$	Delay response time from rising edge of CS_DIS pin	V_{SENSE}<4 V, 0.5 A<Iout<4 A I_{SENSE}=10 % of $I_{SENSE\ max}$ (see *Figure 4*)	-	5	20	µs
$t_{DSENSE2H}$	Delay response time from rising edge of INPUT pin	V_{SENSE}<4 V, 0.5 A<Iout<4 A I_{SENSE}=90 % of $I_{SENSE\ max}$ (see *Figure 4*)	-	80	250	µs
$\Delta t_{DSENSE2H}$	Delay response time between rising edge of output current and rising edge of current sense	V_{SENSE}<4 V, I_{SENSE} =90 % of $I_{SENSEMAX}$, I_{OUT}=90 % of I_{OUTMAX} I_{OUTMAX}=2 A (see *Figure 5*)	-	-	65	µs
$t_{DSENSE2L}$	Delay response time from falling edge of INPUT pin	V_{SENSE}<4 V, 0.5 A<Iout<4 A I_{SENSE}=10 % of $I_{SENSE\ max}$ (see *Figure 4*)	-	100	250	µs

1. Parameter guaranteed by design; it is not tested.

Table 9. Protection(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	V_{CC}=13 V 5 V<V_{CC}<36 V	13.5	19	26.5 26.5	A A
I_{limL}	Short circuit current during thermal cycling	V_{CC}=13 V; T_R<T_j<T_{TSD}	-	7	-	A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5	-	°C
T_{RS}	Thermal reset of STATUS		135	-	-	°C
T_{HYST}	Thermal hysteresis (T_{TSD}-T_R)		-	7	-	°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT}=2 A; V_{IN}=0; L=6 mH	V_{CC}-41	V_{CC}-46	V_{CC}-52	V
V_{ON}	Output voltage drop limitation	I_{OUT}=0.1 A; T_j=-40 °C...150 °C (see *Figure 9*)	-	25	-	mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 10. Logic input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage		-	-	0.9	V
I_{IL}	Low level input current	V_{IN}= 0.9 V	1	-	-	µA
V_{IH}	Input high level voltage		2.1	-	-	V
I_{IH}	High level input current	V_{IN}= 2.1 V	-	-	10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.25	-	-	V
V_{ICL}	Input clamp voltage	I_{IN}= 1 mA I_{IN}= -1 mA	5.5	 -0.7	7	V V
V_{CSDL}	CS_DIS low level voltage		-	-	0.9	V
I_{CSDL}	Low level CS_DIS current	V_{CSD}=0.9 V	1	-	-	µA
V_{CSDH}	CS_DIS high level voltage		2.1	-	-	V
I_{CSDH}	High level CS_DIS current	V_{CSD}=2.1 V	-	-	10	µA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25	-	-	V
V_{CSCL}	CS_DIS clamp voltage	I_{CSD}= 1 mA I_{CSD}= -1 mA	5.5	 -0.7	7	V V

Figure 4. Current sense delay characteristics

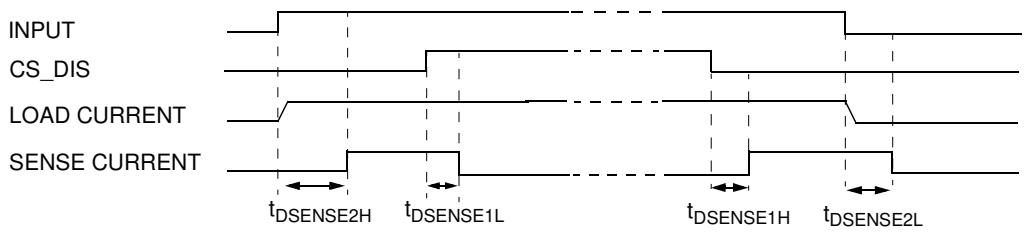


Figure 5. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

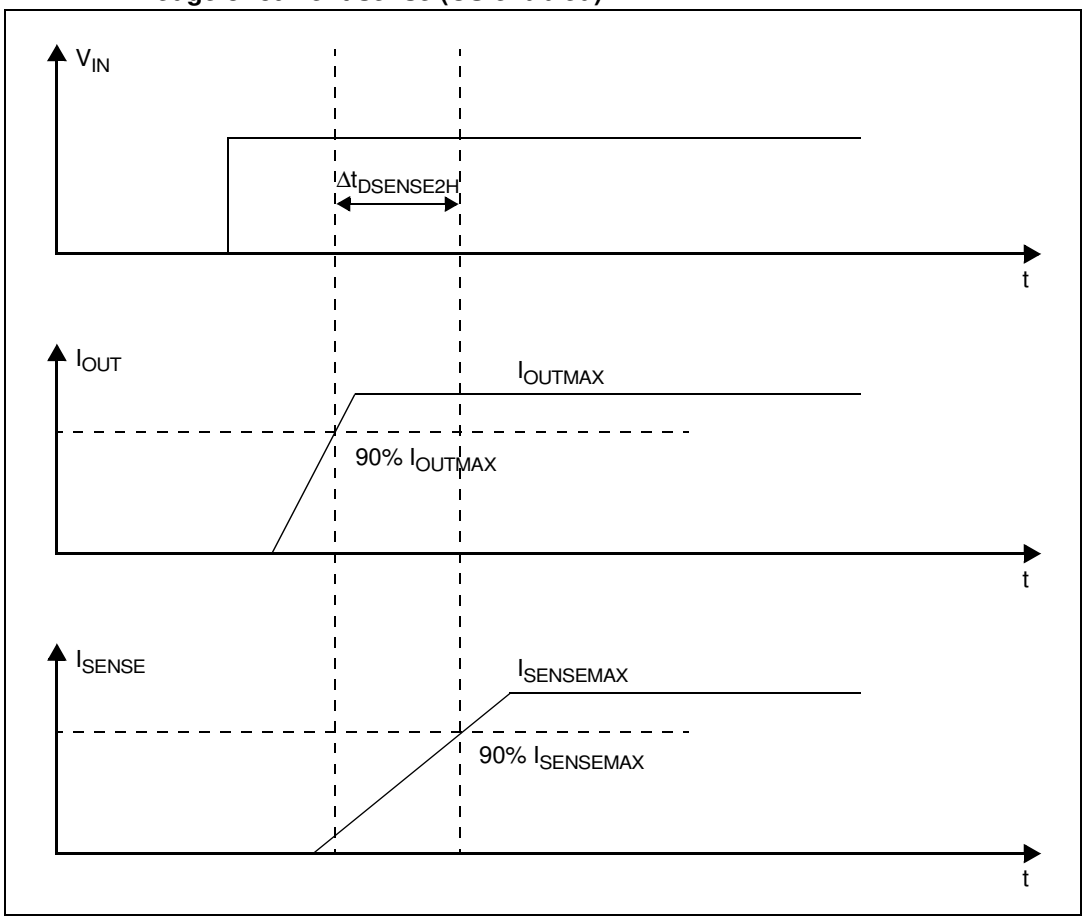


Figure 6. Switching characteristics

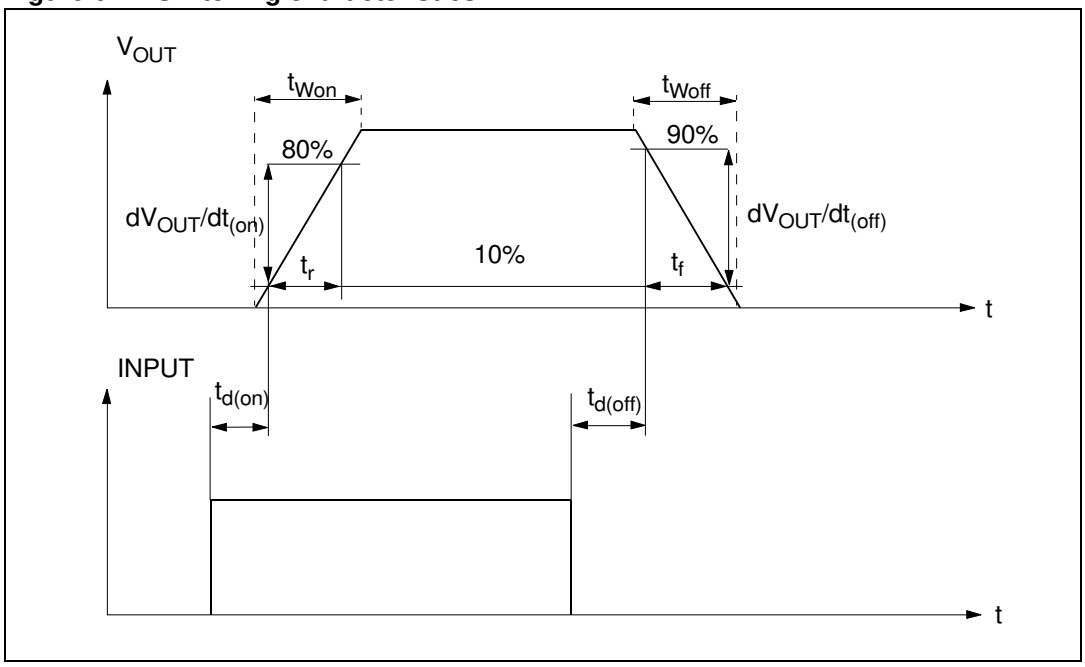


Figure 7. I_{OUT}/I_{SENSE} vs I_{OUT}

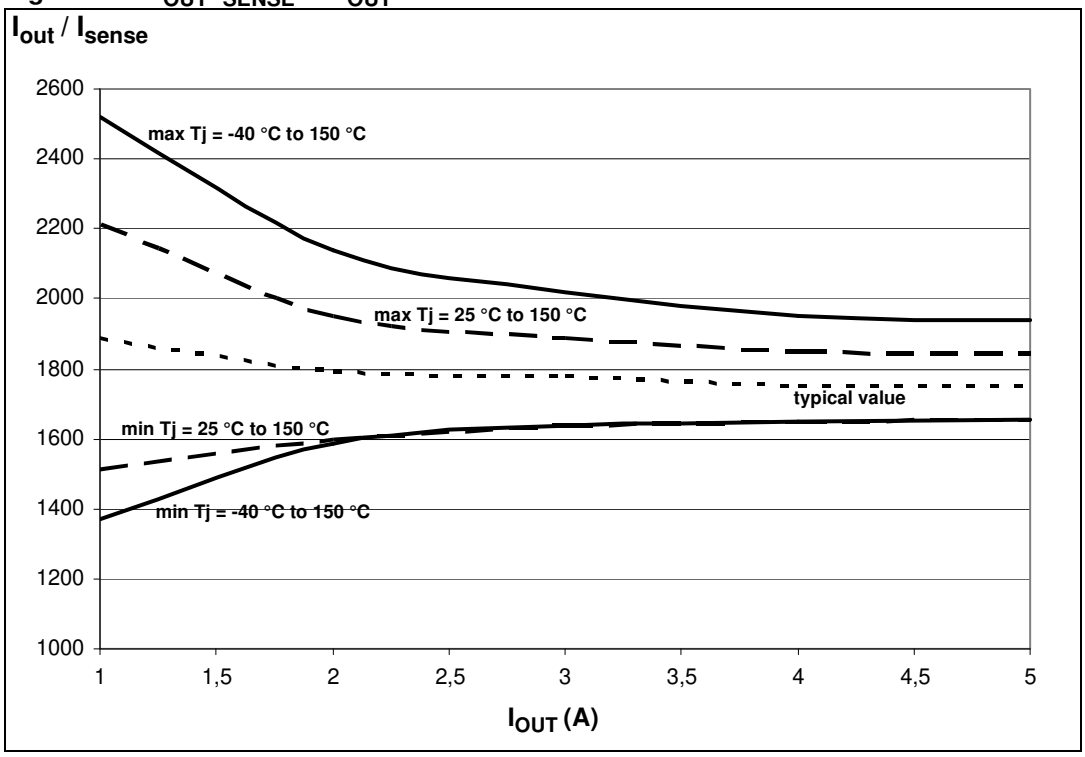
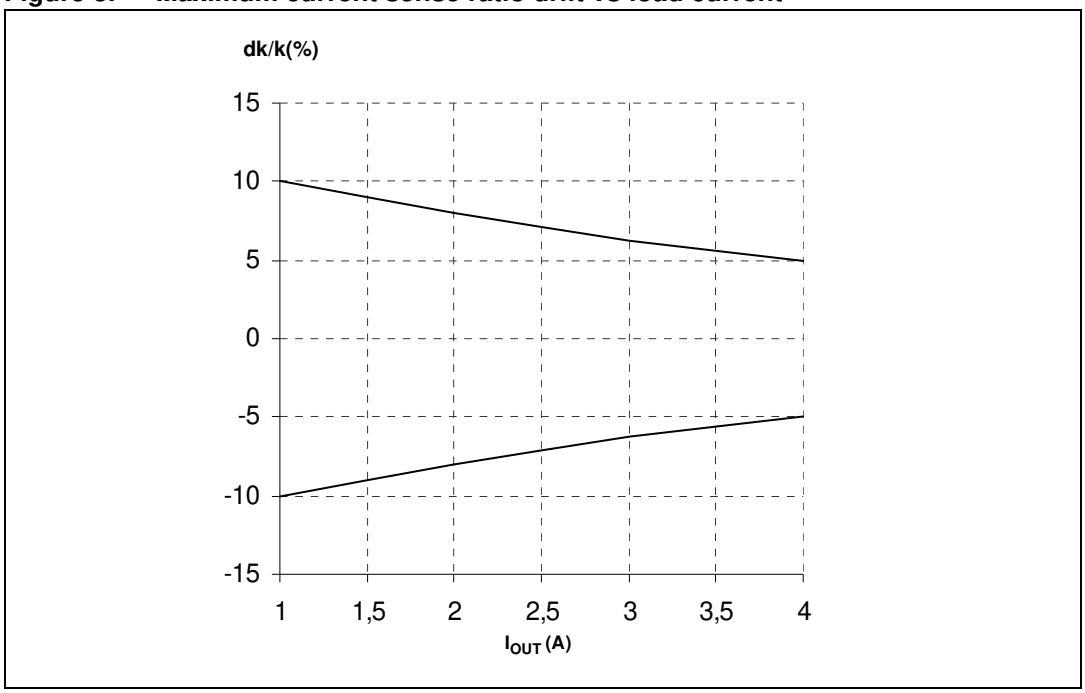


Figure 8. Maximum current sense ratio drift vs load current



Note: Parameter guaranteed by design; it is not tested.

Table 11. Truth table

Conditions	Input	Output	Sense (V_{CSD}=0 V)(1)
Normal operation	L H	L H	0 Nominal
Over temperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Short circuit to GND (Rsc ≤ 10 mΩ)	L H H	L L L	0 0 if $T_j < T_{TSD}$ V_{SENSEH} if $T_j > T_{TSD}$
Short circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

1. If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Figure 9. Output voltage drop limitation

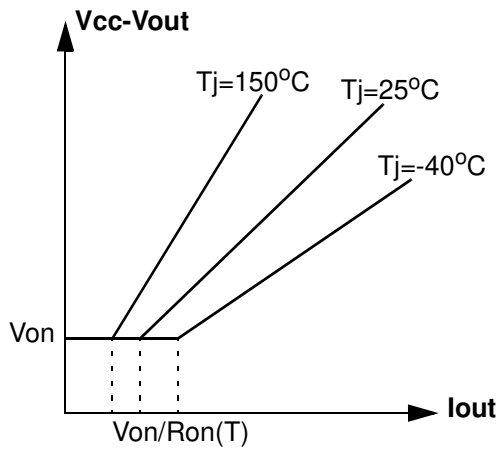


Table 12. Electrical transient requirements (part 1/3)

ISO 7637-2: 2004(E) test pulse	Test levels		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and Impedance
	III	IV				
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4	-6 V	-7 V	1 pulse	-		100 ms, 0.01 Ω
5b(2)	+65 V	+87 V	1 pulse	-		400 ms, 2 Ω

Table 13. Electrical transient requirements (part 2/3)

ISO 7637-2: 2004(E) test pulse	Test level results(1)	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b (2)	C	C

1. The above test levels must be considered referred to V_{CC} = 13.5V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 14. Electrical transient requirements (part 3/3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Electrical characteristics curves

Figure 10. Off-state output current

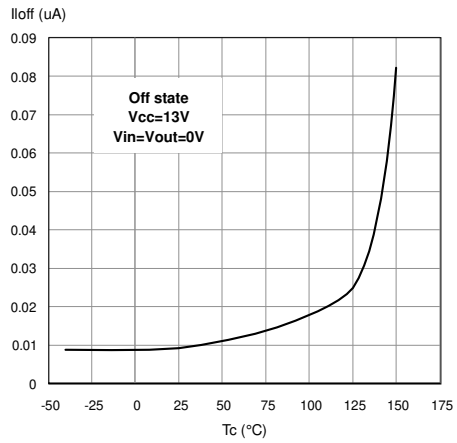


Figure 11. High level input current

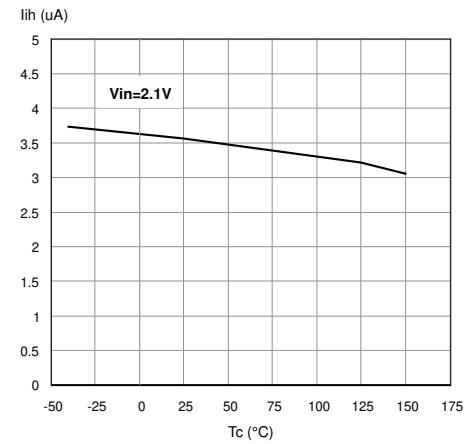


Figure 12. Input clamp voltage

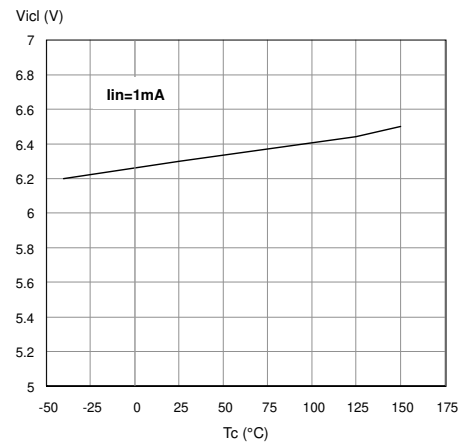


Figure 13. Input low level

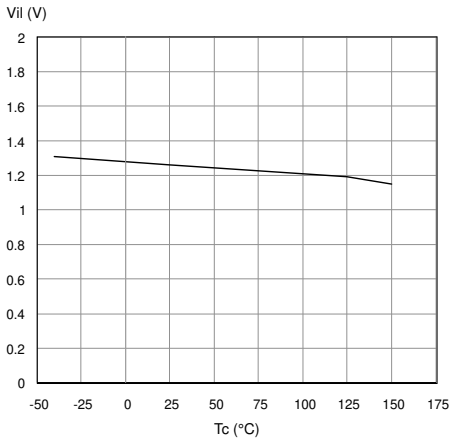


Figure 14. Input high level

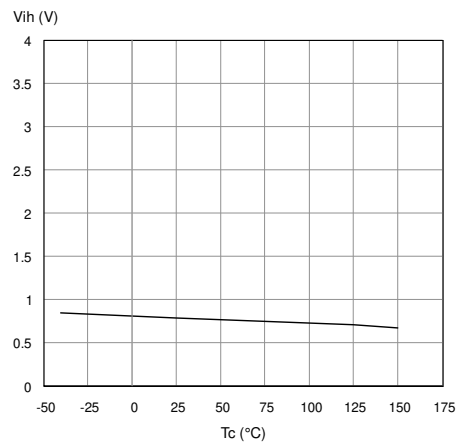


Figure 15. Input hysteresis voltage

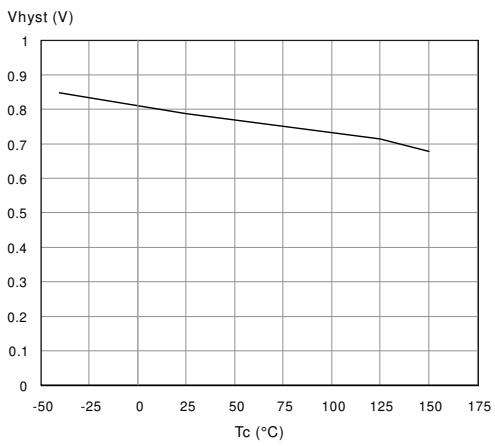


Figure 16. On-state resistance vs T_{case}

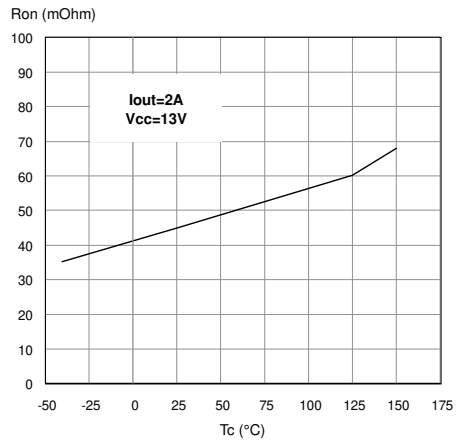


Figure 17. On-state resistance vs V_{CC}

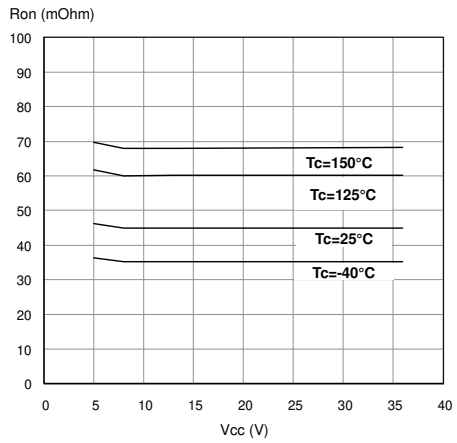


Figure 18. Undervoltage shutdown

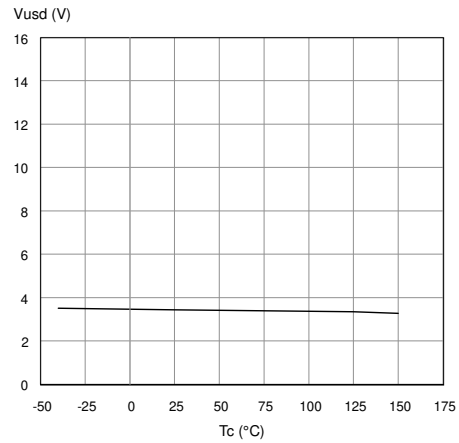


Figure 19. Turn-on voltage slope

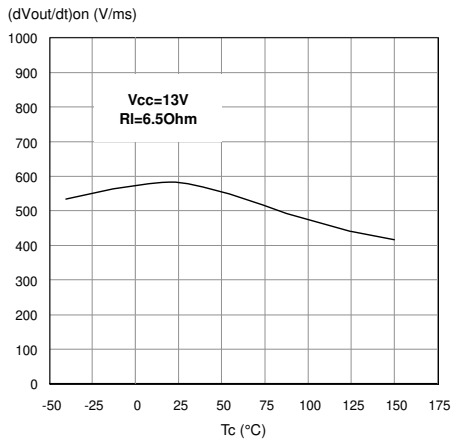


Figure 20. I_{LIMH} vs T_{case}

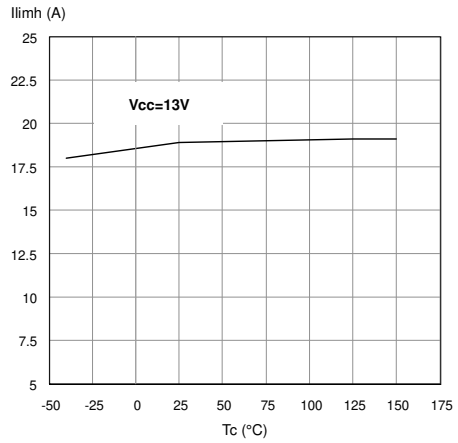


Figure 21. Turn-off voltage slope

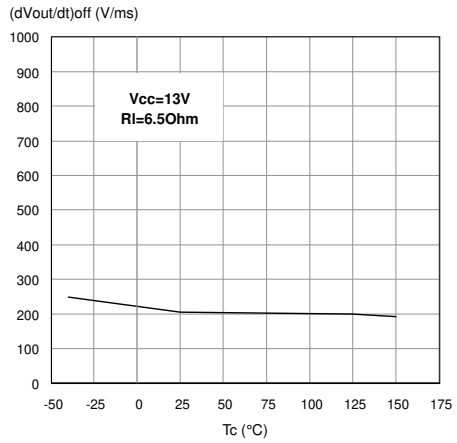


Figure 22. CS_DIS high level voltage

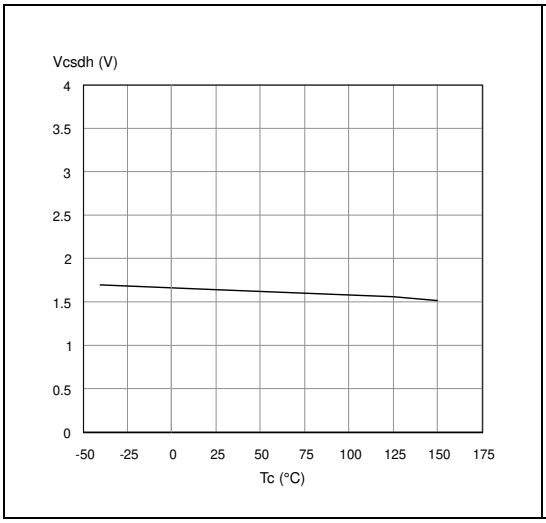


Figure 23. CS_DIS clamp voltage

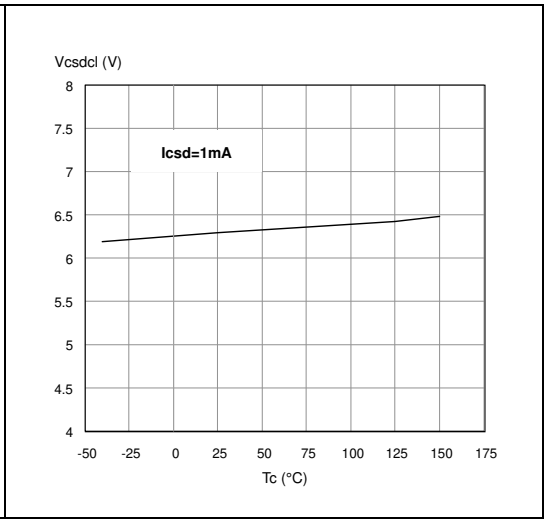
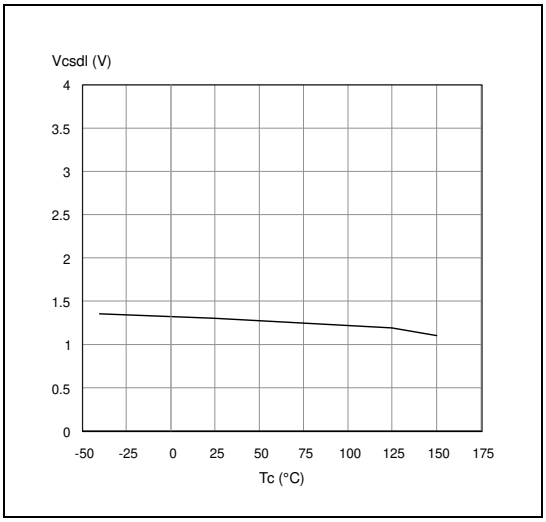
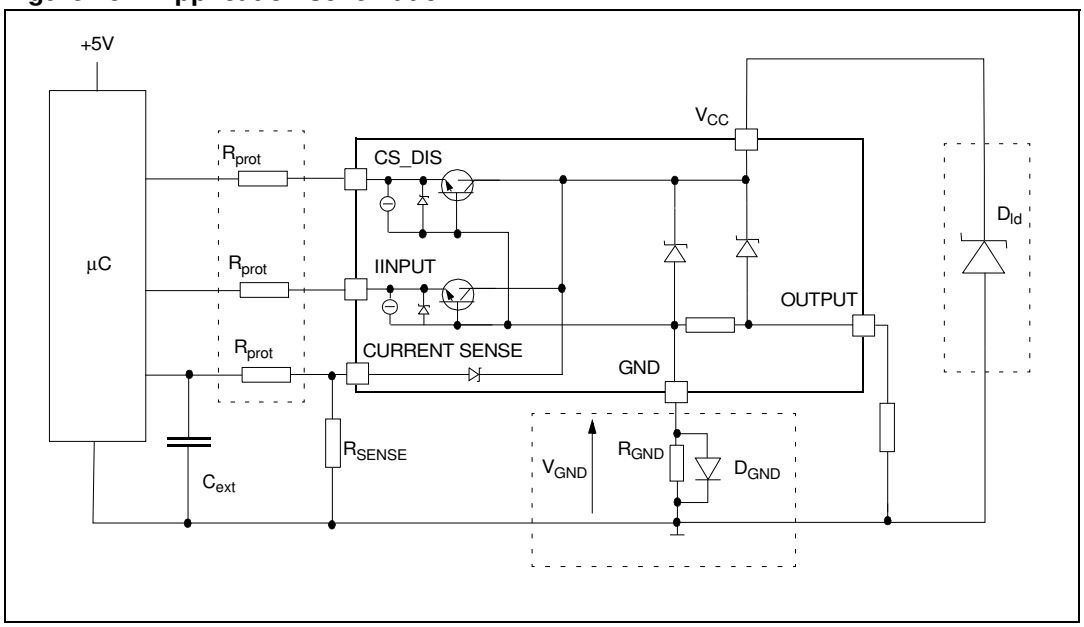


Figure 24. CS_DIS low level voltage



3 Application information

Figure 25. Application schematic



Note: Channel 2, 3, 4 have the same internal circuit as channel 1.

3.1 GND protection network against reverse battery

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600\ mV / (I_{S(on)max})$.
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when $V_{CC}<0$: during reverse battery situations) is:

$P_D= (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2: a diode (D_{GND}) in the ground line.

A resistor (R_{GND}= 1 kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift (≈600mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

3.3 Microcontroller I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$-V_{CCpeak}/I_{latchup} \le R_{prot} \le (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

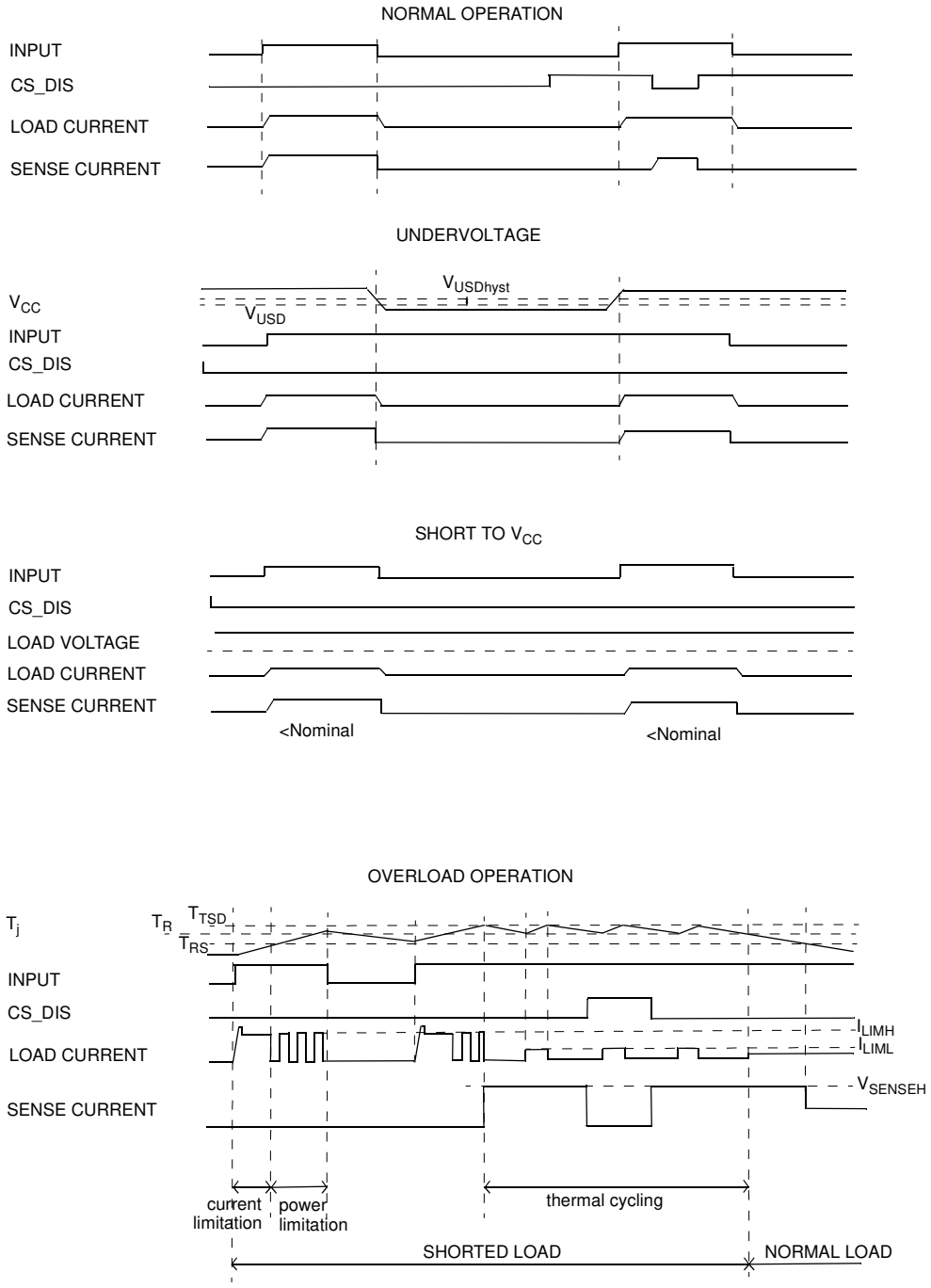
Calculation example:

For V_{CCpeak}= - 100 V and $I_{latchup} \ge$ 20 mA; $V_{OH\mu C} \ge$ 4.5 V

5 kΩ ≤ R_{prot} ≤ 180 kΩ.

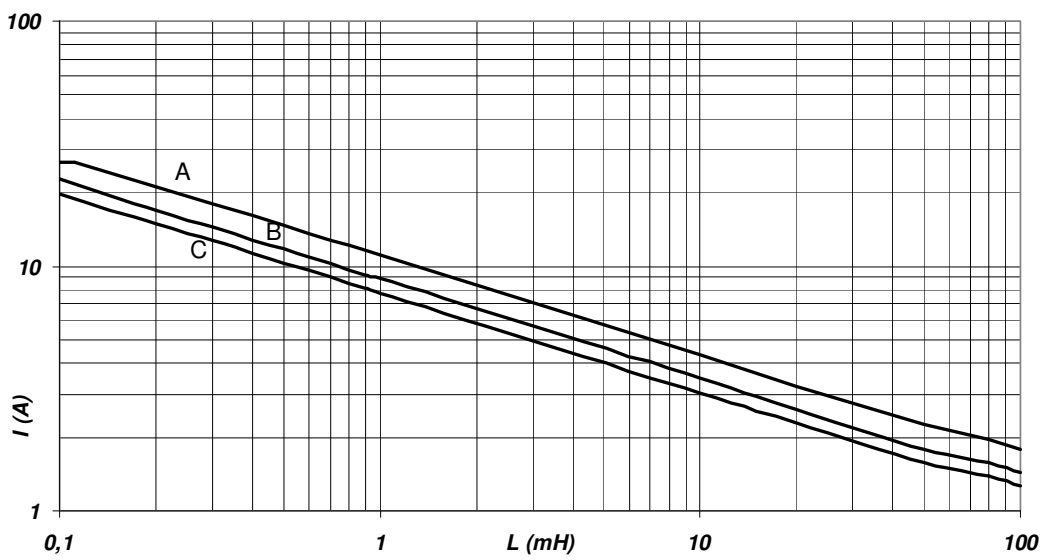
Recommended values: R_{prot} = 10 kΩ, C_{EXT}= 10 nF.

Figure 26. Waveforms

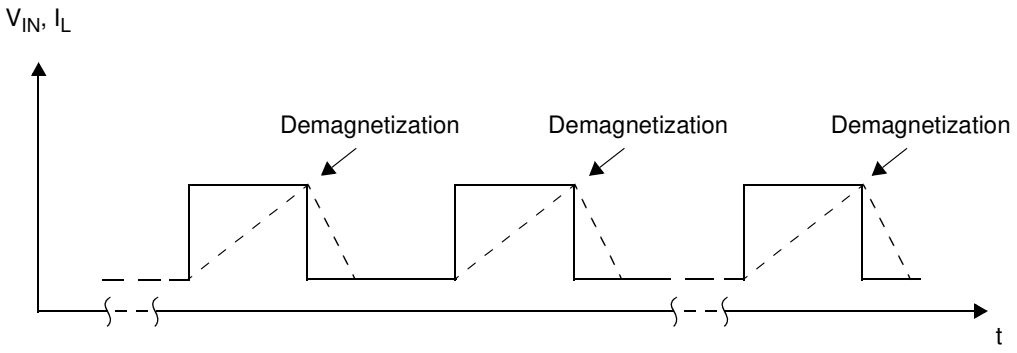


3.4 Maximum demagnetization energy (V_{CC} = 13.5V)

Figure 27. Maximum turn-off current versus inductance (for each channel)



A: T_{jstart} = 150°C single pulse
B: T_{jstart} = 100°C repetitive pulse
C: T_{jstart} = 125°C repetitive pulse



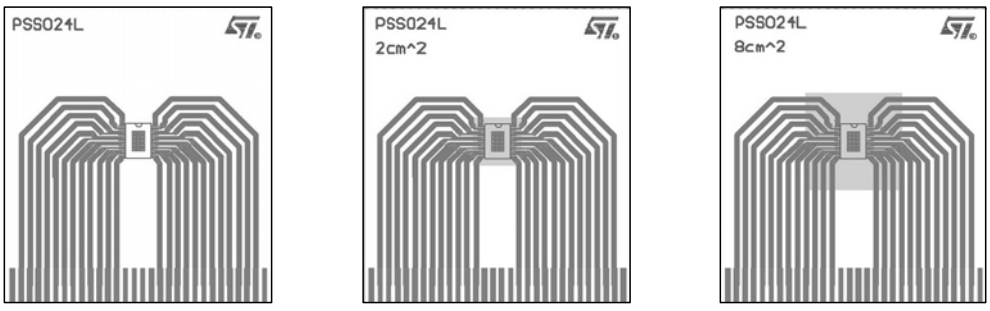
Note: Values are generated with R_L = 0 Ω.

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PC board thermal data

4.1 PowerSSO-24 thermal data

Figure 28. PowerSSO-24 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77 mm x 86 mm, PCB thickness=1.6mm, Cu thickness=70 µm (front and back side), Copper areas: from minimum pad lay-out to 8 cm^2).

Figure 29. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition (one channel on)

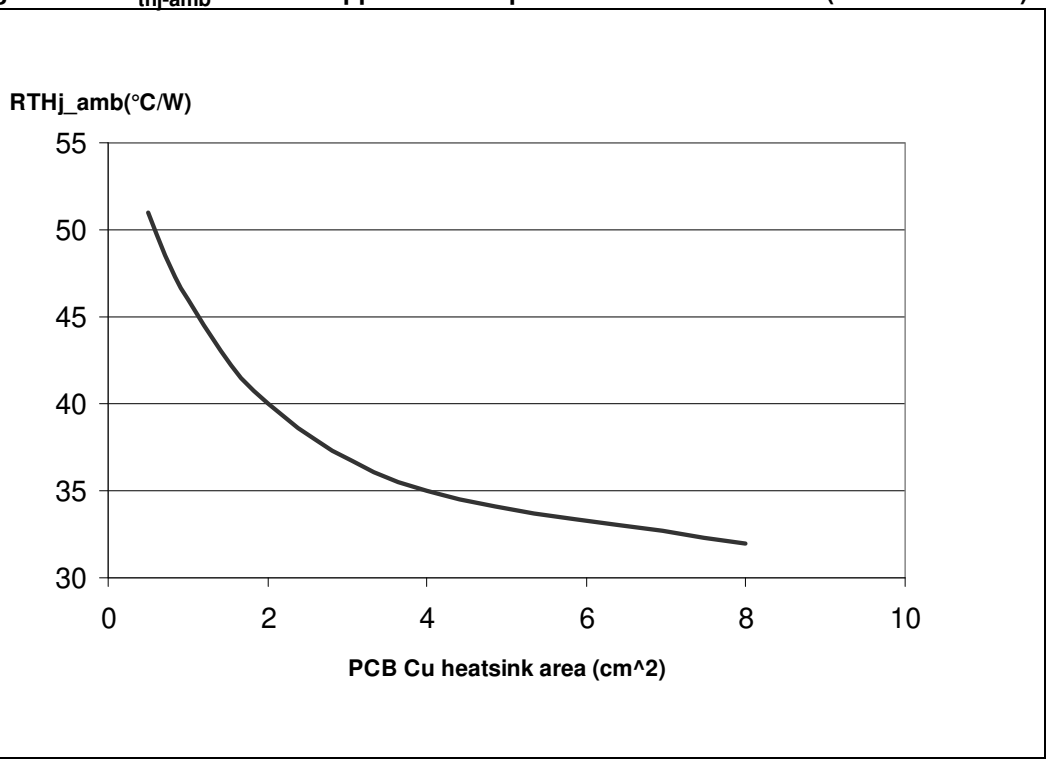


Figure 30. PowerSSO-24 thermal impedance junction ambient single pulse (one channel on)

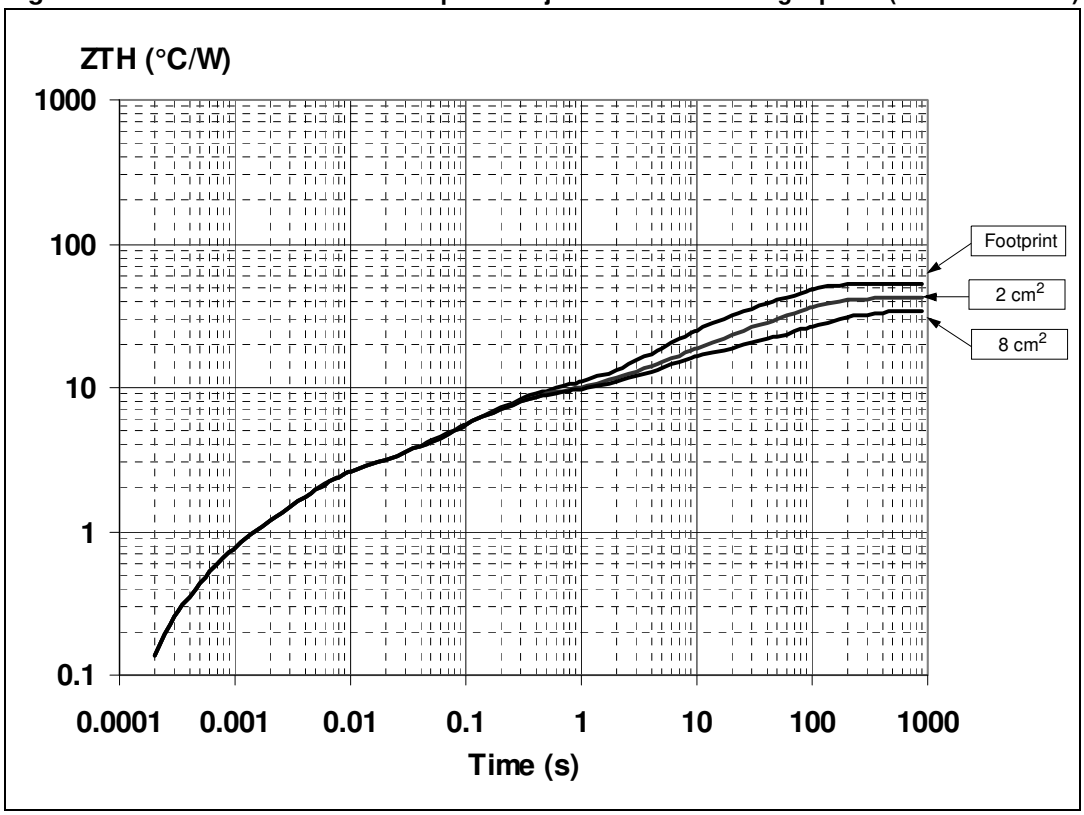
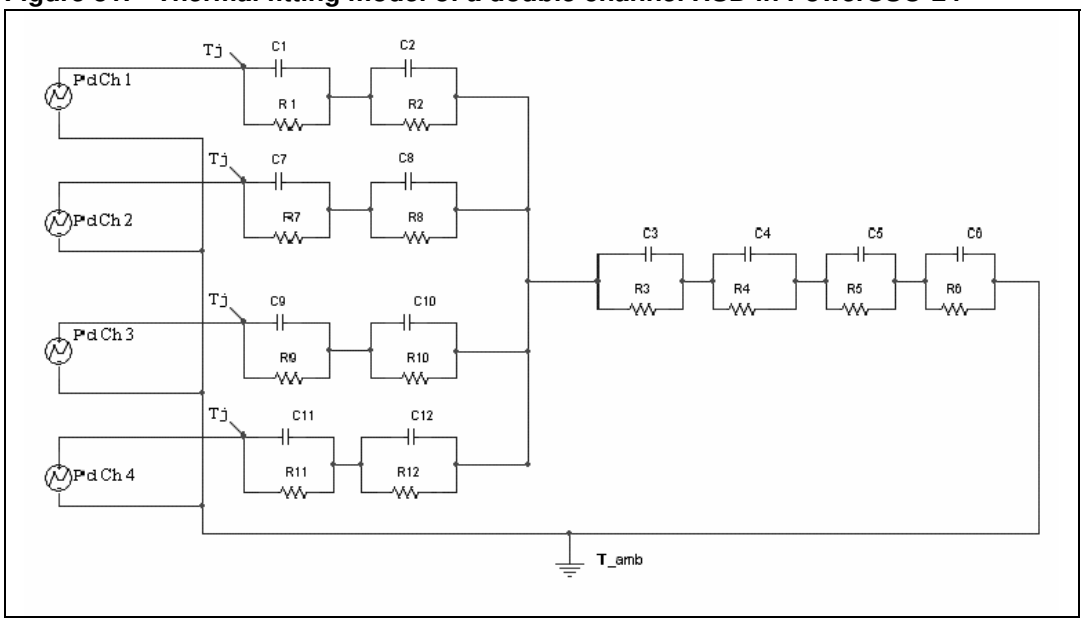


Figure 31. Thermal fitting model of a double channel HSD in PowerSSO-24(a)



a. The fitting model is a semplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.