Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

VNQ6004SA-E

Quad-channel high-side driver with 16-bit SPI interface

Datasheet - production data

PSSO36

Features

Channel	V_{CC}	$R_{ON(typ)}$	$I_{LIMH(min)}$
0–1	28 V	30 mΩ	25 A
2–3	28 V	10 mΩ	55 A

- General
  - 16-bit ST-SPI for full and diagnostic
  - Programmable Bulb/LED mode for ch. 0–1
  - Integrated PWM and phase shift generation unit
  - 160 Hz internal PWM fallback frequency
  - Advanced limp home functionalities for robust fail-safe system
  - Very low standby current
  - Optimized electromagnetic emissions
  - Very low electromagnetic susceptibility
  - In compliance with the 2002/95/EC
- Diagnostic functionalities
  - Multiplex proportional load current sense
  - Synchronous diagnostic of over load and short to GND, output shorted to V_{CC}, ON-state and OFF-state open-load
  - Programmable case over temperature warning
- Protection
  - Load current limitation
  - Self limiting of fast thermal transients
  - Power limitation and over temperature shutdown (latching-off or auto restart)
  - Undervoltage shutdown
  - Overvoltage clamp
  - Reverse battery protected through power outputs self turn-on (no external components)
  - Load dump protected
  - Protection against loss of ground

Description

The VNQ6004SA-E is a device made using STMicroelectronics® VIPower® technology. It is intended for driving resistive or inductive loads directly connected to ground. The device is protected against voltage transient on V_{CC} pin.

Programming, control and diagnostics are implemented via the SPI bus.

An analog current feedback for each channel is connected to the CURRENT-SENSE pin via a multiplexer. A CS_SYNC pin delivers a synchronous signal for sampling the current sense while the corresponding output is on.

The device detects open-load for both on and OFF-state conditions.

Real time diagnostic is available through the SPI bus (open-load, output short to V_{CC}, over temperature, communication error, power limitation).

Output current limitation protects the device in an over load condition. The device can limit the dissipated power to a safe level up to thermal shutdown intervention. Thermal shutdown can be configured as latched off or with automatic restart.

The device enters a limp home mode in case of loss of digital supply (V_{DD}), reset of digital memory or CSN monitoring time-out event. In this mode states of channel 0, 1, 2 or 3 are respectively controlled by four dedicated pins IN0, IN1, IN2 and IN3. Channel 0,1 can be programmed in BULB/LED mode.

Contents

List of tables

List of figures

1 Block diagram and pin description

Figure 1. SPI configurable functionalities

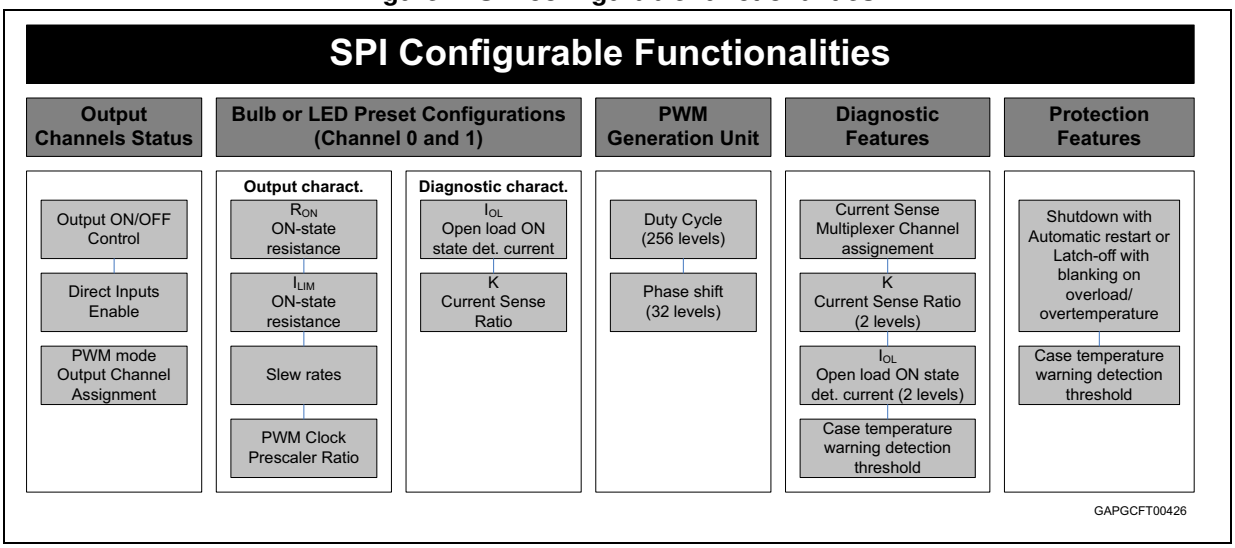


Figure 2. SPI diagnostic reporting

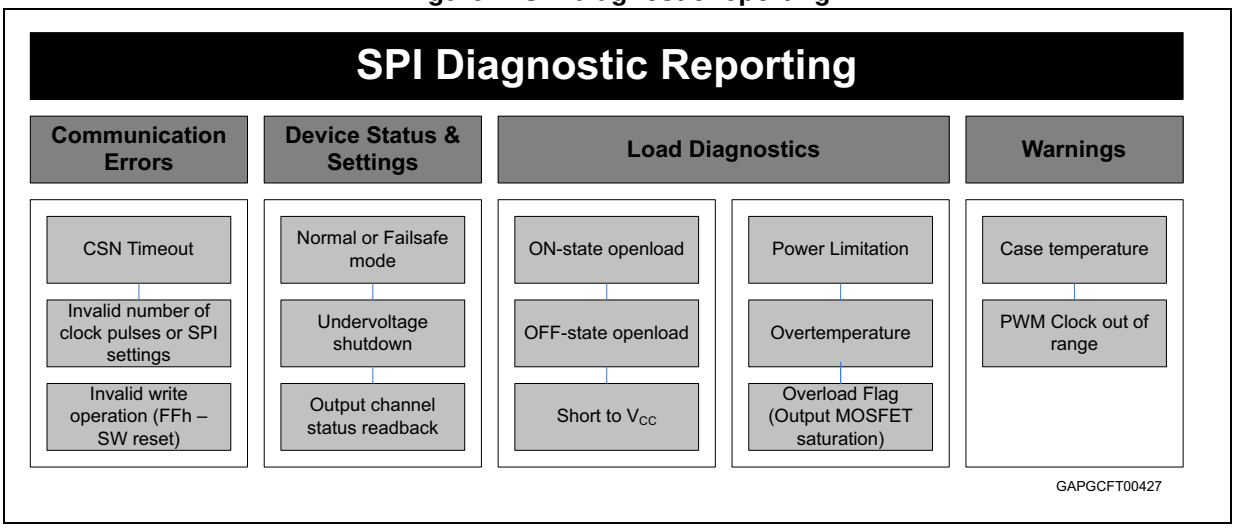
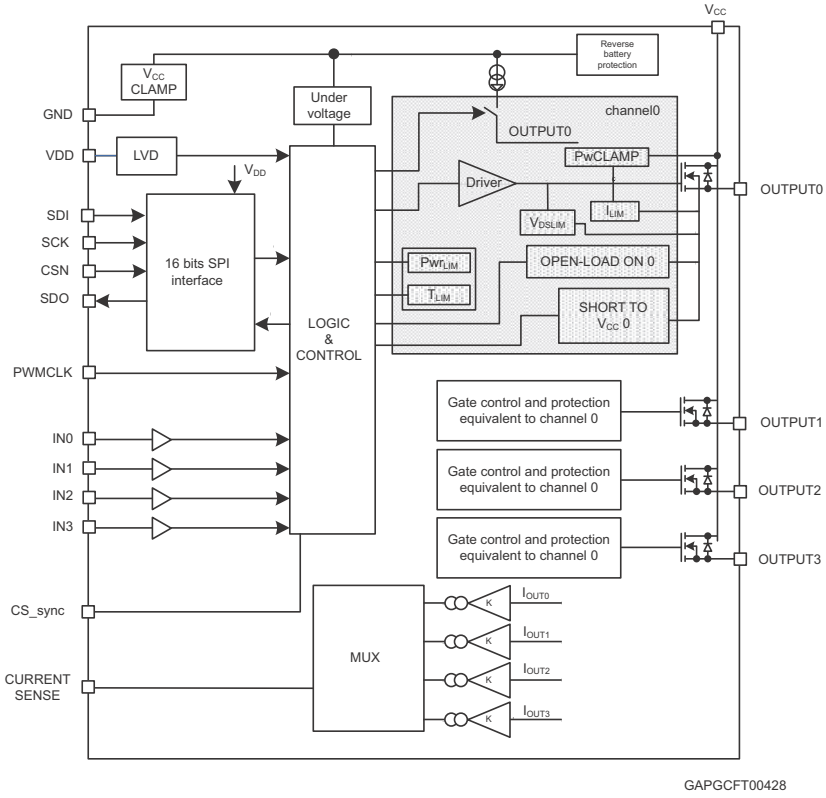
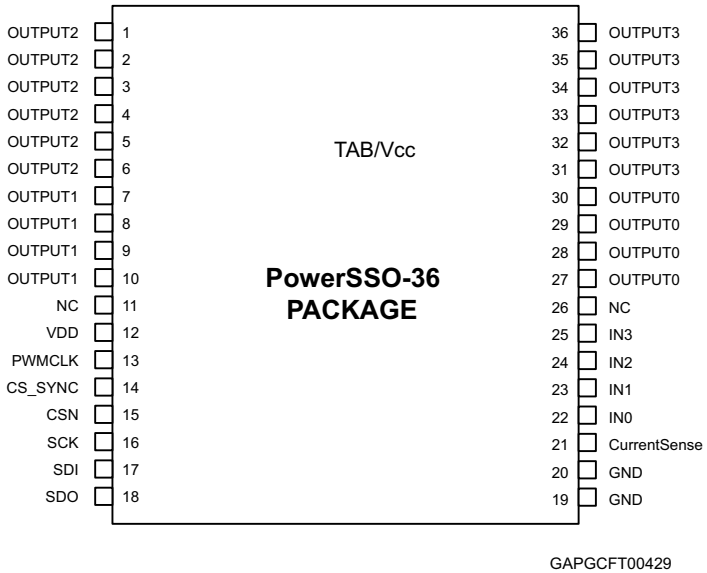


Figure 3. Block diagram



Note:
VNQ6004SA-E block diagram illustrates only a major internal device functionality and it is not intended to mimic any details of hardware design.

Figure 4. Connection diagram (top view—not in scale)



GAPGCFT00429

Note:
Pins 31,32,33,34,35 and 36 (OUTPUT3) must be connected together.
Pins 27,28,29 and 30 (OUTPUT0) must be connected together.
Pins 7,8,9 and 10 (OUTPUT1) must be connected together.
Pins 1,2,3,4,5 and 6 (OUTPUT2) must be connected together.

Table 1. Pin functionality description

Pin number	Name	Function
—	V_{CC}	Battery connection. This is the backside TAB and is the direct connection to drain Power MOSFET switches.
19, 20	GND	Ground connection. This pin serves as the ground connection for the logic part of the device.
27, 28, 29, 30	OUTPUT0	Power OUTPUT 0. It is the direct connection to the source Power MOSFET switch No. 0.
7, 8, 9, 10	OUTPUT1	Power OUTPUT 1. It is the direct connection to the source Power MOSFET switch No. 1.
1, 2, 3, 4, 5, 6	OUTPUT2	Power OUTPUT 2. It is the direct connection to the source Power MOSFET switch No. 2.
31, 32, 33, 34, 35, 36	OUTPUT3	Power OUTPUT 3. It is the direct connection to the source Power MOSFET switch No. 3.
15	CSN	Chip select not (active low). It is the selection pin of the device. It is a CMOS compatible input. It is also used as CSN monitoring pin. It must be toggled within a CSN monitoring timeout period to keep the device from switching to limp home operation.
16	SCK	Serial clock. It is a CMOS compatible input.
17	SDI	Serial data input. Transfers data to be written serially into the device on SCK rising edge.
18	SDO	Serial data output. Transfers data serially out of the device on SCK falling edge.
13	PWMCLK	PWM external clock. The frequency of the internal PWM signal is 1/512 x PWMCLK frequency for channels operating in BULB mode and 1/256 x PWMCLK frequency for channels operating in LED mode. Device defaults to internally generated fixed PWM frequencies if PWMCLK frequency decreases below the minimum specified value.
14	CS_SYNC	Current sense synchronization pin. The pin is high when the output, whose currents is reflected on current sense pin, is on.
22	IN0	Direct Input pin for channel 0. Controls the OUTPUT 0 state in limp home mode, is ORed to SPI control register in normal operating mode when corresponding bit is set in DIENCR (Direct Input ENable) control register.
23	IN1	Direct Input pin for channel 1. Controls the OUTPUT 1 state in limp home mode, is ORed to SPI control register in normal operating mode when corresponding bit is set in DIENCR (Direct Input ENable) control register.
24	IN2	Direct Input pin for channel 2. Controls the OUTPUT 2 state in limp home mode, is ORed to SPI control register in normal operating mode when corresponding bit is set in DIENCR (Direct Input ENable) control register.

Table 1. Pin functionality description (continued)

Pin number	Name	Function
25	IN3	Direct Input pin for channel 3. Controls the OUTPUT 3 state in limp home mode, is ORed to SPI control register in normal operating mode when corresponding bit is set in DIENCR (Direct Input ENable) control register.
12	V_{DD}	External 5V supply. Powers the digital control and SPI interface.
21	Current sense	Analog current sense generator proportional to output current. Current sense ratio can be programmed for each channel. The pin can output the current sense of OUTPUT 0, 1, 2 or 3. The value of resistance that is connected between the CURRENT SENSE pin and device ground determines the reading level for the microcontroller.
26	NC	Not connected

2 Functional description

2.1 Operating modes

The device can operate in 7 different modes:

- Reset mode
  Reset mode is entered after startup, and if the digital voltage V_{DD} falls below V_{DDR}. In this condition, the outputs are controlled by the direct inputs INX. The SPI is inactive, all SPI registers are cleared.
- Fail Safe mode
  After reset, after wake-up from Standby or Sleep mode 1 or 2 and in case of several error conditions, the device operates in Fail Safe mode. In this condition, the outputs are controlled by the direct inputs INX regardless of SPI commands. Diagnosis is available through SPI bus.
- Normal mode
  If the device is in Fail Safe mode, Normal mode can be entered using a special SPI sequence. In Normal mode, outputs can be driven by SPI commands or a combination of SPI command and direct inputs INX. Diagnosis is available through SPI bus and CurrentSense pin.
- Standby mode
  If the device is in Normal mode or Fail Safe mode, Standby mode can be entered using a special SPI sequence. In Standby mode the consumption of the digital part is nearly 0. The outputs are controlled by the direct inputs INX regardless of SPI commands.
- Sleep mode 1
  If the device is in Reset mode and the direct inputs INX are all 0, the device enters Sleep mode 1. In Sleep mode 1, the output stages are off, the current consumption of the digital part is nearly 0 and the current consumption on V_{CC} is below I_{Soff}.
- Sleep mode 2
  If the device is in Standby mode and the direct inputs INX are all 0, the device enters Sleep mode 2. In Sleep mode 2, the output stages are off, the current consumption of the digital part is nearly 0 and the current consumption on V_{CC} is below I_{Soff}.
- Battery undervoltage mode
  If the battery voltage V_{CC} is below the undervoltage threshold, the device enters Battery undervoltage mode. In this condition, the output stages are off regardless of SPI commands.

The Reset mode, the Fail Safe mode and the Sleep mode 1 are combined into the Limp home mode. In this mode the chip is able to operate without the connection to the SPI. All transitions between the states in limp home mode are driven by V_{DD} and INX. The outputs are controlled by the direct inputs INX.

For an overview over the operating modes and the triggering conditions please refer to *Table 2*.

Table 2. Operating modes

Operating mode	Entering conditions	Leaving conditions	Characteristics
Reset	– Startup – Any mode: $V_{DD} < V_{DDR}$ – Sleep 1: INX low to high	– All INX low: sleep 1 – $V_{DD} > V_{DDR}$: fail safe	– Outputs: according to INX – SPI: inactive – Registers: cleared – Diagnostics: not available
Fail Safe	– Reset or sleep 1: $V_{DD} > V_{DDR}$ – Standby or sleep 2: CSN low for $t > t_{stdby\_out}$ – Normal: EN = 0 or CSN time out or SW reset	– $V_{DD} < V_{DDR}$: reset – SPI sequence 1. UNLOCK = 1 2. STBY = 0 and EN = 1: normal – SPI sequence 1. UNLOCK = 1 2. STBY = 1 and EN = 0: fail safe	– Outputs: according to INX – SPI: active – Registers: read/writeable, cleared if entered after HW or SW reset – Diagnostics: SPI possible CurrentSense not possible
Normal	– Fail Safe: SPI sequence 1. UNLOCK = 1 2. STBY = 0 and EN = 1	– $V_{DD} < V_{DDR}$: reset – SPI sequence 1. UNLOCK = 1 2. STBY = 1 and EN = 0: standby – EN = 0 or CSN time out or SW reset: fail safe	– Outputs: according to SPI register settings and INX – SPI: active – Registers: read/writeable – Diagnostics: SPI and CurrentSense possible – Regular toggling of CSN necessary
Standby	– Normal: SPI sequence 1. UNLOCK = 1 2. STBY = 1 and EN = 0 – Fail Safe: SPI sequence 1. UNLOCK = 1 2. STBY = 1 and EN = 0 – Sleep 2: INX low to high	– $V_{DD} < V_{DDR}$: reset – CSN low for $t > t_{stdby\_out}$: fail safe – All INX low: sleep 2	– Outputs: according to INX – SPI: inactive – Registers: frozen – Diagnostics: not available – Low supply current from V_{DD}
Sleep 1	Reset: all INX = 0	– $V_{DD} > V_{DDR}$: fail safe – INX low to high: reset	– Outputs: OFF – SPI: inactive – Registers: cleared – Diagnostics: not available – Low supply current from V_{DD} and V_{CC}

Table 2. Operating modes (continued)

Operating mode	Entering conditions	Leaving conditions	Characteristics
Sleep 2	Standby: all INX = 0	– $V_{DD} < V_{DDR}$: reset – CSN low for $t > t_{stdby\_out}$: fail safe – INX low to high: standby	– Outputs: OFF – SPI: inactive – Registers: frozen – Diagnostics: not available – Low supply current from V_{DD} and V_{CC}
Battery undervoltage	Any mode: $V_{CC} < V_{USD}$	$V_{CC} > V_{USD}$: back to last mode	– Outputs: OFF – SPI: active – Register: read/writeable – Diagnostics: SPI possible, CurrentSense not possible

2.1.1 Reset mode

The device enters Reset mode under three conditions:

- Automatically during startup
- If it is in any other mode and if V_{DD} falls below V_{DDR}
- If it is in Sleep mode 1 and if one input INX is set to 1

In Reset mode, the output stages are according to the inputs INX. The SPI is inactive and all SPI registers are cleared. The reset bit inside the Global Status Byte is set to 0. The diagnostics is not available, but the protection are fully functional. In case of over temperature or power limitation, the outputs work in Autorestart.

Reset mode can be left with 2 conditions:

- If V_{DD} rises above V_{DDR}, the device enters Fail Safe mode
- If all inputs INX are 0, the device enters Sleep mode 1.

2.1.2 Fail Safe mode

The device enters Fail Safe mode under five conditions:

- If it is in Reset mode or in Sleep mode 1 and V_{DD} rises above V_{DDR}
- If it is in Standby mode or in Sleep mode 2 and CSN is low for $t > t_{stdby\_out}$
- If it is in Normal mode and bit EN is cleared
- If it is in Normal mode and CSN is not toggled within t_{WHCH} (CSN timeout)
- If it is in Normal mode and the SPI sends a SW reset (Command byte = FFh).

In Fail Safe mode, the output stages are according to the inputs INX. The SPI is active. The reset bit is 0 if the last state was Reset mode or the last command was a SW reset and it is set to 1 after the first SPI access. The SPI diagnostics is available, the CurrentSense pin is not available. The protection are fully functional. In case of over temperature or power limitation, the outputs work in Autorestart.

The device exits Fail Safe mode under two conditions:

- If the SPI sends the goto Normal mode sequence, the device enters Normal mode:
  - In a first communication set bit UNLOCK = 1
    In the consecutive communication set bit STBY = 0 and bit EN = 1
  - This mechanism avoids entering the Normal mode unintentionally.
- If the SPI sends the goto standby mode sequence, the device enters Standby mode:
  - In a first communication set bit UNLOCK = 1
    In the consecutive communication set bit STBY = 1 and bit EN = 0
  - This mechanism avoids entering the Standby mode unintentionally.
- If V_{DD} falls below V_{DDR}, the device enters Reset mode.

2.1.3 Normal mode

The device enters Normal mode if it is in Fail Safe mode and the SPI sends the goto Normal mode sequence:

- In a first communication set bit UNLOCK = 1
  In the consecutive communication set bit STBY = 0 and bit EN = 1
- This mechanism avoids entering the Normal mode unintentionally.

In Normal mode, the output stages are controlled by the SPI and the INX settings. The SPI is active. CSN must be toggled regularly within t_{WHCH} to keep the device in Normal mode. The SPI diagnostics and the CurrentSense pin are both available. The protection are fully functional. The outputs can be set to Autorestart or Latch. In Autorestart the outputs are switched on again automatically after an over temperature or power limitation event, while in Latch the relevant status register has to be cleared to switch them on again.

Normal mode can be left with 5 conditions:

- If V_{DD} falls below V_{DDR}, the device enters Reset mode.
- If the SPI sends the goto standby sequence, the devices enters Standby mode:
  - In a first communication set UNLOCK = 1
    In the consecutive communication set STBY = 1 and EN = 0
  - This mechanism avoids entering the Standby mode unintentionally.
- If the SPI clears the EN bit (EN = 0), the devices enters Fail Safe mode
- CSN time out: If CSN is not toggled within the minimum CSN monitoring timeout period t_{WHCH}, the device enters Fail Safe mode.
- If the SPI sends a SW reset command (Command byte = FFh), all registers are cleared and the device enters Fail Safe mode.

2.1.4 Standby mode

The device enters Standby mode under three conditions:

- If it is in Fail Safe mode and the SPI sends the goto standby sequence:
  - In a first communication set UNLOCK = 1
    In the consecutive communication set STBY = 1 and EN = 0
  - This mechanism avoids entering the Standby mode unintentionally.
- If it is in Normal mode and the SPI sends the goto standby sequence:
  - In a first communication set UNLOCK = 1
    In the consecutive communication set STBY = 1 and EN = 0
  - This mechanism avoids entering the Standby mode unintentionally.
- If it is in Sleep mode 2 and one input INX is set to one.

The output stages are according to INX settings, the current from V_{DD} is nearly 0.The SPI is inactive and all registers are frozen to the last state. The diagnostics is not available.

Standby mode can be left with three conditions:

- If V_{DD} falls below V_{DDR}, the device enters Reset mode.
- If CSN is low for $t > t_{stdby\_out}$, the device wakes up. As EN has been set to 0, the device enters Fail Safe mode and recovers full functionality with command of the outputs and diagnostics.
- If all direct inputs INX are 0, the device enters Sleep Mode 2 resulting in minimal supply current from V_{CC} and V_{DD}.

2.1.5 Sleep mode 1

The device enters Sleep mode 1, if it is in Reset mode and if all inputs INX are 0.

All outputs are off, the current from V_{DD} is nearly 0, and the current from V_{CC} is reduced to I_{Soff}. The SPI is inactive and all registers are cleared. The diagnostics is not available.

Sleep mode 1 can be left with two conditions:

- If V_{DD} rises above V_{DDR}, the device enters Fail Safe mode.
- If one of the inputs INX is set to 1, the device enters Reset mode.

2.1.6 Sleep mode 2

The device enters Sleep mode 2, if it is in Standby mode and if all inputs INX are 0.

All outputs are off, the current from V_{DD} is nearly 0, and the current from V_{CC} is reduced to I_{Soff}. The SPI is inactive and all registers are frozen to the last state. The diagnostics is not available.

Sleep mode 2 can be left with three conditions:

- If V_{DD} falls below V_{DDR}, the device enters Reset mode.
- If CSN is low for $t > t_{stdby\_out}$, the device enters Fail Safe mode.
- If one of the inputs INX is set to 1, the device enters Standby mode.

2.1.7 Battery undervoltage mode

If the battery supply voltage V_{CC} falls below the undervoltage shutdown threshold V_{USD} while VDD remains above the reset threshold V_{DDR}, the device enters Battery undervoltage mode independent from the operation mode. In Battery undervoltage mode, the outputs are turned off. The SPI is active and the SPI register contents are retained. The SPI diagnostics is available, the CurrentSense pin is not available. The bit VCCUV in the general status register GENSTR is set. If V_{CC} rises above the threshold V_{USD} + $V_{USDhyst}$, the device returns to the last mode and VCCUV is cleared.

Figure 5. Battery undervoltage shutdown diagram

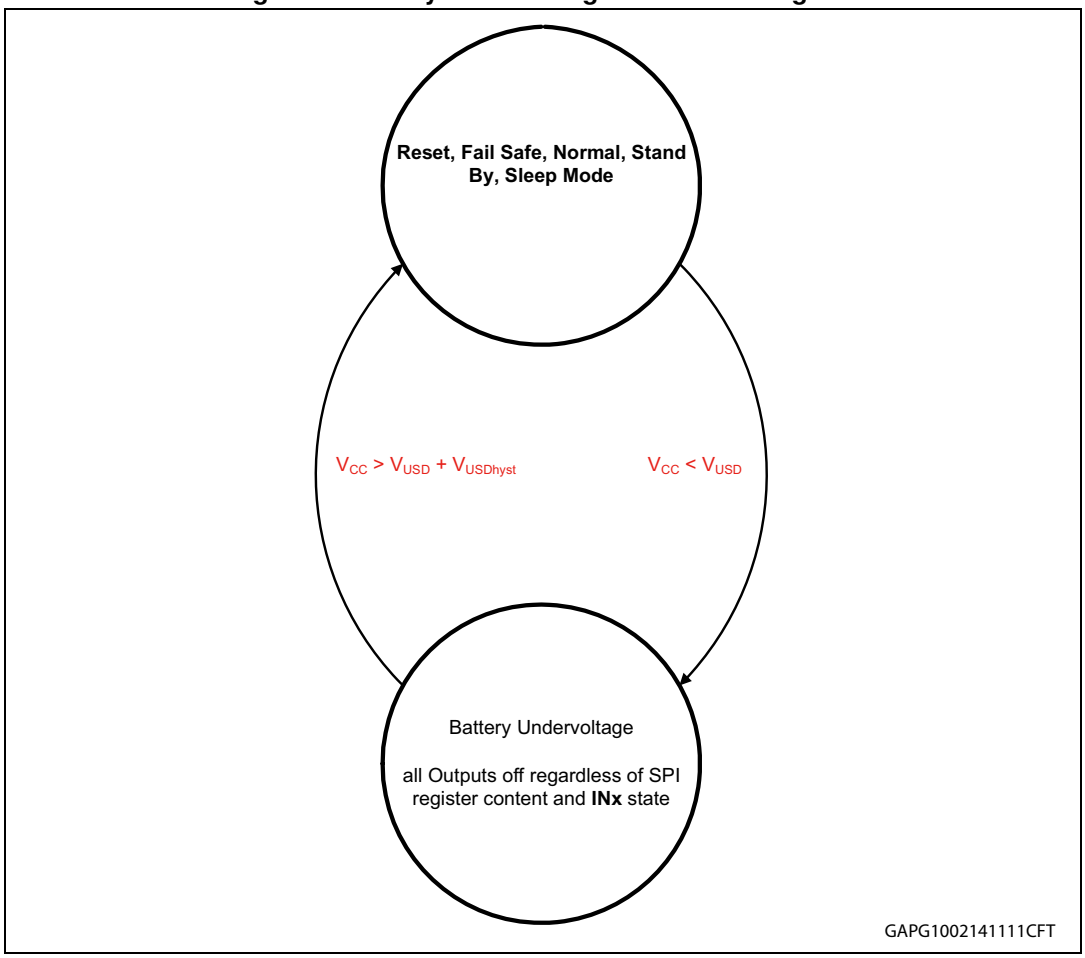
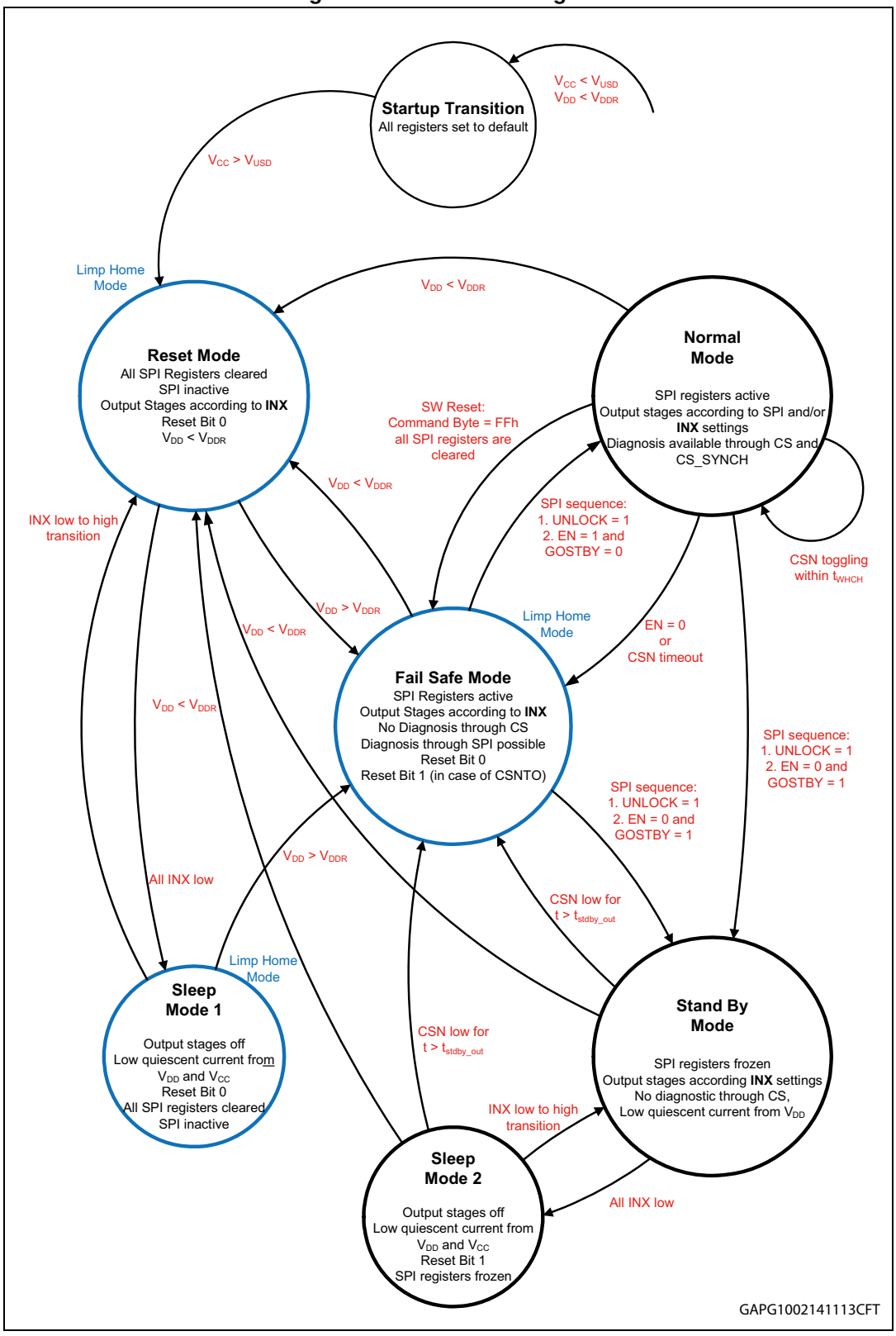


Figure 6. Device state diagram



2.2 Programmable functions

2.2.1 Outputs configuration

The status of the output drivers is configured via the SPI output control register (SOCR), the direct input enable control register (DIENCR), the PWM mode control register (PWMCR) and the channel control register (CCR). The DIENCR selects if the outputs OUTPUTX are controlled also by the direct inputs INX or only by the SOCR. The PWMCR selects if the outputs operates in PWM mode. Please refer to *Table 3* for details.

Table 3. Output control truth table

DIENCRX	INX	SOCRX	PWMCRX	OUTPUTX
0	X	0	0	OFF
0	X	0	1	OFF
0	X	1	0	ON
0	X	1	1	PWM
1	L	0	0	OFF
1	L	0	1	OFF
1	L	1	0	ON
1	L	1	1	PWM
1	H	X	0	ON
1	H	X	1	PWM

The output channels 0 and 1 can be configured to operate in BULB or LED mode using the channel control register (CCR). If the relevant bit in CCR is 0, the output is configured in BULB mode, if it is set to 1, the output is configured in LED mode. This configuration has an influence on the base frequency for PWM operation (see below in this chapter), on the open-load thresholds (see *Chapter 2.2.4*) and on the current sense ratio (see *Chapter 2.2.6*).

PWM operation

If the PWMCRX bit is set, the relevant output OUTPUTX operates in PWM mode. The duty cycle and the phase of the PWM signal are configured via the DUTYCXCR and the PHASEXCR registers, respectively.

The signal on the PWMCLK is divided internally by 512 or 256 depending on the output operating mode (BULB mode or LED mode) to generate the base frequency for the output.

The duty cycle of the output signal is configured for each OUTPUTX with the DUTYCXCR register using 8 bits (MSB first). DUTYCXCR = 00h means that the duty cycle is 0, and consequently the output is OFF, while DUTYCXCR = FFh results in a maximum duty cycle of 255/256 = 99.6 %. To switch the output permanently ON, it is necessary to select PWMCRX = 0 (see *Table 3*).

The phase shift of the output signal is configured for each OUTPUTX with the PHASEXCR register using 5 bits (MSB first, bit2–bit0 are ignored). PHASEXCR = 00h means a phase shift of 0, while PHASEXCR = F8h results in a maximum phase shift of 31/32 = 96.9 %. The phase shift is relative to the base frequency of the selected channel. Thus, the exact point in

time when the channel switches on depends also on the operating mode (BULB or LED mode) of the selected channel.

Below, an example with a 30% duty cycle and a 16% phase is given:

1. 30% duty cycle results in a DUTYCXCR register content equal to 76 = 4Ch (30 % x 256 = 76).
2. 16% phase results in a PHASECXR register content equal to 5 (16 % x 32 = 5), equivalent to a content of 40 = 28 h for a 8 bit register.

Table 4. Example of DUTYCXCR register

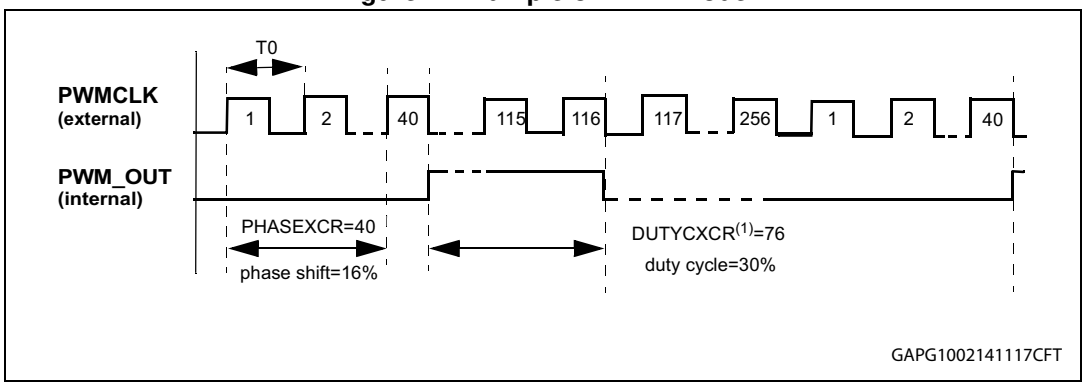
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	1	0	0	1	1	0	0

Table 5. Example of PHASEXCR register

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	1	0	1	X	X	X

Figure 7 shows the resulting waveforms.

Figure 7. Example of PWM mode



Note: 1 If the frequency on PWMCLK is too low ($f < f_{pwm}$), the device falls back to an internally generated PWM frequency of about 160 Hz in BULB mode and 320 Hz in LED mode. In this case the PWMLOW bit in the General Status Register (GENSTR) and the global error flag are set.

2 The application should ensure that the duty cycle is not chosen too low. For very low duty cycle there are two restrictions: Due to the slew-rate control of the outputs, the outputs do not switch on and off immediately. Therefore, for low duty cycles, the output pulses are no longer rectangular but change to triangular form, resulting in a non-linear duty cycle - power relationship. Moreover, if the output is switched off while the voltage drop on the PowerMOS V_{DS} is still above V_{DSmax}, this causes a false over load detection (see also Section 2.2.3).

2.2.2 Case over temperature

If the case temperature rises above the case thermal detection pre-warning threshold T_{CSD}, the bit T_{FRAME} in the Global Status Byte is set. T_{FRAME} is cleared automatically when the case temperature drops below the case temperature reset threshold T_{CR}. The typical value

of T_{CSD} can be set using the bits CTDTH1 and CTDTH0 inside the CTLR register (see *Section 3.3.1*).

2.2.3 Protections

Junction over temperature

If the junction temperature of one channel rises above the shutdown temperature T_{TSD}, an over temperature event (OT) is detected. The channel is switched OFF and the corresponding bit in the over temperature status register OTFLTR (address 30h) is set. Consequently, the thermal shutdown bit (bit 4) in the Global Status Byte and the Global Error Flag are set.

Each output channel can be either set in Autorestart or Latched OFF operation in case of junction over temperature event by setting the corresponding ASDTCR register bit (address 08h).

In Autorestart operation, the output is switched off as described and switches on again automatically when the junction temperature falls below the reset temperature T_R. The status bit is latched during OFF-state of the channel in order to allow asynchronous diagnostic and it is automatically cleared when the junction temperature falls below the thermal reset temperature of OT detection T_{RS}.

In Latched OFF operation, the output remains switched OFF until the junction temperature falls below T_{RS} and a read and clear command is sent.

Power limitation

If the difference between junction temperature and case temperature ($\Delta T = T_j - T_c$) rises above the power limitation threshold ΔT_{PLIM}, a power limitation event is detected. The corresponding bit in the power limitation status register PWLMFLTR (address 33h) is set and the channel is switched OFF. Consequently, the power limitation bit (bit 4) in the Global Status Byte and the Global Error Flag are set.

Each output channel can be either set in Autorestart or Latched OFF operation in case of power limitation event by setting the corresponding ASDTCR register bit (address 08h).

In Autorestart operation, the output is switched off as described and switches on again automatically when ΔT falls below the reset threshold $\Delta T_{PLIMreset}$. The status bit is latched during OFF-state of the channel in order to allow asynchronous diagnostic and it is automatically cleared in ON-state when the power limitation event is removed.

In Latched OFF operation, the output remains switched OFF until ΔT falls below the reset threshold $\Delta T_{PLIMreset}$ and a read and clear command is sent.

Each time a channel is switched on via the corresponding bit in SOCR, a blanking time $t_{blanking}$ is initialized which masks a power limitation event and its relevant diagnostic in the PWLMFLTR register. The blanking time does not account for an over temperature event, i.e. the outputs are switched OFF and the relevant bits in OTFLTR are set even during the blanking time, or for an over load event.

The blanking filter is only active, if the channel is turned on through SOCR. There are, however, additional conditions which cause the output to switch from OFF to steady ON-state or to PWM output which do not activate the blanking filter. Refer to *Table 6* for more details.

Table 6. Activation of blanking filter in case of power limitation

Action	Output state	Blanking filter
SOCR = 0 to 1	Switches from off to steady state or PWM according to PWMCR	Active
SOCR = 0 DIEN = 1 INX = 0 to 1	Switches from off to steady state or PWM according to PWMCR	Not active
SOCR = 1, DIEN = 0 PWMCR = 1 DUTYCRX = 00h to nonzero value	Switches from off to PWM	Not active
SOCR = 1, DIEN = 0 PWMCR = 1 to 0 DUTYCRX = 00h	Switches from off to steady state	Not active

Over load

During low duty cycle PWM operation on a shorted load, ON-time may be too short to allow power limitation or over temperature detection. Current sense output is 0. This would make detection of this over load condition impossible. To overcome this, always when an output channel is turned OFF, the voltage drop on the PowerMOS (V_{DS}) is measured. If V_{DS} exceeds the threshold V_{DSmax}, an over load condition is detected. The corresponding bit in the over load status register OVLFLTR (address 34H) is set. Consequently, the over load bit (bit 4) in the Global Status Byte and the Global Error Flag are set.

The OVLFLTR is a warning and the channel can be switched on again even if the OVLFLTRX bit is set. The OVLFLTRX bit remains unchanged until a read and clear command on OVLFLTR is sent by the SPI or until the output is turned off the next time, when V_{DS} is evaluated again.

If the output channel is switched ON for a very short time, V_{DS} might be greater than V_{DSmax} even if the output is not in over load state so that a false warning is issued. Please refer to *Table 37* for more details.

2.2.4 Open-load ON-state detection

If the current through the output during the ON-state falls below the open-load ON-state detection thresholds, an open-load condition is detected for the relevant channel. The corresponding bit in the open-load ON-state status register (OLFLTR) is set. At the same time, the open-load at ON-state bit (bit 2) in the Global Status Byte and the Global Error Flag are set.

Two different open-load ON-state detection thresholds (see *Table 7*) can be set for each channel by writing into OLONCR register (address 06H). For channel related information, bit0 corresponds to channel0, bit1 to channel1, bit2 to channel2, bit3 to channel3.

Table 7. Nominal open-load thresholds

Channel	OLONCRX	I_{OLnom} BULB mode	I_{OLnom} LED mode
0, 1	0	75 mA	19 mA
	1	470 mA	160 mA
2, 3	0	180 mA	—
	1	1250 mA	—

2.2.5 Open-load OFF-state detection

If the output voltage V_{OUT} in OFF-state of the output is greater than the open-load detection threshold voltage V_{OL}, an open-load OFF-state / Stuck to V_{CC} event is detected (see *Figure 8*). The corresponding bit in the Open-load OFF-state / Stuck to VCC status register STKFLTR (Address 32h) is set. Consequently, the OLOFF bit (bit 1) in the Global Status Register and the Global Error Flag are set. To avoid false detection, the diagnosis starts after turn-off of a channel with an additional delay t_{DOLOFF}.

To distinguish between an open-load OFF-state event and a short to VCC condition, an internal pull-up current generator can be enabled for each channel by setting the corresponding bit in the open-load OFF-state control register (OLOFFCR, address 07h), see *Table 8*.

The activated pull-up current generators are active in Normal Mode, in Fail Safe Mode and in Standby Mode. In Sleep Mode 2, the current generators are switched off. The register contents, however, are saved also in Sleep Mode 2, consequently the current generators are reactivated after a return to Standby or a wakeup to Fail Safe Mode. A hardware reset ($V_{DD} < V_{DDR}$) or a software reset (Command byte = FFh) clears all register contents and hence the current generators are switched off.

Figure 8. Open-load OFF-state detection

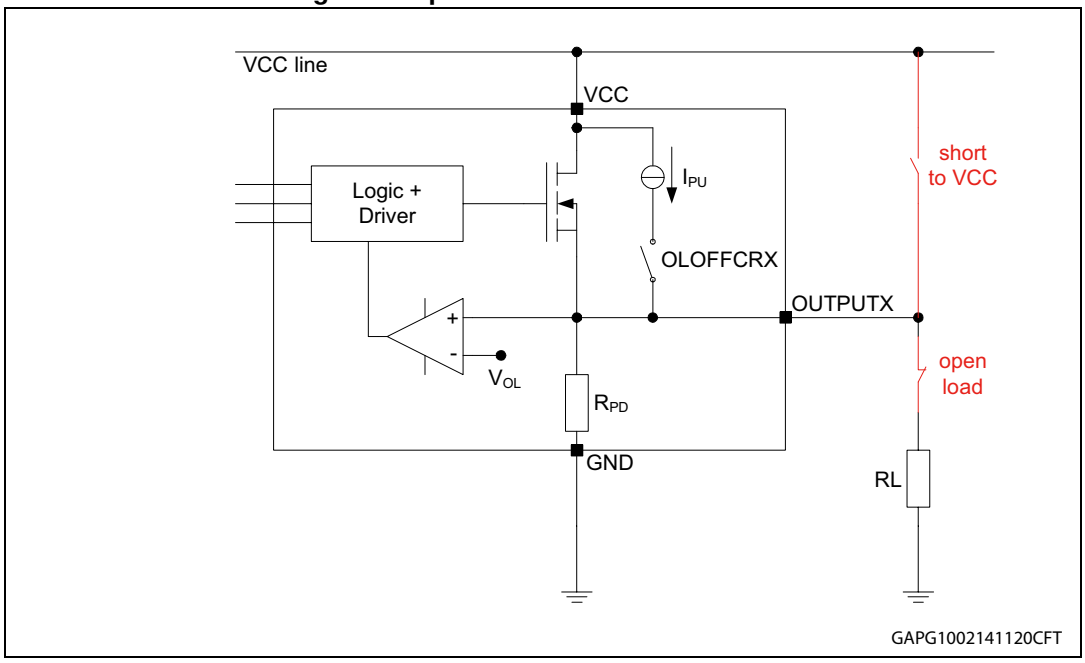


Table 8. STKFLTR state

	With internal pull-up generator	Without internal pull-up generator
Case 1: load connected	“0” / no fault	“0” / no fault
Case 2: no load	“1” / fault	“0” / no fault
Case 3: output shorted to V_{CC}	“1” / fault	“1” / fault

2.2.6 Current sense

Each channel integrates an analog current sense function which can be connected to the current sense pin by setting the CURSEN bit (bit 3) in the CTLR register (address 00H) and by setting the corresponding channel in the CSMUXCR register (address 03H).

The ratio between output current and sense current can be also selected by writing into the CSRATCR register (address 04H).

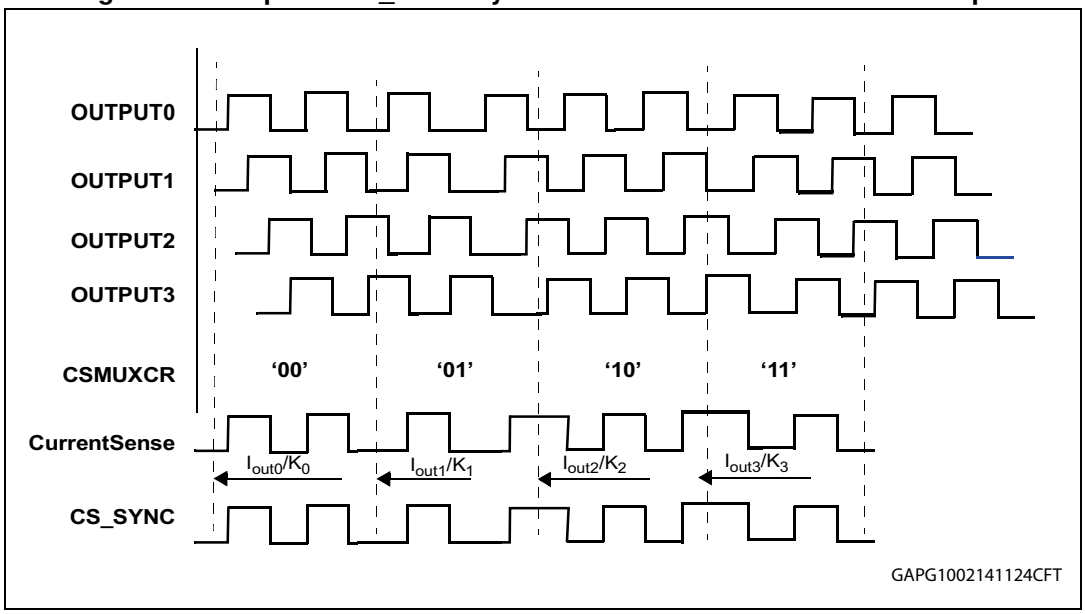
The current sense ratio is as shown in *Table 9*.

Table 9. Current sense ratio

Channel	CSRATCRX	Current sense ratio K (typical) BULB mode	Current sense ratio K (typical) LED mode
0, 1	0	2080	700
	1	5360	1900
2, 3	0	5800	—
	1	15250	—

The output CS_SYNC provides a synchronization signal for the current sense pin. It is “1” if the corresponding output is ON, and “0” if the output is OFF. If no output is selected (CURSEN = 0), CS_SYNC is in high impedance state. Please refer also to *Figure 9*.

Figure 9. Example of CS_SYNC synchronization and the current sense pin



2.3 Test mode (reserved)

The Digital core and most of the advanced functionalities integrated in the VNQ6004SA-E are tested by setting the device in a special Test Mode. In this state, the CSN monitoring timeout control is disabled and the functionality of the other SPI pins (SDI and SDO) might be different from the standardized communication protocol, whilst other pins might be configured as diagnostic I/O's.

Test Mode is intended only for the ST serial production testing flow.

Accessing Test Mode in the application might lead the device to operate in uncontrolled conditions.

Entering Test Mode is prevented by operating the device within its Absolute Maximum Ratings.