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Quad channel high-side driver with MultiSense analog feedback for automotive applications

Datasheet - production data



Features

Max transient supply voltage	V_{CC}	41 V
Operating voltage range	V_{CC}	4 to 28 V
Typ. on-state resistance (per ch)	R_{ON}	40 mΩ
Current limitation (typ)	I_{LIMH}	34 A
Standby current (max)	I_{STBY}	0.5 µA

- General
 - Quad channel smart high-side driver with MultiSense analog feedback
 - LED Mode for channel 0 and 1
 - Very low standby current
 - Compatible with 3 V and 5 V CMOS outputs
- MultiSense diagnostic functions
 - Multiplexed analog feedback of: Load current with high precision proportional current mirror; V_{CC} supply voltage; T_{CHIP} device temperature
 - Overload and short to ground (power limitation) indication
 - Thermal shutdown indication
 - OFF-state open load detection
 - Output short to V_{CC} detection
 - Sense enable/disable
- Protections
 - Undervoltage shutdown
 - Overvoltage clamp
 - Load current limitation

- Self limiting of fast thermal transients
- Configurable latch-off on overtemperature or power limitation with dedicated fault reset pin
- Loss of ground and loss of V_{CC}
- Reverse battery through self turn-on
- Electrostatic discharge protection

Applications

- All types of Automotive resistive, inductive and capacitive loads
- Specially intended for Automotive Turn Indicators (up to P27W or SAE1156 and R5W paralleled or LED Rear Combinations)

Description

The VNQ7040AY-E is a quad channel high-side driver manufactured using the latest ST proprietary VIPower® technology and housed in PowerSSO-36 package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, and to provide protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off.

A FaultRST pin unlatches the output in case of fault or disables the latch-off functionality.

A dedicated multifunction multiplexed analog output pin delivers sophisticated diagnostic functions such as high precision proportional load current sense, supply voltage feedback and chip temperature sense, in addition to the detection of overload and short circuit to ground, short to V_{CC} and OFF-state open-load.

The device features a dedicated LED Mode.

Contents

1	Block diagram and pin description	7
2	Electrical specification	9
2.1	Absolute maximum ratings	9
2.2	Thermal data	10
2.3	Electrical characteristics	11
2.3.1	General electrical specification	11
2.3.2	Bulb mode (default)	17
2.4	Electrical characteristics curves - Bulb Mode	21
2.4.1	LED Mode (Channel 0 and 1)	24
2.5	Electrical characteristics curves - LED mode	28
2.5.1	Truth tables	32
2.5.2	Immunity to electrical transient disturbances on VCC (ISO 7637-2)	34
3	Protections	35
3.1	Power limitation	35
3.2	Thermal shutdown	35
3.3	Current limitation	35
3.4	Negative voltage clamp	35
4	Application information	36
4.1	Protection against reverse battery	36
4.2	Immunity against transient electrical disturbances	37
4.3	MCU I/Os protection	37
4.4	Multisense - analog current sense	38
4.4.1	Principle of Multisense signal generation	40
4.4.2	T _{CASE} and V _{CC} monitor	42
4.4.3	Short to VCC and OFF-state open-load detection	43
4.5	Maximum demagnetization energy (V _{CC} = 16 V)	44
5	Package and PCB thermal data	45
5.1	PowerSSO-36 thermal data	45

6	Package information	49
6.1	ECOPACK®	49
6.2	PowerSSO-36 mechanical data	49
6.3	Packing information	51
7	Order codes	52
8	Revision history	53

List of tables

Table 1.	Pin functions	7
Table 2.	Suggested connections for unused and not connected pins	8
Table 3.	Absolute maximum ratings	9
Table 4.	Thermal data.	10
Table 5.	Power section	11
Table 6.	Logic Inputs ($7 \text{ V} < V_{CC} < 28 \text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$)	12
Table 7.	Protections ($7 \text{ V} < V_{CC} < 18 \text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$).	13
Table 8.	MultiSense ($7 \text{ V} < V_{CC} < 18 \text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$).	14
Table 9.	Power section in Bulb Mode ($7 \text{ V} < V_{CC} < 28 \text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified)	17
Table 10.	Switching in Bulb Mode ($V_{CC} = 13 \text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified).	17
Table 11.	MultiSense in Bulb Mode ($7 \text{ V} < V_{CC} < 18 \text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$).	18
Table 12.	Switching in LED Mode ($V_{CC} = 13 \text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified)	24
Table 13.	Power section in LED Mode ($7 \text{ V} < V_{CC} < 28 \text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified)	25
Table 14.	MultiSense in LED Mode ($7 \text{ V} < V_{CC} < 18 \text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$)	25
Table 15.	Truth table.	32
Table 16.	MultiSense multiplexer addressing	32
Table 17.	Bulb/LED Mode Configuration	33
Table 18.	Electrical transient requirements (part 1/3)	34
Table 19.	Electrical transient requirements (part 2/3)	34
Table 20.	Electrical transient requirements (part 3/3)	34
Table 21.	ISO 7637-2 - electrical transient conduction along supply line	37
Table 22.	MultiSense pin levels in off-state	42
Table 23.	PCB properties	46
Table 24.	Thermal parameters	48
Table 25.	PowerSSO-36 mechanical data	50
Table 26.	Device summary	52
Table 27.	Document revision history	53

List of figures

Figure 1.	Block diagram	7
Figure 2.	Configuration diagram (top view)	8
Figure 3.	Current and voltage conventions	9
Figure 4.	Bulb Mode - I_{OUT}/I_{SENSE} versus I_{OUT}	20
Figure 5.	Bulb Mode - current sense precision vs. I_{OUT}	20
Figure 6.	OFF-state output current	21
Figure 7.	Standby current	21
Figure 8.	$I_{GND(ON)}$ vs. I_{out}	21
Figure 9.	Logic Input high level voltage	21
Figure 10.	Logic Input low level voltage	21
Figure 11.	High level logic input current	21
Figure 12.	Low level logic input current	22
Figure 13.	Logic Input hysteresis voltage	22
Figure 14.	FaultRST Input clamp voltage	22
Figure 15.	Undervoltage shutdown	22
Figure 16.	On-state resistance vs. T_{case}	22
Figure 17.	On-state resistance vs. V_{CC}	22
Figure 18.	Turn-on voltage slope	23
Figure 19.	Turn-off voltage slope	23
Figure 20.	W_{on} vs. T_{case}	23
Figure 21.	W_{off} vs. T_{case}	23
Figure 22.	I_{LIMH} vs. T_{case}	23
Figure 23.	OFF-state open-load voltage detection threshold	23
Figure 24.	V_{sense} clamp vs. T_{case}	24
Figure 25.	V_{senseh} vs. T_{case}	24
Figure 26.	LED Mode - I_{OUT}/I_{SENSE} versus I_{OUT}	26
Figure 27.	LED Mode - current sense precision vs. I_{OUT}	27
Figure 28.	On-state resistance vs. T_{case}	28
Figure 29.	On-state resistance vs. V_{CC}	28
Figure 30.	Turn-on voltage slope	28
Figure 31.	Turn-off voltage slope	28
Figure 32.	W_{on} vs. T_{case}	29
Figure 33.	W_{off} vs. T_{case}	29
Figure 34.	I_{LIMH} vs. T_{case}	29
Figure 35.	Switching times and Pulse skew	30
Figure 36.	MultiSense timings (current sense mode)	30
Figure 37.	Multisense timings (chip temperature and VCC sense mode)	31
Figure 38.	T_{DSKON}	31
Figure 39.	Application diagram	36
Figure 40.	Simplified internal structure	36
Figure 41.	Multisense and diagnostic – block diagram	39
Figure 42.	Multisense block diagram	40
Figure 43.	Analogue HSD – open-load detection in off-state	41
Figure 44.	Open-load / short to VCC condition	42
Figure 45.	GND voltage shift	43
Figure 46.	Maximum turn off current versus inductance	44
Figure 47.	PowerSSO-36 PC board	45
Figure 48.	$R_{thj-amb}$ vs PCB copper area in open box free air condition	46

Figure 49.	PowerSSO-36 thermal impedance junction ambient	47
Figure 50.	Thermal fitting model of a HSD in PowerSSO-36	47
Figure 51.	PowerSSO-36 package dimensions	49
Figure 52.	PowerSSO-36 tube shipment (no suffix)	51
Figure 53.	PowerSSO-36 tape and reel shipment (suffix "TR")	51

1 Block diagram and pin description

Figure 1. Block diagram

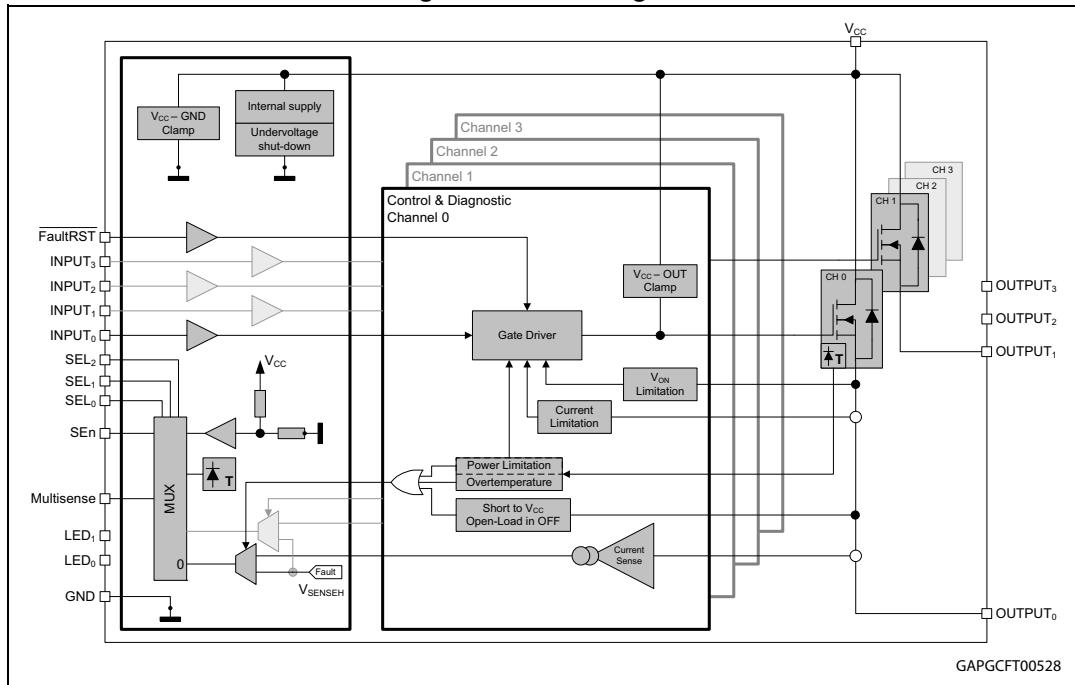
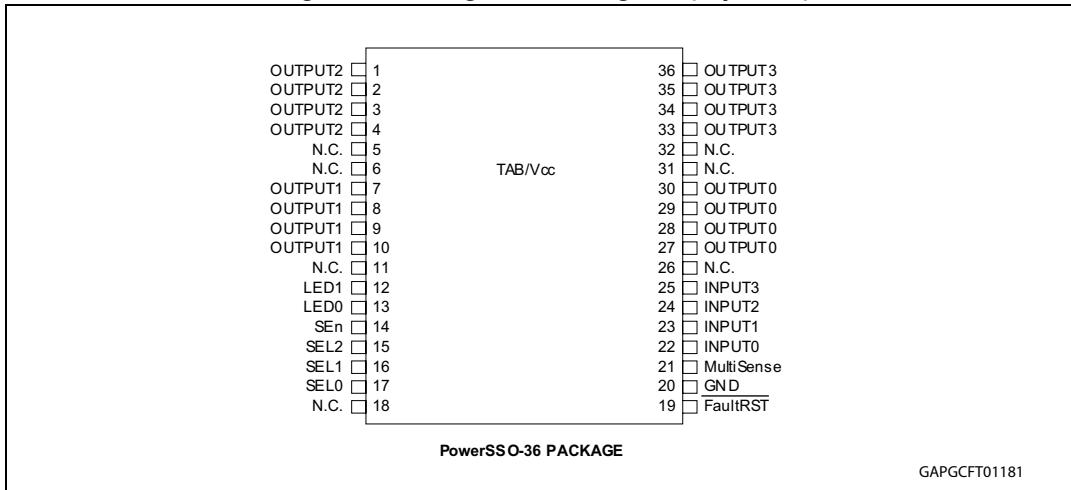


Table 1. Pin functions

Name	Function
V_{CC}	Battery connection.
$OUTPUT_{0,1,2,3}$	Power output.
GND	Ground connection.
$INPUT_{0,1,2,3}$	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. They control output switch state.
MultiSense	Multiplexed analog sense output pin; it delivers a current proportional to the selected diagnostic: load current, supply voltage or chip temperature.
SEn	Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the MultiSense diagnostic pin
$LED_{0,1}$	Active high compatible with 3 V and 5 V CMOS outputs pin; they enable the LED mode on logic high level (see Table 15: Truth table).
$SEL_{0,1,2}$	Active high compatible with 3 V and 5 V CMOS outputs pin; they address the MultiSense multiplexer (see Table 15: Truth table).
$\overline{FaultRST}$	Active low compatible with 3 V and 5 V CMOS outputs pin; it unlatches the output in case of fault; If kept low, sets the outputs in auto-restart mode.

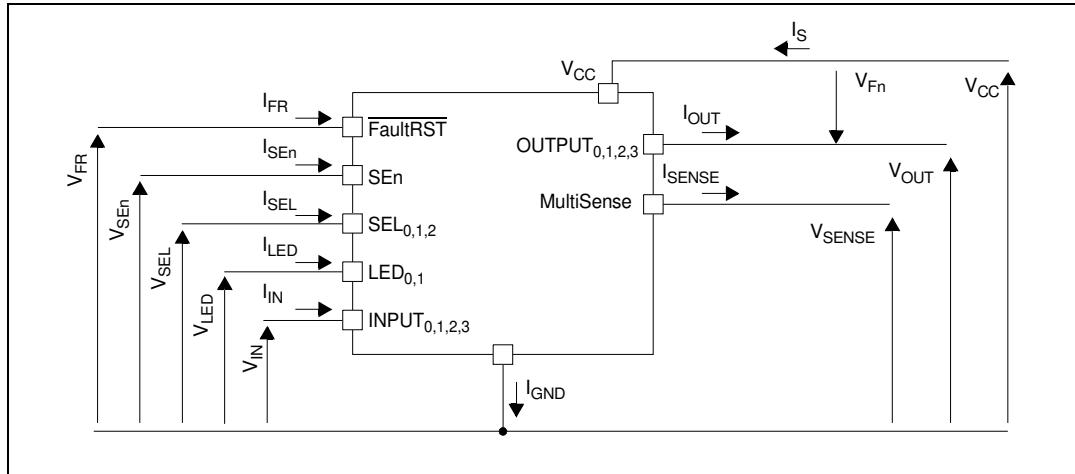
Figure 2. Configuration diagram (top view)**Table 2. Suggested connections for unused and not connected pins**

Connection / pin	MultiSense	N.C.	Output	Input	SEN, SELx, LEDx, FaultRST
Floating	Not allowed	X ⁽¹⁾	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 15 kΩ resistor	Through 15 kΩ resistor

1. X: do not care.

2 Electrical specification

Figure 3. Current and voltage conventions



$$1. \quad V_{Fn} = V_{OUTn} - V_{CC}$$

2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	38	V
$-V_{CC}$	Reverse DC supply voltage	16	
V_{CCPK}	Maximum transient supply voltage (ISO7637-2:2004 Pulse 5b level IV clamped to 40 V; $R_L = 4 \Omega$)	40	
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	OUTPUT _{0,1,2,3} DC output current	Internally limited	A
$-I_{OUT_0,1}$	OUTPUT _{0,1} Reverse DC output current	10	
$-I_{OUT_2,3}$	OUTPUT _{2,3} Reverse DC output current	10	
I_{IN}	INPUT _{0,1,2,3} DC input current	-1 to 10	mA
I_{LED}	LED _{0,1} DC input current		
I_{SEn}	SEn DC input current		
I_{SEL}	SEL _{0,1,2} DC input current		
I_{FR}	FaultRST DC input current	-1 to 10	mA

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{FR}	FaultRST DC input voltage	7.5	V
I_{SENSE}	MultiSense pin DC output current ($V_{GND} = V_{CC}$ and $V_{SENSE} < 0$ V)	-10	mA
	MultiSense pin DC output current in reverse ($V_{CC} < 0$ V)	20	mA
E_{MAX}	Maximum switching energy (single pulse) ($T_{DEMAG} = 0.4$ ms; $T_{jstart} = 150$ °C)	36	mJ
V_{ESD}	Electrostatic discharge (JEDEC 22A-114F)		
	– INPUT _{0,1,2,3}	4000	V
	– MultiSense	2000	V
	– LED _{0,1} , SEn, SEL _{0,1,2} , FaultRST	4000	V
	– OUTPUT _{0,1,2,3}	4000	V
	– V_{CC}	4000	V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Typ. value	Unit
$R_{thj-board}$	Thermal resistance junction-board (JEDEC JESD 51-5 / 51-8) ⁽¹⁾⁽²⁾	4.9	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-5) ⁽¹⁾⁽³⁾	52.5	
$R_{thj-amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-7) ⁽¹⁾⁽²⁾	18	

1. One channel ON.
2. Device mounted on four-layers 2s2p PCB
3. Device mounted on two-layers 2s0p PCB with 2 cm² heatsink copper trace

2.3 Electrical characteristics

$7 \text{ V} < V_{\text{CC}} < 28 \text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified.

All typical values refer to $V_{\text{CC}} = 13 \text{ V}$; $T_j = 25^\circ\text{C}$, unless otherwise specified.

2.3.1 General electrical specification

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage	$V_{\text{CC}} = 13 \text{ V}$; $V_{\text{INx}} = V_{\text{OUTx}} = V_{\text{FR}} = V_{\text{SEn}} = 0 \text{ V}$; $V_{\text{SEL}0,1,2} = 0 \text{ V}$; $V_{\text{LED}0,1} = 0 \text{ V}$; $T_j = 25^\circ\text{C}$	4	13	28	V
V_{USD}	Undervoltage shutdown				4	
V_{USDReset}	Undervoltage shutdown reset				5	
V_{USDHyst}	Undervoltage shutdown hysteresis			0.3		
V_{clamp}	Clamp voltage	$I_S = 20 \text{ mA}; 25^\circ\text{C} < T_j < 150^\circ\text{C}$	41	46	52	V
		$I_S = 20 \text{ mA}; T_j = -40^\circ\text{C}$	38			V
I_{STBY}	Supply current in standby at $V_{\text{CC}} = 13 \text{ V}^{(1)}$	$V_{\text{CC}} = 13 \text{ V}$; $V_{\text{INx}} = V_{\text{OUTx}} = V_{\text{FR}} = V_{\text{SEn}} = 0 \text{ V}$; $V_{\text{SEL}0,1,2} = 0 \text{ V}$; $V_{\text{LED}0,1} = 0 \text{ V}$; $T_j = 25^\circ\text{C}$			0.5	μA
		$V_{\text{CC}} = 13 \text{ V}$; $V_{\text{INx}} = V_{\text{OUTx}} = V_{\text{FR}} = V_{\text{SEn}} = 0 \text{ V}$; $V_{\text{SEL}0,1,2} = 0 \text{ V}$; $V_{\text{LED}0,1} = 0 \text{ V}$; $T_j = 85^\circ\text{C}^{(2)}$			0.5	μA
		$V_{\text{CC}} = 13 \text{ V}$; $V_{\text{INx}} = V_{\text{OUTx}} = V_{\text{FR}} = V_{\text{SEn}} = 0 \text{ V}$; $V_{\text{SEL}0,1,2} = 0 \text{ V}$; $V_{\text{LED}0,1} = 0 \text{ V}$; $T_j = 125^\circ\text{C}$;			3	μA
$t_{\text{D_STBY}}$	Standby mode blanking time	$V_{\text{CC}} = 13 \text{ V}$; $V_{\text{INx}} = V_{\text{OUTx}} = V_{\text{FR}} = 0 \text{ V}$; $V_{\text{SEL}0,1,2} = 0 \text{ V}$; $V_{\text{LED}0,1} = 0 \text{ V}$; $V_{\text{SEn}} = 5 \text{ V}$ to 0 V	60	300	550	μs
$I_{\text{S(ON)}}$	Supply current	$V_{\text{CC}} = 13 \text{ V}$; $V_{\text{SEn}} = V_{\text{FR}} = V_{\text{SEL}0,1} = 0 \text{ V}$; $V_{\text{INx}} = 5 \text{ V}$; $I_{\text{OUT}0,1,2,3} = 0 \text{ A}$		10	16	mA
$I_{\text{GND(ON)}}$	Control stage current consumption in ON state. All channels active.	$V_{\text{CC}} = 13 \text{ V}$; $V_{\text{SEn}} = 5 \text{ V}$; $V_{\text{FR}} = V_{\text{SEL}0,1} = 0 \text{ V}$; $V_{\text{INx}} = 5 \text{ V}$; $I_{\text{OUT}0,1,2,3} = 2.5 \text{ A}$			18.5	mA
$I_{\text{L(off)}}$	Off-state output current at $V_{\text{CC}} = 13 \text{ V}^{(1)}$	$V_{\text{INx}} = V_{\text{OUTx}} = 0 \text{ V}$; $V_{\text{CC}} = 13 \text{ V}$; $T_j = 25^\circ\text{C}$	0	0.01	0.5	μA
		$V_{\text{INx}} = V_{\text{OUTx}} = 0 \text{ V}$; $V_{\text{CC}} = 13 \text{ V}$; $T_j = 125^\circ\text{C}$	0		3	
V_F	Output - V_{CC} diode voltage ⁽³⁾	$I_{\text{OUT}} = -2.5 \text{ A}$; $T_j = 150^\circ\text{C}$			0.7	V

1. PowerMOS leakage included.

2. Parameter specified by design; not subject to production test.
3. For each channel.

Table 6. Logic Inputs (7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
INPUT_{0,1,2,3} characteristics						
V _{IL}	Input low level voltage				0.9	V
I _{IL}	Low level input current	V _{IN} = 0.9 V	1			µA
V _{IH}	Input high level voltage		2.1			V
I _{IH}	High level input current	V _{IN} = 2.1 V			10	µA
V _{I(hyst)}	Input hysteresis voltage		0.2			V
V _{ICL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.2	V
		I _{IN} = -1 mA		-0.7		
FaultRST characteristics						
V _{FRL}	Input low level voltage				0.9	V
I _{FRL}	Low level input current	V _{IN} = 0.9 V	1			µA
V _{FRH}	Input high level voltage		2.1			V
I _{FRH}	High level input current	V _{IN} = 2.1 V			10	µA
V _{FR(hyst)}	Input hysteresis voltage		0.2			V
V _{FRCL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.5	V
		I _{IN} = -1 mA		-0.7		
SEL_{0,1,2} characteristics (7 V < V_{CC} < 18 V)						
V _{SELL}	Input low level voltage				0.9	V
I _{SELL}	Low level input current	V _{IN} = 0.9 V	1			µA
V _{SELH}	Input high level voltage		2.1			V
I _{SELH}	High level input current	V _{IN} = 2.1 V			10	µA
V _{SEL(hyst)}	Input hysteresis voltage		0.2			V
V _{SELCL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.2	V
		I _{IN} = -1 mA		-0.7		
LED_{0,1} characteristics (7 V < V_{CC} < 18 V)						
V _{LEDL}	Input low level voltage				0.9	V
I _{LEDL}	Low level input current	V _{IN} = 0.9 V	1			µA
V _{LEDH}	Input high level voltage		2.1			V
I _{LEDH}	High level input current	V _{IN} = 2.1 V			10	µA
V _{LED(hyst)}	Input hysteresis voltage		0.2			V

Table 6. Logic Inputs (7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{LEDCL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.2	V
		I _{IN} = -1 mA		-0.7		
SEn characteristics (7 V < V_{CC} < 18 V)						
V _{SEnL}	Input low level voltage				0.9	V
I _{SEnL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{SEnH}	Input high level voltage		2.1			V
I _{SEnH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{SEn(hyst)}	Input hysteresis voltage		0.2			V
V _{SEnCL}	Input clamp voltage	I _{IN} = 1 mA	5.3		7.2	V
		I _{IN} = -1 mA		-0.7		

Table 7. Protections (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T _{TSD}	Shutdown temperature		150	175	200	°C
T _R	Reset temperature ⁽¹⁾		T _{RS} + 1	T _{RS} + 5		
T _{RS}	Thermal reset of fault diagnostic indication	V _{FR} = 0 V; V _{SEn} = 5 V	135			
T _{HYST}	Thermal hysteresis (T _{TSD} -T _R) ⁽¹⁾			5		
ΔT _{J_SD}	Dynamic temperature			60		K
t _{LATCH_RST}	Fault reset time for output unlatch ⁽¹⁾	V _{FR} = 5 V to 0 V; V _{SEn} = 5 V; V _{INx} = 5 V; V _{SEL0,1,2} = 0 V	3	10	20	μs
V _{DEMAG}	Turn-off output voltage clamp	I _{OUT} = 2 A; L = 6 mH; T _j = -40 °C	V _{CC} - 38			V
		I _{OUT} = 2 A; L = 6 mH; T _j = 25 °C to 150 °C	V _{CC} - 41	V _{CC} - 46	V _{CC} - 52	V
V _{ON}	Output voltage drop limitation	I _{OUT} = 0.25 A		20		mV

1. Parameter guaranteed by design and characterization; not subject to production test.

Table 8. MultiSense ($7 \text{ V} < V_{CC} < 18 \text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SENSE_CL}	MultiSense clamp voltage	$V_{SEN} = 0 \text{ V}; I_{SENSE} = 1 \text{ mA}$	-17		-12	V
		$V_{SEN} = 0 \text{ V}; I_{SENSE} = -1 \text{ mA}$		-0.7		V
Current Sense characteristics						
I_{SENSE0}	MultiSense leakage current	MultiSense disabled: $V_{SEN} = 0 \text{ V}$;	0		0.5	μA
		MultiSense disabled: $-1 \text{ V} < V_{SENSE} < 5 \text{ V}^{(1)}$	-0.5		0.5	
		MultiSense enabled: $V_{SEN} = 5 \text{ V}$ All channels ON; $I_{OUTX} = 0 \text{ A}$; Ch _X diagnostic selected; – E.G. Ch ₀ : $V_{IN0} = 5 \text{ V}; V_{IN1,2,3} = 5 \text{ V};$ $V_{SEL0,1,2} = 0 \text{ V}; I_{OUT0} = 0 \text{ A};$ $I_{OUT1,2,3} = 2.5 \text{ A}$	0		2	
		MultiSense enabled: $V_{SEN} = 5 \text{ V}$ Ch _X OFF; Ch _X diagnostic selected; – E.G. Ch ₀ : $V_{IN0} = 0 \text{ V}; V_{IN1,2,3} = 5 \text{ V};$ $V_{SEL0,1,2} = 0 \text{ V}; I_{OUT0} = 0 \text{ A};$ $I_{OUT1,2,3} = 2.5 \text{ A}$	0		2	
$V_{OUT_MSD}^{(1)}$	Output Voltage for MultiSense shutdown	$V_{SEN} = 5 \text{ V}; R_{SENSE} = 2.7 \text{ k}\Omega$ – E.g. Ch ₀ : $V_{IN0} = 5 \text{ V}; V_{SEL0,1,2} = 0 \text{ V};$ $I_{OUT0} = 2.5 \text{ A}$		5		V
V_{SENSE_SAT}	Multisense saturation voltage	$V_{CC} = 7 \text{ V}; R_{SENSE} = 2.7 \text{ K};$ $V_{SEN} = 5 \text{ V}; V_{IN0} = 5 \text{ V}; V_{SEL0,1,2} = 0 \text{ V};$ $I_{OUT0} = 4.5 \text{ A}; T_j = 150^\circ\text{C}$	5			V
$I_{SENSE_SAT}^{(1)}$	CS saturation current	$V_{CC} = 7 \text{ V}; V_{SENSE} = 4 \text{ V}; V_{IN0} = 5 \text{ V};$ $V_{SEN} = 5 \text{ V}; V_{SEL0,1,2} = 0 \text{ V}; T_j = 150^\circ\text{C}$	4			mA
$I_{OUT_SAT_BULB}^{(1)}$	Output saturation current in BULB mode	$V_{CC} = 7 \text{ V}; V_{SENSE} = 4 \text{ V}; V_{IN0} = 5 \text{ V};$ $V_{SEN} = 5 \text{ V}; V_{SEL0,1,2} = 0 \text{ V}; T_j = 150^\circ\text{C}$	8			A
$I_{OUT_SAT_LED}^{(1)}$	Output saturation current in LED mode	$V_{CC} = 7 \text{ V}; V_{SENSE} = 4 \text{ V}; V_{IN0} = 5 \text{ V};$ $V_{SEN} = 5 \text{ V}; V_{SEL0,1,2} = 0 \text{ V}; T_j = 150^\circ\text{C}$	2.3			A
OFF-state diagnostic						
V_{OL}	OFF state open load voltage detection threshold	$V_{SEN} = 5 \text{ V}; \text{Ch}_X \text{ OFF}; \text{Ch}_X \text{ diagnostic selected}$ – E.G: Ch ₀ $V_{IN0} = 0 \text{ V}; V_{SEL0,1,2} = 0 \text{ V}$	2	3	4	V
$I_{L(off2)}$	OFF state output sink current	$V_{IN} = 0 \text{ V}; V_{OUT} = V_{OL};$ $T_j = -40^\circ\text{C} \text{ to } 125^\circ\text{C}$	-100		-15	μA

Table 8. MultiSense (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{DSTKON}	OFF state diagnostic delay time from falling edge of INPUT (see <i>Figure 35</i>)	V _{SEN} = 5 V; Ch _X ON to OFF transition; Ch _X diagnostic selected – E.G: Ch ₀ V _{IN0} = 5 V to 0 V; V _{SEL0,1,2} = 0 V; V _{OUT0} > 4 V	100	350	700	μs
t _{D_OL_V}	Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn	V _{INx} = 0 V; V _{FR} = 0 V; V _{SEL0,1,2} = 0 V; V _{OUT0} = 4 V; V _{SEN} = 0 V to 5 V			60	μs
t _{D_VOL}	OFF state diagnostic delay time from rising edge of V _{OUT}	V _{SEN} = 5V; Ch _X OFF; Ch _X diagnostic selected – E.G: Ch ₀ V _{IN0} = 0 V; V _{SEL0,1,2} = 0 V; V _{OUT0} = 0 V to 4 V		5	30	μs
Chip temperature analog feedback						
V _{SENSE_TC}	MultiSense output voltage proportional to chip temperature	V _{SEN} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; V _{SEL2} = 5 V; R _{SENSE} = 1 kΩ; V _{INx} = 0 V; T _j = -40°C	2.325	2.41	2.495	V
		V _{SEN} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; V _{SEL2} = 5 V; R _{SENSE} = 1 kΩ; V _{INx} = 0 V; T _j = 25°C	1.985	2.07	2.155	V
		V _{SEN} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; V _{SEL2} = 5 V; R _{SENSE} = 1 kΩ; V _{INx} = 0 V; T _j = 125°C	1.435	1.52	1.605	V
dV _{SENSE_TC} /dT ⁽²⁾	Temperature coefficient	T _j = -40°C to 150°C		-5.5		mV/K
Transfer function		V _{SENSE_TC} (T) = V _{SENSE_TC} (T ₀) + dV _{SENSE_TC} /dT * (T-T ₀)				
V_{CC} supply voltage analog feedback						
V _{SENSE_VCC}	MultiSense output voltage proportional to V _{CC} supply voltage	V _{CC} = 13 V; V _{SEN} = 5 V; V _{SEL0,1,2} = 5 V; V _{INx} = 0 V; R _{SENSE} = 1 kΩ	3.16	3.23	3.3	V
Transfer function ⁽²⁾		V _{SENSE_VCC} = V _{CC} / 4				
Fault diagnostic feedback (see <i>Table 15</i>)						
V _{SENSEH}	MultiSense output voltage in fault condition	V _{CC} = 13 V; R _{SENSE} = 1 kΩ	5		6.6	V
I _{SENSEH}	MultiSense output current in fault condition	V _{CC} = 13 V; V _{SENSE} = 5 V	7	20	30	mA
MultiSense timings (Chip Temperature Sense mode - see <i>Figure 37</i>)						
t _{DSENSE3H}	V _{SENSE_TC} settling time from rising edge of SEn	V _{SEN} = 0 V to 5 V; V _{SEL0} = V _{SEL1} = 0 V; V _{SEL2} = 5 V; R _{SENSE} = 1 kΩ			60	μs

Table 8. MultiSense (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{DSENSE3L}	V _{SENSE_TC} disable delay time from falling edge of SEn	V _{SEn} = 5 V to 0 V; V _{SEL0} = V _{SEL1} = 0 V; V _{SEL2} = 5 V; R _{SENSE} = 1 kΩ			20	μs
MultiSense timings (V_{CC} Voltage Sense mode - see Figure 37)						
t _{DSENSE4H}	V _{SENSE_VCC} settling time from rising edge of SEn	V _{SEn} = 0 V to 5 V; V _{SEL0} = V _{SEL1} = V _{SEL2} = 5 V; R _{SENSE} = 1 kΩ			60	μs
t _{DSENSE4L}	V _{SENSE_VCC} disable delay time from falling edge of SEn	V _{SEn} = 5 V to 0 V; V _{SEL0} = V _{SEL1} = V _{SEL2} = 5 V; R _{SENSE} = 1 kΩ			20	μs
MultiSense Timings (Multiplexer transition times)⁽³⁾						
t _{D_XtoY}	MultiSense transition delay from Ch _X to Ch _Y	V _{IN2} = 5 V; V _{IN3} = 5 V; V _{SEn} = 5 V; V _{SEL0} = 0 V to 5 V; V _{SEL1} = 5 V; V _{SEL2} = 0 V; I _{OUT2} = 0 A; I _{OUT3} = 2.5 A; R _{SENSE} = 1 kΩ			20	μs
t _{D_CstoTC}	MultiSense transition delay from current sense to T _C sense	V _{IN0} = 5 V; V _{SEn} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = V _{SEL2} = 0 V to 5 V; I _{OUT0} = 1.25 A; R _{SENSE} = 1 kΩ			60	μs
t _{D_TCtoCS}	MultiSense transition delay from T _C sense to current sense	V _{IN0} = 5 V; V _{SEn} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = V _{SEL2} = 5 V to 0 V; I _{OUT0} = 1.25 A; R _{SENSE} = 1 kΩ			20	μs
t _{D_CstoVCC}	MultiSense transition delay from current sense to V _{CC} sense	V _{IN2} = 5 V; V _{SEn} = 5 V; V _{SEL0} = 5 V; V _{SEL1} = 5 V; V _{SEL2} = 0 V to 5 V; I _{OUT2} = 1.25 A; R _{SENSE} = 1 kΩ			60	μs
t _{D_VCCtoCS}	MultiSense transition delay from V _{CC} sense to current sense	V _{IN2} = 5 V; V _{SEn} = 5 V; V _{SEL1} = 5 V; V _{SEL0} = V _{SEL2} = 5 V to 0 V; I _{OUT2} = 1.25 A; R _{SENSE} = 1 kΩ			20	μs
t _{D_TCtoVCC}	MultiSense transition delay from T _C sense to V _{CC} sense	V _{SEn} = 5 V; V _{SEL1,2} = 5 V; V _{SEL0} = 0 V to 5 V; R _{SENSE} = 1 kΩ			20	μs
t _{D_VCCtoTC}	MultiSense transition delay from V _{CC} sense to T _C sense	V _{SEn} = 5 V; V _{SEL1,2} = 5 V; V _{SEL0} = 5 V to 0 V; R _{SENSE} = 1 kΩ			20	μs
t _{D_CstoVSENSEH}	MultiSense transition delay from stable current sense on Ch _X to V _{SENSEH} on Ch _Y	V _{IN0} = 5 V; V _{IN1} = 0 V; V _{OUT1} > 4 V; V _{SEn} = 5 V; V _{SEL2} = 0 V; V _{SEL1} = 0 V; V _{SEL0} = 0 V to 5 V; I _{OUT0} = 2.5 A; R _{SENSE} = 1 kΩ			60	μs

1. Parameter guaranteed by design and characterization; not subject to production test.

2. V_{CC} sensing and T_C sensing are referred to GND potential.

3. Transition delay are measured up to +/- 10% of final conditions.

2.3.2 Bulb mode (default)

Table 9. Power section in Bulb Mode ($7 \text{ V} < V_{CC} < 28 \text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{ON_0,1,2,3_BULB}$	On-state resistance in Bulb Mode Ch0, Ch1, Ch2 and Ch3	$I_{OUT} = 2.5 \text{ A}; T_j = 25^\circ\text{C}$		40		$\text{m}\Omega$
		$I_{OUT} = 2.5 \text{ A}; T_j = 150^\circ\text{C}$			80	
		$I_{OUT} = 2.5 \text{ A}; V_{CC} = 4 \text{ V}; T_j = 25^\circ\text{C}$			60	
$R_{ON_REV_0,1,2,3}$	On-state resistance in Reverse Battery Ch0, Ch1, Ch2 and Ch3	$V_{CC} = -13 \text{ V}$ $I_{OUT} = -2.5 \text{ A}; T_j = 25^\circ\text{C}$		40		$\text{m}\Omega$
$I_{LIMH_0,1,2,3_BULB}^{(1)}$	DC short circuit current in Bulb Mode Ch0, Ch1, Ch2 and Ch3	$V_{CC} = 13 \text{ V}$	24	34	48	A
		$4 \text{ V} < V_{CC} < 18 \text{ V}^{(2)}$			48	
$I_{LIML_0,1,2,3_BULB}$	Short circuit current during thermal cycling in Bulb Mode Ch0, Ch1, Ch2 and Ch3	$V_{CC} = 13 \text{ V}$ $T_R < T_j < T_{TSD}$		9		
$V_{ON_0,1,2,3_BULB}$	Output voltage drop limitation in Bulb Mode Ch0, Ch1, Ch2 and Ch3	$I_{OUT} = 0.25 \text{ A}$		20		mV

1. Parameter guaranteed by an indirect test sequence.
2. Parameter guaranteed by design and characterization; not subject to production test.

Table 10. Switching in Bulb Mode ($V_{CC} = 13 \text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Channel 0, 1, 2 and 3						
$t_{d(on)_0,1,2,3}^{(1)}$	Turn-on delay time at $T_j = 25^\circ\text{C}$	$R_L = 5.2 \Omega$	10	60	120	μs
$t_{d(off)_0,1,2,3}^{(1)}$	Turn-off delay time at $T_j = 25^\circ\text{C}$	$R_L = 5.2 \Omega$	10	50	100	
$(dV_{OUT}/dt)_{on_0,1,2,3}^{(1)}$	Turn-on voltage slope at $T_j = 25^\circ\text{C}$	$R_L = 5.2 \Omega$	0.1	0.5	0.7	$\text{V}/\mu\text{s}$
$(dV_{OUT}/dt)_{off_0,1,2,3}^{(1)}$	Turn-off voltage slope at $T_j = 25^\circ\text{C}$	$R_L = 5.2 \Omega$	0.1	0.5	0.7	
$W_{ON_0,1,2,3}$	Switching energy losses at turn-on (t_{won})	$R_L = 5.2 \Omega$	—	0.2	0.52 ⁽²⁾	mJ

Table 10. Switching in Bulb Mode ($V_{CC} = 13\text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$W_{OFF_0,1,2,3}$	Switching energy losses at turn-off (t_{woff})	$R_L = 5.2\ \Omega$	—	0.2	0.5 ⁽²⁾	mJ
$t_{SKEW_0,1,2,3}^{(1)}$	Differential pulse skew ($t_{PHL} - t_{PLH}$)	$R_L = 5.2\ \Omega$	-65	-15	35	μs

1. See *Figure 35: Switching times and Pulse skew*.

2. Parameter guaranteed by design and characterization, not subject to production test.

Table 11. MultiSense in Bulb Mode ($7\text{ V} < V_{CC} < 18\text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Current sense characteristics						
Channel 0, 1, 2 and 3						
$K_{OL_CH0,1_B}$	I_{OUT}/I_{SENSE}	$I_{OUT} = 10\text{ mA}; V_{SENSE} = 0.5\text{ V}; V_{SEN} = 5\text{ V}$	430			
$K_{OL_CH2,3_B}$	I_{OUT}/I_{SENSE}	$I_{OUT} = 10\text{ mA}; V_{SENSE} = 0.5\text{ V}; V_{SEN} = 5\text{ V}$	430			
$dK_{cal}/K_{cal}^{(1)(2)}$	Current sense ratio drift at calibration point	$I_{CAL} = 30\text{ mA}; I_{OUT} = 10\text{ mA to } 50\text{ mA}; V_{SENSE} = 0.5\text{ V}; V_{SEN} = 5\text{ V}$	-35		35	%
$K_{LED_CH0,1_B}$	I_{OUT}/I_{SENSE}	$I_{OUT} = 0.05\text{ A}; V_{SENSE} = 0.5\text{ V}; V_{SEN} = 5\text{ V}$	720	1440	2160	
$K_{LED_CH2,3_B}$	I_{OUT}/I_{SENSE}	$I_{OUT} = 0.05\text{ A}; V_{SENSE} = 0.5\text{ V}; V_{SEN} = 5\text{ V}$	720	1440	2160	
$K_0_CH0,1_B$	I_{OUT}/I_{SENSE}	$I_{OUT} = 0.25\text{ A}; V_{SENSE} = 0.5\text{ V}; V_{SEN} = 5\text{ V}$	930	1550	2170	
$K_0_CH2,3_B$	I_{OUT}/I_{SENSE}	$I_{OUT} = 0.25\text{ A}; V_{SENSE} = 0.5\text{ V}; V_{SEN} = 5\text{ V}$	930	1550	2170	
$dK_0/K_0^{(1)(2)}$	Current sense ratio drift	$I_{OUT} = 0.25\text{ A}; V_{SENSE} = 0.5\text{ V}; V_{SEN} = 5\text{ V}$	-20		20	%
$K_1_CH0,1_B$	I_{OUT}/I_{SENSE}	$I_{OUT} = 0.5\text{ A}; V_{SENSE} = 4\text{ V}; V_{SEN} = 5\text{ V}$	1110	1590	2070	
$K_1_CH2,3_B$	I_{OUT}/I_{SENSE}	$I_{OUT} = 0.5\text{ A}; V_{SENSE} = 4\text{ V}; V_{SEN} = 5\text{ V}$	1085	1550	2015	
$dK_1/K_1^{(1)(2)}$	Current sense ratio drift	$I_{OUT} = 0.5\text{ A}; V_{SENSE} = 4\text{ V}; V_{SEN} = 5\text{ V}$	-15		15	%
$K_2_CH0,1_B$	I_{OUT}/I_{SENSE}	$I_{OUT} = 2\text{ A}; V_{SENSE} = 4\text{ V}; V_{SEN} = 5\text{ V}$	1160	1450	1740	
$K_2_CH2,3_B$	I_{OUT}/I_{SENSE}	$I_{OUT} = 2\text{ A}; V_{SENSE} = 4\text{ V}; V_{SEN} = 5\text{ V}$	1130	1410	1690	

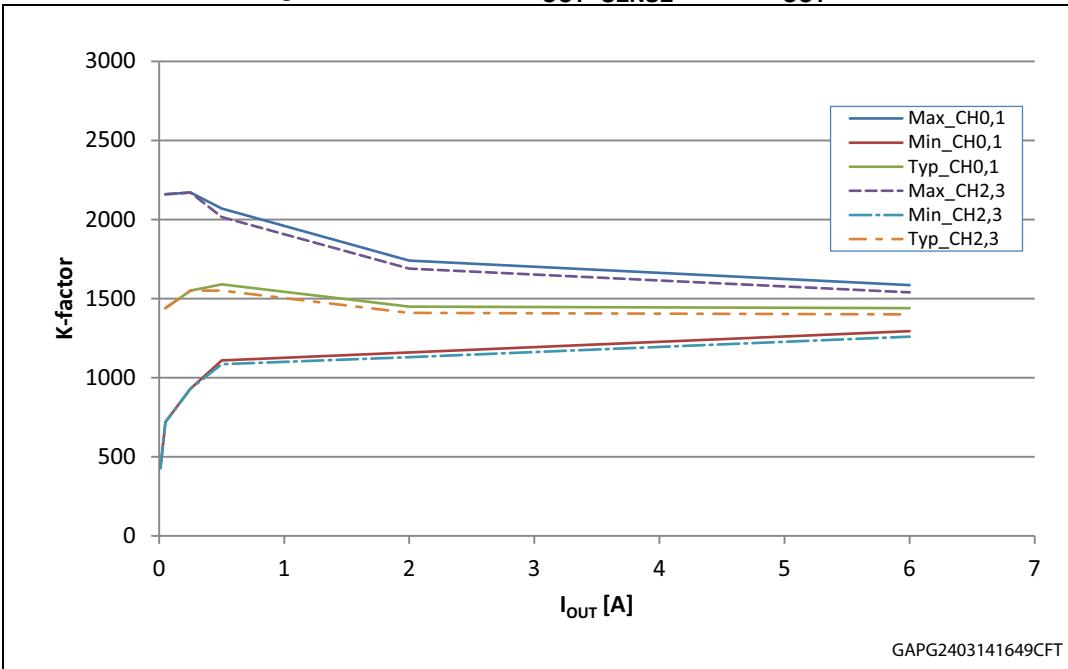
Table 11. MultiSense in Bulb Mode ($7 \text{ V} < V_{CC} < 18 \text{ V}$; $-40^\circ\text{C} < T_j < 150^\circ\text{C}$) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$dK_2/K_2^{(1)(2)}$	Current sense ratio drift	$I_{OUT} = 2 \text{ A}; V_{SENSE} = 4 \text{ V}; V_{SEn} = 5 \text{ V}$	-10		10	%
$K_{3_CH0,1_B}$	I_{OUT}/I_{SENSE}	$I_{OUT} = 6 \text{ A}; V_{SENSE} = 4 \text{ V}; V_{SEn} = 5 \text{ V}$	1295	1440	1585	
$K_{3_CH2,3_B}$	I_{OUT}/I_{SENSE}	$I_{OUT} = 6 \text{ A}; V_{SENSE} = 4 \text{ V}; V_{SEn} = 5 \text{ V}$	1260	1400	1540	
$dK_3/K_3^{(1)(2)}$	Current sense ratio drift	$I_{OUT} = 6 \text{ A}; V_{SENSE} = 4 \text{ V}; V_{SEn} = 5 \text{ V}$	-5		5	%

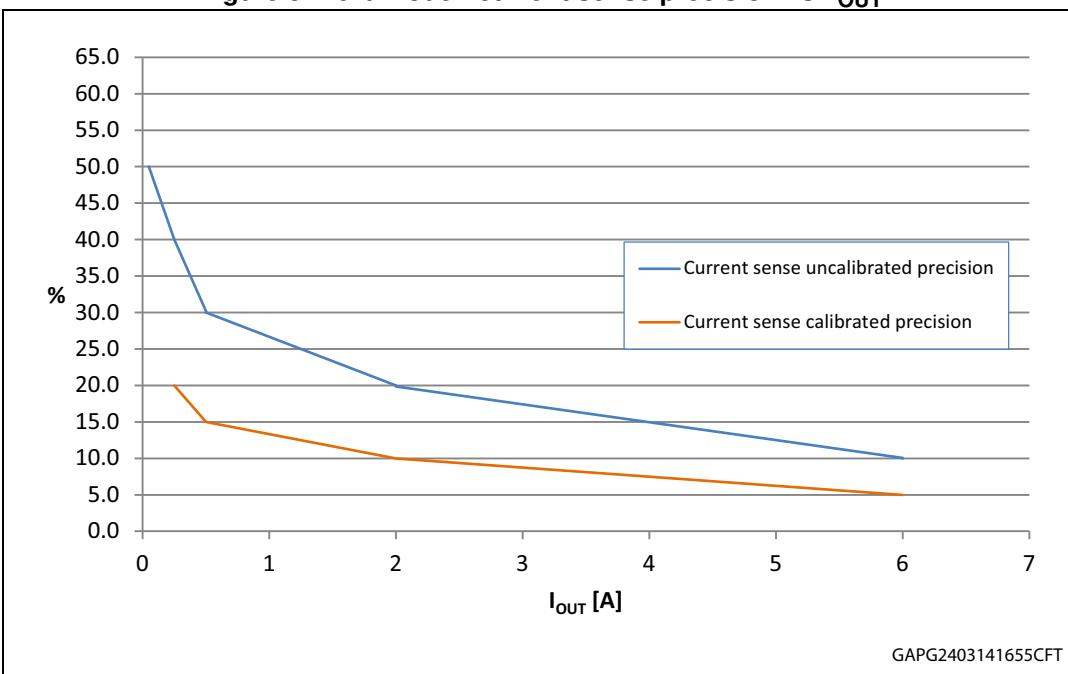
MultiSense timings (Current Sense mode see [Figure 36](#))**Channel 0, 1, 2 and 3**

$t_{DSENSE1H}$	Current sense settling time from rising edge of SEn	$V_{IN} = 5 \text{ V}; V_{SEn} = 0 \text{ V to } 5 \text{ V}; R_{SENSE} = 1 \text{ k}\Omega; R_L = 5.2 \Omega$			60	μs
$t_{DSENSE1L}$	Current sense disable delay time from falling edge of SEn	$V_{SEn} = 5 \text{ V to } 0 \text{ V}; R_{SENSE} = 1 \text{ k}\Omega; R_L = 5.2 \Omega$		5	20	μs
$t_{DSENSE2H}$	Current sense settling time from rising edge of INPUT	$V_{IN} = 0 \text{ V to } 5 \text{ V}; V_{SEn} = 5 \text{ V}; R_{SENSE} = 1 \text{ k}\Omega; R_L = 5.2 \Omega$		100	250	μs
$\Delta t_{DSENSE2H}$	Current sense settling time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	$V_{IN} = 5 \text{ V}; V_{SEn} = 5 \text{ V}; R_{SENSE} = 1 \text{ k}\Omega; R_L = 5.2 \Omega$			100	μs
$t_{DSENSE2L}$	Current sense turn-off delay time from falling edge of INPUT	$V_{IN} = 5 \text{ V to } 0 \text{ V}; V_{SEn} = 5 \text{ V}; R_{SENSE} = 1 \text{ k}\Omega; R_L = 5.2 \Omega$		50	250	μs

1. Parameter specified by design; not subject to production test.
2. All values refer to $V_{CC} = 13 \text{ V}$; $T_j = 25^\circ\text{C}$, unless otherwise specified.

Figure 4. Bulb Mode - I_{OUT}/I_{SENSE} versus I_{OUT} 

GAPG2403141649CFT

Figure 5. Bulb Mode - current sense precision vs. I_{OUT} 

GAPG2403141655CFT

2.4 Electrical characteristics curves - Bulb Mode

Figure 6. OFF-state output current

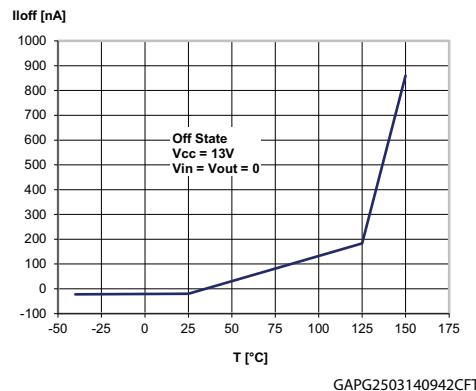


Figure 7. Standby current

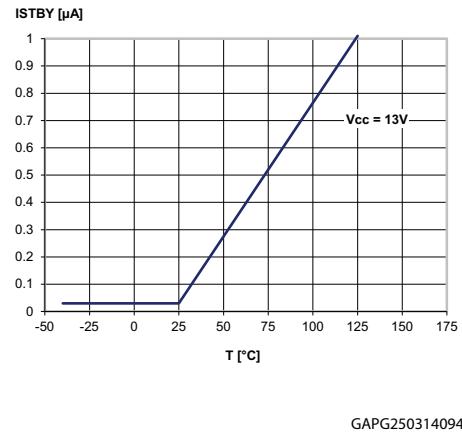


Figure 8. $I_{GND(ON)}$ vs. I_{out}

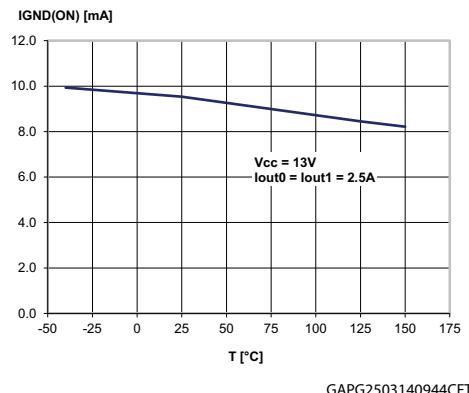


Figure 9. Logic Input high level voltage

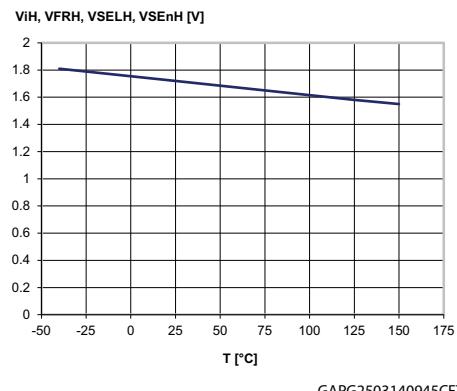


Figure 10. Logic Input low level voltage

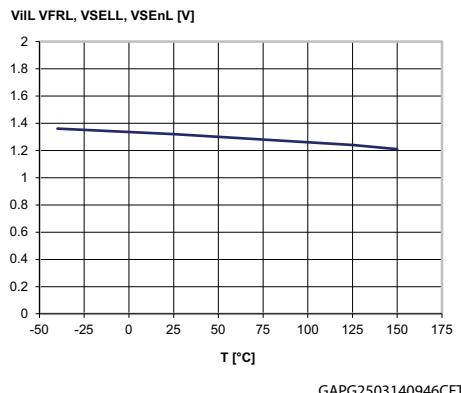


Figure 11. High level logic input current

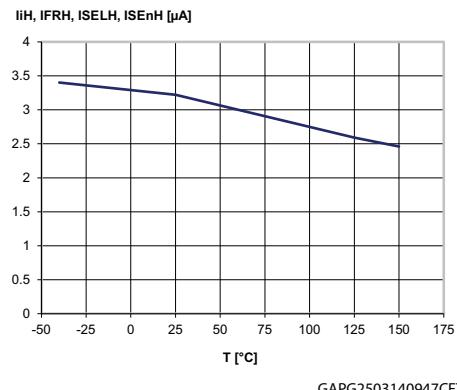


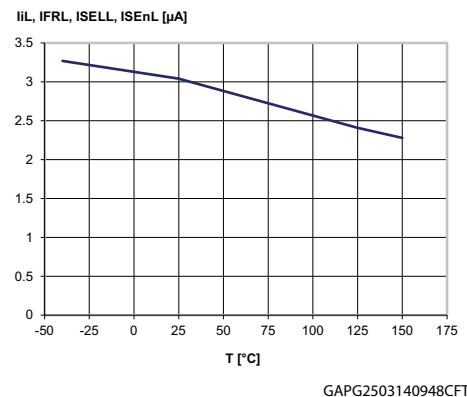
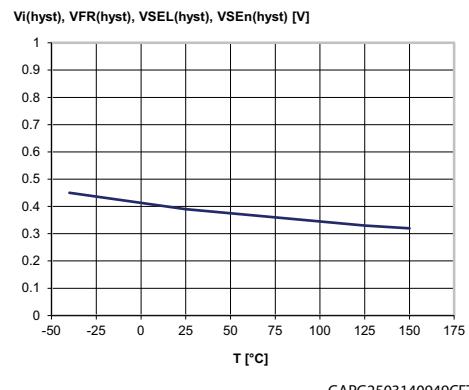
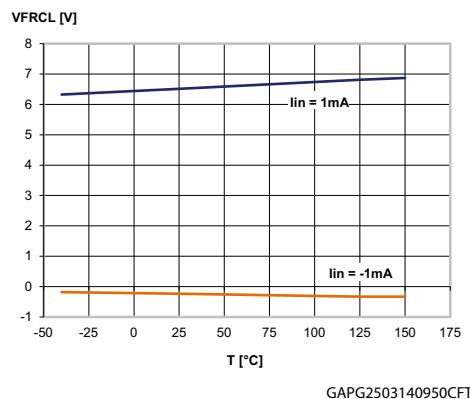
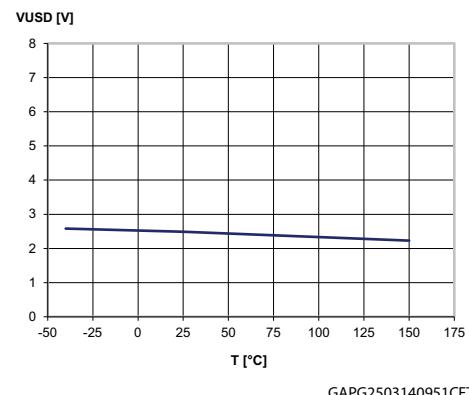
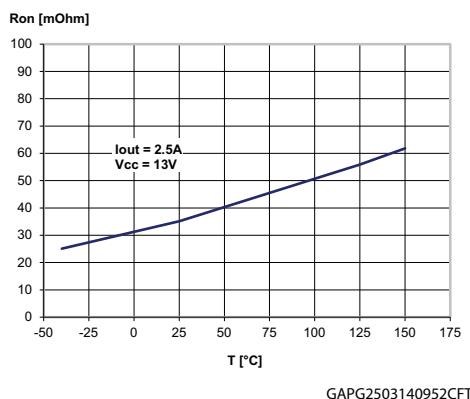
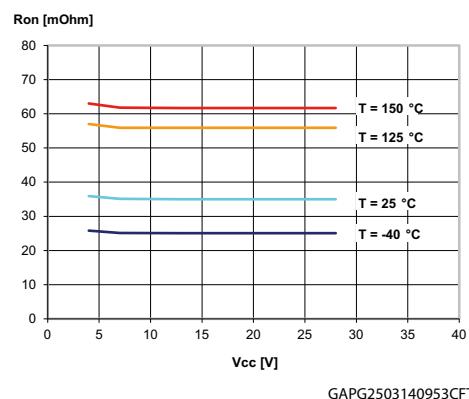
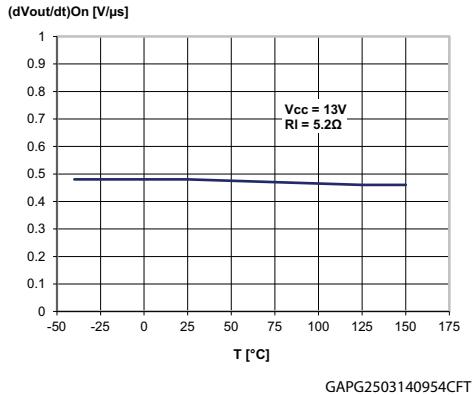
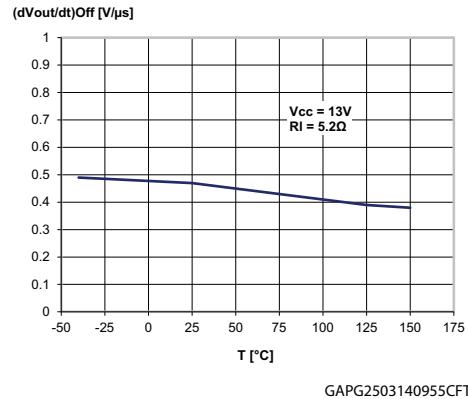
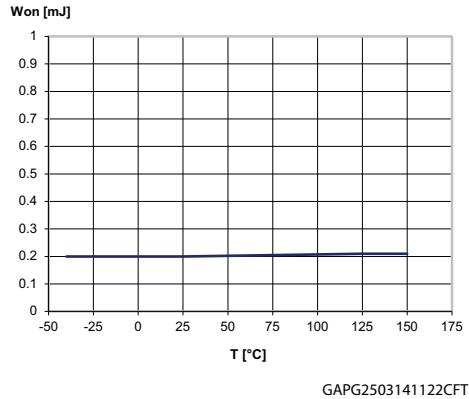
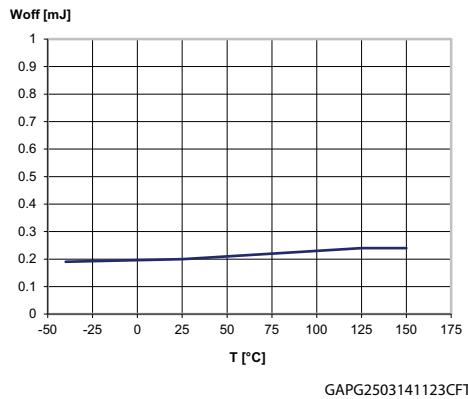
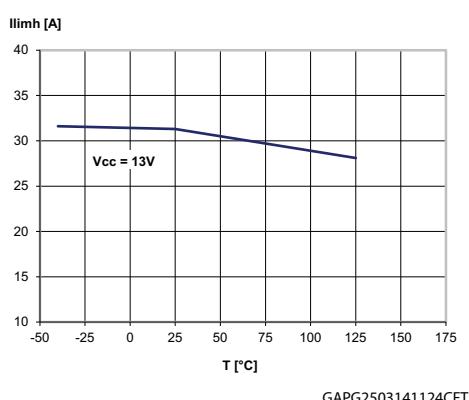
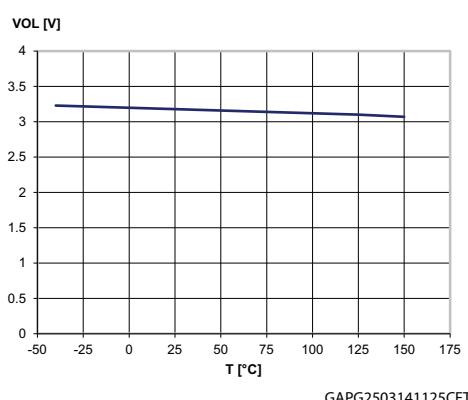
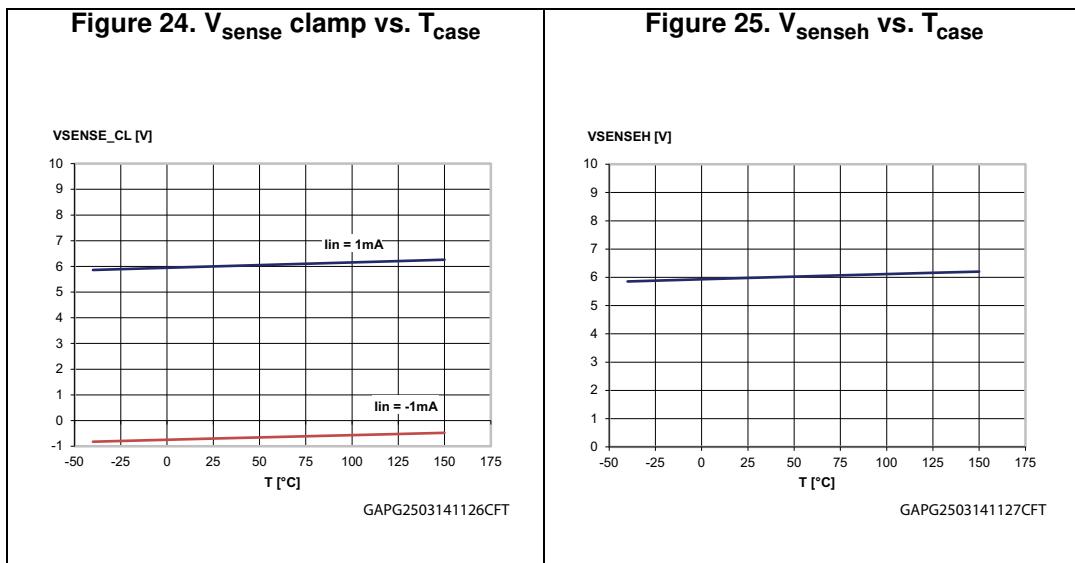
Figure 12. Low level logic input current**Figure 13. Logic Input hysteresis voltage****Figure 14. FaultRST Input clamp voltage****Figure 15. Undervoltage shutdown****Figure 16. On-state resistance vs. T_{case}****Figure 17. On-state resistance vs. V_{CC}**

Figure 18. Turn-on voltage slope**Figure 19. Turn-off voltage slope****Figure 20. Won vs. T_{case}** **Figure 21. Woff vs. T_{case}** **Figure 22. I_{LIMH} vs. T_{case}** **Figure 23. OFF-state open-load voltage detection threshold**



2.4.1 LED Mode (Channel 0 and 1)

Table 12. Switching in LED Mode ($V_{CC} = 13\text{ V}$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)_0,1_LED}^{(1)}$	Turn-on delay time at $T_j = 25\text{ }^{\circ}\text{C}$	$R_L = 22.8\text{ }\Omega$	10	65	120	μs
$t_{d(off)_0,1_LED}^{(1)}$	Turn-off delay time at $T_j = 25\text{ }^{\circ}\text{C}$	$R_L = 22.8\text{ }\Omega$	10	40	100	μs
$(dV_{OUT}/dt)_{on_0,1_LED}^{(1)}$	Turn-on voltage slope at $T_j = 25\text{ }^{\circ}\text{C}$	$R_L = 22.8\text{ }\Omega$	0.2	0.5	0.8	V/μs
$(dV_{OUT}/dt)_{off_0,1_LED}^{(1)}$	Turn-off voltage slope at $T_j = 25\text{ }^{\circ}\text{C}$	$R_L = 22.8\text{ }\Omega$	0.1	0.5	0.7	V/μs
$W_{ON_0,1_LED}$	Switching energy losses at turn-on (t_{won})	$R_L = 22.8\text{ }\Omega$	—	0.04	0.1 ⁽²⁾	mJ
$W_{OFF_0,1_LED}$	Switching energy losses at turn-off (t_{woff})	$R_L = 22.8\text{ }\Omega$	—	0.045	0.11 ⁽²⁾	mJ
$t_{SKEW_0,1_LED}^{(1)}$	Differential Pulse skew ($t_{PHL} - t_{PLH}$)	$R_L = 22.8\text{ }\Omega$	-75	-25	25	μs

- See [Figure 35: Switching times and Pulse skew](#).
- Parameter guaranteed by design and characterization, not subject to production test.

Table 13. Power section in LED Mode (7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R _{ON_0,1_LED}	On-state resistance in LED Mode Ch0 and Ch1	I _{OUT} = 0.57 A; T _j = 25°C		140		mΩ
		I _{OUT} = 0.57 A; T _j = 150°C			280	
		I _{OUT} = 0.57 A; V _{CC} = 5 V; T _j = 25°C			210	
I _{LIMH_0,1_LED} ⁽¹⁾	DC short circuit current in Bulb Mode Ch0 and Ch1	V _{CC} = 13 V	5.5	8	11	A
		4 V < V _{CC} < 18 V ⁽²⁾				
I _{LIML_0,1_LED}	Short circuit current during thermal cycling in Bulb Mode Ch0 and Ch1	V _{CC} = 13 V; T _R < T _j < T _{TSD}		2		A
V _{ON_0,1_LED}	Output voltage drop limitation in LED Mode Ch0 and Ch1	I _{OUT} = 0.07 A		20		mV

1. Parameter guaranteed by an indirect test sequence.
2. Parameter guaranteed by design and characterization; not subject to production test.

Table 14. MultiSense in LED Mode (7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K _{OL}	I _{OUT} /I _{SENSE}	I _{OUT} = 0.01 A; V _{SENSE} = 0.5 V; V _{SENSE} = 5 V	120			
dK _{cal} /K _{cal} ⁽¹⁾⁽²⁾	Current sense ratio drift at calibration point	I _{cal} = 17.5 mA; I _{OUT} = 10 mA to 25 mA; V _{SENSE} = 0.5 V; V _{SENSE} = 5 V	-30		30	%
K _{LED}	I _{OUT} /I _{SENSE}	I _{OUT} = 0.025 A; V _{SENSE} = 0.5 V; V _{SENSE} = 5 V	150	380	610	
dK _{LED} /K _{LED} ⁽¹⁾⁽²⁾	Current sense ratio drift	I _{OUT} = 0.025 A; V _{SENSE} = 0.5 V; V _{SENSE} = 5 V	-25		25	%
K _{0_CH0,1_L}	I _{OUT} /I _{SENSE}	I _{OUT} = 0.15 A; V _{SENSE} = 4 V; V _{SENSE} = 5 V	240	405	570	
dK ₀ /K ₀ ⁽¹⁾⁽²⁾	Current sense ratio drift	I _{OUT} = 0.15 A; V _{SENSE} = 4 V; V _{SENSE} = 5 V	-15		15	%
K _{1_CH0,1_L}	I _{OUT} /I _{SENSE}	I _{OUT} = 0.7 A; V _{SENSE} = 4 V; V _{SENSE} = 5 V	300	380	460	
dK ₁ /K ₁ ⁽¹⁾⁽²⁾	Current sense ratio drift	I _{OUT} = 0.7 A; V _{SENSE} = 4 V; V _{SENSE} = 5 V	-8		8	%
MultiSense timings (Current Sense mode - see Figure 36)						
t _{DSENSE1H}	Current sense settling time from rising edge of SEn	V _N = 5 V; V _{SENSE} = 0 V to 5 V; R _{SENSE} = 1 kΩ; R _L = 22.8 Ω			60	μs