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VP2450

P-Channel Enhancement-Mode Vertical DMOS FET

Features

- Free from Secondary Breakdown
- Low Power Drive Requirement
- Ease of Paralleling
- Low C_{ISS} and Fast Switching Speeds
- High Input Impedance and High Gain
- Excellent Thermal Stability
- Integral Source-drain Diode

Applications

- Motor Controls
- Converters
- Amplifiers
- Switches
- Power Supply Circuits
- Drivers: Relays, Hammers, Solenoids, Lamps, Memory, Displays, Bipolar Transistors, etc.

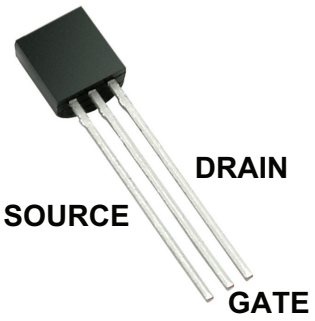
General Description

The VP2450 is a low-threshold, Enhancement-mode (normally-off) transistor that utilizes a vertical Double-diffused Metal-Oxide Semiconductor (DMOS) structure and a well-proven silicon gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

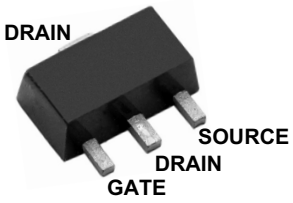
This Vertical DMOS Field-Effect Transistor (FET) is ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Types

TO-92



SOT-89



See Table 3-1 for pin information.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Drain-to-source Voltage ..... BV_{DSS}
Drain-to-gate Voltage ..... BV_{DGS}
Gate-to-source Voltage ..... ±20V
Operating and Storage Temperatures ..... –55°C to +150°C

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: For all specifications, $T_A = T_J = +25°C$ unless otherwise noted.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
DC PARAMETER (Note 1 unless otherwise stated)						
Drain-to-source Breakdown Voltage	BV_{DSS}	–500	—	—	V	V_{GS} = 0V, I_D = –250 µA
Gate Threshold Voltage	$V_{GS(th)}$	–1.5	—	–3.5	V	$V_{GS} = V_{DS}$, I_D = –1 mA
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	—	–4.8	mV/°C	$V_{GS} = V_{DS}$, I_D = –1 mA (Note 2)
Gate Body Leakage Current	I_{GSS}	—	—	–100	nA	V_{GS} = ±20V, V_{DS} = 0V
Zero Gate Voltage Drain Current	I_{DSS}	—	—	–10	µA	V_{GS} = 0V, V_{DS} = Maximum Rating
		—	—	–1	mA	V_{DS} = 0.8 Maximum Rating, V_{GS} = 0V, T_A = 125°C (Note 2)
On-state Drain Current	$I_{D(ON)}$	–75	—	—	mA	V_{GS} = –4.5V, V_{DS} = –15V
		–200	—	—		V_{GS} = –10V, V_{DS} = –15V
Static Drain-to-source On-state Resistance	$R_{DS(ON)}$	—	—	35	Ω	V_{GS} = –4.5V, I_D = –50 mA
		—	—	30		V_{GS} = –10V, I_D = –100 mA
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	—	0.75	%/°C	V_{GS} = –10V, I_D = –100 mA (Note 2)
AC PARAMETER (Note 2)						
Forward Transconductance	G_{FS}	150	320	—	mmho	V_{DS} = –15V, I_D = –100 mA
Input Capacitance	C_{ISS}	—	—	190	pF	V_{GS} = 0V, V_{DS} = –25V, f = 1 MHz
Common Source Output Capacitance	C_{OSS}	—	—	75		
Reverse Transfer Capacitance	C_{RSS}	—	—	20		
Turn-on Delay Time	$t_{d(ON)}$	—	—	10	ns	V_{DD} = –25V, I_D = –200 mA, R_{GEN} = 25Ω
Rise Time	t_r	—	—	25		
Turn-off Delay Time	$t_{d(OFF)}$	—	—	45		
Fall Time	t_f	—	—	25		
DIODE PARAMETER						
Diode Forward Voltage Drop	V_{SD}	—	—	–1.8	V	V_{GS} = 0V, I_{SD} = –100 mA (Note 1)
Reverse Recovery Time	t_{rr}	—	300	—	ns	V_{GS} = 0V, I_{SD} = –100 mA (Note 2)

Note 1: All DC parameters are 100% tested at 25°C unless otherwise stated. (Pulse test: 300 µs pulse, 2% duty cycle)

2: Specification is obtained by characterization and is not 100% tested.

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise noted, for all specifications $T_A = T_J$ = +25°C.						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
TEMPERATURE RANGE						
Operating Temperature	T_A	–55	—	+150	°C	
Storage Temperature	T_S	–55	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
TO-92	θ_{JA}	—	132	—	°C/W	
SOT-89	θ_{JA}	—	133	—	°C/W	

THERMAL CHARACTERISTICS

Package	**I_D (Note 1) (Continuous) (mA)**	**I_D (Pulsed) (mA)**	**Power Dissipation at T_A= 25°C (W)**	**I_{DR} (Note 1) (mA)**	**I_{DRM} (mA)**
TO-92	–100	–300	0.74	–100	–300
SOT-89	–160	–800	1.6 (**Note 2**)	–160	–800

Note 1: I_D (continuous) is limited by maximum T_J.

2: Mounted on FR5 board, 25 mm x 25 mm X 1.57 mm

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

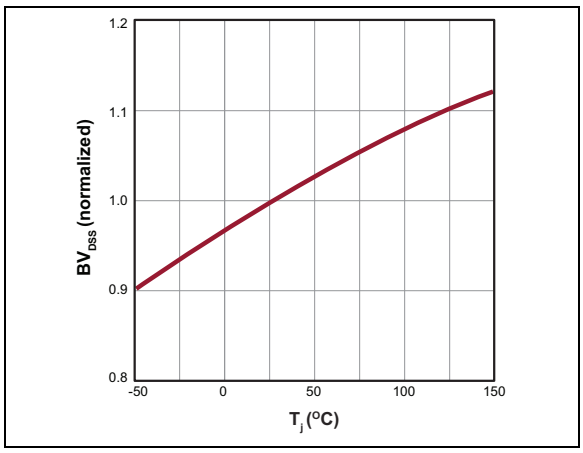


FIGURE 2-1: *BV_{DSS} Variation with Temperature.*

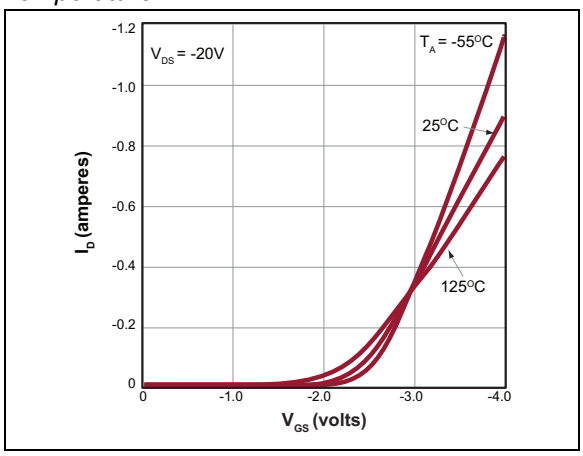


FIGURE 2-2: *Transfer Characteristics.*

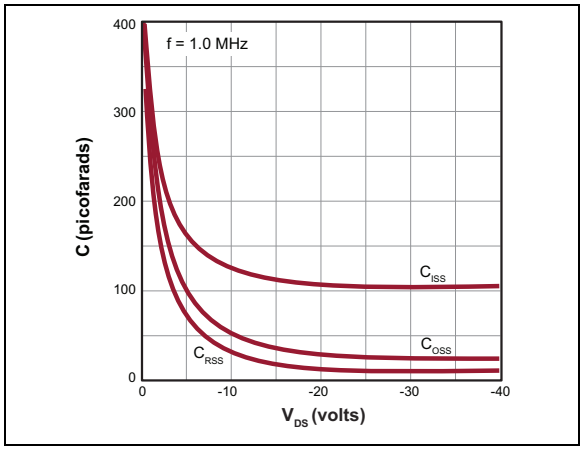


FIGURE 2-3: *Capacitance vs. Drain-to-source Voltage.*

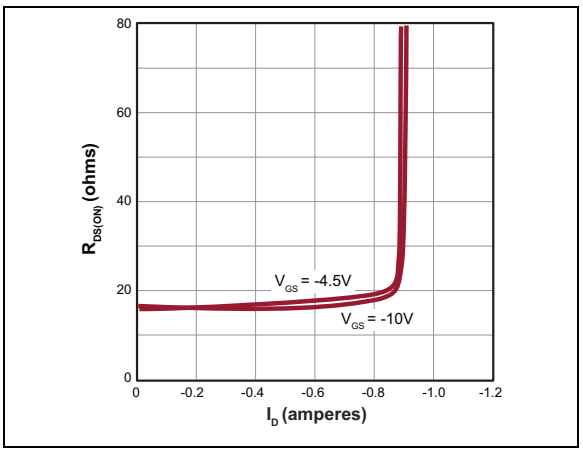


FIGURE 2-4: *On-resistance vs. Drain Current.*

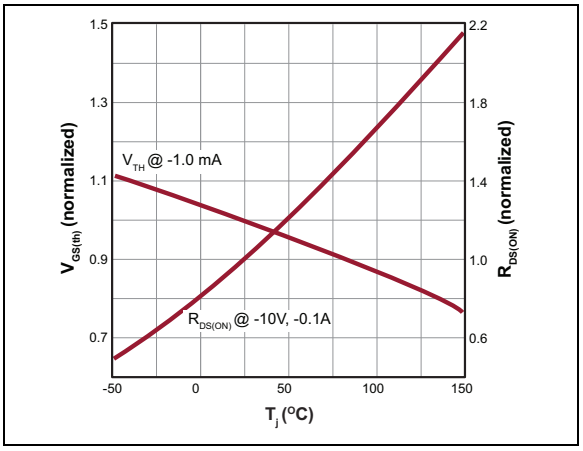


FIGURE 2-5: *$V_{GS(th)}$ and $R_{DS(ON)}$ Variation with Temperature.*

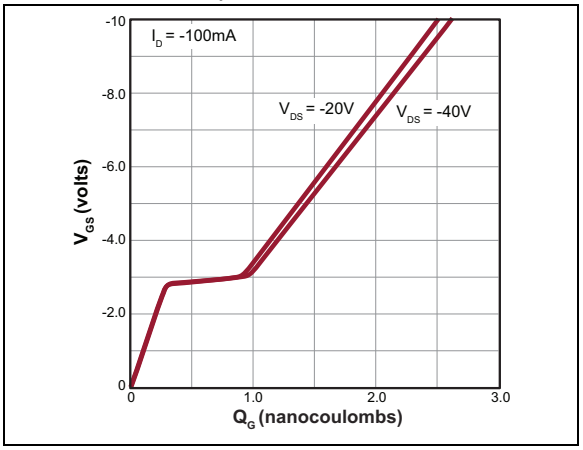


FIGURE 2-6: *Gate Drive Dynamic Characteristics.*

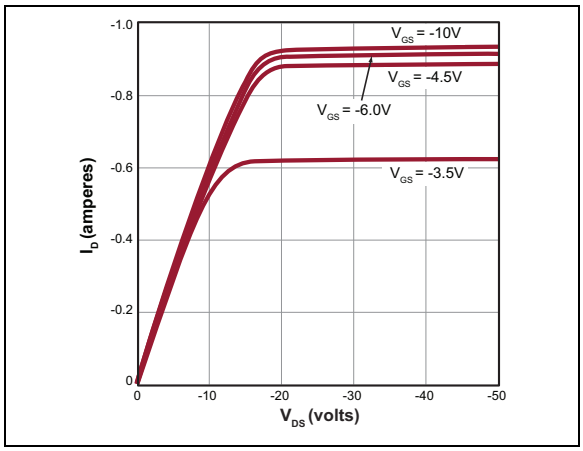


FIGURE 2-7: *Output Characteristics.*

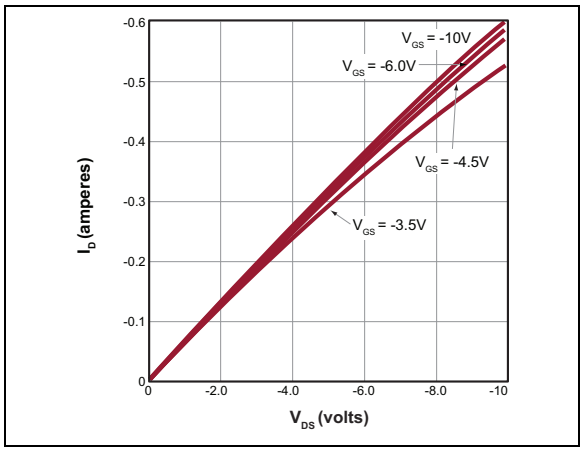


FIGURE 2-10: *Saturation Characteristics.*

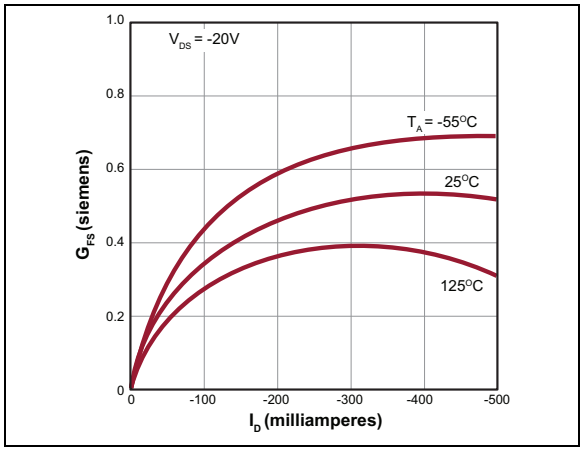


FIGURE 2-8: *Transconductance vs. Drain Current.*

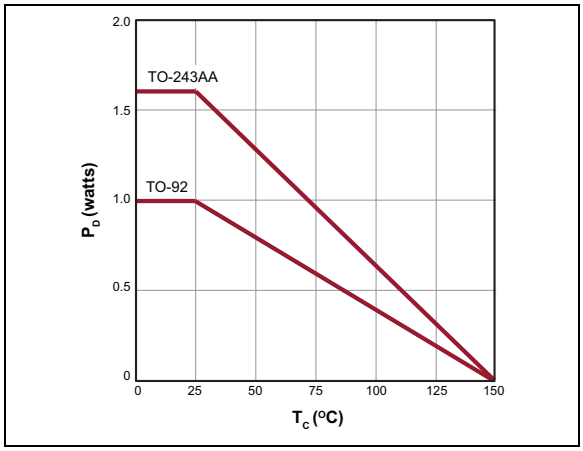


FIGURE 2-11: *Power Dissipation vs. Case Temperature.*

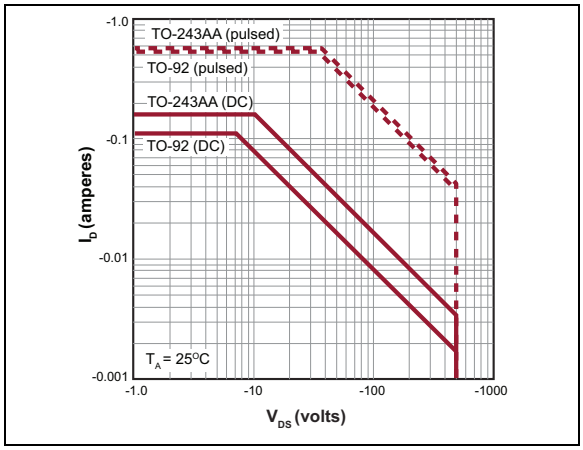


FIGURE 2-9: *Maximum Rated Safe Operating Area.*

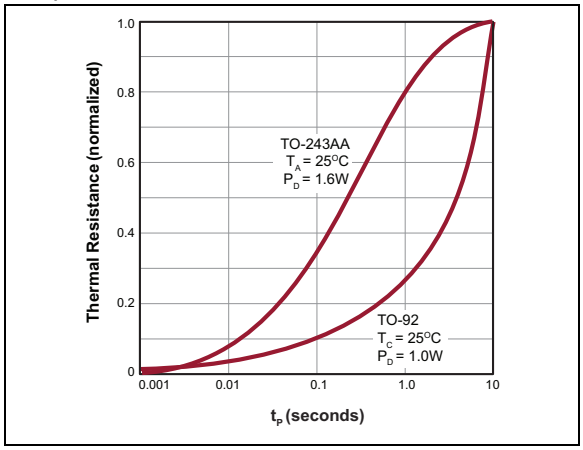


FIGURE 2-12: *Thermal Response Characteristics.*

3.0 PIN DESCRIPTION

The details on the pins of VP2450 (TO-92 and SOT-89) are listed on Table 3-1. Refer to **Package Types** for the location of pins.

TABLE 3-1: PIN FUNCTION TABLE

TO-92 Pin Number	SOT-89 Pin Number	Pin Name	Description
1	3	Source	Source
2	1	Gate	Gate
3	2,4	Drain	Drain

4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for VP2450.

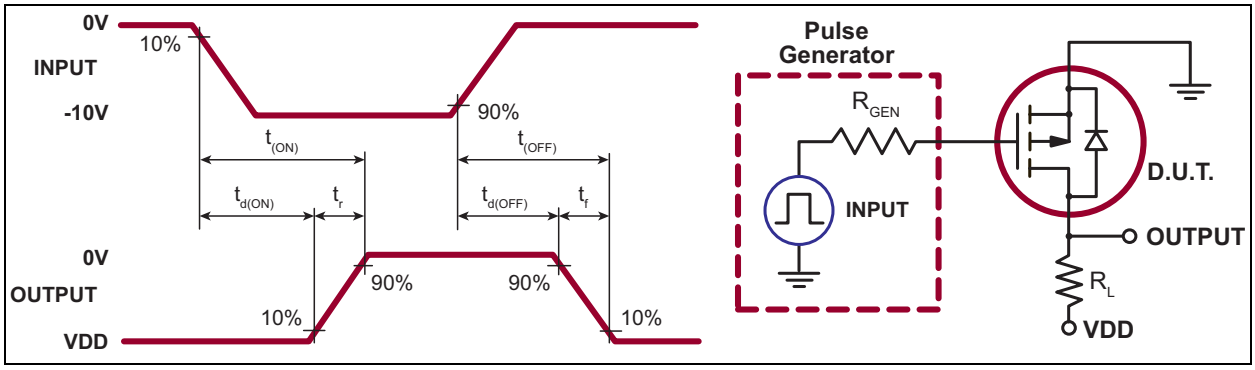


FIGURE 4-1: *Switching Waveforms and Test Circuit.*

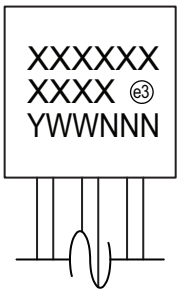
PRODUCT SUMMARY

BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (Maximum) (Ω)	$I_{D(ON)}$ (Minimum) (mA)	$V_{GS(th)}$ (Maximum) (V)
–500	30	–200	–0.4

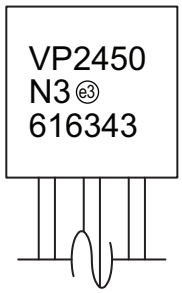
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

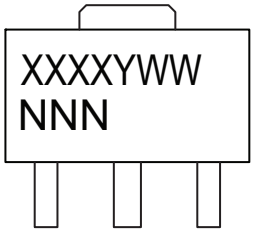
3-lead TO-92



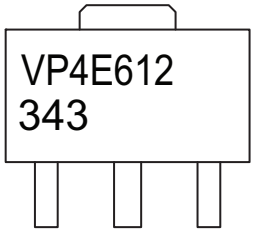
Example



3-lead SOT-89



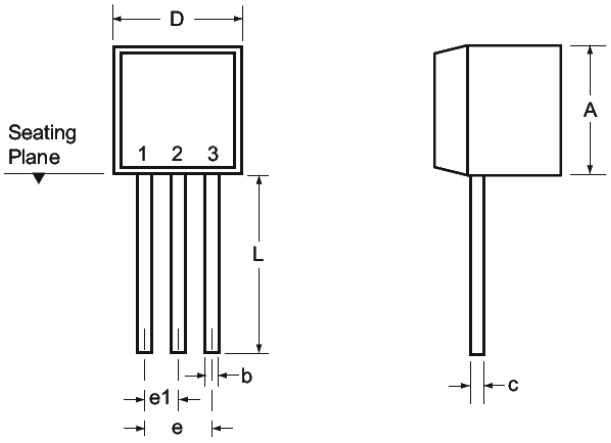
Example

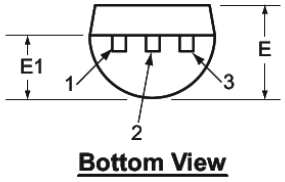


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

3-Lead TO-92 Package Outline (L/LL/N3)



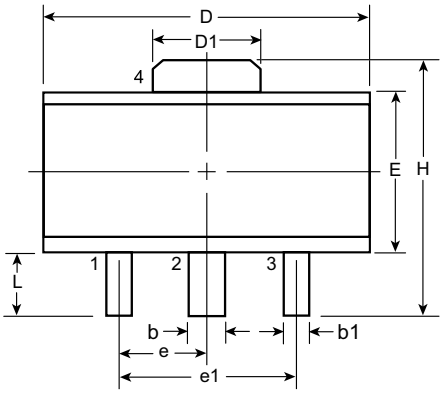


Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

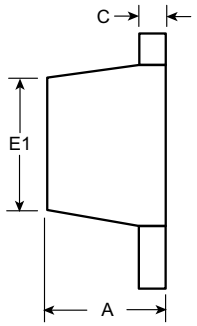
Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014†	.014†	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022†	.022†	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

3-Lead TO-243AA (SOT-89) Package Outline (N8)



Top View



Side View

Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00†	1.50 BSC	3.00 BSC	3.94	0.73†
	NOM	-	-	-	-	-	-	-	-			-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.
† This dimension differs from the JEDEC drawing
***Drawings not to scale**.*

APPENDIX A: REVISION HISTORY

Revision A (September 2016)

- Converted Supertex Doc# DSFP-VP2450 to Microchip DS20005569A.
- Changed the “TO-243AA (SOT-89)” package to “SOT-89.”
- Limited package options to TO-92 (1000/Bag) and SOT-89 (2000/Reel).
- Made minor text changes throughout the document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	VP2450	=	P-Channel Enhancement-Mode Vertical DMOS FET
Packages:	N3	=	3-lead TO-92
	N8	=	3-lead SOT-89
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(Blank)	=	1000/Bag for an N3 Package 2000/Reel for an N8 Package

Examples:

a) VP2450N3-G: P-Channel Enhancement-Mode Vertical DMOS FET, 3-lead TO-92 Package, 1000/Bag

b) VP2450N8-G: P-Channel Enhancement-Mode Vertical DMOS FET, 3-lead SOT-89 Package, 2000/Reel

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