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NVMe PCIe SSD
M.2
Manual

NVMe PCIe SSD is a non-volatile, solid-state storage device delivering uncompromising performance, reliability and ruggedness for environmentally challenging applications.

Revision History

Date	Revision	Description	Checked By
3/30/17	A	Initial Release from modified PSFNP5xxxxVxxx_A. update PN table performance and features, and PCI Express Device Link Capabilities Register. Change lanes from 4 to 2.	
7/13/17	B	Revise temperature spec	
7/26/17	C	Add TLC PN's	
8/14/17	D	Add 1TB PN	

Legal Information

Legal Information

Ordering Information: M.2 80mm PCIe SSD Solid-State Drive

Part Number	Interface	Application	User Capacity (GB)	Encryption	Temperature	NAND
VPFNP5120GDEBMTL	PCIe/NVMe	Enterprise	120	Pyrite/AES256 OPAL 2.0	-25'C to +70'C	TSB 15nm MLC L-die
VPFNP5240GDEAMTL	PCIe/NVMe	Enterprise	240	Pyrite/AES256 OPAL 2.0	-25'C to +70'C	TSB 15nm MLC L-die
VPFNP5480GDEZMTL	PCIe/NVMe	Enterprise	480	Pyrite/AES256 OPAL 2.0	-25'C to +70'C	TSB 15nm MLC L-die
VPFNP5120GDCHWT3	PCIe/NVMe	Enterprise	120	Pyrite/AES256 OPAL 2.0	0'C to +70'C	TSB TLC 3D NAND
VPFNP5240GDCHWT3	PCIe/NVMe	Enterprise	240	Pyrite/AES256 OPAL 2.0	0'C to +70'C	TSB TLC 3D NAND
VPFNP5480GDCHWT3	PCIe/NVMe	Enterprise	480	Pyrite/AES256 OPAL 2.0	0'C to +70'C	TSB TLC 3D NAND
VPFNP5001TDCFWT3	PCIe/NVMe	Enterprise	1000	Pyrite/AES256 OPAL 2.0	0'C to +70'C	TSB TLC 3D NAND

Notes:
1. Usable capacity based on a level of over-provisioning applied to wear leveling, bad sectors, index tables etc.
2. SSD's ship unformatted from the factory unless otherwise requested.
3. 1 GB = 1,000,000,000 Byte
4. One Sector = 512 Byte.
5. Lowercase x is a wildcard character that represents the device code for Flash device capacity

.

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1 Introduction

This document describes the specification of Viking SSD which uses PCIe interface. The Viking SSD is fully consist of semiconductor device and using NAND Flash Memory which has a high reliability and a high technology in a small form factor for using a SSD and supporting Peripheral Component Interconnect Express (PCIe) 3.0 interface standard up to 2 lanes shows much faster performance than previous SATA SSDs It could also provide rugged features with an extreme environment with a high MTBF.

1.1 Features

The SSD delivers the following features:

- Native-PCIe SSD for enterprise application
- PCI Express Gen3: Single port X2 lanes
- Compliant with PCI Express Base Specification Rev. 3.0
- Compliant with NVM Express Specification Rev.1.2
- Static and Dynamic Wear Leveling and Bad Block Management
- RoHS / Halogen-Free Compliant
- Support up to queue depth 64K
- Support Power Management: ASPM/PCI-PM L0s, L1, L1.1 and L1.2
- Support SMART and TRIM commands
- Support 48-bit addressing mode
- Firmware update
- Firmware support for encryption

1.2 PCIE Interface

- PCI Express Gen3: Single port X2 lanes, 4Gb/s
- Compliant with PCI Express Base Specification Rev. 3.0
- Compliant with NVM Express Specification Rev.1.2

For a list of supported commands and other specifics, refer to Chapter 5 and 6.

2 Product Specifications

2.1 Capacity and LBA count

Raw Capacity (GB)	User Capacity (GB)	LBA Count
128	120	234,441,648
256	240	468,862,128
512	480	937,703,088
1000	960	1,875,385,008

Notes:

1. Per www.idema.org, LBA1-03 spec,
   LBA counts = (97,696,368) + (1,953,504 * (Advertised Capacity in GBytes – 50))

2.2 Performance

Table 2-1: Maximum Sustained Read and Write Bandwidth and Power Consumption

Capacity (GB)	Flash Structure	Performance				Power Consumption		
		Read (MB/s)	Write (MB/s)			Read (mW)	Write (mW)	Idle (mW)
120	32GB x 4, BGA, 15nm	1,600	TBD			4,440	3,370	400
240	64GB x 4, BGA, 15nm	1,600	TBD			4,890	4,810	400
480	128GB x 4, BGA, 15nm	1,600	1,300			5,110	6,920	400
960	256GB x 4, BGA, 15nm	1,600	1,300			5,120	6,930	400

Notes:

1. Performance measured using CrystalDiskMark and ATTO
2. Performance may vary from flash configuration and platform.
3. Refer to Application Note AN0006 for Viking SSD Benchmarking Methodology.
4. Data is based on SSD's using Toshiba MLC 15nm L die
5. Typical Power Consumption at 3.3V

Table 2-2: Maximum Random Read and Write Input/Output Operations per Second (IOPS)

Access Type	128GB	256GB	512GB
Read, 4K, IOPS	Up to TBD	Up to TBD	Up to TBD
Write, 4K, IOPS	Up to TBD	Up to TBD	Up to TBD

Notes:
1. Refer to Application Note AN0006 for Viking SSD Benchmarking Methodology

2.2.1 Throughput

Based on the available space of the disk, the SSD will regulate the read/write speed and manage the performance of throughput. When there still remains a lot of space, the firmware will continuously perform read/write action. There is still no need to implement garbage collection to allocate and release memory, which will accelerate the read/write processing to improve the performance. Contrarily, when the space is going to be used up, the SSD will slow down the read/write processing, and implement garbage collection to release memory. Hence, read/write performance will become slower.

2.2.2 Predict & Fetch

Normally, when the Host tries to read data from a PCIe SSD, the PCIe SSD will only perform one read action after receiving one command. However, the Viking SSD applies Predict & Fetch to improve the read speed. When the host issues sequential read commands to the PCIe SSD, the PCIe SSD will automatically expect that the following will also be read commands. Thus, before receiving the next command, flash has already prepared the data. Accordingly, this accelerates the data processing time, and the host does not need to wait so long to receive data.

2.3 Electrical Characteristics

2.3.1 Absolute Maximum Ratings

Values shown are stress ratings only. Functional operation outside normal operating values is not implied. Extended exposure to absolute maximum ratings may affect reliability.

Table 2-3: Absolute Maximum Ratings

Description	Min	Max	Unit
Maximum Voltage Range for Vin	-0.2	3.6	V
Maximum Temperature Range	-40	85	c

2.3.2 Supply Voltage

The operating voltage is 3.3V

Table 2-4: Operating Voltage

Description	Min	Max	Unit
Operating Voltage for 3.3 V (+/- 5%)	3.135	3.465	V

2.4 Environmental Conditions

2.4.1 Temperature and Altitude

Table 2-5: Temperature and Altitude Related Specifications

Conditions	Operating	Shipping	Storage
Commercial Temperature- Case [1]	-25'C to +70'C	-40 to 85°C	-40 to 85°C
Humidity (non-condensing)	90% under 40C	93% under 40C	93% under 40C

Notes:

1. Tc is measured at the surface of NAND Flash package

2.4.2 Shock and Vibration

SSD products are tested in accordance with environmental specification for shock and vibration

Table 2-6: Shock and Vibration Specifications

Stimulus	Description
Shock(non-operating)	1500G (0.5ms duration x,y,z with 1/2 sine wave)
Vibration (non-operating)	(60min /axis on 3 axes) Displacement: 1.52mm (20 ~ 80 Hz) Acceleration: 20G (80 ~ 2,000 Hz)

2.4.3 Electromagnetic Immunity

M.2 is an embedded product for host systems and is designed not to impair with system functionality or hinder system EMI/FCC compliance.

2.5 Reliability

Table 2-7: Reliability Specifications

Parameter	Description	
ECC	Correct up to 120 bits error in 2K Byte data	
MTBF	2,000,000 hours	
Write Endurance **(MLC)**	**Capacity**	**TBW**
	120GB	175
	240GB	349
	480GB	698
	960GB	1396
Write Endurance **(TLC)**	**Capacity**	**TBW**
	120GB	TBD
	240GB	TBD
	480GB	TBD
	960GB	TBD
Data retention	> 90 days at NAND expiration	

Notes:
1. The reliability specification follows JEDEC standards JESD218A and JESD219A
2. Average Minimum Program/Erase cycles (MLC, 3000)

2.6 Data Security

2.6.1 Power Loss Protection: Flushing Mechanism

Power Loss Protection is a mechanism to prevent data loss during unexpected power failure. DRAM is a volatile memory and frequently used as temporary cache or buffer between the controller and the NAND flash to improve the SSD performance. However, one major concern of the DRAM is that it is not able to keep data during power failure. Accordingly, the SSD applies the

GuaranteedFlush technology, which requests the controller to transfer data to the cache. DDR performs as a cache, and its sizes include 256MB, 512MB, 1024MB or 2048MB. Only when the data is fully committed to the NAND flash will the controller send acknowledgement (ACK) to the host. Such implementation can prevent false-positive performance and the risk of power cycling issues.
Additionally, it is critical for a controller to shorten the time the in-flight data stays in the cache. Thus, the SSD applies an algorithm to reduce the amount of data resides in the cache to provide a better performance. This SmartCacheFlush technology allows incoming data to only have a "pit stop" in the cache and then move to the NAND flash at once. If the flash is jammed due to particular file sizes (such as random 4KB data), the cache will be treated as an "organizer", consolidating incoming data into groups before written into the flash to improve write amplification. In sum, with Flush Mechanism, the SSD proves to provide the reliability required by consumer, industrial, and enterprise-level applications.

2.6.2 Secure Erase

Secure Erase is a standard ATA command and will write all "0xFF" to fully wipe all the data on hard drives and SSDs. When this command is issued, the SSD controller will empty its storage blocks and return to its factory default settings.

2.6.3 Write Protect

When a SSD contains too many bad blocks and data are continuously written in, then the SSD might not be usable anymore. Thus, Write Protect is a mechanism to prevent data from being written in and protect the accuracy of data that are already stored in the SSD.

2.6.4 Encryption

- Pyrite
- AES256
- OPAL 2.0

2.7 Flash Management

2.7.1 Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. The SSD applies a BCH ECC algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption.

2.7.2 Wear Leveling

NAND flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.
Advanced Wear Leveling algorithm, can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND flash is greatly improved.

2.7.3 Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Viking implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

2.7.4 TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

2.7.5 SMART

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

2.7.6 Over-Provision

Over Provisioning refers to the inclusion of extra NAND capacity in a SSD, which is not visible and cannot be used by users. With Over Provisioning, the performance and IOPS (Input/Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

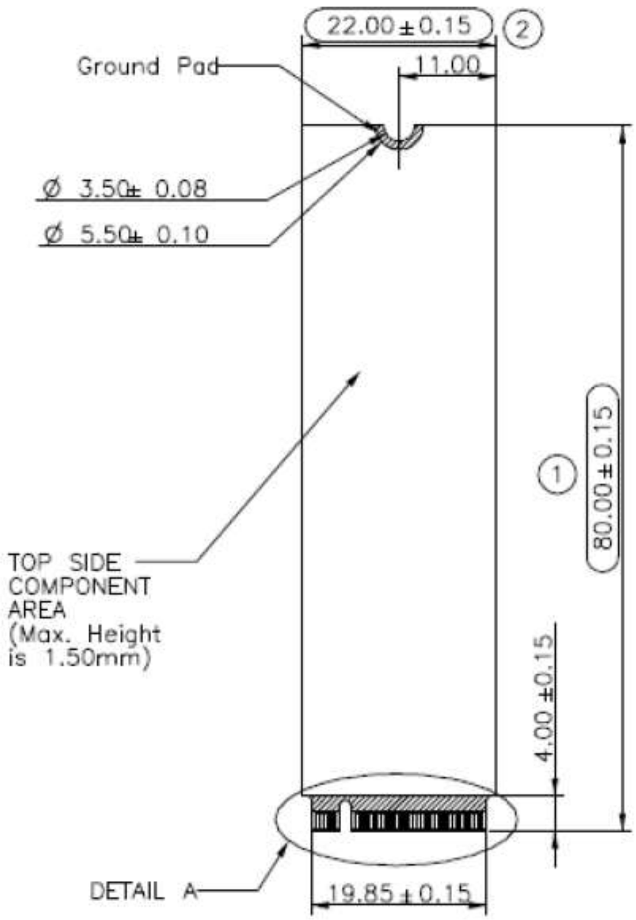
2.7.7 Firmware Upgrade

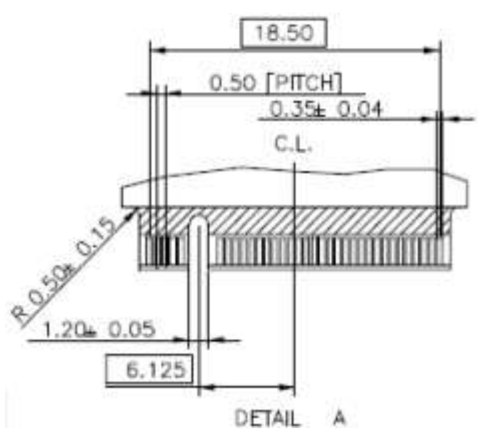
Firmware can be considered as a set of instructions on how the device communicates with the host. Firmware will be upgraded when new features are added, compatibility issues are fixed, or read/write performance gets improved.

3 Mechanical Information

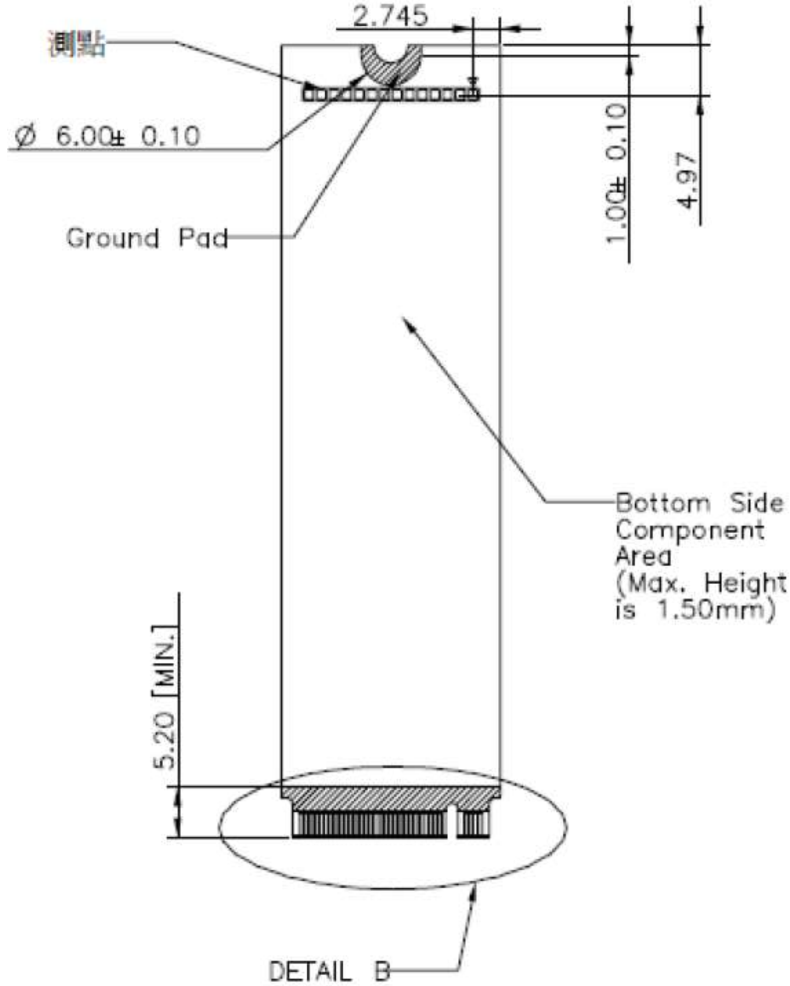
Figure 3-1: Dimension Details for M.2 80mm length

Top View

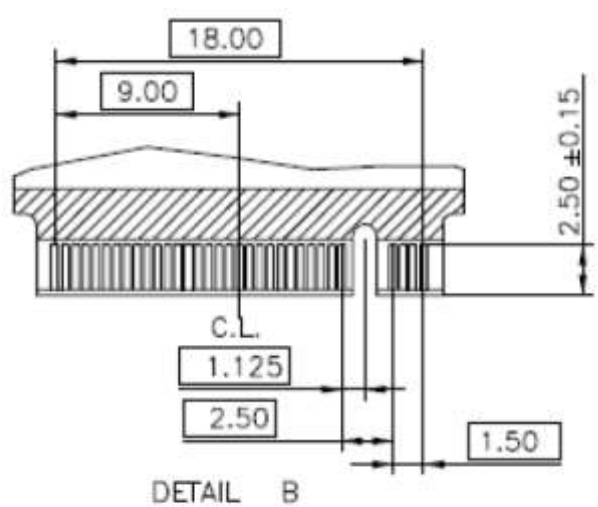




Bottom View

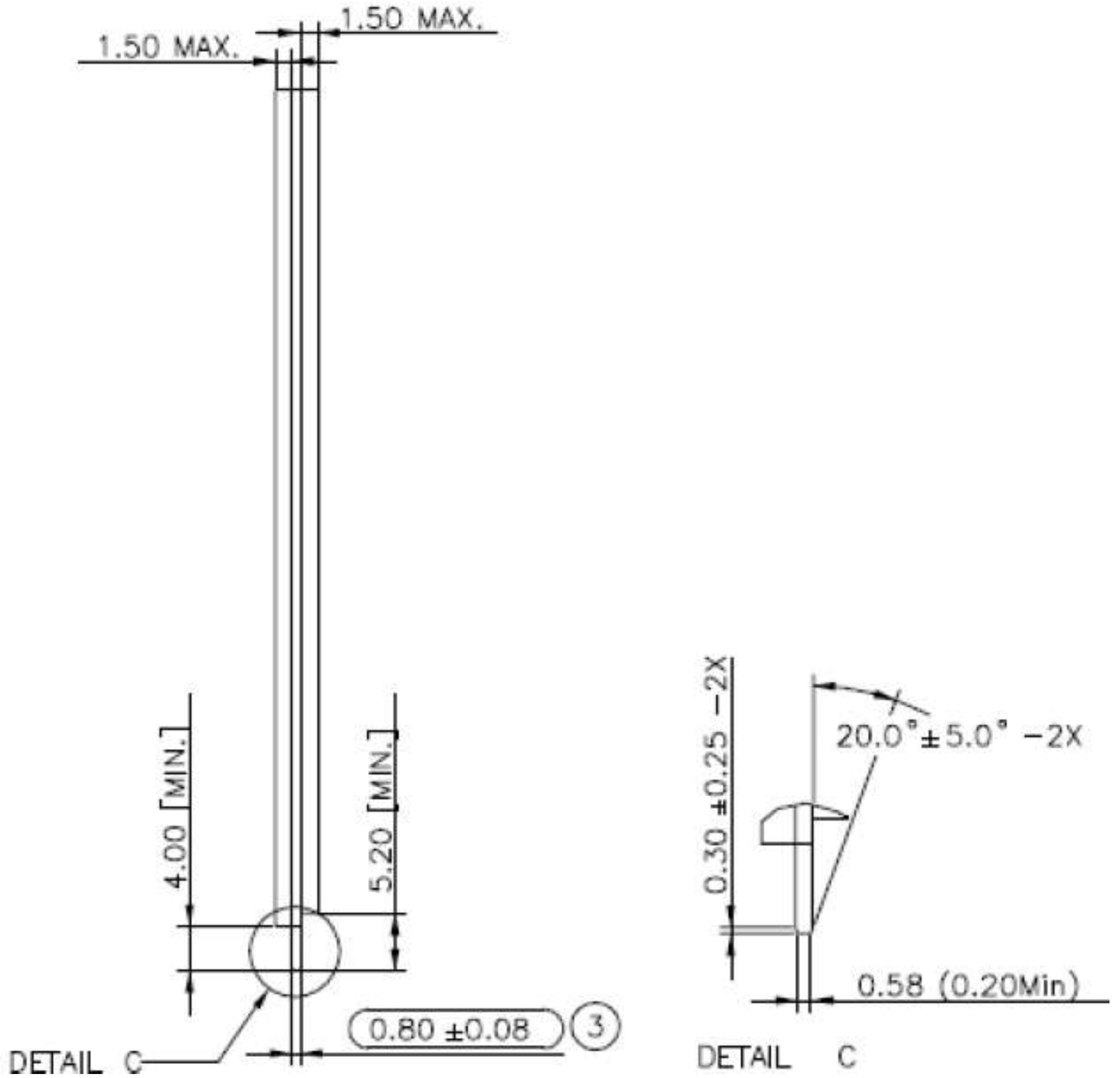


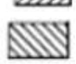
2.745
測點
Ø 6.00± 0.10
Ground Pad
1.00± 0.10
4.97
Bottom Side Component Area (Max. Height is 1.50mm)
5.20 [MIN.]
DETAIL B



18.00
9.00
2.50 ±0.15
C.L.
1.125
2.50
1.50
DETAIL B

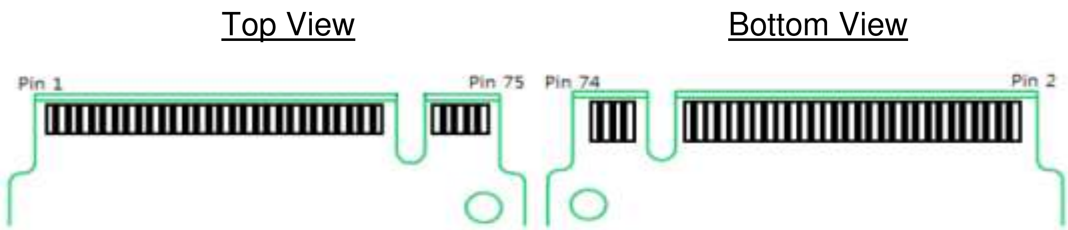
Side View



Notes:
1. M.2 2280-D5-M: 80mm (L) x 22mm (W) x 3.8mm (H)
2. All dimensions are in millimeter
3. General tolerance is ± 0.15mm
4. Max component height designated by ………. 
5. No component area designated by ………… 
6. No component (signal vias/Signal copper/Print 
7. Check points locations at ……………..……… (1) (2) (3)

3.1 Card Edge Detail

Figure 3-2: Signal and Power Pins on M.2 card edge



3.2 M.2 SSD Weight

Table 3-1: M.2 SSD weight

Length	Weight	Unit of measure
80 mm	< 8	Grams

4 Pin and Signal Descriptions

4.1 Signal and Power Description Tables

Table 4-1: M.2 PCIE Connector Pinouts

Pin #	Assignment	Description	Pin #	Assignment	Description
1	GND	Return current path	2	3.3V	3.3V source
3	GND	Return current path	4	3.3V	3.3V source
5	PETn3	PCIe TX	6	N/C	N/C
7	PETp3	PCIe TX	8	N/C	N/C
9	GND	Return current path	10	LED1#	Device Active Signal
11	PERn3	PCIe Rx	12	3.3V	3.3V source
13	PERp3	PCIe Rx	14	3.3V	3.3V source
15	GND	Return current path	16	3.3V	3.3V source
17	PETn2	PCIe TX	18	3.3V	3.3V source
19	PETp2	PCIe TX	20	N/C	N/C
21	GND	Return current path	22	N/C	N/C
23	PERn2	PCIe Rx	24	N/C	N/C
25	PERp2	PCIe Rx	26	N/C	N/C
27	GND	Return current path	28	N/C	N/C
29	PETn1	PCIe TX	30	N/C	N/C
31	PETp1	PCIe TX	32	N/C	N/C
33	GND	Return current path	34	N/C	N/C
35	PERn1	PCIe Rx	36	N/C	N/C
37	PERp1	PCIe Rx	38	N/C	N/C
39	GND	Return current path	40	N/C	N/C
41	PETn0	PCIe TX	42	N/C	N/C
43	PETp0	PCIe TX	44	N/C	N/C
45	GND	Return current path	46	N/C	N/C

Pin #	Assignment	Description	Pin #	Assignment	Description
47	PERn0	PCIe Rx	48	N/C	N/C
49	PERp0	PCIe Rx	50	PERST#	PCIe Reset
51	GND	Return current path	52	CLKREQ#	PCIe Device Clock Request
53	REFCLKN	PCIe Reference Clock	54	PEWake#	N/C
55	REFCLKP	PCIe Reference Clock	56	N/C	N/C
57	GND	Return current path	58	N/C	N/C
67	N/C	N/C	68	SUSCLK	32.768 kHz clk input by host
69	PEDET	N/C	70	3.3V	3.3V source
71	GND	Return current path	72	3.3V	3.3V source
73	GND	Return current path	74	3.3V	3.3V source
75	GND	Return current path			

Note

1. Pin 59 through 66 are reserved for the module key

5 PCIe and NVM Express Registers

5.1 PCI Express Registers

5.1.1 PCI Register Summary

Table 5-1: PCI Register Summary

Start Address	End Address	Name	Type
00h	3Fh	PCI Header	PCI Capability
40h	47h	PCI Power Management Capability	PCI Capability
50h	67h	MSI Capability	PCI Capability
70h	A3h	PCI Express Capability	PCI Capability
B0h	BBh	MSI-X Capability	PCI Capability
100h	12Bh	Advanced Error Reporting Capability	PCI Capability
148h	157h	Device Serial No Capability	PCI Capability
158h	167h	Power Budgeting Capability	PCI Capability
168h	17Bh	Secondary PCI Express Header	PCI Capability
188h	18Fh	Latency Tolerance Reporting (LTR)	PCI Capability
190h	19Fh	L1 Substates Capability Register	PCI Capability

5.1.2 PCI Header Registers

Table 5-2: PCI Header Register Summary

Start Address	End Address	Symbol	Description
00h	03h	ID	Identifiers
04h	05h	CMD	Command Register
06h	07h	STS	Device Status
08h	08h	RID	Revision ID
09h	0Bh	CC	Class Codes
0Ch	0Ch	CLS	Cache Line Size
0Dh	0Dh	MLT	Master Latency Timer
0Eh	0Eh	HTYPE	Header Type
0Fh	0Fh	BIST	Built in Self Test
10h	13h	MLBAR (BAR0)	Memory Register Base Address (lower 32-bit)
14h	17h	MUBAR (BAR1)	Memory Register Base Address (upper 32-bit)
18h	1Bh	IDBAR (BAR2)	Index/Data Pair Register Base Address
1Ch	1Fh	BAR3	Reserved
20h	23h	BAR4	Reserved
24h	27h	BAR5	Reserved
28h	2Bh	CCPTR	CardBus CIS Pointer
2Ch	2Fh	SS	Subsystem Identifiers
30h	33h	EROM	Expansion ROM Base Address
34h	34h	CAP	Capabilities Pointer
35h	3Bh	R	Reserved
3Ch	3Dh	INTR	Interrupt Information
3Eh	3Eh	MGNT	Minimum Grant
3Fh	3Fh	MLAT	Maximum Latency