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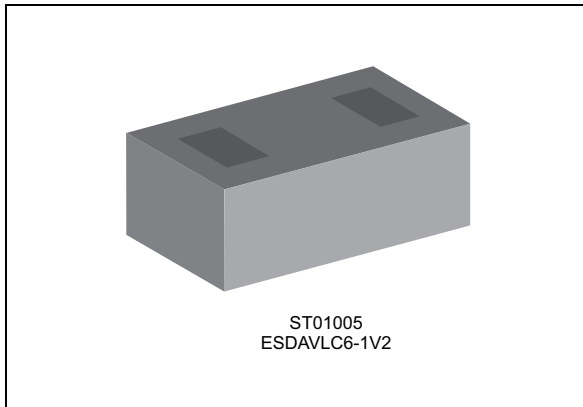
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## Single line low capacitance Transil™ for ESD protection

Datasheet – production data



### Features

- Ultra small PCB area = 0.09 mm<sup>2</sup>
- Unidirectional device
- Very low diode capacitance
- Low leakage current
- RoHS compliant

### Applications

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- Smart phones and accessories
- Portable multimedia devices and accessories
- Tablets

### Description

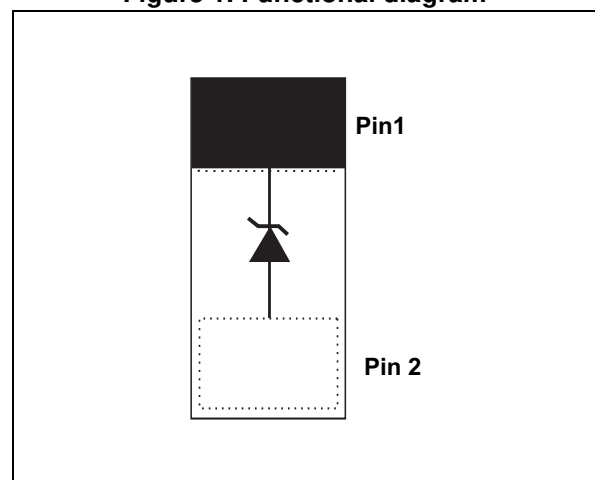
The ESDAVLC6-1V2 is a single line unidirectional Transil diode designed specially for the protection of integrated circuits into portable equipment and miniaturized electronics devices subject to ESD transient overvoltage.

The device is ideal for applications where both reduced printed circuit board space and high ESD protection level are required.

### Complies with following standards:

- IEC 61000-4-2 level 4:
  - ±8 kV contact discharge
  - ±15 kV air discharge

Figure 1. Functional diagram



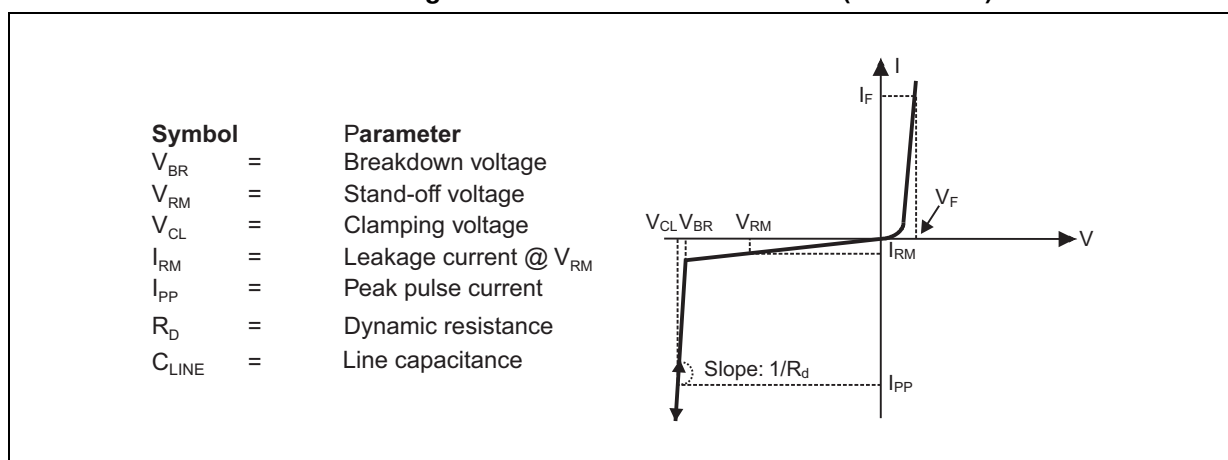
TM: Transil is a trademark of STMicroelectronics

# 1 Characteristics

**Table 1. Absolute maximum ratings ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

Symbol	Parameter		Value	Unit
$V_{PP}$	Peak pulse voltage	IEC 61000-4-2 contact discharge IEC 61000-4-2 air discharge	$\pm 8$ $\pm 15$	kV
$T_j$	Operating temperature range		-40 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage temperature range		- 55 to +150	$^{\circ}\text{C}$
$T_L$	Maximum lead temperature for soldering during 10 s		260	$^{\circ}\text{C}$

**Figure 2. Electrical characteristics (definitions)**



**Table 2. Electrical characteristics (values,  $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{BR}$	Breakdown voltage	$I_R = 1\text{ mA}$	6			V
$I_{RM}$	Leakage current	$V_{RM} = 3\text{ V}$			50	nA
$C_{line}$	Line capacitance, I/O to GND	$V_R = 0\text{ V}$ , $F = 1\text{ MHz}$ , $V_{osc} = 30\text{ mV}$		5	7	pF

Figure 3. ESD response to IEC 61000-4-2 (typical values, +8 kV contact discharge)

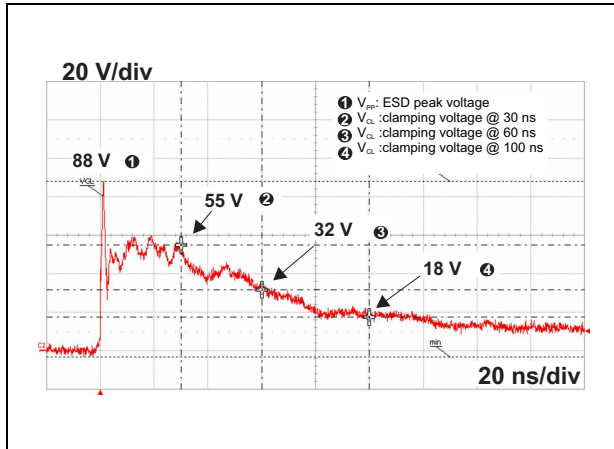


Figure 4. ESD response to IEC 61000-4-2 (typical values, -8 kV contact discharge)

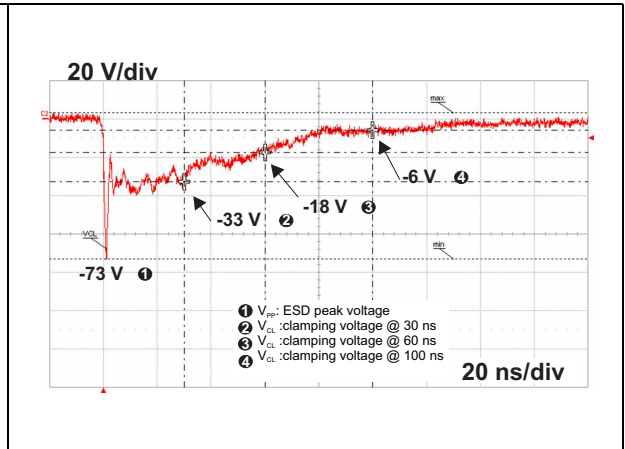
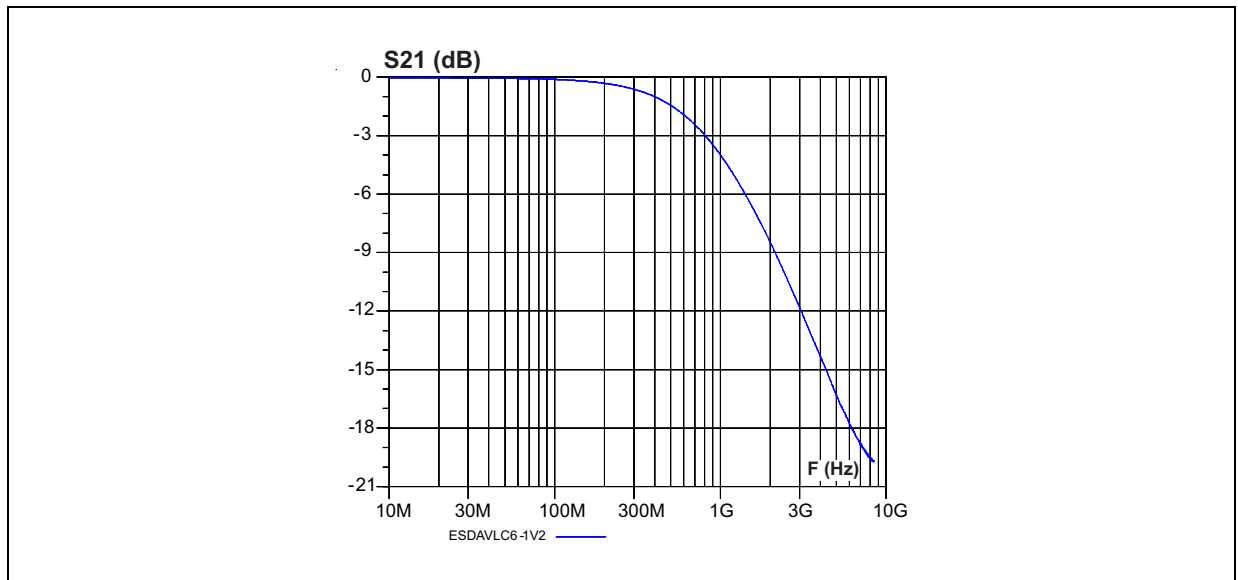


Figure 5. S21 attenuation measurement



## 2 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

Figure 6. Package dimensions

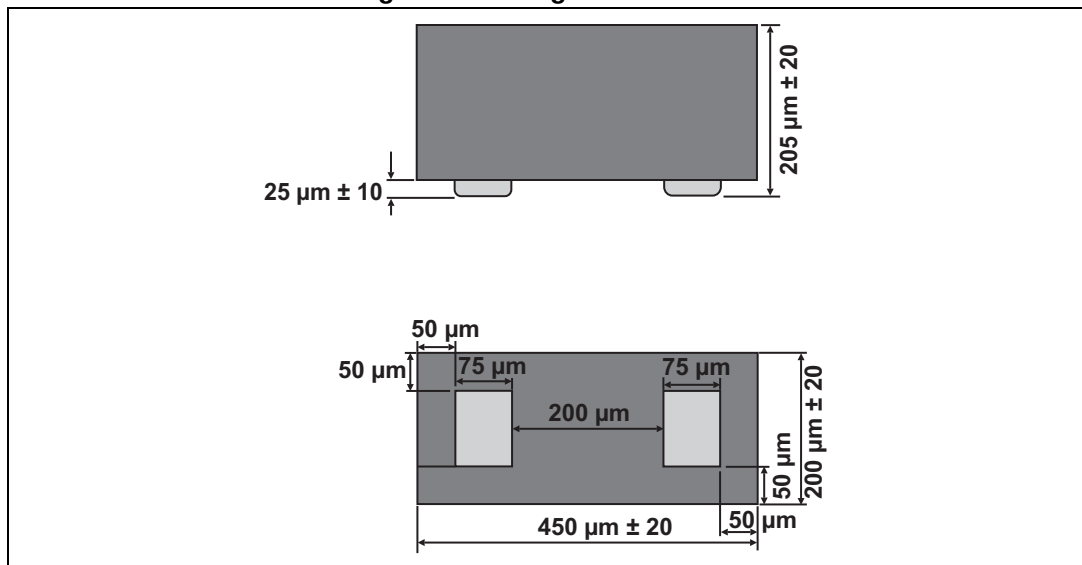
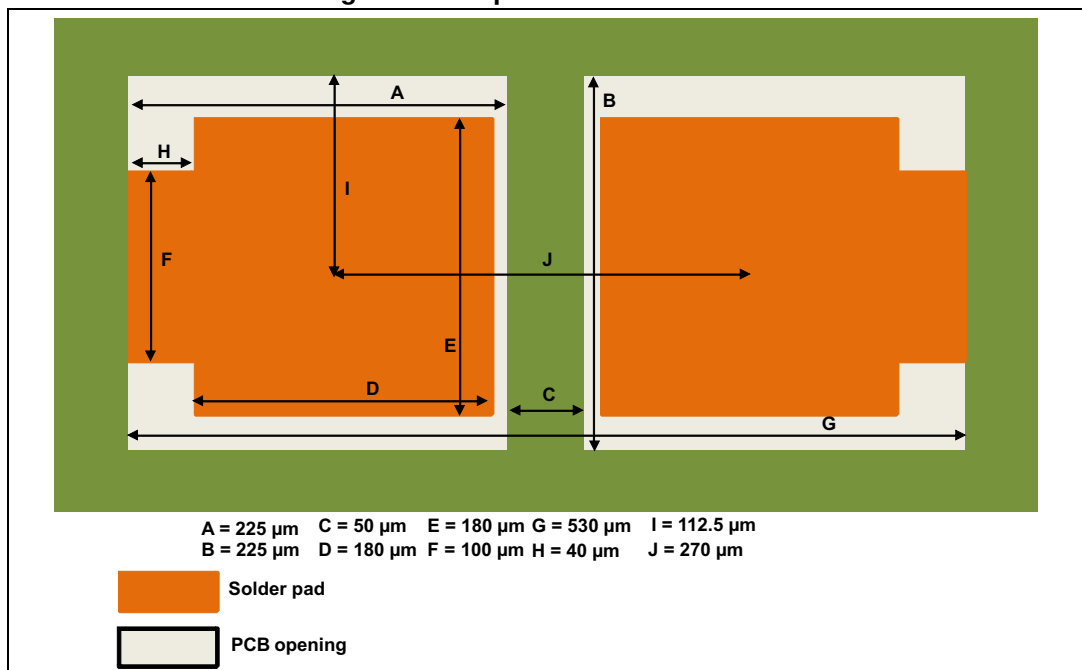


Figure 7. Footprint recommendation

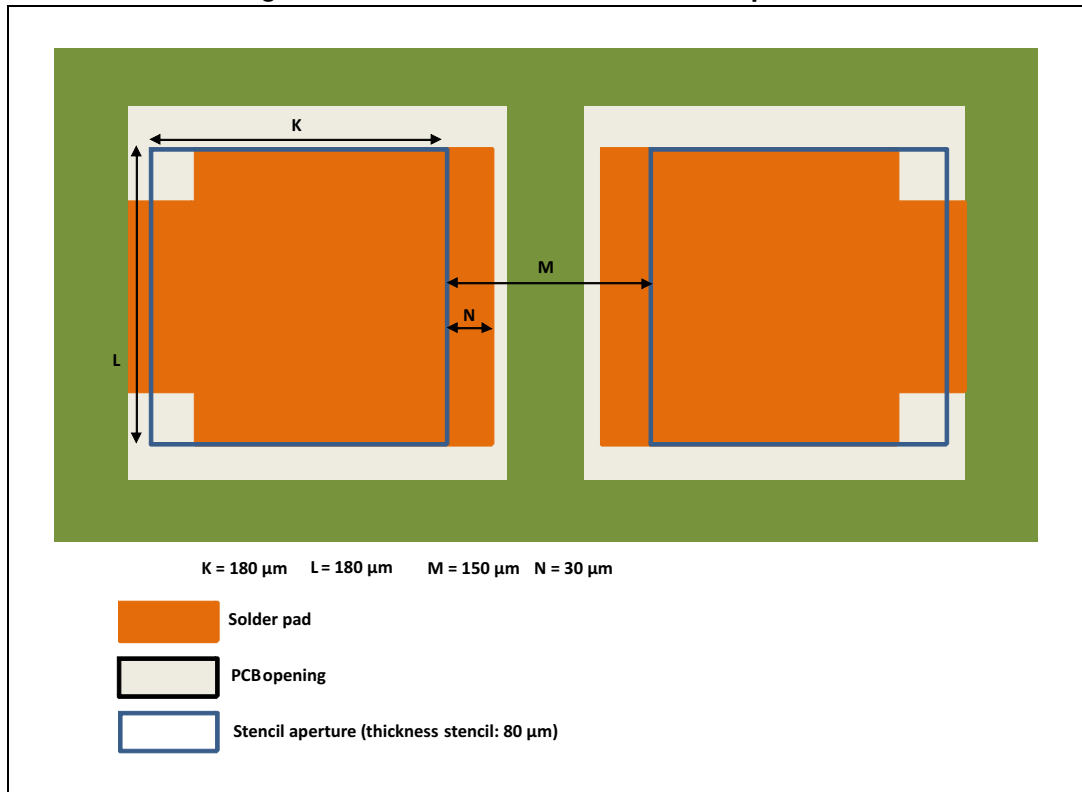


### 3 Recommendation on PCB assembly

#### 3.1 Stencil opening design

Stencil opening thickness: 80  $\mu\text{m}$

Figure 8. Recommended stencil window position



#### 3.2 Solder paste

1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. "No clean" solder paste recommended.
3. Offers a high tack force to resist component displacement during PCB movement.
4. Solder paste with fine particles: type 4 (powder particle size 20-38  $\mu\text{m}$  per IPC J-STD-005).

### 3.3 Placement

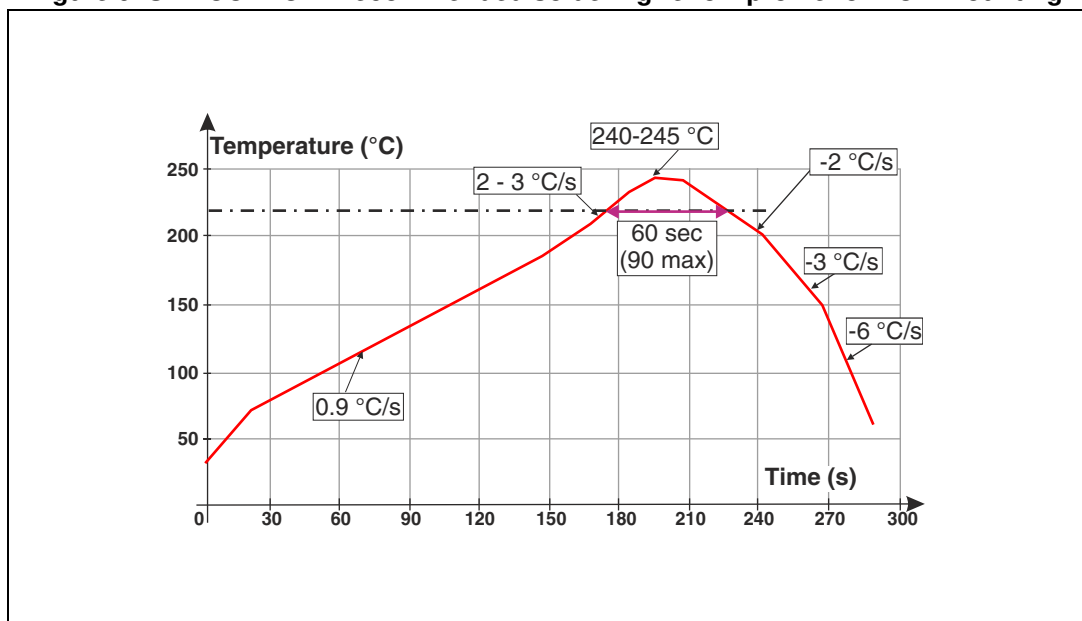
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Tolerance of  $\pm 0.02$  mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

### 3.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

### 3.5 Reflow profile

Figure 9. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

## 4 Ordering information

Figure 10. Ordering information scheme

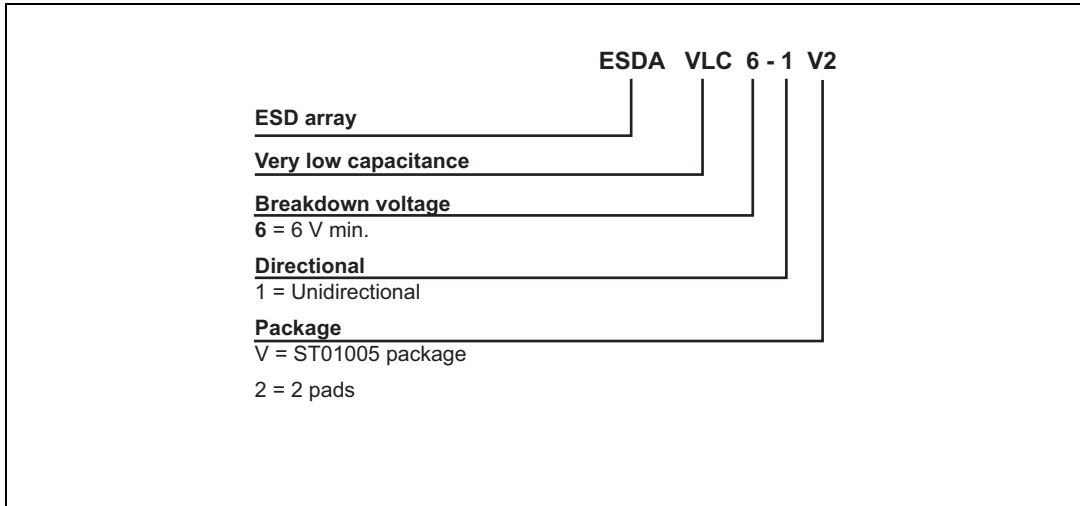


Table 3. Ordering information

Order code	Marking	Weight	Base qty	Delivery mode
ESDAVLC6-1V2	L	0.041 mg	20 000	Tape and reel

## 5 Revision history

Table 4. Document revision history

Date	Revision	Changes
05-Jun-2014	1	First issue



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