Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

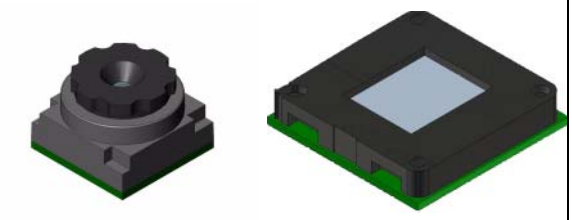
VL6524
VS6524

VGA single-chip camera module

Preliminary Data

Features

- 640H x 480V active pixels
- 3.6 µm pixel size, 1/6 inch optical format
- RGB Bayer color filter array
- Integrated 10-bit ADC
- Integrated digital image processing functions, including defect correction, lens shading correction, demosaic function, sharpening, gamma correction and color space conversion
- Embedded camera controller for automatic exposure control, automatic white balance control, black level compensation, 50/60 Hz flicker cancellation and flashgun support
- Up to 30 fps progressive scan, flexible subsampling and cropping modes
- ITU-R BT.656-4 YUV (YCbCr) 4:2:2 with embedded syncs, RGB 565, RGB 444 or Bayer 10-bit output formats
- Viewlive feature allows different sizes, formats and reconstruction settings to be applied to alternate frames
- 8-bit parallel video interface, horizontal and vertical syncs, 24 MHz clock
- Two-wire serial control interface (I^2C)
- On-chip PLL, 6.5 to 26 MHz clock input
- Analog power supply, from 2.4 V to 3.0 V
- Separate I/O power supply, 1.8 V or 2.8 V levels
- 3.3 V tolerant I/O for power supply > 2.7 V
- Integrated power management with power switch, automatic power-on reset and power-safe pins
- Low power consumption, ultra low standby current
- Dual-element plastic lens, F# 2.8, ~59° DFOV (VS6524)



SmOP **LGA**

Description

The VL6524/VS6524 is a general purpose VGA resolution CMOS color digital camera featuring low size and low power consumption. This complete camera module is ready to connect to camera enabled baseband processors, back-end IC devices or PDA engines.

Applications

- Mobile phone
- Videophone
- Video surveillance
- Medical
- Machine Vision
- Toys
- PDA
- Biometry
- Bar Code Reader
- Lighting Control

Contents

List of tables

List of figures

1 Overview

1.1 Description

The VL6524/VS6524 is a VGA resolution CMOS imaging device designed for low power systems.

Video data is output from the VS6524 over an 8-bit parallel bus in RGB, YCbCr or bayer formats and is controlled via an I²C interface.

The VL6524/VS6524 requires an analogue power supply of between 2.4 V to 3.0 V and a digital supply of either 1.8 V or 2.8 V (dependant on interface levels required). An input clock is required in the range 6.5 MHz to 26 MHz.

The device contains an embedded video processor and delivers fully color processed images at up to 30 frames per second. The video processor integrates a wide range of image enhancement functions, designed to ensure high image quality, these include:

- Automatic exposure control
- Automatic white balance
- Lens shading compensation
- Defect correction algorithms
- Demosaic (Bayer to RGB conversion)
- Matrix compensation
- Sharpening
- Gamma correction
- Flicker cancellation

2 Electrical interface

The device has 20 electrical connections as listed in *Table 1*. The physical orientation of the pins on the device is shown in *Figure 36 on page 63*.

Table 1. VL6524/VS6524 signal description

Pad socket	Pad name	I/O	Description
1	GND	PWR	Analogue ground
2	D02	OUT	Data output D2
3	D03	OUT	Data output D3
4	HSYNC	OUT	Horizontal synchronization output
5	VSYNC	OUT	Vertical synchronization output
6	D07	OUT	Data output D7
7	D06	OUT	Data output D6
8	D05	OUT	Data output D5
9	D04	OUT	Data output D4
10	CLK	IN	Clock input - 6.5 MHz to 26 MHz
11	GND	PWR	Digital ground
12	FSO	OUT	Flash output
13	CE	IN	Chip enable signal active HIGH
14	SCL	IN	I²C clock input
15	SDA	I/O	I²C data line
16	AVDD	PWR	Analogue supply 2.4 V to 3.0 V
17	D01	OUT	Data output D1
18	D00	OUT	Data output D0
19	PCLK	OUT	Pixel qualification clock
20	VDD	PWR	Digital supply 1.8 V OR 2.8 V

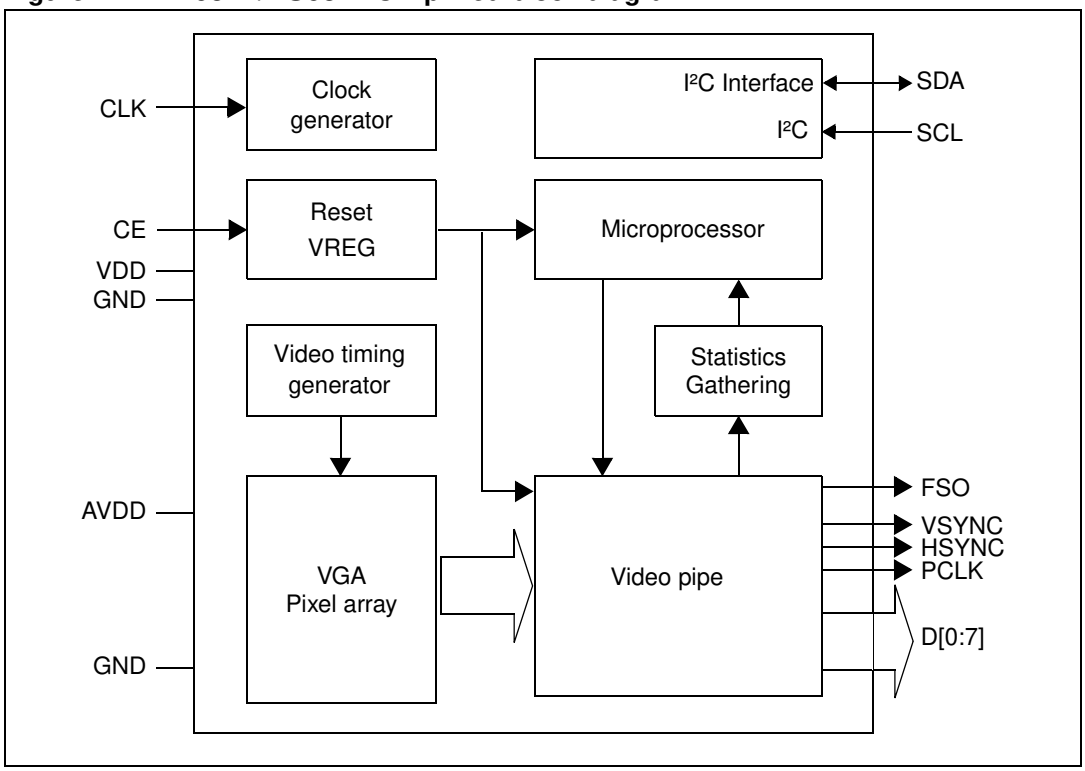
3 System architecture

The VL6524/VS6524 consists of the following main blocks:

- VGA-sized pixel array
- Video timing generator
- Video pipe
- Statistics gathering unit
- Clock generator
- Microprocessor

A simplified block diagram is shown in *Figure 1*.

Figure 1. VL6524/VS6524 simplified block diagram



3.1 Operation

A video timing generator controls a VGA-sized pixel array to produce raw images at up to 30 frames per second. The analogue pixel information is digitized and passed into the video pipe. The video pipe contains a number of different functions (explained in detail later). At the end of the video pipe data is output to the host system over an 8-bit parallel interface along with qualification signals.

The whole system is controlled by an embedded microprocessor that is running firmware stored in an internal ROM. The external host communicates with this microprocessor over an I²C interface. The microprocessor does not handle the video data itself but is able to control all the functions within the video pipe. Real-time information about the video data is gathered by a statistics engine and is available to the microprocessor. The processor uses this information to perform real-time image control tasks such as automatic exposure control.

3.1.1 Video pipe

The main functions contained within the VL6524/VS6524 video processing pipe are as follows.

Gain and offset: This function is used to apply gain and offset to data coming from the sensor array. The required gain and offset values result from the automatic exposure and white balance functions from the microprocessor.

Anti-vignette: This function is used to compensate for the radial roll-off in intensity caused by the lens. By default the anti-vignette setting matches the lens used in this module and does not need to be adjusted.

Crop: This function allows the user to select an arbitrary Window Of Interest (WOI) from the VGA-sized pixel array. It is fully accessible to the user.

Defect correction: This function runs a defect correction filter over the data in order to remove defects from the final output. This function has been optimized to attain the minimum level of defects from the system and does not need to be adjusted.

Demosaic: This module performs an interpolation on the Bayer data from the sensor array to produce an RGB image. It also applies an anti-alias filter.

Subsampler: This module allows the image to be sub-sampled in the X and Y directions by 2, 3, 4, 5 or 6.

Matrix: This function performs a color-space conversion from the sensor RGB data to standard RGB color space.

Sharpening: This module increases the high frequency content of the image in order to compensate for the low-pass filtering effects of the previous modules.

Gamma: This module applies a programmable gain curve to the output data. It is user adjustable.

YUV conversion: This module performs color space conversion from RGB to YUV. It is used to control the contrast and color saturation of the output image as well as the fade to black feature.

Dither: This module is used to reduce the contouring effect seen in RGB images with truncated data.

Output formatter: This module controls the embedded codes which are inserted into the data stream to allow the host system to synchronize with the output data. It also controls the optional HSYNC and VSYNC output signals.

3.2 Microprocessor functions

The microprocessor inside the VL6524/VS6524 performs the following tasks:

Host communication: handles the I²C communication with the host processor.

Video pipe configuration: configures the video pipe modules to produce the output required by the host.

Automatic exposure control: In normal operation the VL6524/VS6524 determines the appropriate exposure settings for a particular scene and outputs correctly exposed images.

Flicker cancellation: The 50/60Hz flicker frequency present in the lighting (due to fluorescent lighting) can be cancelled by the system.

Automatic white balance: The microprocessor adjusts the gains applied to the individual color channels in order to achieve a correctly color balanced image.

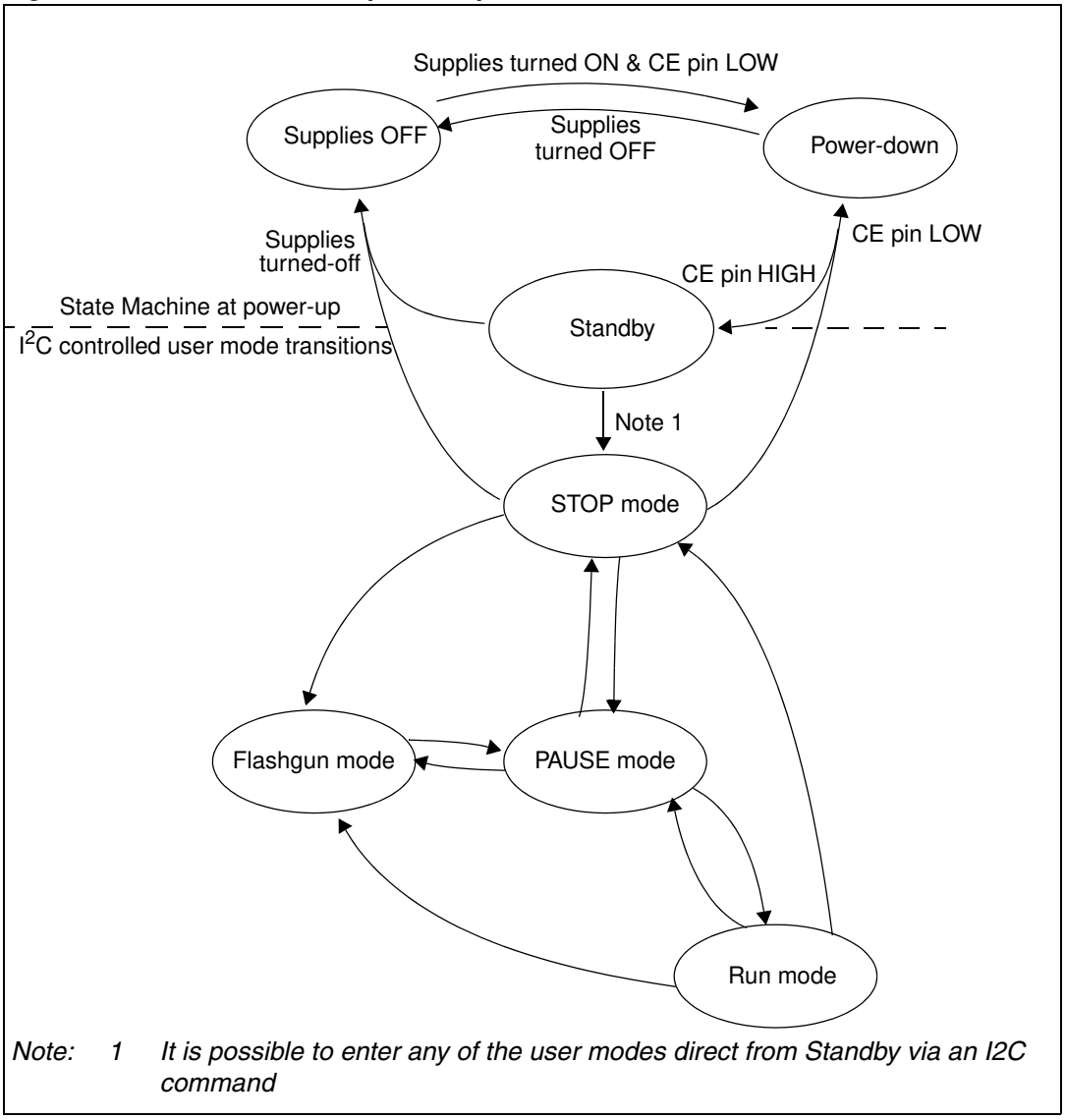
Dark calibration: The microprocessor uses information from special dark lines within the pixel array to apply an offset to the video data and ensure a consistent ‘black’ level.

Active noise management: The microprocessor is able to modify certain video pipe functions according to the current exposure settings determined by the automatic exposure controller. The main purpose of this is to improve the noise level in the system under low lighting conditions. Functions that require a reduction in strength under low lighting conditions (e.g. sharpening) are controlled by ‘dampers’. Functions that require an increase in strength under low lighting conditions are controlled by ‘promoters’. The fade to black operation is also controlled by the microprocessor

4 Operational modes

The VL6524/VS6524 has a number of operational modes. The STANDBY mode is entered and exited by driving the hardware CE signal. Transitions between all other modes are initiated by I²C transactions from the host system or automatically after time-outs.

Figure 2. State machine at power -up and user mode transitions



Note: 1 It is possible to enter any of the user modes direct from Standby via an I2C command

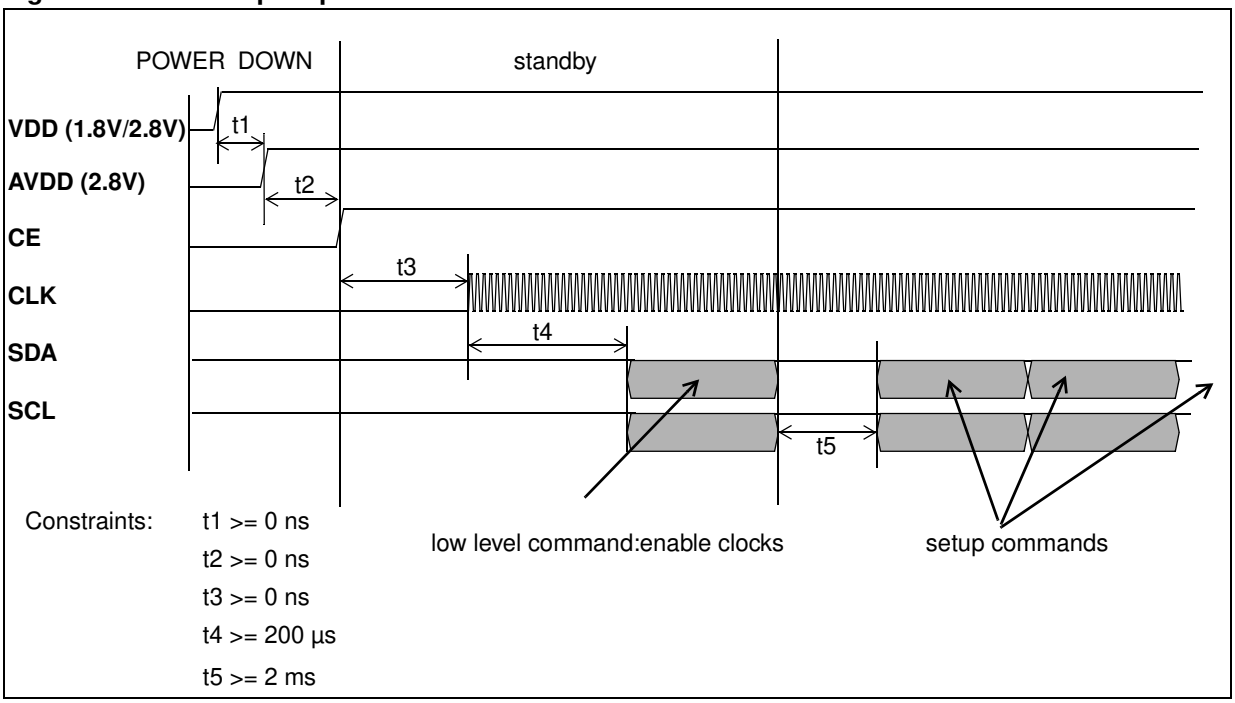
Power Down/Up: The power down state is entered from all other modes when CE is pulled low or the supplies are removed.
During the power-down state (CE = logic 0)

- The internal digital supply of the VL6524/VS6524 is shut down by an internal switch mechanism. This method allows a very low power-down current value.
- The device inputs / outputs are fail-safe, and consequently can be considered high impedance.

During the power-up sequence (CE = logic 1)

- The digital supplies must be on and stable.
- The internal digital supply of the VL6524/VS6524 is enabled by an internal switch mechanism.
- All internal registers are reset to default values by an internal power on reset cell.

Figure 3. Power up sequence



STANDBY mode: The VL6524/VS6524 enters STANDBY mode when the CE pin on the device is pulled HIGH. Power consumption is very low, most clocks inside the device are switched off.
In this state I²C communication is possible when CLK is present and when the microprocessor is enabled by writing the value 0x06 to the *MicroEnable* register 0xC003 (*Table 7 on page 43*).

All registers are reset to their default values. The device I/O pins have a very high-impedance.

Note: On exit from STANDBY mode, the VL6524/VS6524 is in a transient mode called UNINITIALISED, this mode is not a user mode.

STOP mode: This is a low power mode. The analogue section of the VL6524/VS6524 is switched off and all registers are accessed over the I²C interface. A run command received in this state automatically sets a transition through the PAUSE state to the run mode.

PAUSE mode: In this mode all VL6524/VS6524 clocks are running and all registers are accessible but no data is output from the device. The device is ready to start streaming but is halted. This mode is used to set up the required output format before outputting any data.

Note: The PowerManagement register bTimeToPowerdown can be adjusted in PAUSE mode but has no effect until the next RUN to PAUSE transition (Table 13 on page 45).

RUN mode: This is the fully operational mode.

ViewLive: this feature allows different sizes, formats and reconstruction settings to be applied to alternate frames of data, while in run mode.

FLASHGUN mode: In flashgun mode, the array is configured for use with an external flashgun. A flash is triggered and a single frame of data is output and the device automatically switches to Pause Mode.

4.1 Mode transitions

Transitions between operating modes are normally controlled by the host by writing to the *mode control* register (*Section 11.4 on page 43*). Some transitions can occur automatically after a time out. If there is no activity in the PAUSE state then an automatic transition to the STOP state occurs. This function is controlled by the *power management control* register (*Section 11.8 on page 45*). Writing 0xFF disables the automatic transition to STOP mode.

5 Clock control

5.1 Input clock

The VL6524/VS6524 contains an internal PLL allowing it to produce accurate frame rates from a wide range of input clock frequencies. The allowable input range is from 6.5 MHz to 26 MHz. The input clock frequency must be programmed in the *uwExtClockFreqNum (MSB)*, *uwExtClockFreqNum (LSB)* and *bExtClockFreqDen* registers (*Table 12: Clock manager input control on page 44*). To program an input frequency of 6.5 MHz, the numerator can be set to 13 and the denominator to 2. The default input frequency is 12 MHz.

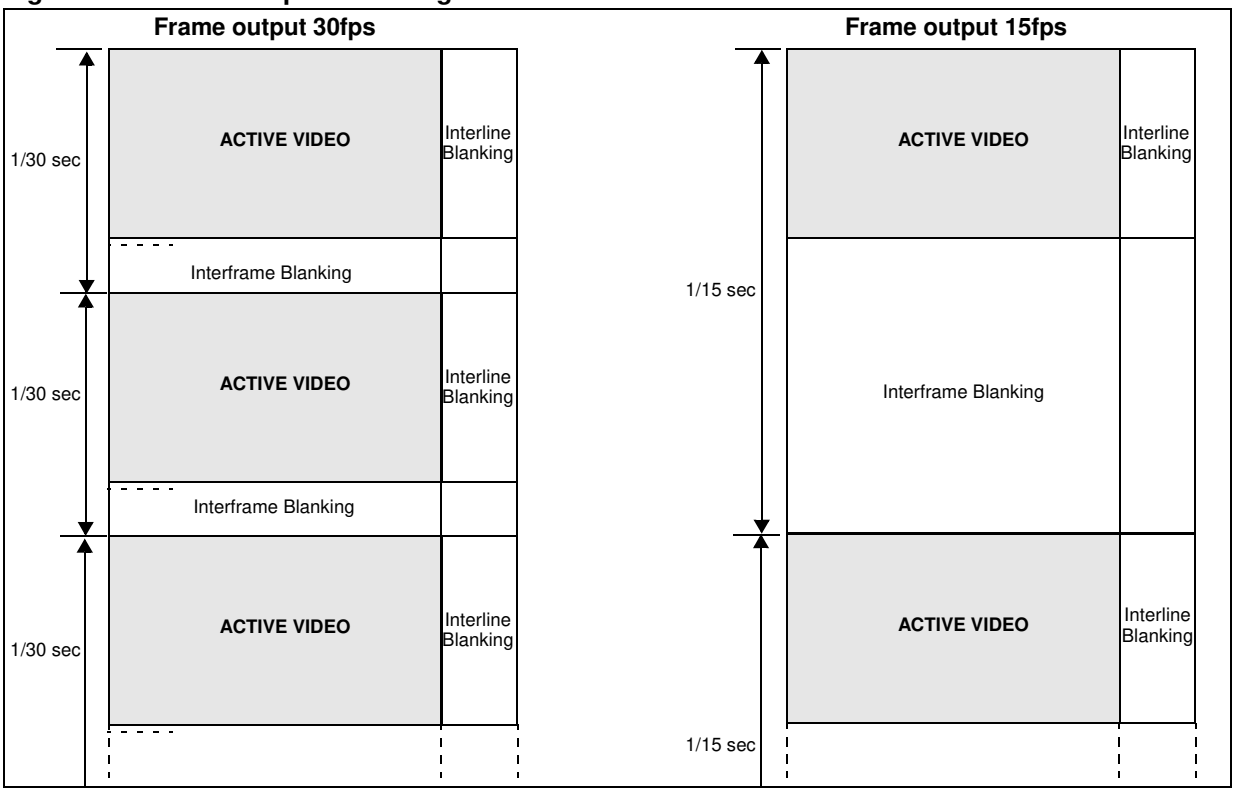
5.2 System clock division

It is possible to set an overall system clock division of 2 in the *bEnableGlobalSystemClockDivision* register (*Table 12: Clock manager input control on page 44*). This results in a PCLK of 12MHz and a maximum frame rate of 15fps VGA.

5.3 Pixel clock (PCLK)

All data output from the VL6524/VS6524 is qualified by the PCLK output. The PCLK frequency is 24 MHz (equivalent to a 12 MHz pixel rate as each pixel is represented by 2 bytes of data). For frame rates less than 30 fps the PCLK frequency is not reduced, instead additional interframe lines are added into the output data stream.

Figure 4. Frame output format against framerate



Similarly when using sub-sampled output modes the PCLK frequency is not reduced but instead pairs of PCLKs are 'dropped', see *Section 6.1.2: Subsampling module* for details.

The PCLK edge used to qualify the output data is fully programmable. It is also possible to program the state of the PCLK line (high or low) for the times when it is inactive.

5.4 PCLK gating

By default the PCLK output from the VL6524/VS6524 is *not* continuous. The PCLK qualifies all video data (and embedded codes if selected) on each video line and each interframe line but does *not* qualify the interline blanking data. In non-subsampled modes the PCLK is continuous *during* the video data output. The operation of the PCLK can be controlled using the *bPClkSetup* register (*Table 29: Output formatter control on page 53*).

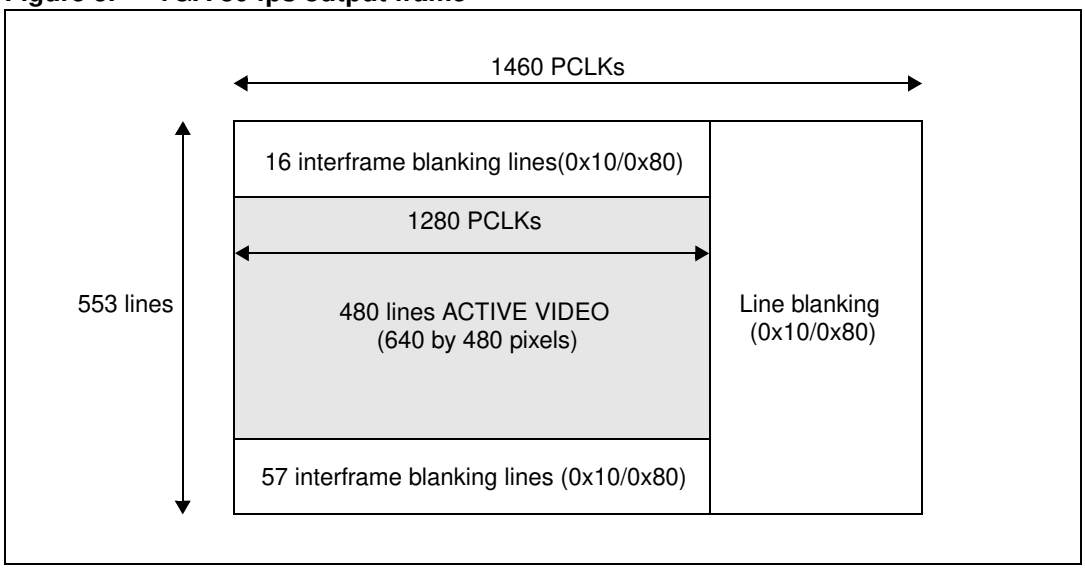
6 Output frame size control

6.1 Frame format

An output frame consists of a number of active lines and a number of interframe lines. Each line consists of embedded line codes (if selected), active pixel data and interline blank data. Note that by default the interline blanking data is *not* qualified by the PCLK and therefore is not captured by the host system.

The default 30 fps VGA output frame is shown in *Figure 5*.

Figure 5. VGA 30 fps output frame



If embedded codes are enabled then 8 additional clocks are required in every line to qualify the codes and 8 fewer interline clocks are output leaving the total constant at 1460 clocks per line.

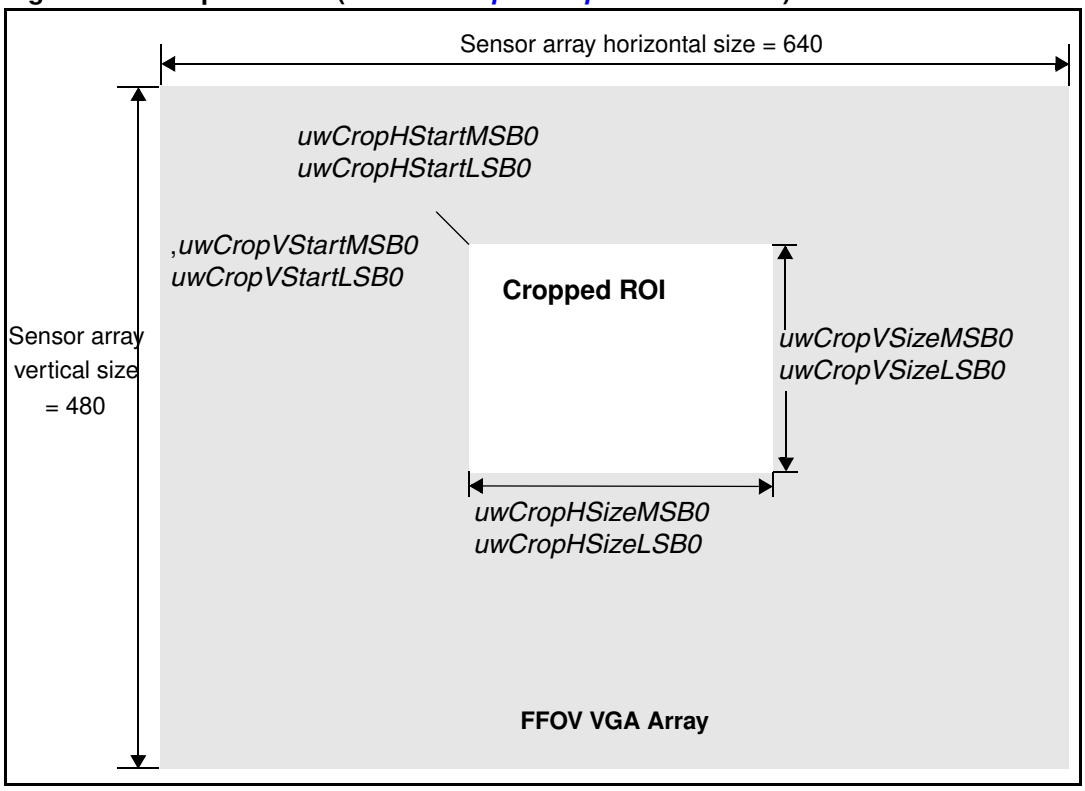
By default the PCLK output does not qualify the line blanking data and so each line contains only 1280 clocks (or 1288 if embedded codes are enabled).

The values which are output during line and frame blanking are an alternating pattern of 0x10 and 0x80 by default. These values can be changed by writing to the BlankData_MSB and BlankData_LSB registers in the *Output formatter control* bank (*Table 29 on page 53*).

6.1.1 Cropping module

The VL6524/VS6524 contains a cropping module which can be used to define a window of interest within the full VGA array size. The user can set a start location and the required output size. *Figure 6* shows the example with pipe setup bank0.

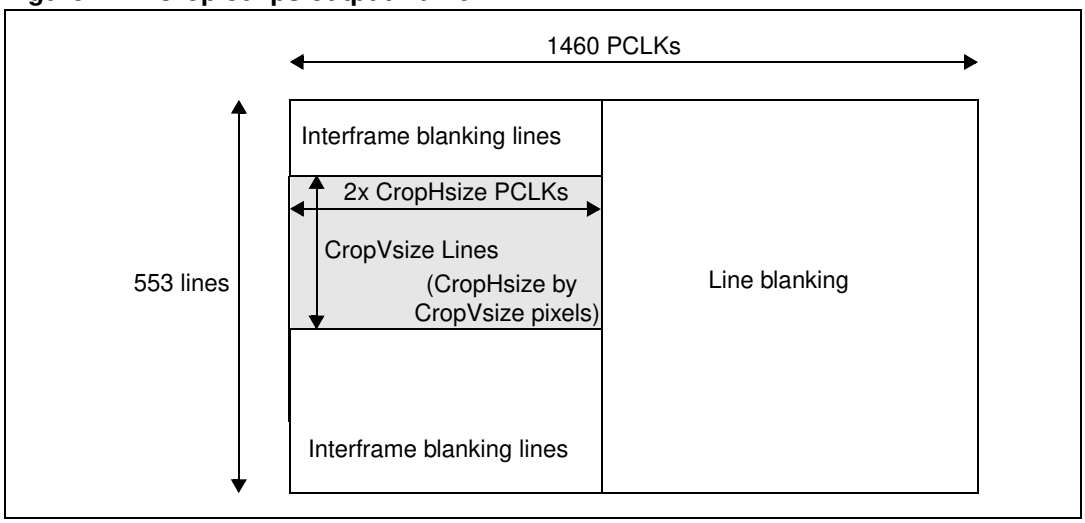
Figure 6. Crop controls (*Table 16: Pipe setup bank0 control*)



Complete lines which fall outside the window of interest are replaced in the output data frame with lines of blanking data thus the overall frame length is *not* reduced.

The portion of the output line which contains video data is reduced in length to contain only those pixels defined by the window of interest. However the *overall* line length remains unchanged as the number of interline clocks increases by the same amount.

Figure 7. Crop 30 fps output frame



6.1.2 Subsampling module

The VL6524/VS6524 has a built in sub-sampler which can divide the image by 1, 2, 3, 4, 5, or 6.

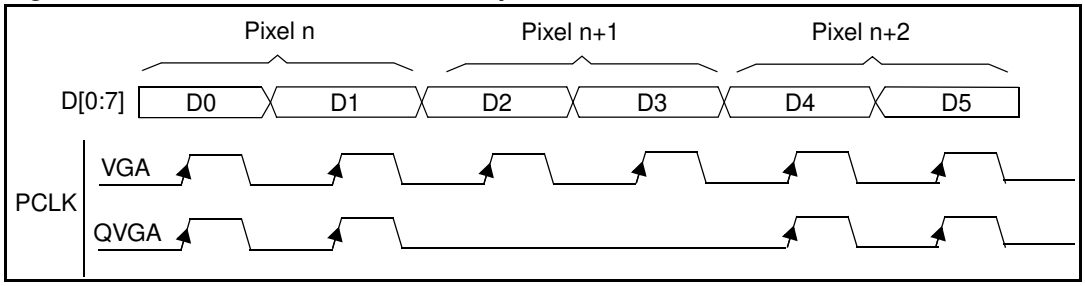
Using the sub-sampler gives output images with reduced resolution but the same field of view as the full VGA image or the region of interest defined in the cropping module. *Table 2* lists the available image sizes.

Table 2. Subsampled image sizes

Subsample ratio	Image format	Image dimensions
1 (default)	VGA	640 by 480
2	QVGA	320 by 240
3	-	213 by 160
4	QQVGA	160 by 120
5	SQCIF	128 by 96
6	-	106 by 80

Subsampled images are produced by 'dropping' PCLKs so that only certain pixels are qualified in the output data stream. The figure below indicates a portion of the PCLK waveform for VGA and QVGA images. The effect of this is that the *time* taken to readout one line of the image remains constant in all subsampled modes - it is just the number of clocks that changes.

Figure 8. PCLK waveform in subsampled modes



It is possible to use the crop module and the sub-sampler together to achieve almost any required image size. When using the crop *and* subsampling functions together then the number of lines in a frame must be an integer multiple of the subsample ratio.

6.2 Frame rate control

The VL6524/VS6524 features an extremely flexible frame rate controller. Using registers *uwDesiredFrame Rate_Num (MSB)*, *uwDesiredFrame Rate_Num (LSB)* and *bDesiredFrameRate_ Den* any desired frame rate between 1 and 30 fps can be selected (see *Table 14 on page 45* for register description). To program a required frame rate of 7.5 fps the numerator can be set to 15 and the denominator to 2. The default frame rate is 30 fps.

Slower frame rates are achieved by adding interframe lines. This results in a longer frame period and therefore a longer period over which integration is possible. Due to the longer

integration time available, slower frame rates have improved performance in low light conditions.

6.2.1 Horizontal mirror and vertical flip

The image data output from the VL6524/VS6524 can be mirrored horizontally or flipped vertically (or both).

These functions are available in the *Pipe setup bank0 control* register bank (*Table 16 on page 45*).

6.3 ViewLive Operation

ViewLive is an option which allows different size, format and image settings to be applied to alternate frames of the output data.

The controls for ViewLive function are found in the *View live control* register bank where the *fEnable* register allows the host to enable or disable the function and the *InitalPipeSetupBank* register selects which pipe setup bank is output first (see *Table 18: View live control on page 48* for register description).

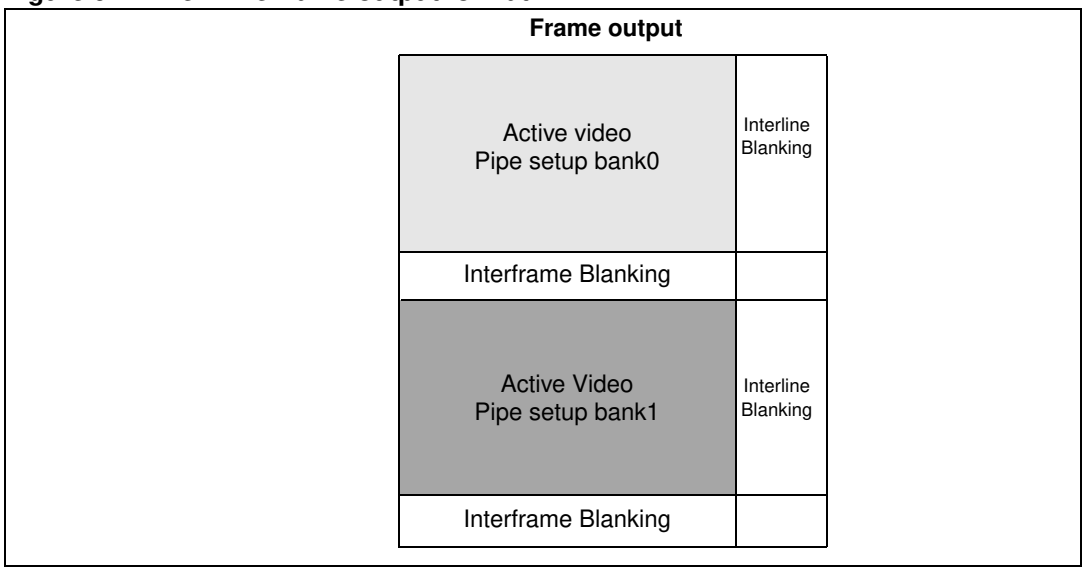
6.3.1 Video pipe setup

The key controls for VL6524/VS6524 video pipe setup are grouped into register banks called *Pipe setup bank0 control* and *Pipe setup bank1 control* (*Section 11.11* and *Section 11.12*).

Pipe setup bank0 control setup is used when ViewLive is disabled.

When ViewLive is enabled the output data switches between *Pipe setup bank0 control* and *Pipe setup bank1 control* on each alternate frame.

Figure 9. ViewLive frame output format



6.4 Context switching

It is possible to control which pipe setup bank is used and to switch between banks without the need to pause streaming, the change will occur at the next frame boundary after the change to the register has been made.

For example this function allows the VL6524/VS6524 to stream an output targeting a display (e.g. RGB 444) and switch to capture an image (e.g. YUV 4:2:2) with no need to pause streaming or enter any other operating mode.

The register *bNonViewLive_ ActivePipeSetupBank* allows selection of the pipe setup bank (*Table 15 on page 45*).

7 Output data formats

The VL6524/VS6524 supports the following data formats:

- YUV4:2:2
- RGB565
- RGB444 (encapsulated as 565)
- RGB444 (zero padded)
- Bayer 10-bit

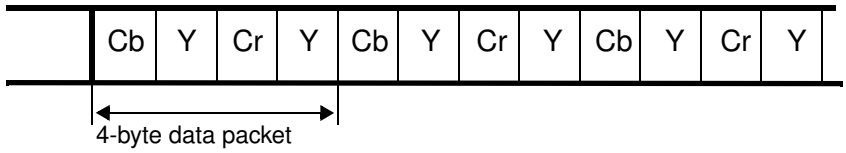
In all output formats there are 2 output bytes per pixel.

The required data format is selected using the *bdataFormat0* register described in *Table 16: Pipe setup bank0 control on page 45*. The various options available for each format are controlled using the *bRgbSetup* and *bYuvSetup* registers (*Table 29: Output formatter control on page 53*).

7.1 YUV 4:2:2 data format

YUV 422 data format requires 4 bytes of data to represent 2 adjacent pixels. ITU601-656 defines the order of the Y, Cb and Cr components as shown in *Figure 10*.

Figure 10. Standard Y Cb Cr data order



The VL6524/VS6524 *bYuvSetup* register (*Table 29: Output formatter control on page 53*) can be programmed to change the order of the components as follows:

Figure 11. Y Cb Cr data swapping options

	Y first	Cb first	Components order in 4-byte data packet 1st	2nd	3rd	4th
	1	1	Y	Cb	Y	Cr
DEFAULT	0	1	Cb	Y	Cr	Y
	1	0	Y	Cr	Y	Cb
	0	0	Cr	Y	Cb	Y

7.2 RGB and Bayer data formats

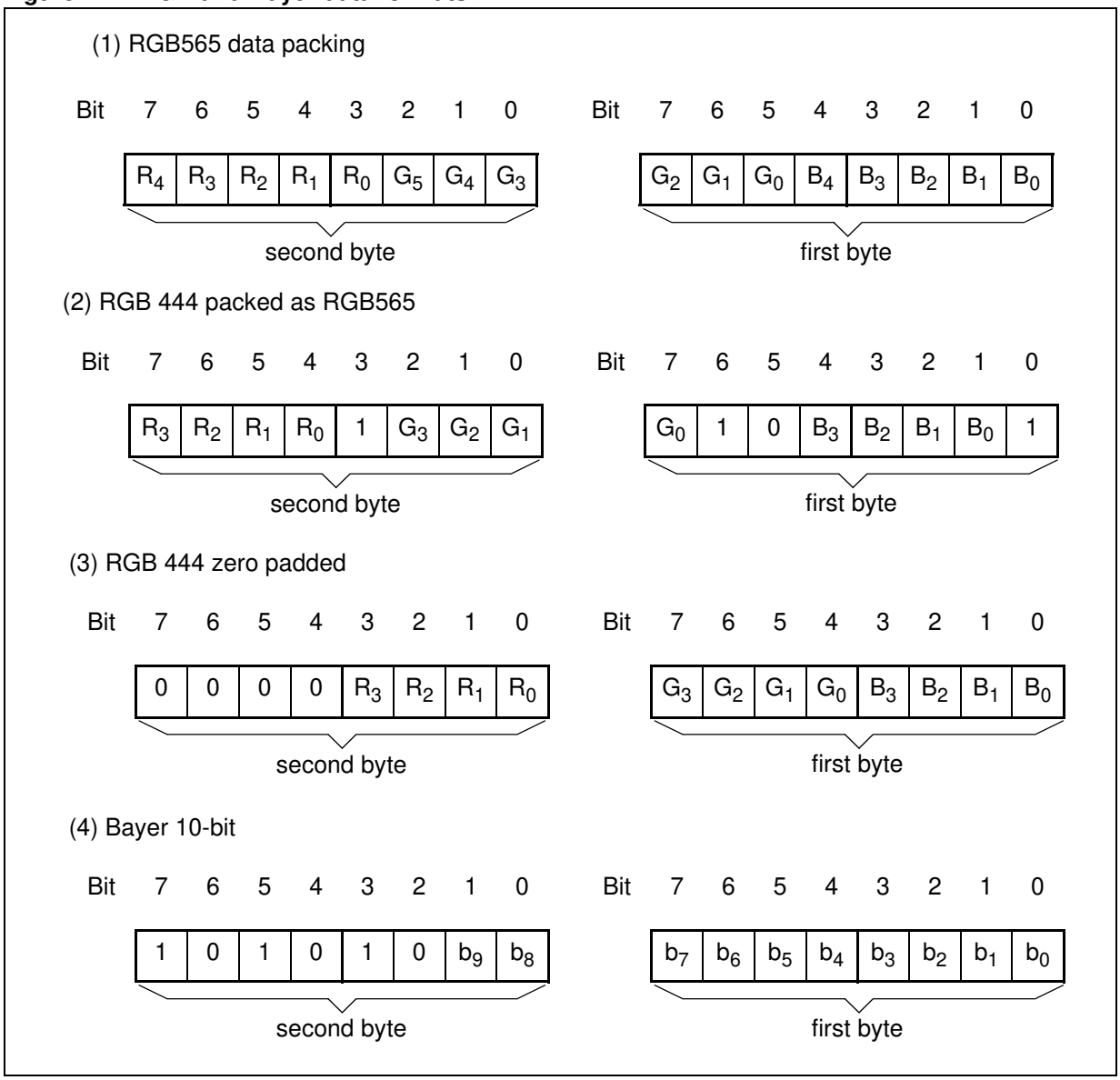
The VL6524/VS6524 can output RGB data in the following formats:

- RGB565
- RGB444 (encapsulated as RGB565)
- RGB444 (zero padded)
- Bayer 10-bit

Note: Pixels in Bayer 10-bit data output are defect corrected, correctly exposed and white balanced. Any or all of these functions can be disabled.

In each of these modes, two bytes of data are required for each output pixel. The encapsulation of the data is shown in *Figure 12*.

Figure 12. RGB and Bayer data formats



7.2.1 Manipulation of RGB data

It is possible to modify the encapsulation of the RGB data in a number of ways:

- swap the location of the RED and BLUE data
- reverse the bit order of the individual color channel data
- reverse the order of the data bytes themselves

7.2.2 Dithering

An optional dithering function can be enabled for each RGB output mode to reduce the appearance of contours produced by RGB data truncation. This is enabled through the *DitherControl* register (*Table 28 on page 52*).