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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



**VSC8531-01 Datasheet**  
**Single Port Gigabit Ethernet Copper PHY with**  
**RGMII/RMII Interfaces**





**Microsemi Corporate Headquarters**

One Enterprise, Aliso Viejo,  
CA 92656 USA

Within the USA: +1 (800) 713-4113

Outside the USA: +1 (949) 380-6100

Fax: +1 (949) 215-4996

Email: [sales.support@microsemi.com](mailto:sales.support@microsemi.com)

[www.microsemi.com](http://www.microsemi.com)

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# 1 Revision History

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The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 4.0

Revision 4.0 was the first publication of this document.

## 2 Overview

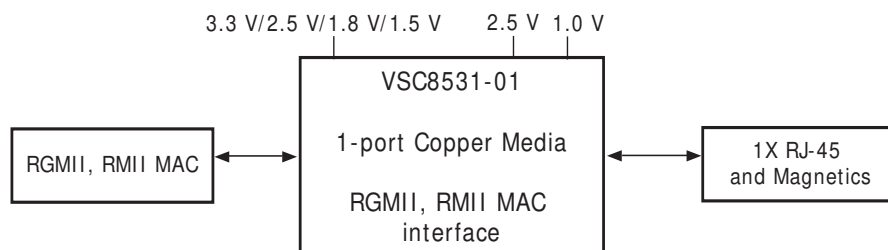
The VSC8531-01 device is designed for space-constrained 10/100/1000BASE-T applications. It features integrated, line-side termination to conserve board space, lower EMI, and improve system performance. Additionally, integrated RGMII timing compensation eliminates the need for on-board delay lines.

Microsemi's EcoEthernet™ v2.0 technology supports IEEE 802.3az Energy-Efficient Ethernet (EEE) and power-saving features to reduce power based on link state and cable reach. VSC8531-01 optimizes power consumption in all link operating speeds and features a Wake-on-LAN (WoL) power management mechanism for bringing the PHY out of a low-power state using designated magic packets.

Fast link failure (FLF) indication for high availability networks identifies the onset of a link failure in less than 1 ms typical to go beyond the IEEE 802.3 standard requirement of 750 ms ±10 ms (link master). Potential link failure events can be more flexibly monitored using an enhanced FLF2 state machine, which goes beyond FLF indication by enabling signaling of the link potentially going down within 10 μs.

The following illustration shows a high-level, general view of a typical VSC8531-01 application.

**Figure 1 • Application Diagram**



## 2.1 Key Features

This section lists the main features and benefits of the VSC8531-01 device.

### 2.1.1 Superior PHY and Interface Technology

- Integrated 10/100/1000BASE-T Ethernet copper transceiver (IEEE 802.3ab compliant) with the industry's only non-TDR-based VeriPHY™ cable diagnostics algorithm
- Patented line driver with low EMI voltage mode architecture and integrated line-side termination resistors
- Wake-on-LAN using magic packets
- HP Auto-MDIX and manual MDI/MDIX support
- RGMII/RMII MAC interface
- Jumbo frame support up to 16 kilobytes with programmable synchronization FIFOs

### 2.1.2 Fast Link Up/Link Drop Modes

- Fast link failure indication (<1 ms typical, programmable down to <10 μs)
- Supports 1000Base-T forced mode for both master and slave end point configurations with constant link self-monitoring and link auto-reset should the link come down

### 2.1.3 Best-in-Class Power Consumption

- EcoEthernet™ v2.0 green energy efficiency with ActiPHY™, PerfectReach™, and IEEE 802.3az Energy-Efficient Ethernet
- Fully optimized power consumption for all link speeds
- Clause 45 registers to support Energy-Efficient Ethernet

### 2.1.4 Key Specifications

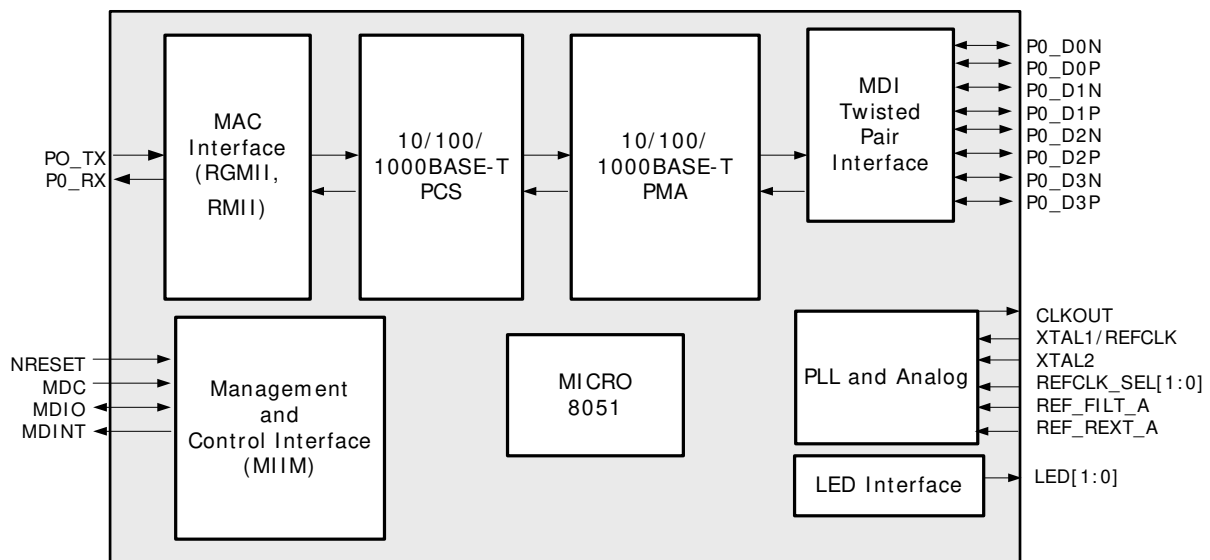
- Compliant with IEEE 802.3 (10BASE-T, 100BASE-TX, and 1000BASE-T) specifications
- Supports RGMII, RMII

- Supports 1.5 V, 1.8 V, 2.5 V, and 3.3 V CMOS for RGMII versions 1.3 and 2.0 (without HSTL support), as well as RMII version 1.2
- Supports a variety of clock sources: 25 MHz Xtal, 25 MHz OSC, 50 MHz OSC, 125 MHz OSC
- Supports programmable output frequencies of 25 MHz, 50 MHz, or 125 MHz, regardless of chosen Xtal or OSC frequencies
- Supports a wide array of stand-alone hardware configuration options
- Supports all 5 bits of MDIO/MDC addressing possible for managed mode designs using pull-up/pull-down resistors
- Devices support operating temperatures of  $-40\text{ }^{\circ}\text{C}$  ambient to  $125\text{ }^{\circ}\text{C}$  junction or  $0\text{ }^{\circ}\text{C}$  ambient to  $125\text{ }^{\circ}\text{C}$  junction
- Optionally reports if a link partner is requesting inline Power-over-Ethernet (PoE and PoE+)
- Available in 6 mm x 6 mm, 48-pin QFN package

## 2.2 Block Diagram

The following illustration shows the primary functional blocks of the VSC8531-01 device.

**Figure 2 • Block Diagram**



## 3 Functional Descriptions

This section describes the functional aspects of the VSC8531-01 device, including available configurations, operational features, and testing functionality. It also defines the device setup parameters that configure the device for a particular application.

### 3.1 Operating Modes

The following table lists the operating modes of the VSC8531-01 device.

**Table 1 • Operating Modes**

Operating Mode	Supported Media
RGMII-Cat5	10/100/1000BASE-T
RMII-Cat5	10/100BASE-T

### 3.2 MAC Interface

The VSC8531-01 device supports RMII version 1.2 and RGMII versions 1.3 and 2.0, and MAC interfaces at 1.5 V, 1.8 V, 2.5 V, and 3.3 V operating voltages. In order to help reduce EMI, the VSC8531-01 device also includes edge rate programmability for the MAC interface signals through register 27E2.7:5.

The recommended values for  $R_S$  (as shown in [Figure 3](#), page 5, [Figure 5](#), page 6, and [Figure 6](#), page 7) are listed in the following table.

**Table 2 • Recommended Values for  $R_S$  ( $\pm 5\%$ )**

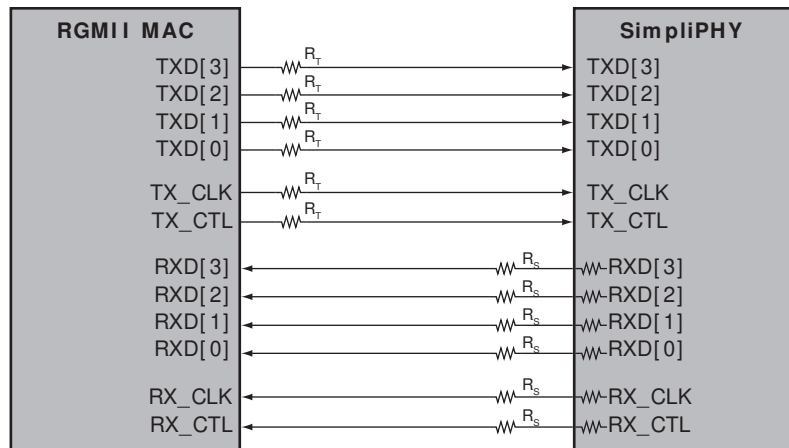
VDDMAC Value	$R_S$ Value
1.5 V	27 $\Omega$
1.8 V	33 $\Omega$
2.5 V	39 $\Omega$
3.3 V	39 $\Omega$

Refer to the MAC datasheet for the value to use for  $R_T$ .

#### 3.2.1 RGMII MAC Interface Mode

The VSC8531-01 device supports RGMII versions 1.3 and 2.0 (without HSTL modes). The RGMII interface supports all three speeds (10 Mbps, 100 Mbps, and 1000 Mbps) and is used as an interface to a RGMII-compatible MAC. The device is compliant with the RGMII interface specification when VDDMAC is operating at 2.5 V. While the RGMII specification only specifies operation at 2.5 V, the device can also support the RGMII interface at 1.5 V, 1.8 V, and 3.3 V.

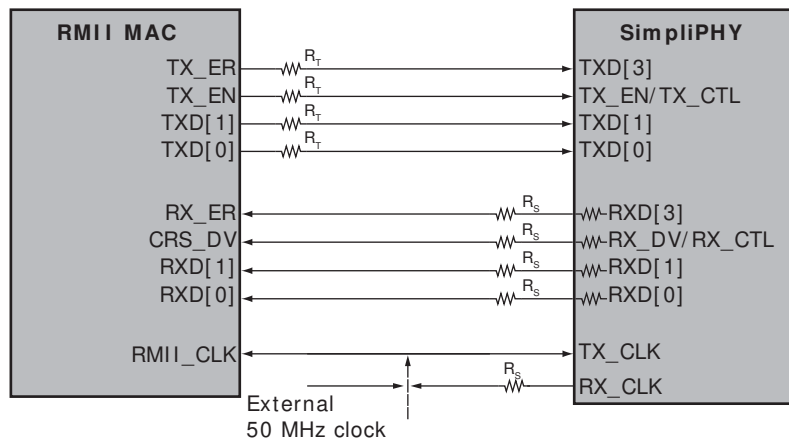
Figure 3 • RGMII MAC Interface



### 3.2.2 RMII Mode

The RMII interface supports 10 Mbps and 100 Mbps speeds, and is used as an interface to a RMII-compatible MAC. The device is compliant with the RMII interface specification when VDDMAC is operating at 3.3 V. While the RMII specification only specifies operation at 3.3 V, the device can also support the RMII interface at 1.5 V, 1.8 V, and 2.5 V.

Figure 4 • RMII MAC Interface



#### 3.2.2.1 RMII Pin Allocation

The following table lists the chip pins used for RMII signaling in RMII mode.

Table 3 • RMII Pin Allocation

Chip Pin	RMII Signal
TX_CLK	RMII_CLKIN
RX_CLK	RMII_CLKOUT
TXD3	TX_ER (to support 802.3az)
TXD1	TXD1
TXD0	TXD0
TX_CTL	TX_EN
RXD1	RXD1

**Table 3 • RMI Pin Allocation (continued)**

Chip Pin	RMI Signal
RXD0	RXD0
RXD3	RX_ER
RX_CTL	CRS_DV

Even though the RMI specification does not call for the use of TX\_ER signal, it is required in order to support Energy-Efficient Ethernet (802.3az).

### 3.2.2.2 RMI Clocking Overview

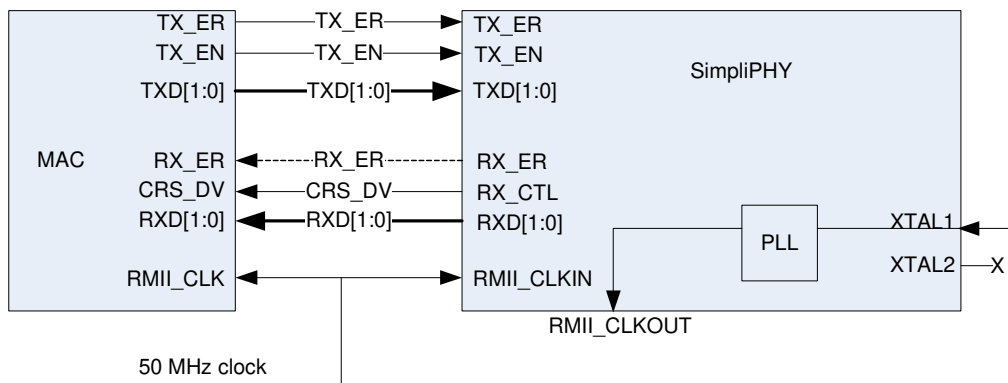
When the device is in RMI mode, the clock inputs to the device need to support the various modes in which RMI devices can operate. There are two basic modes of operation in RMI mode:

- Mode 1—system provides a 50 MHz clock that is used to clock the RMI interface and must be used as the chip reference clock.
- Mode 2—PHY operates from a 25 MHz or 125 MHz reference clock, and sources the 50 MHz clock used for the RMI interface.

These two modes of operation and the clocking schemes are described in the following sections.

#### 3.2.2.2.1 Mode 1

In this mode of operation, an external source is used to provide a 50 MHz clock through the RMI\_CLKIN and the XTAL1 pin. This 50 MHz clock is used as the main clock for the RMI interface, and must be used as the reference clock for the PHY connected to the XTAL1 pin. In this mode, the RMI\_CLKOUT signal from the PHY is not used. The RMI\_CLKOUT is enabled by default and that clock output should be disabled through register 27E2.4. The following figure illustrates RMI signal connections at the system level.

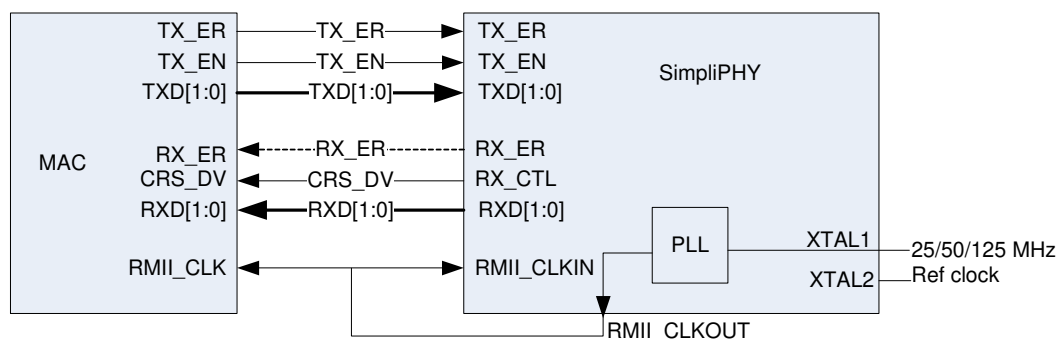
**Figure 5 • Mode 1**

#### 3.2.2.2.2 Mode 2

In this mode of operation, the PHY operates from a 25 MHz crystal (XTAL1 and XTAL2) or 25 MHz/125 MHz single-ended external clock (XTAL1), and sources the 50 MHz clock required for the RMI interface. This 50 MHz clock is output from the PHY on the RMI\_CLKOUT pin and then connected to the MAC and PHY RMI\_CLKIN signals. In this mode, the PHY generates a 50 MHz clock for the system and that clock output is enabled. The following figure illustrates RMI signal connections at the system level.



Figure 6 • Mode 2



### 3.2.3 MAC Interface Edge Rate Control

The VSC8531-01 device includes programmable control of the rise/fall times for the MAC interface signals. The default setting will select the fastest rise/fall times. However, the fast edge rate will result in higher power consumption on the MAC interface and may result in higher EMI.

It is recommended that the user select the appropriate edge rate setting based on the VDDMAC supply voltage, as shown in the following table.

**Table 4 • Recommended Edge Rate Settings**

VDDMAC Voltage	Edge Rate Setting
3.3 V	100
2.5 V	100
1.8 V	111
1.5 V	111

In order to further reduce power consumption and EMI, the user may elect to choose a slower edge rate than recommended if the end application supports it.

The MAC interface signal rise/fall times can be changed by writing to register bits 27E2.7:5. The typical change in edge rate for each setting at various VDDMAC voltages is shown in the following table.

**Table 5 • MAC Interface Edge Rate Control**

Register Setting	Edge Rate Change (VDDMAC)			
	3.3 V	2.5 V	1.8 V	1.5 V
111 (fastest)	Default	Default	Default (recommended)	Default (recommended)
110	-2%	-3%	-5%	-6%
101	-4%	-6%	-9%	-14%
100	-7% (recommended)	-10% (recommended)	-16%	-21%
011	-10%	-14%	-23%	-29%
010	-17%	-23%	-35%	-42%
001	-29%	-37%	-52%	-58%
000 (slowest)	-53%	-63%	-76%	-77%

These values are based on measurements performed on typical silicon at nominal supply and room temperature settings.

## 3.3 Hardware Mode Strapping and PHY Addressing

The VSC8531-01 device provides hardware-configured modes of operation that are achieved by sampling output pins on the rising edge of reset and externally pulling the pin to a logic HIGH or LOW (based on the desired configuration). These output pins are required by the device as inputs while NRESET is asserted and the logic state of the pin is latched in the device upon de-assertion of NRESET. To ensure correct operation of the hardware strapping function, any other device connected to these pins must not actively drive a signal onto them.

The following table describes the pins used for this purpose and their respective modes.

**Table 6 • Hardware Mode Strapping and PHY Addressing**

Pin(s)	Operation Mode
CLKOUT	Enable/disable CLKOUT signal
RX_CLK	Managed or unmanaged mode
RXD0	Signal A
RXD1	Signal B
RXD2	Signal C
RXD3	Signal D
RX_CTL	Signal E

### 3.3.1 CLKOUT Signal Configuration

When the CLKOUT signal is pulled LOW and the state of that signal is latched to logic 0 on the rising edge of reset, the CLKOUT output is disabled and the device will drive a logic low level on that pin after reset de-assertion. When the CLKOUT signal is pulled HIGH externally and the state of that signal is latched to logic 1, the CLKOUT output is enabled. This behavior can also be controlled through register 13G.15.

The CLKOUT signal is frequency-locked to the reference clock signal input through XTAL1/XTAL2 pins. The frequency of CLKOUT can be programmed to the following values through register 13G.14:13:

- 25 MHz
- 50 MHz
- 125 MHz

### 3.3.2 Managed Mode

When RX\_CLK pin is pulled LOW and the state of that signal is latched to logic 0 on the rising edge of reset, the device operates in a managed mode. In managed mode, the remaining 5 signals (A–E) are used to set the PHY address, allowing up to 32 devices to reside on the shared MDIO bus. In this mode, the device can be configured using register access and no additional hardware configurability is provided. The following table lists the assigned PHY address values in managed mode.

**Table 7 • Managed Mode**

Signal	PHY Address Values
Signal A	PHY address bit 0
Signal B	PHY address bit 1
Signal C	PHY address bit 2
Signal D	PHY address bit 3
Signal E	PHY address bit 4

### 3.3.3 Unmanaged Mode

When RX\_CLK is pulled HIGH externally and the state of that signal is latched to logic 1 on the rising edge of reset, the device operates in an unmanaged mode. In unmanaged mode, the PHY address of the device is fixed to 5'b00000. The signals A–E are used to set default chip configurations, as described in the following sections.

**Note:** Operating the device in unmanaged mode requires that the NRESET pin is asserted twice during device configuration (for more information, see [Configuration](#), page 24).

**Note:** The default values for the following registers depend on the chosen hardware strapping options.

- 0.13, 0.6—Forced speed selection
- 0.12—Enable autonegotiation
- 0.8—Duplex
- 0.9:8—1000BASE-T capability
- 23.12:11—MAC interface selection
- 19E1.3:2—Force MDI crossover
- 20E2.6:4—RX\_CLK delay
- 20E2.2:0—TX\_CLK delay

Additionally, the following registers are set to 1 by default in unmanaged mode.

- 28.6—ActiPHY enable
- 20E1.4—Link speed autodownshift enable

#### 3.3.3.1 Signals A and B

Signals A and B are used to set the RGMII RX\_CLK and TX\_CLK delay settings (as defined in register 20E2), as per the following table.

**Table 8 • Signals A and B**

Signals A, B	RX_CLK and TX_CLK Delay Setting
0, 0	000 - 0.2 ns
0, 1	010 - 1.1 ns
1, 0	100 - 2.0 ns
1, 1	110 - 2.6 ns

#### 3.3.3.2 Signals C and D

Signals C and D are used to select the link advertisement settings, as defined in the following table.

**Table 9 • Signals C and D**

Signals C, D	Link Advertisement
0, 0	Default mode of operation, 10/100/1000 FDX/HDX, autoneg ON
0, 1	10/100 FDX/HDX, autoneg ON (disable 1000BT advertisements)
1, 0	100BTX, HDX forced mode, autoneg OFF
1, 1	10BT, HDX forced mode, autoneg OFF

#### 3.3.3.3 Signal E

Signal E is used to select between RMII and RGMII MAC interface modes. When the state of Signal E is latched to logic 0 on the rising edge of reset, the device operates in RGMII mode. When the state of Signal E is latched to logic 1 on the rising edge of reset, the device operates in RMII mode.

**Note:** RMII only supports 10/100 Mbps speeds. When RMII mode is selected, the link advertisement selection must also be changed to either 01, 10, or 11 settings, as defined in [Table 9](#), page 9.

**Note:** Correct configuration of the device is an end user responsibility, and no attempt is made in the device to disallow incorrect configurations.

Additionally, in unmanaged mode, the following settings are changed from their default values:

- Enable link speed downshift (register 20E1.4 set to 1)
- Enable ActiPHY (register 28.6 set to 1)

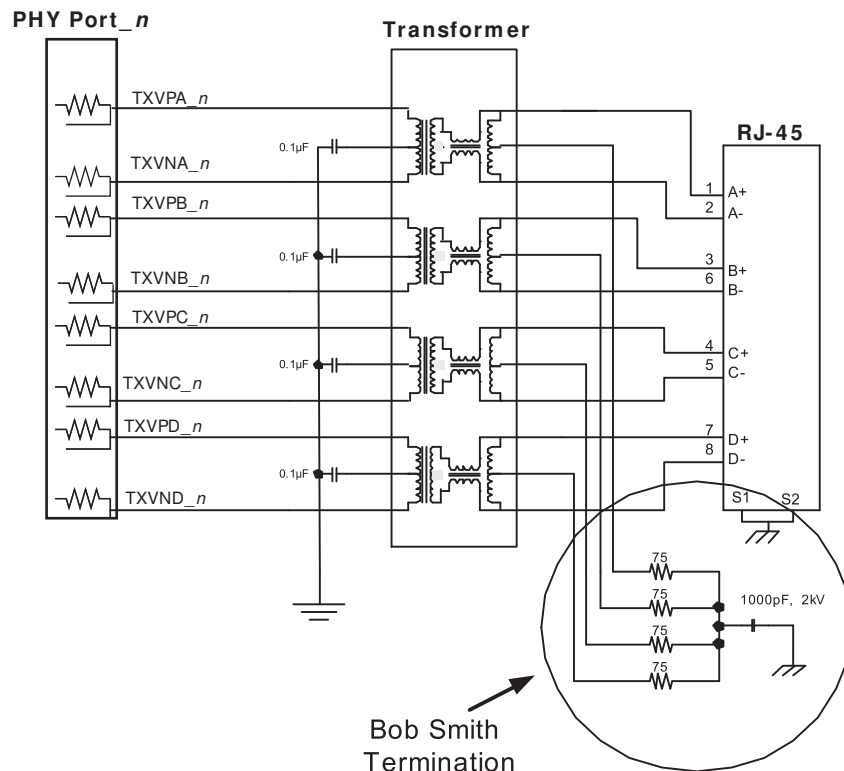
## 3.4 Cat5 Twisted Pair Media Interface

The twisted pair interface is compliant with IEEE 802.3-2008 and the IEEE 802.3az-2010 standard for Energy-Efficient Ethernet.

### 3.4.1 Voltage Mode Line Driver

The VSC8531-01 device uses a patented voltage mode line driver that allows it to fully integrate the series termination resistors that are required to connect the PHY's Cat5 interface to an external 1:1 transformer. The interface does not require the user to place an external voltage on the center tap of the magnetic. The following figure illustrates the connections.

**Figure 7 • Cat5 Media Interface**



### 3.4.2 Cat5 Auto-Negotiation and Parallel Detection

The VSC8531-01 device supports twisted pair auto-negotiation, as defined by IEEE 802.3-2008 Clause 28 and IEEE 802.3az-2010. The auto-negotiation process evaluates the advertised capabilities of the local PHY and its link partner to determine the best possible operating mode. In particular, auto-negotiation can determine speed, duplex configuration, and master or slave operating modes for 1000BASE-TX. Auto-negotiation also enables a connected MAC to communicate with its link partner MAC through the VSC8531-01 device using optional next pages to set attributes that may not otherwise be defined by the IEEE standard.

If the Category 5 (Cat5) link partner does not support auto-negotiation, the VSC8531-01 device automatically uses parallel detection to select the appropriate link speed.

Auto-negotiation is disabled by clearing register 0, bit 12. When auto-negotiation is disabled, the state of register bits 0.6, 0.13, and 0.8 determine the device operating speed and duplex mode.

**Note:** While 10BASE-T and 100BASE-TX do not require auto-negotiation, IEEE 802.3-2008 Clause 40 has defined 1000BASE-T to require auto-negotiation.

### 3.4.3 Automatic Crossover and Polarity Detection

For trouble-free configuration and management of Ethernet links, the VSC8531-01 device includes a robust automatic crossover detection feature for all three speeds on the twisted pair interface (10BASE-T, 100BASE-T, and 1000BASE-T). Known as HP Auto-MDIX, the function is fully compliant with Clause 40 of IEEE 802.3-2008.

Additionally, the device detects and corrects polarity errors on all MDI pairs—a useful capability that exceeds the requirements of the standard.

Both HP Auto-MDIX detection and polarity correction are enabled in the device by default. Default settings can be changed using device register bits 18.5:4. Status bits for each of these functions are located in register 28.

**Note:** The VSC8531-01 device can be configured to perform HP Auto-MDIX, even when auto-negotiation is disabled and the link is forced into 10/100 speeds. To enable this feature, set register 18.7 to 0. To use the feature, also set register 0.12 to 0.

The HP Auto-MDIX algorithm successfully detects, corrects, and operates with any of the MDI wiring pair combinations listed in the following table, which shows that twisted pair A (of four twisted pairs A, B, C, and D) is connected to the RJ45 connector 1, 2 in normal MDI mode.

**Table 10 • Supported MDI Pair Combinations**

RJ45 Connections				
1, 2	3, 6	4, 5	7, 8	Mode
A	B	C	D	Normal MDI
B	A	D	C	Normal MDI-X
A	B	D	C	Normal MDI with pair swap on C and D pair
B	A	C	D	Normal MDI-X with pair swap on C and D pair

### 3.4.4 Manual MDI/MDIX Setting

As an alternative to HP Auto-MDIX detection, the PHY can be forced to be MDI or MDI-X using register 19E1, bits 3:2. Setting these bits to 10 forces MDI and setting 11 forces MDI-X. Leaving the bits 00 enables the HP Auto-MDIX setting to be based on register 18, bits 7 and 5.

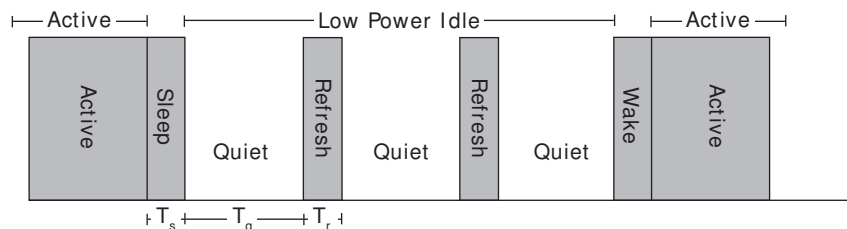
### 3.4.5 Link Speed Downshift

For operation in cabling environments that are incompatible with 1000BASE-T, the VSC8531-01 device provides an automatic link speed downshift option. When enabled, the device automatically changes its 1000BASE-T auto-negotiation advertisement to the next slower speed after a set number of failed attempts at 1000BASE-T. No reset is required to get out of this state when a subsequent link partner with 1000BASE-T support is connected. This feature is useful in setting up in networks using older cable installations that include only pairs A and B, and not pairs C and D.

To configure and monitor link speed downshifting, set register 20E1, bits 4:1.

### 3.4.6 Energy-Efficient Ethernet

The VSC8531-01 device supports the IEEE 802.3az-2010 Energy-Efficient Ethernet standard to provide a method for reducing power consumption on an Ethernet link during times of low utilization. It uses low power idles (LPI) to achieve this objective.

**Figure 8 • Low Power Idle Operation**

Using LPI, the usage model for the link is to transmit data as fast as possible and then return to a low power idle state. Energy is saved on the link by cycling between active and low power idle states. During LPI, power is reduced by turning off unused circuits and using this method, energy use scales with bandwidth utilization. The VSC8531-01 device uses LPI to optimize power dissipation in 100BASE-TX and 1000BASE-T modes of operation.

In addition, the IEEE 802.3az-2010 standard defines a 10BASE-Te mode that reduces transmit signal amplitude from 5 V peak-to-peak to approximately 3.3 V peak-to-peak. This mode reduces power consumption in 10 Mbps link speed and fully interoperates with legacy 10BASE-T-compliant PHYs over 100 m Cat5 cable or better.

To configure the VSC8531-01 device in 10BASE-Te mode, set register 17E2.15 to 1 for each port. Additional energy-efficient Ethernet features are controlled through Clause 45 registers. For more information, see [Clause 45 Registers to Support Energy-Efficient Ethernet and 802.3bf](#), page 57.

## 3.5 Reference Clock

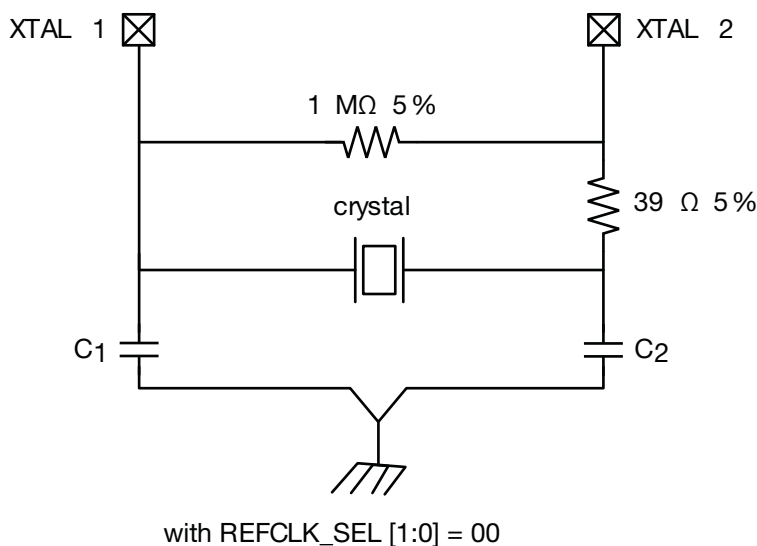
The VSC8531-01 device supports multiple reference clock input options to allow maximum system level flexibility. There are two REFCLK\_SEL signals available to allow an end user to select between the various options. The following table shows the functionality and associated reference clock frequency.

**Table 11 • REFCLK Frequency Selection**

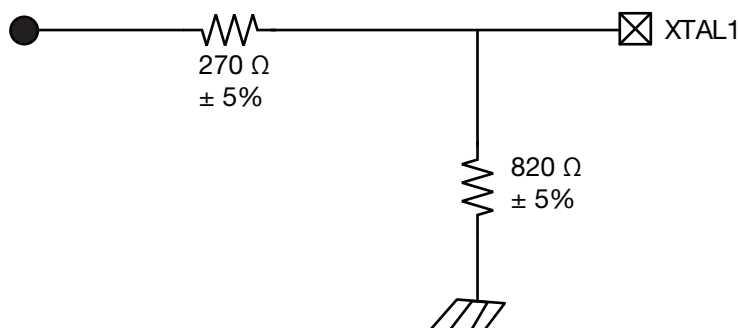
REFCLK_SEL [1:0]	Reference Clock Mode
00	25 MHz, on-chip oscillator ON (XTAL1/2 pins)
01	25 MHz, on-chip oscillator OFF (XTAL1 pin)
10	50 MHz, on-chip oscillator OFF (XTAL1 pin)
11	125 MHz, on-chip oscillator OFF (XTAL1 pin)

The following figure shows a reference tank circuit for a fundamental mode crystal.

**Note:** For best performance, traces on PCB should be of similar length and Kelvin-connected to ground.

**Figure 9 • XTAL Reference Clock**

The following figure shows an external 3.3 V reference clock.

**Figure 10 • External 3.3 V Reference Clock**

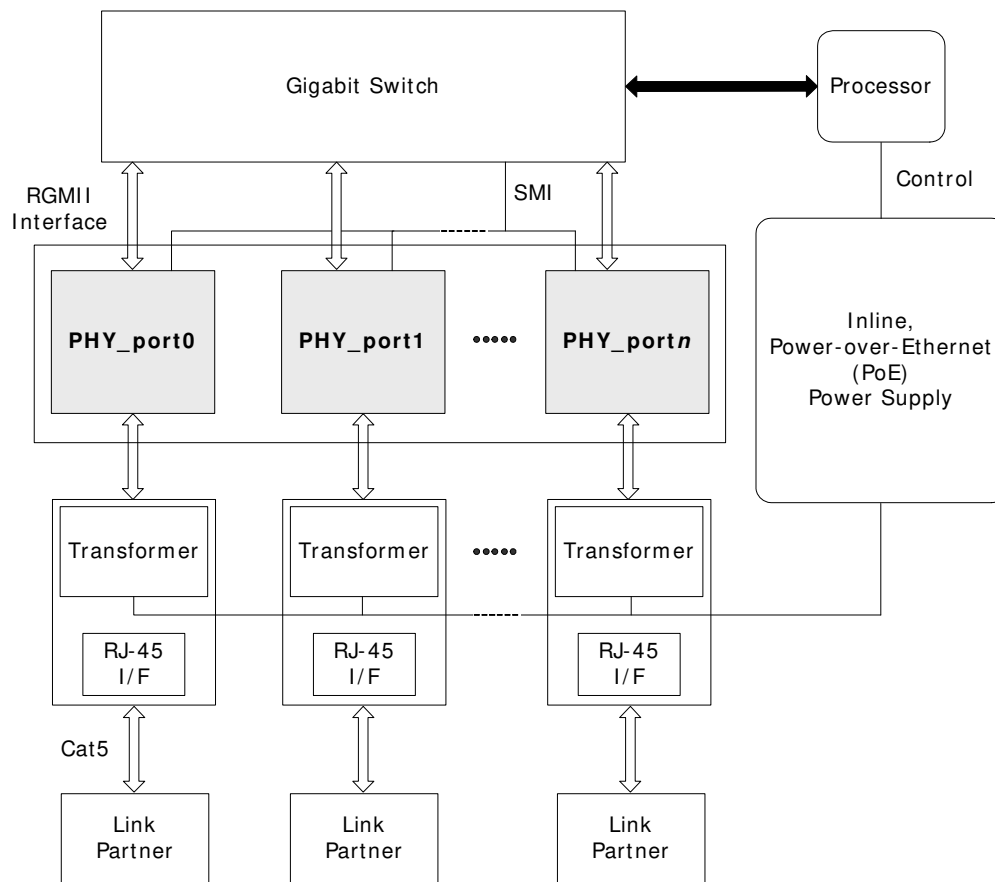
**Note:** Reference clock source less than  $\lambda/10$  from XTAL1, and routing capacitance less than 1 pF.

**Note:** No voltage scaling is required for a 2.5 V external reference.

## 3.6 Ethernet Inline-Powered Devices

The VSC8531-01 device can detect legacy inline-powered devices in Ethernet network applications. Inline-powered detection capability is useful in systems that enable IP phones and other devices (such as wireless access points) to receive power directly from their Ethernet cable, similar to office digital phones receiving power from a private branch exchange (PBX) office switch over telephone cabling. This type of setup eliminates the need for an external power supply and enables the inline-powered device to remain active during a power outage, assuming that the Ethernet switch is connected to an uninterrupted power supply, battery, back-up power generator, or other uninterruptible power source.

For more information about legacy inline-powered device detection, visit the Cisco website at [www.cisco.com](http://www.cisco.com). The following illustration shows an example of an inline-powered Ethernet switch application.

**Figure 11 • Inline-Powered Ethernet Switch Diagram**


The following procedure describes the steps that an Ethernet switch must perform to process inline-power requests made by a link partner that is, in turn, capable of receiving inline-power:

1. Enable the inline-powered device detection mode on each VSC8531-01 PHY using its serial management interface. Set register bit 23E1.10 to 1.
2. Ensure that the auto-negotiation enable bit (register 0.12) is also set to 1. In the application, the device sends a special fast link pulse signal to the link partner. Reading register bit 23E1.9:8 returns 00 during the search for devices that require Power-over-Ethernet (PoE).
3. The VSC8531-01 PHY monitors its inputs for the fast link pulse signal looped back by the link partner. A link partner capable of receiving PoE loops back the fast link pulses when the link partner is in a powered down state. This is reported when register bit 23E1.9:8 reads back 01. It can also be verified as an inline-power detection interrupt by reading register bit 26.9, which should be a 1, and which is subsequently cleared and the interrupt de-asserted after the read. When a link partner device does not loop back the fast link pulse after a specific time, register bit 23E1.9:8 automatically resets to 10.
4. If the VSC8531-01 PHY reports that the link partner requires PoE, the Ethernet switch must enable inline-power on this port, independent of the PHY.
5. The PHY automatically disables inline-powered device detection when the register bits 23E1.9:8 automatically reset to 10, and then automatically changes to its normal auto-negotiation process. A link is then autonegotiated and established when the link status bit is set (register bit 1.2 is set to 1).
6. In the event of a link failure (indicated when register bit 1.2 reads 0), it is recommended that the inline-power be disabled to the inline-powered device independent of the PHY. The VSC8531-01 PHY disables its normal auto-negotiation process and re-enables its inline-powered device detection mode.



## 3.7 IEEE 802.3af Power-over-Ethernet Support

The VSC8531-01 device is compatible with designs intended for use in systems that supply power to data terminal equipment (DTE) by means of the MDI or twisted pair cable, as described in IEEE 802.3af Clause 33.

## 3.8 ActiPHY Power Management

In addition to the IEEE-specified power down control bit (device register bit 0.11), the VSC8531-01 device also includes an ActiPHY power management mode for each PHY. This mode enables support for power-sensitive applications. It utilizes a signal-detect function that monitors the media interface for the presence of a link to determine when to automatically power down the PHY. The PHY wakes up at a programmable interval and attempts to wake up the link partner PHY by sending a burst of fast link pulse over copper media.

The ActiPHY power management mode is enabled on a per-port basis during normal operation at any time by setting register bit 28.6 to 1.

The following operating states are possible when ActiPHY mode is enabled:

- Low power state
- Link partner wake-up state
- Normal operating state (link-up state)

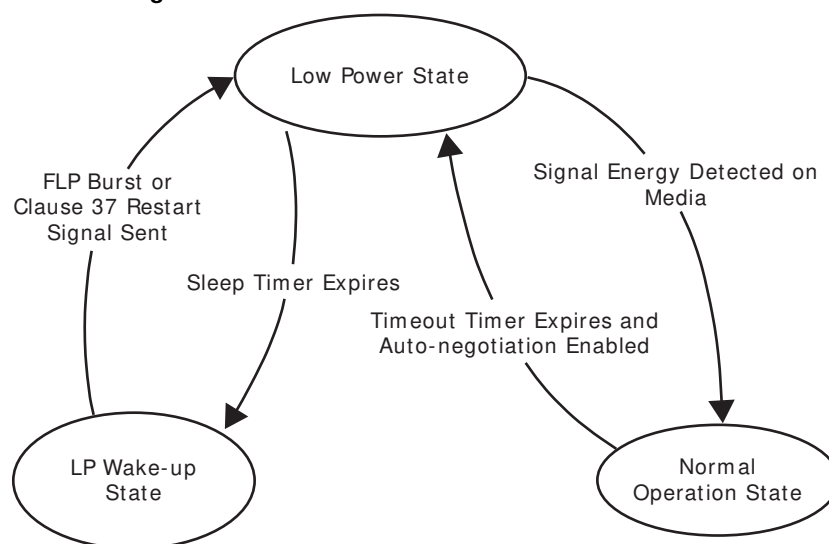
The VSC8531-01 device switches between the low power state and link partner wake-up state at a programmable rate (the default is two seconds) until signal energy has been detected on the media interface pins. When signal energy is detected, the PHY enters the normal operating state. If the PHY is in its normal operating state and the link fails, the PHY returns to the low power state after the expiration of the link status time-out timer. After reset, the PHY enters the low power state.

When auto-negotiation is enabled in the PHY, the ActiPHY state machine operates as described.

When auto-negotiation is disabled and the link is forced to use 10BASE-T or 100BASE-TX modes while the PHY is in its low power state, the PHY continues to transition between the low power and link partner wake-up states until signal energy is detected on the media pins. At that time, the PHY transitions to the normal operating state and stays in that state even when the link is dropped. When auto-negotiation is disabled while the PHY is in the normal operation state, the PHY stays in that state when the link is dropped and does not transition back to the low power state.

The following illustration shows the relationship between ActiPHY states and timers.

**Figure 12 • ActiPHY State Diagram**



### 3.8.1 Low Power State

In the low power state, all major digital blocks are powered down. However, the SMI interface (MDC, MDIO, and MDINT) functionality is provided.

In this state, the PHY monitors the media interface pins for signal energy. The PHY comes out of low power state and transitions to the normal operating state when signal energy is detected on the media. This happens when the PHY is connected to an auto-negotiation-capable link partner or another PHY in enhanced ActiPHY link partner wake-up state

In the absence of signal energy on the media pins, the PHY periodically transitions from low-power state to link partner wake-up state, based on the programmable sleep timer (register bits 20E1.14:13). The actual sleep time duration is randomized from –80 ms to 60 ms to avoid two linked PHYs in ActiPHY mode entering a lock-up state during operation.

### 3.8.2 Link Partner Wake-Up State

In the link partner wake-up state, the PHY attempts to wake up the link partner. Up to three complete fast link pulse bursts are sent on alternating pairs A and B of the Cat5 media for a duration based on the wake-up timer, which is set using register bits 20E1.12:11.

In this state, SMI interface (MDC, MDIO, and MDINT) functionality is provided.

After sending signal energy on the relevant media, the PHY returns to the low power state.

### 3.8.3 Normal Operating State

In the normal operating state, the PHY establishes a link with a link partner. When the media is unplugged or the link partner is powered down, the PHY waits for the duration of the programmable link status time-out timer, which is set using register bit 28.7 and bit 28.2. It then enters the low power state.

## 3.9 Serial Management Interface

The VSC8531-01 device includes an IEEE 802.3-compliant Serial Management Interface (SMI) that is affected by use of its MDC and MDIO pins. The SMI provides access to device control and status registers. The register set that controls the SMI consists of 32 16-bit registers, including all required IEEE-specified registers. Additional pages of registers are accessible using device register 31.

Energy-efficient Ethernet control registers are available through the SMI using Clause 45 registers and Clause 22 register access in registers 13 through 14.

The SMI is a synchronous serial interface with input data to the VSC8531-01 device on the MDIO pin that is clocked on the rising edge of the MDC pin. The output data is sent on the MDIO pin on the rising edge of the MDC signal. The interface can be clocked at a rate from 0 MHz to 12.5 MHz, depending on the total load on MDIO. An external 2 k $\Omega$  pull-up resistor is required on the MDIO pin.

### 3.9.1 SMI Frames

Data is transferred over the SMI using 32-bit frames with an optional, arbitrary-length preamble. Before the first frame can be sent, at least two clock pulses on MDC must be provided with the MDIO signal at logic one to initialize the SMI state machine. The following illustrations show the SMI frame format for read and write operations.