Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

VSC8540-04 Datasheet
Single Port Industrial Grade Fast Ethernet Copper PHY with RGMII/MII/RMII Interfaces

Microsemi
Power Matters.™

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

© 2017 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.

About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

Contents

1 Revision History 1
1.1 Revision 4.0 1
2 Overview 2
2.1 Key Features 2
2.1.1 Superior PHY and Interface Technology 2
2.1.2 Synchronous Ethernet and IEEE 1588 Time Stamp Support 2
2.1.3 Fast Link Up/Link Drop Modes 2
2.1.4 Best-in-Class Power Consumption 2
2.1.5 Key Specifications 3
2.2 Block Diagram 3
3 Functional Descriptions 4
3.1 Operating Modes 4
3.2 MAC Interface 4
3.2.1 RGMII MAC Interface Mode 4
3.2.2 MII Interface Mode 5
3.2.3 RMII Mode 5
3.2.4 MAC Interface Edge Rate Control 7
3.3 Hardware Mode Strapping and PHY Addressing 8
3.3.1 CLKOUT Signal Configuration 9
3.3.2 Managed Mode 9
3.3.3 Unmanaged Mode 9
3.3.4 MII or RGMII/RMII MAC Interface Mode 10
3.3.5 CLKOUT Frequency Selection 11
3.4 Cat5 Twisted Pair Media Interface 11
3.4.1 Voltage Mode Line Driver 11
3.4.2 Cat5 Auto-Negotiation and Parallel Detection 11
3.4.3 Automatic Crossover and Polarity Detection 12
3.4.4 Manual MDI/MDIX Setting 12
3.4.5 Energy-Efficient Ethernet 12
3.5 Reference Clock 13
3.6 Ethernet Inline-Powered Devices 14
3.7 IEEE 802.3af Power-over-Ethernet Support 16
3.8 ActiPHY Power Management 16
3.8.1 Low Power State 17
3.8.2 Link Partner Wake-Up State 17
3.8.3 Normal Operating State 17
3.9 Media Recovered Clock Output 17
3.9.1 Clock Output Squelch 17
3.10 Serial Management Interface 17
3.10.1 SMI Frames 18
3.10.2 SMI Interrupt 19
3.11 LED Interface 19
3.11.1 LED Modes 19
3.11.2 Basic Serial LED Mode 20
3.11.3 Extended LED Modes 21
3.11.4 LED Behavior 21
3.12 Wake-On-LAN and SecureOn 22
3.13 Fast Link Failure Indication 23

3.14 Fast Link Failure 2™ (FLF2™) Indication . . . 23
3.15 Forced Speed Mode Link-Up Timing . . . 23
3.16 Testing Features . . . 23
3.16.1 Ethernet Packet Generator . . . 23
3.16.2 Far-End Loopback . . . 24
3.16.3 Near-End Loopback . . . 24
3.16.4 Connector Loopback . . . 24
3.16.5 VeriPHY Cable Diagnostics . . . 25
3.17 Configuration . . . 25
3.17.1 Managed Applications . . . 25
3.17.2 Unmanaged Applications . . . 26
3.17.3 Initialization . . . 26

4 Registers . . . 27
4.1 Register and Bit Conventions . . . 27
4.2 IEEE 802.3 and Main Registers . . . 28
4.2.1 Mode Control . . . 29
4.2.2 Mode Status . . . 30
4.2.3 Device Identification . . . 30
4.2.4 Auto-Negotiation Advertisement . . . 31
4.2.5 Link Partner Auto-Negotiation Capability . . . 31
4.2.6 Auto-Negotiation Expansion . . . 32
4.2.7 Transmit Auto-Negotiation Next Page . . . 32
4.2.8 Auto-Negotiation Link Partner Next Page Receive . . . 32
4.2.9 MMD Access Control Register . . . 33
4.2.10 MMD Address or Data Register . . . 33
4.2.11 100BASE-TX Status Extension . . . 33
4.2.12 Bypass Control . . . 34
4.2.13 Error Counter 1 . . . 34
4.2.14 Error Counter 2 . . . 34
4.2.15 Error Counter 3 . . . 35
4.2.16 Extended Control and Status . . . 35
4.2.17 Extended PHY Control 1 . . . 36
4.2.18 Extended PHY Control 2 . . . 37
4.2.19 Interrupt Mask . . . 37
4.2.20 Interrupt Status . . . 38
4.2.21 Device Auxiliary Control and Status . . . 39
4.2.22 LED Mode Select . . . 39
4.2.23 LED Behavior . . . 40
4.2.24 Extended Page Access . . . 40
4.3 Extended Page 1 Registers . . . 41
4.3.1 VeriPHY Status 1 . . . 41
4.3.2 Cu Media CRC Good Counter . . . 42
4.3.3 Extended Mode Control . . . 42
4.3.4 ActiPHY Control . . . 42
4.3.5 PoE and Miscellaneous Functionality . . . 43
4.3.6 VeriPHY Control 1 . . . 44
4.3.7 VeriPHY Control 2 . . . 44
4.3.8 VeriPHY Control 3 . . . 44
4.3.9 Ethernet Packet Generator (EPG) Control 1 . . . 45
4.3.10 Ethernet Packet Generator Control 2 . . . 46
4.4 Extended Page 2 Registers . . . 46
4.4.1 Cu PMD Transmit Control . . . 46
4.4.2 EEE Control . . . 48
4.4.3 RGMII Control . . . 49
4.4.4 Wake-on-LAN MAC Address [15:0] . . . 50
4.4.5 Wake-on-LAN MAC Address [31:16] . . . 50

4.4.6 Wake-on-LAN MAC Address [47:32] . . . 50
4.4.7 Secure-On Password [15:0] . . . 50
4.4.8 Secure-On Password [31:16] . . . 51
4.4.9 Secure-On Password [47:32] . . . 51
4.4.10 Wake-on-LAN and MAC Interface Control . . . 51
4.4.11 Extended Interrupt Mask . . . 52
4.4.12 Extended Interrupt Status . . . 52
4.5 General Purpose Registers . . . 53
4.5.1 CLKOUT Control . . . 53
4.5.2 GPIO Control 2 . . . 54
4.5.3 Fast Link Configuration . . . 54
4.5.4 Recovered Clock Control . . . 54
4.5.5 Enhanced LED Control . . . 55
4.6 Clause 45 Registers to Support Energy-Efficient Ethernet and 802.3bf . . . 55
4.6.1 PMA/PMD Status 1 . . . 56
4.6.2 PCS Status 1 . . . 56
4.6.3 EEE Capability . . . 57
4.6.4 EEE Wake Error Counter . . . 57
4.6.5 EEE Advertisement . . . 57
4.6.6 EEE Link Partner Advertisement . . . 57

5 Electrical Specifications . . . 59
5.1 DC Characteristics . . . 59
5.1.1 VDDMAC, VDDIO, and VDDMDIO (2.5 V) . . . 59
5.1.2 VDDMAC, VDDIO, and VDDMDIO (3.3 V) . . . 59
5.1.3 VDDMAC and VDDMDIO (1.5 V) . . . 60
5.1.4 VDDMAC and VDDMDIO (1.8 V) . . . 60
5.1.5 VDDMDIO (1.2 V) . . . 60
5.1.6 XTAL1 . . . 61
5.1.7 LED . . . 61
5.1.8 Internal Pull-Up or Pull-Down Resistors . . . 61
5.1.9 Current Consumption . . . 61
5.1.10 Thermal Diode . . . 62
5.2 AC Characteristics . . . 63
5.2.1 Reference Clock . . . 63
5.2.2 Recovered Clock . . . 64
5.2.3 CLKOUT . . . 65
5.2.4 RMII_CLKOUT . . . 65
5.2.5 Basic Serial LEDs . . . 66
5.2.6 RMII AC Characteristics . . . 66
5.2.7 MII Transmit . . . 66
5.2.8 MII Receive . . . 67
5.2.9 Uncompensated RGMII . . . 67
5.2.10 Compensated RGMII . . . 69
5.2.11 Serial Management Interface . . . 69
5.2.12 Reset Timing . . . 70
5.3 Operating Conditions . . . 71
5.4 Stress Ratings . . . 71

6 Pin Descriptions . . . 72
6.1 Pin Identifications . . . 72
6.2 Pin Diagram . . . 72
6.3 Pins by Function . . . 73

7 Package Information . . . 78
7.1 Package Drawing . . . 78

7.2 Thermal Specifications 79
7.3 Moisture Sensitivity 80
8 Design Considerations 81
8.1 Link status LED remains on while COMA_MODE pin is asserted high 81
8.2 LED pulse stretch enable turns off LED pins 81
8.3 10BASE-T signal amplitude 81
8.4 Receive error counter only clears when NRESET applied in RMII mode 81
8.5 Anomalous PCS error indications in Energy Efficient Ethernet mode 81
8.6 10BASE-T half-duplex linkup after initial reset from power up 81
9 Ordering Information 83

Figures

Figure 1 Application Diagram . . . 2
Figure 2 Block Diagram . . . 3
Figure 3 RGMII MAC Interface . . . 5
Figure 4 MII MAC Interface . . . 5
Figure 5 RMII MAC Interface . . . 6
Figure 6 Mode 1 . . . 7
Figure 7 Mode 2 . . . 7
Figure 8 Cat5 Media Interface . . . 11
Figure 9 Low Power Idle Operation . . . 12
Figure 10 XTAL Reference Clock . . . 13
Figure 11 External 3.3 V Reference Clock . . . 14
Figure 12 Inline-Powered Ethernet Switch Diagram . . . 15
Figure 13 ActiPHY State Diagram . . . 16
Figure 14 SMI Read Frame . . . 18
Figure 15 SMI Write Frame . . . 18
Figure 16 MDINT Configured as an Open-Drain (Active-Low) Pin . . . 19
Figure 17 Wake-on-LAN Functionality . . . 22
Figure 18 Far-End Loopback Diagram . . . 24
Figure 19 Near-End Loopback Diagram . . . 24
Figure 20 Connector Loopback Diagram . . . 25
Figure 21 Register Space Diagram . . . 27
Figure 22 Thermal Diode . . . 63
Figure 23 Test Circuit for Recovered Clock Outputs Signal . . . 65
Figure 24 Basic Serial LED Timing . . . 66
Figure 25 MII Transmit Timing . . . 67
Figure 26 MII Receive Timing . . . 67
Figure 27 Uncompensated RGMII Timing . . . 68
Figure 28 Compensated Input RGMII Timing . . . 69
Figure 29 Compensated Output RGMII Timing . . . 69
Figure 30 Serial Management Interface Timing . . . 70
Figure 31 Pin Diagram . . . 73
Figure 32 Package Drawing . . . 79

Tables

Table 1 Operating Modes . . . 4
Table 2 Recommended Values for R_S (± 5%) . . . 4
Table 3 RMII Pin Allocation . . . 6
Table 4 Recommended Edge Rate Settings . . . 7
Table 5 MAC Interface Edge Rate Control . . . 8
Table 6 Hardware Mode Strapping and PHY Addressing . . . 8
Table 7 Managed Mode . . . 9
Table 8 Signals A and B . . . 10
Table 9 Signals C and D . . . 10
Table 10 CLKOUT Frequency Selection . . . 11
Table 11 Supported MDI Pair Combinations . . . 12
Table 12 REFCLK Frequency Selection . . . 13
Table 13 LED Drive State . . . 19
Table 14 LED Mode and Function Summary . . . 20
Table 15 LED Serial Bitstream Order . . . 21
Table 16 Extended LED Mode and Function Summary . . . 21
Table 17 Forced Speed Mode Link-Up Timing . . . 23
Table 18 IEEE 802.3 Registers . . . 28
Table 19 Main Registers . . . 28
Table 20 Mode Control, Address 0 (0x00) . . . 29
Table 21 Mode Status, Address 1 (0x01) . . . 30
Table 22 Identifier 1, Address 2 (0x02) . . . 30
Table 23 Identifier 2, Address 3 (0x03) . . . 30
Table 24 Device Auto-Negotiation Advertisement, Address 4 (0x04) . . . 31
Table 25 Auto-Negotiation Link Partner Ability, Address 5 (0x05) . . . 31
Table 26 Auto-Negotiation Expansion, Address 6 (0x06) . . . 32
Table 27 Auto-Negotiation Next Page Transmit, Address 7 (0x07) . . . 32
Table 28 Auto-Negotiation LP Next Page Receive, Address 8 (0x08) . . . 32
Table 29 MMD EEE Access, Address 13 (0x0D) . . . 33
Table 30 MMD Address or Data Register, Address 14 (0x0E) . . . 33
Table 31 100BASE-TX Status Extension, Address 16 (0x10) . . . 33
Table 32 Bypass Control, Address 18 (0x12) . . . 34
Table 33 Extended Control and Status, Address 19 (0x13) . . . 34
Table 34 Extended Control and Status, Address 20 (0x14) . . . 34
Table 35 Extended Control and Status, Address 21 (0x15) . . . 35
Table 36 Extended Control and Status, Address 22 (0x16) . . . 35
Table 37 Extended PHY Control 1, Address 23 (0x17) . . . 36
Table 38 Extended PHY Control 2, Address 24 (0x18) . . . 37
Table 39 Interrupt Mask, Address 25 (0x19) . . . 37
Table 40 Interrupt Status, Address 26 (0x1A) . . . 38
Table 41 Auxiliary Control and Status, Address 28 (0x1C) . . . 39
Table 42 LED Mode Select, Address 29 (0x1D) . . . 40
Table 43 LED Behavior, Address 30 (0x1E) . . . 40
Table 44 Extended/GPIO Register Page Access, Address 31 (0x1F) . . . 41
Table 45 Extended Registers Page 1 Space . . . 41
Table 46 VeriPHY Status Register 1, Address 16E1 (0x10) . . . 41
Table 47 Cu Media CRC Good Counter, Address 18E1 (0x12) . . . 42
Table 48 Extended Mode Control, Address 19E1 (0x13) . . . 42
Table 49 Extended PHY Control 3, Address 20E1 (0x14) . . . 42
Table 50 Extended PHY Control 4, Address 23E1 (0x17) . . . 43
Table 51 VeriPHY Control Register 1, Address 24E1 (0x18) . . . 44
Table 52 VeriPHY Control Register 2, Address 25E1 (0x19) . . . 44
Table 53 VeriPHY Control Register 3, Address 26E1 (0x1A) . . . 44
Table 54 VeriPHY Control Register 3 Fault Codes . . . 44

Table 55 EPG Control Register 1, Address 29E1 (0x1D) . . . 45
Table 56 EPG Control Register 2, Address 30E1 (0x1E) . . . 46
Table 57 Extended Registers Page 2 Space . . . 46
Table 58 Cu PMD Transmit Control, Address 16E2 (0x10) . . . 47
Table 59 EEE Control, Address 17E2 (0x11) . . . 48
Table 60 RGMII Control, Address 20E2 (0x14) . . . 49
Table 61 Wake-on-LAN MAC Address, 21E2 (0x15) . . . 50
Table 62 Wake-on-LAN MAC Address, 22E2 (0x16) . . . 50
Table 63 Wake-on-LAN MAC Address, 23E2 (0x17) . . . 50
Table 64 Secure-On Password, 24E2 (0x18) . . . 50
Table 65 Secure-On Password, 25E2 (0x19) . . . 51
Table 66 Secure-On Password, 26E2 (0x1A) . . . 51
Table 67 WoL and MAC Interface Control, Address 27E2 (0x1B) . . . 51
Table 68 Extended Interrupt Mask, Address 28E2 (0x1C) . . . 52
Table 69 Extended Interrupt Status, Address 29E2 (0x1D) . . . 52
Table 70 General Purpose Registers Space . . . 53
Table 71 CLKOUT Control, Address 13G (0x0D) . . . 53
Table 72 GPIO Control 2, Address 14G (0x0E) . . . 54
Table 73 MAC Configuration and Fast Link Register, Address 19G (0x13) . . . 54
Table 74 Recovered Clock Control, Address 23G (0x17) . . . 54
Table 75 Enhanced LED Control, Address 25G (0x19) . . . 55
Table 76 Clause 45 Registers Page Space . . . 55
Table 77 PMA/PMD Status 1 . . . 56
Table 78 PCS Status 1, Address 3.1 . . . 56
Table 79 EEE Capability, Address 3.20 . . . 57
Table 80 EEE Wake Error Counter, Address 3.22 . . . 57
Table 81 EEE Advertisement, Address 7.60 . . . 57
Table 82 EEE Advertisement, Address 7.61 . . . 57
Table 83 802.3bf Registers . . . 58
Table 84 VDDMAC, VDDIO, and VDDMDIO (2.5 V) DC Characteristics . . . 59
Table 85 VDDMAC, VDDIO, and VDDMDIO (3.3 V) DC Characteristics . . . 59
Table 86 VDDMAC and VDDMDIO DC Characteristics (1.5 V) . . . 60
Table 87 VDDMAC and VDDMDIO DC Characteristics (1.8 V) . . . 60
Table 88 VDDMDIO DC Characteristics . . . 60
Table 89 XTAL1 DC Characteristics . . . 61
Table 90 LED DC Characteristics . . . 61
Table 91 Internal Pull-Up or Pull-Down Resistors (MII/RGMII/RMII Interface) . . . 61
Table 92 Internal Pull-Up or Pull-Down Resistors (Other I/Os) . . . 61
Table 93 Current Consumption . . . 62
Table 94 Current Consumption (VDDMAC) . . . 62
Table 95 Thermal Diode Parameters . . . 63
Table 96 RefClk . . . 63
Table 97 XTAL RefClk . . . 64
Table 98 Recovered Clock AC Characteristics . . . 64
Table 99 CLKOUT AC Characteristics . . . 65
Table 100 RMII_CLKOUT AC Characteristics . . . 65
Table 101 Basic Serial LEDs AC Characteristics . . . 66
Table 102 RMII AC Characteristics . . . 66
Table 103 MII Transmit AC Characteristics . . . 66
Table 104 MII Receive AC Characteristics . . . 67
Table 105 Uncompensated RGMII AC Characteristics . . . 67
Table 106 PHY Input (GTX_CLK Delay When Register 20E2.[2:0]=011’b) . . . 69
Table 107 PHY Output (RX_CLK Delay When Register 20E2.[6:4]=100’b) . . . 69
Table 108 Serial Management Interface AC Characteristics . . . 69
Table 109 Reset Timing AC Characteristics . . . 70
Table 110 Recommended Operating Conditions . . . 71
Table 111 Stress Ratings . . . 71
Table 112 Pin Type Symbol Definitions . . . 72
Table 113 Thermal Resistances . . . 80

Table 114 Ordering Information 83

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.0

Revision 4.0 was the first publication of this document.

2 Overview

The VSC8540-04 device is designed for space-constrained 10/100BASE-TX applications. It features integrated, line-side termination to conserve board space, lower EMI, and improve system performance. Additionally, integrated RGMII timing compensation eliminates the need for on-board delay lines.

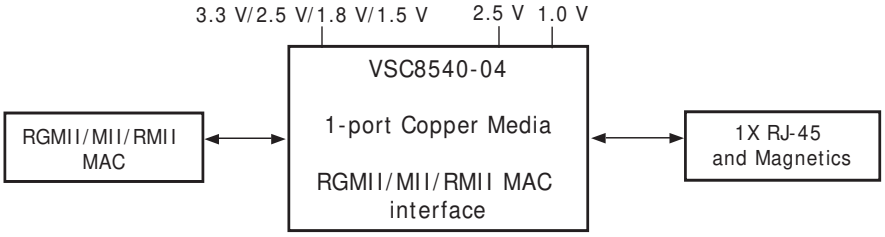
Microsemi's EcoEthernet™ v2.0 technology supports IEEE 802.3az Energy-Efficient Ethernet (EEE) and power-saving features to reduce power based on link state and cable reach. VSC8540-04 optimizes power consumption in all link operating speeds and features a Wake-on-LAN (WoL) power management mechanism for bringing the PHY out of a low-power state using designated magic packets.

Fast link failure (FLF) indication for high availability networks identifies the onset of a link failure in accordance with the 802.3 link status register value for 10BASE-T/100BASE-TX links. Potential link failure events can be more flexibly monitored using an enhanced FLF2 state machine, which goes beyond FLF indication by enabling signaling of the link potentially going down within 150 µS.

The device includes recovered clock output for Synchronous Ethernet applications. Programmable clock squelch control is included to inhibit undesirable clocks from propagating and to help prevent timing loops.

The following illustration shows a high-level, general view of a typical VSC8540-04 application.

Figure 1 • **Application Diagram**



2.1 Key Features

This section lists the main features and benefits of the VSC8540-04 device.

2.1.1 Superior PHY and Interface Technology

- Integrated 10/100BASE-TX Ethernet copper transceiver with the industry's only non-TDR-based VeriPHY™ cable diagnostics algorithm
- Patented line driver with low EMI voltage mode architecture and integrated line-side termination resistors
- Wake-on-LAN using magic packets
- HP Auto-MDIX and manual MDI/MDIX support
- RGMII/MII/RMII MAC interface
- Jumbo frame support up to 16 kilobytes with programmable synchronization FIFOs

2.1.2 Synchronous Ethernet and IEEE 1588 Time Stamp Support

- Recovered clock output with programmable clock squelch control for G.8261 Synchronous Ethernet applications
- Clock output squelch to inhibit clocks during auto-negotiation and no link status
- Clause 45 registers to support IEEE 802.3bf

2.1.3 Fast Link Up/Link Drop Modes

- Fast link failure indication (<1 ms typical, programmable down to <10 µS)

2.1.4 Best-in-Class Power Consumption

- EcoEthernet™ v2.0 green energy efficiency with ActiPHY™, PerfectReach™, and IEEE 802.3az Energy-Efficient Ethernet

- Fully optimized power consumption for all link speeds
- Clause 45 registers to support Energy-Efficient Ethernet

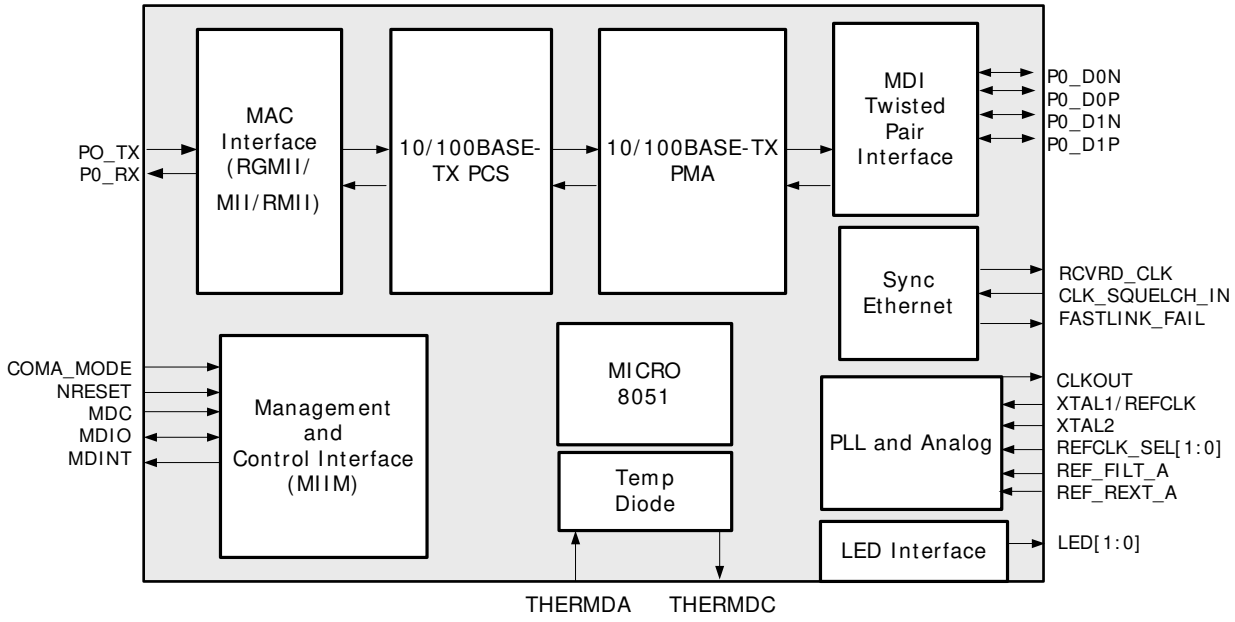
2.1.5 Key Specifications

- Compliant with IEEE 802.3 (10BASE-T, 100BASE-TX) specifications
- Supports RGMII, MII, RMII
- Supports 1.5 V, 1.8 V, 2.5 V, and 3.3 V CMOS for RGMII versions 1.3 and 2.0 (without HSTL support), MII as well as RMII version 1.2
- Supports a variety of clock sources: 25 MHz Xtal, 25 MHz OSC, 50 MHz OSC, 125 MHz OSC
- Supports programmable output frequencies of 25 MHz, 50 MHz, or 125 MHz, regardless of chosen Xtal or OSC frequencies
- Supports a wide array of stand-alone hardware configuration options
- Supports all 5 bits of MDIO/MDC addressing possible for managed mode designs using pull-up/pull-down resistors
- Device supports operating temperature of –40 °C ambient to 125 °C junction
- Optionally reports if a link partner is requesting inline Power-over-Ethernet (PoE and PoE+)
- Available in 8 mm x 8 mm, 68-pin QFN package

2.2 Block Diagram

The following illustration shows the primary functional blocks of the VSC8540-04 device.

Figure 2 • **Block Diagram**



3 Functional Descriptions

This section describes the functional aspects of the VSC8540-04 device, including available configurations, operational features, and testing functionality. It also defines the device setup parameters that configure the device for a particular application.

3.1 Operating Modes

The following table lists the operating modes of the VSC8540-04 device.

Table 1 • **Operating Modes**

Operating Mode	Supported Media
RGMII-Cat5	10/100BASE-TX
MII-Cat5	10/100BASE-TX
RMII-Cat5	10/100BASE-TX

3.2 MAC Interface

The VSC8540-04 device supports RMII version 1.2, RGMII versions 1.3 and 2.0, and MII MAC interfaces at 1.5 V, 1.8 V, 2.5 V, and 3.3 V operating voltages. In order to help reduce EMI, the VSC8540-04 device also includes edge rate programmability for the MAC interface signals through register 27E2.7:5.

The recommended values for R_S (as shown in Figure 3, page 5, Figure 6, page 7, and Figure 7, page 7) are listed in the following table.

Table 2 • **Recommended Values for R_S (± 5%)**

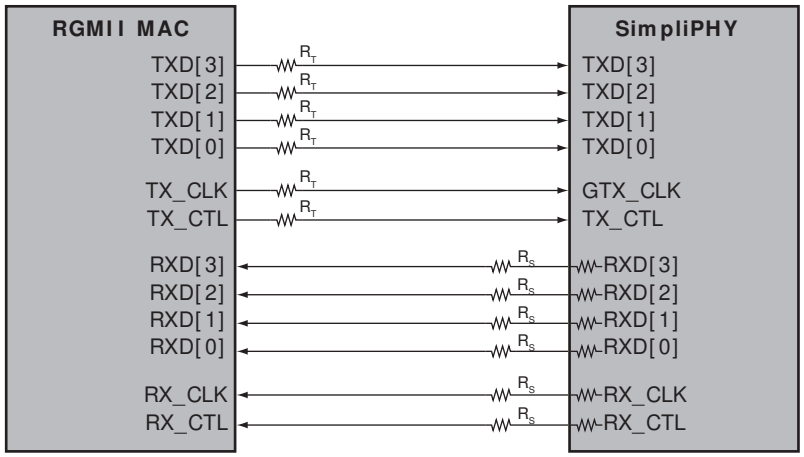
VDDMAC Value	R_S Value
1.5 V	27 Ω
1.8 V	33 Ω
2.5 V	39 Ω
3.3 V	39 Ω

Refer to the MAC datasheet for the value to use for R_T.

3.2.1 RGMII MAC Interface Mode

The VSC8540-04 device supports RGMII versions 1.3 and 2.0 (without HSTL modes). The RGMII interface supports 10 Mbps and 100 Mbps speeds, and is used as an interface to a RGMII-compatible MAC. The device is compliant with the RGMII interface specification when VDDMAC is operating at 2.5 V. While the RGMII specification only specifies operation at 2.5 V, the device can also support the RGMII interface at 1.5 V, 1.8 V, and 3.3 V.

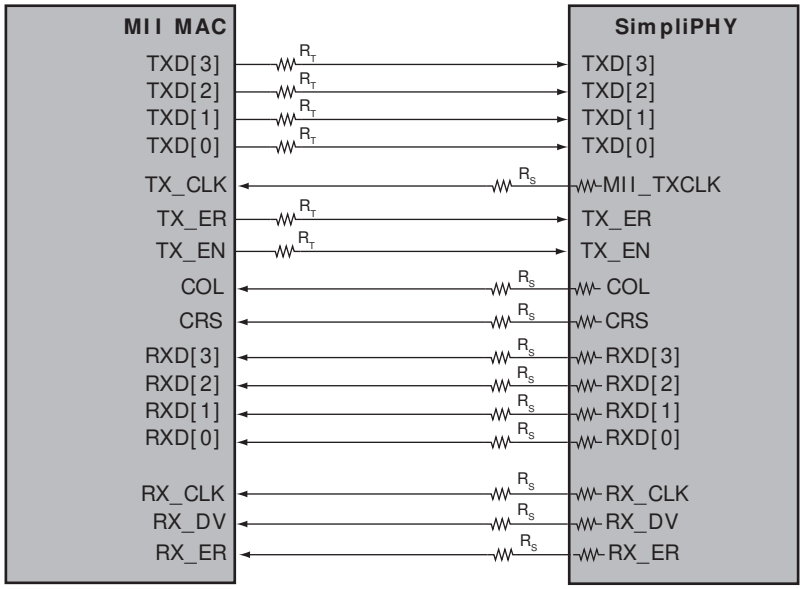
Figure 3 • **RGMII MAC Interface**



3.2.2 MII Interface Mode

The MII interface supports 10 Mbps and 100 Mbps speeds, and is used as an interface to a MII-compatible MAC. The device is compliant with the MII interface specification when VDDMAC is operating at 3.3 V. While the MII specification only specifies operation at 3.3 V, the device can also support the MII interface at 1.5 V, 1.8 V, and 2.5 V.

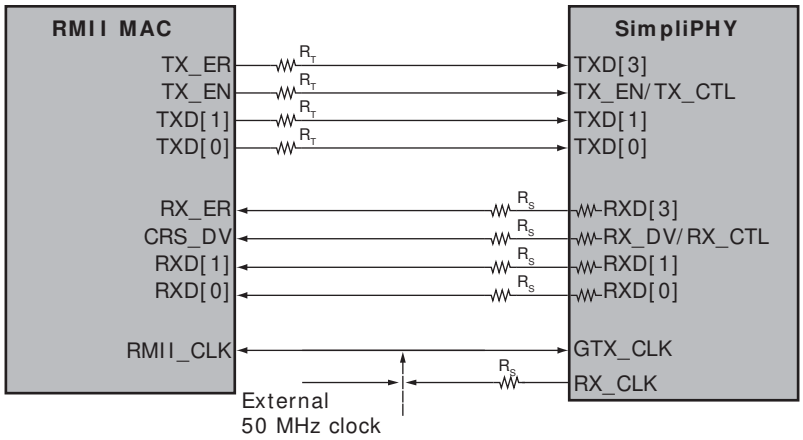
Figure 4 • **MII MAC Interface**



3.2.3 RMII Mode

The RMII interface supports 10 Mbps and 100 Mbps speeds, and is used as an interface to a RMII-compatible MAC. The device is compliant with the RMII interface specification when VDDMAC is operating at 3.3 V. While the RMII specification only specifies operation at 3.3 V, the device can also support the RMII interface at 1.5 V, 1.8 V, and 2.5 V.

Figure 5 • **RMII MAC Interface**



3.2.3.1 RMII Pin Allocation

The following table lists the chip pins used for RMII signaling in RMII mode.

Table 3 • **RMII Pin Allocation**

Chip Pin	RMII Signal
TX_CLK	RMII_CLKIN
RX_CLK	RMII_CLKOUT
TXD3	TX_ER (to support 802.3az)
TXD1	TXD1
TXD0	TXD0
TX_EN/TX_CTL	TX_EN
RXD1	RXD1
RXD0	RXD0
RXD3	RX_ER
RX_DV/RX_CTL	CRS_DV

Even though the RMII specification does not call for the use of TX_ER signal, it is required in order to support Energy-Efficient Ethernet (802.3az).

3.2.3.2 RMII Clocking Overview

When the device is in RMII mode, the clock inputs to the device need to support the various modes in which RMII devices can operate. There are two basic modes of operation in RMII mode:

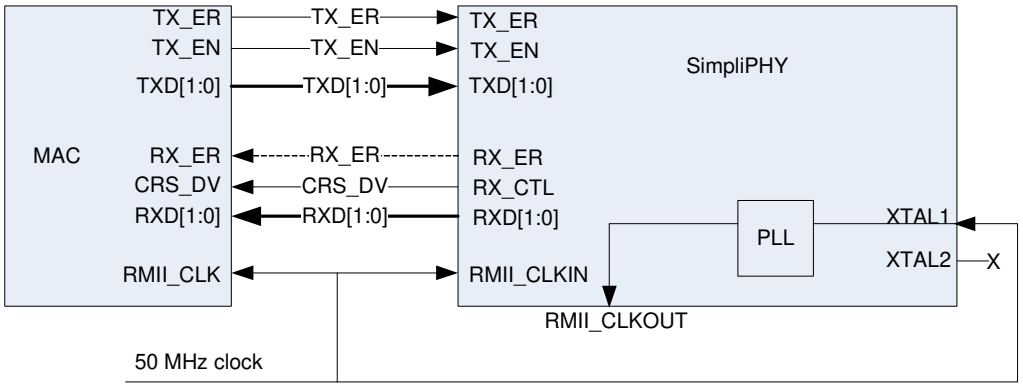
- Mode 1—system provides a 50 MHz clock that is used to clock the RMII interface and must be used as the chip reference clock.
- Mode 2—PHY operates from a 25 MHz or 125 MHz reference clock, and sources the 50 MHz clock used for the RMII interface.

These two modes of operation and the clocking schemes are described in the following sections.

3.2.3.2.1 Mode 1

In this mode of operation, an external source is used to provide a 50 MHz clock through the RMII_CLKIN and the XTAL1 pin. This 50 MHz clock is used as the main clock for the RMII interface, and must be used as the reference clock for the PHY connected to the XTAL1 pin. In this mode, the RMII_CLKOUT signal from the PHY is not used. The RMII_CLKOUT is enabled by default and that clock output should be disabled through register 27E2.4. The following figure illustrates RMII signal connections at the system level.

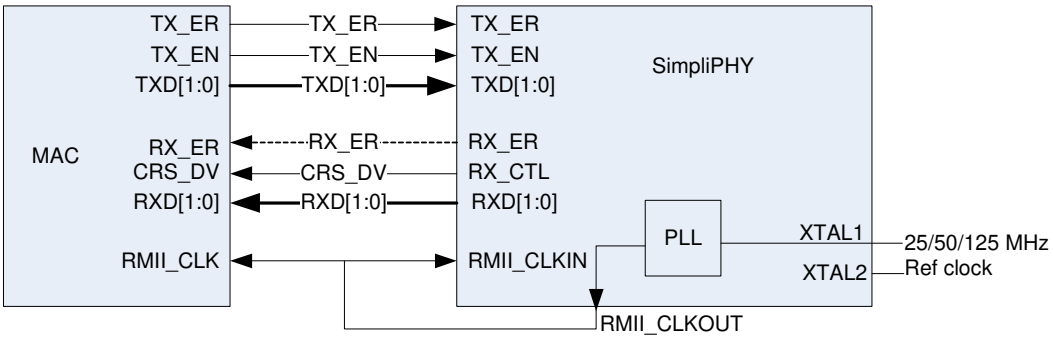
Figure 6 • **Mode 1**



3.2.3.2.2 Mode 2

In this mode of operation, the PHY operates from a 25 MHz crystal (XTAL1 and XTAL2) or 25 MHz/125 MHz single-ended external clock (XTAL1), and sources the 50 MHz clock required for the RMII interface. This 50 MHz clock is output from the PHY on the RMII_CLKOUT pin and then connected to the MAC and PHY RMII_CLKIN signals. In this mode, the PHY generates a 50 MHz clock for the system and that clock output is enabled. The following figure illustrates RMII signal connections at the system level.

Figure 7 • **Mode 2**



3.2.4 MAC Interface Edge Rate Control

The VSC8540-04 device includes programmable control of the rise/fall times for the MAC interface signals. The default setting will select the fastest rise/fall times. However, the fast edge rate will result in higher power consumption on the MAC interface and may result in higher EMI.

It is recommended that the user select the appropriate edge rate setting based on the VDDMAC supply voltage, as shown in the following table.

Table 4 • **Recommended Edge Rate Settings**

VDDMAC Voltage	Edge Rate Setting
3.3 V	100
2.5 V	100
1.8 V	111
1.5 V	111

In order to further reduce power consumption and EMI, the user may elect to choose a slower edge rate than recommended if the end application supports it.

The MAC interface signal rise/fall times can be changed by writing to register bits 27E2.7:5. The typical change in edge rate for each setting at various VDDMAC voltages is shown in the following table.

Table 5 • **MAC Interface Edge Rate Control**

	Edge Rate Change (VDDMAC)			
Register Setting	**3.3 V**	**2.5 V**	**1.8 V**	**1.5 V**
111 (fastest)	Default	Default	Default (recommended)	Default (recommended)
110	–2%	–3%	–5%	–6%
101	–4%	–6%	–9%	–14%
100	–7% (recommended)	–10% (recommended)	–16%	–21%
011	–10%	–14%	–23%	–29%
010	–17%	–23%	–35%	–42%
001	–29%	–37%	–52%	–58%
000 (slowest)	–53%	–63%	–76%	–77%

These values are based on measurements performed on typical silicon at nominal supply and room temperature settings.

3.3 Hardware Mode Strapping and PHY Addressing

The VSC8540-04 device provides hardware-configured modes of operation that are achieved by sampling output pins on the rising edge of reset and externally pulling the pin to a logic HIGH or LOW (based on the desired configuration). These output pins are required by the device as inputs while NRESET is asserted and the logic state of the pin is latched in the device upon de-assertion of NRESET. To ensure correct operation of the hardware strapping function, any other device connected to these pins must not actively drive a signal onto them.

The following table describes the pins used for this purpose and their respective modes.

Table 6 • **Hardware Mode Strapping and PHY Addressing**

Pin(s)	**Operation Mode**
CLKOUT	Enable/disable CLKOUT signal
RX_CLK	Managed or unmanaged mode
RXD0	Signal A
RXD1	Signal B
RXD2	Signal C
RXD3	Signal D
RX_DV/RX_CTL	Signal E
MII_TXCLK	Select MII or RGMII/RMII MAC interface mode
RXD4	PHY address bit 0 in unmanaged mode
RXD5	PHY address bit 1 in unmanaged mode
RXD6	CLKOUT frequency selection bit 0
RXD7	CLKOUT frequency selection bit 1

3.3.1 CLKOUT Signal Configuration

When the CLKOUT signal is pulled LOW and the state of that signal is latched to logic 0 on the rising edge of reset, the CLKOUT output is disabled and the device will drive a logic low level on that pin after reset de-assertion. When the CLKOUT signal is pulled HIGH externally and the state of that signal is latched to logic 1, the CLKOUT output is enabled. This behavior can also be controlled through register 13G.15.

The CLKOUT signal is frequency-locked to the reference clock signal input through XTAL1/XTAL2 pins. The frequency of CLKOUT can be programed to the following values through register 13G.14:13:

- 25 MHz
- 50 MHz
- 125 MHz

3.3.2 Managed Mode

When RX_CLK pin is pulled LOW and the state of that signal is latched to logic 0 on the rising edge of reset, the device operates in a managed mode. In managed mode, the remaining 5 signals (A–E) are used to set the PHY address, allowing up to 32 devices to reside on the shared MDIO bus. In this mode, the device can be configured using register access and no additional hardware configurability is provided. The following table lists the assigned PHY address values in managed mode.

Table 7 • **Managed Mode**

Signal	PHY Address Values
Signal A	PHY address bit 0
Signal B	PHY address bit 1
Signal C	PHY address bit 2
Signal D	PHY address bit 3
Signal E	PHY address bit 4

3.3.3 Unmanaged Mode

When RX_CLK is pulled HIGH externally and the state of that signal is latched to logic 1 on the rising edge of reset, the device operates in an unmanaged mode. The signals A–E are used to set default chip configurations, as described in the following sections.

Note: Operating the device in unmanaged mode requires that the NRESET pin is asserted twice during device configuration (for more information, see Configuration, page 25).

Note: The default values for the following registers depend on the chosen hardware strapping options.

- 0.13, 0.6—Forced speed selection
- 0.12—Enable autonegotiation
- 0.8—Duplex
- 23.12:11—MAC interface selection
- 19E1.3:2—Force MDI crossover
- 20E2.6:4—RX_CLK delay
- 20E2.2:0—TX_CLK delay

Additionally, the following registers are set to 1 by default in unmanaged mode.

- 28.6—ActiPHY enable

3.3.3.1 Signals A and B

Signals A and B are used to set the RGMII RX_CLK and TX_CLK delay settings (as defined in register 20E2), as per the following table.

Table 8 • **Signals A and B**

Signals A, B	RX_CLK and TX_CLK Delay Setting
0, 0	000 - 0.2 ns
0, 1	010 - 1.1 ns
1, 0	100 - 2.0 ns
1, 1	110 - 2.6 ns

3.3.3.2 Signals C and D

Signals C and D are used to select the link advertisement settings, as defined in the following table.

Table 9 • **Signals C and D**

Signals C, D	Link Advertisement
0, 0/1	Default mode of operation, 10/100 FDX/HDX, autoneg ON
1, 0	100BTX, HDX forced mode, autoneg OFF
1, 1	10BT, HDX forced mode, autoneg OFF

3.3.3.3 Signal E

Signal E is used to select between RMII and RGMII MAC interface modes. When the state of Signal E is latched to logic 0 on the rising edge of reset, the device operates in RGMII mode. When the state of Signal E is latched to logic 1 on the rising edge of reset, the device operates in RMII mode.

Note: RMII only supports 10/100 Mbps speeds. When RMII mode is selected, the link advertisement selection must also be changed to either 01, 10, or 11 settings, as defined in Table 9, page 10.

Note: Correct configuration of the device is an end user responsibility, and no attempt is made in the device to disallow incorrect configurations.

Additionally, in unmanaged mode, the following settings are changed from their default values:

- Enable ActiPHY (register 28.6 set to 1)

3.3.3.4 PHY Address Bit 0/1 Selection in Unmanaged Mode

The RXD4 and RXD5 pins can be pulled LOW or HIGH externally to set the bit 0 and bit 1 of the device PHY address. The upper 3 bits of the PHY address are always set to 0, and the lower 2 bits can be set to one of 4 possible combinations through this external strapping option to provide a total of 4 PHY addresses in unmanaged operation.

3.3.4 MII or RGMII/RMII MAC Interface Mode

When MII_TXCLK pin is pulled LOW externally and the state of that signal is latched to logic 0 on the rising edge of reset, the device operates in a RGMII mode. When MII_TXCLK pin is pulled HIGH externally and the state of that signal is latched to logic 1 on the rising edge of reset, the device operates in MII mode. This signal is bonded out to a package pin.

Note: If unmanaged mode is selected and Signal E is latched as a logic 1 (indicating RMII mode), the device will default to RMII mode regardless of the latched state of the MII_TXCLK.

3.3.5 CLKOUT Frequency Selection

The RXD6 and RXD7 pins can be pulled LOW or HIGH externally to set the bit 0 and bit 1 default values of the CLKOUT frequency selection register 13G.14:13. The following table describes the allowed default CLKOUT frequency settings.

Table 10 • **CLKOUT Frequency Selection**

CLKOUT Frequency Selection	CLKOUT Frequency
00	25 MHz
01	50 MHz
10	125 MHz
11	Reserved

The CLKOUT frequency can be changed from the default setting to any of the other settings on any device variant by modifying the register bits through the SMI interface.

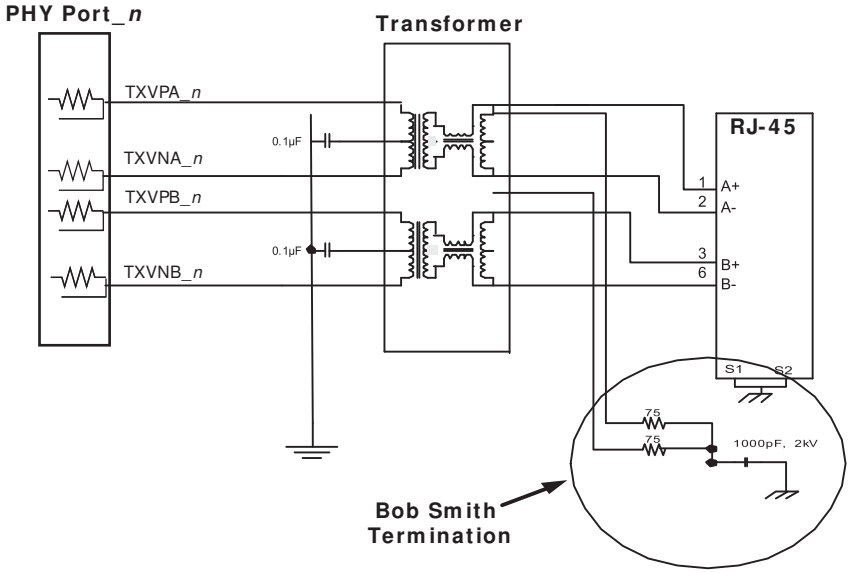
3.4 Cat5 Twisted Pair Media Interface

The twisted pair interface is compliant with IEEE 802.3-2008 and the IEEE 802.3az-2010 standard for Energy-Efficient Ethernet.

3.4.1 Voltage Mode Line Driver

The VSC8540-04 device uses a patented voltage mode line driver that allows it to fully integrate the series termination resistors that are required to connect the PHY's Cat5 interface to an external 1:1 transformer. The interface does not require the user to place an external voltage on the center tap of the magnetic. The following figure illustrates the connections.

Figure 8 • **Cat5 Media Interface**



3.4.2 Cat5 Auto-Negotiation and Parallel Detection

The VSC8540-04 device supports twisted pair auto-negotiation, as defined by IEEE 802.3-2008 Clause 28 and IEEE 802.3az-2010. The auto-negotiation process evaluates the advertised capabilities of the local PHY and its link partner to determine the best possible operating mode. In particular, auto-negotiation can determine speed and duplex configuration. Auto-negotiation also enables a connected MAC to communicate with its link partner MAC through the VSC8540-04 device using optional next pages to set attributes that may not otherwise be defined by the IEEE standard.

If the Category 5 (Cat5) link partner does not support auto-negotiation, the VSC8540-04 device automatically uses parallel detection to select the appropriate link speed.

Auto-negotiation is disabled by clearing register 0, bit 12. When auto-negotiation is disabled, the state of register bits 0.6, 0.13, and 0.8 determine the device operating speed and duplex mode.

3.4.3 Automatic Crossover and Polarity Detection

For trouble-free configuration and management of Ethernet links, the VSC8540-04 device includes a robust automatic crossover detection feature for allspeeds on the twisted pair interface. Known as HP Auto-MDIX, the function is fully compliant with Clause 40 of IEEE 802.3-2008.

Additionally, the device detects and corrects polarity errors on all MDI pairs—a useful capability that exceeds the requirements of the standard.

Both HP Auto-MDIX detection and polarity correction are enabled in the device by default. Default settings can be changed using device register bits 18.5:4. Status bits for each of these functions are located in register 28.

Note: The VSC8540-04 device can be configured to perform HP Auto-MDIX, even when auto-negotiation is disabled and the link is forced into 10/100 speeds. To enable this feature, set register 18.7 to 0. To use the feature, also set register 0.12 to 0.

The HP Auto-MDIX algorithm successfully detects, corrects, and operates with any of the MDI wiring pair combinations listed in the following table, which shows that twisted pair A is connected to the RJ45 connector 1, 2 in normal MDI mode.

Table 11 • **Supported MDI Pair Combinations**

RJ45 Connections		
1, 2	**3, 6**	**Mode**
A	B	Normal MDI
B	A	Normal MDI-X

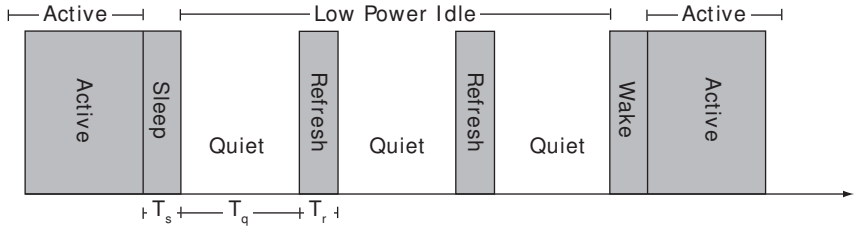
3.4.4 Manual MDI/MDIX Setting

As an alternative to HP Auto-MDIX detection, the PHY can be forced to be MDI or MDI-X using register 19E1, bits 3:2. Setting these bits to 10 forces MDI and setting 11 forces MDI-X. Leaving the bits 00 enables the HP Auto-MDIX setting to be based on register 18, bits 7 and 5.

3.4.5 Energy-Efficient Ethernet

The VSC8540-04 device supports the IEEE 802.3az-2010 Energy-Efficient Ethernet standard to provide a method for reducing power consumption on an Ethernet link during times of low utilization. It uses low power idles (LPI) to achieve this objective.

Figure 9 • **Low Power Idle Operation**



Using LPI, the usage model for the link is to transmit data as fast as possible and then return to a low power idle state. Energy is saved on the link by cycling between active and low power idle states. During LPI, power is reduced by turning off unused circuits and using this method, energy use scales with bandwidth utilization. The VSC8540-04 device uses LPI to optimize power dissipation in 100BASE-TXmode.

In addition, the IEEE 802.3az-2010 standard defines a 10BASE-Te mode that reduces transmit signal amplitude from 5 V peak-to-peak to approximately 3.3 V peak-to-peak. This mode reduces power consumption in 10 Mbps link speed and fully interoperates with legacy 10BASE-T-compliant PHYs over 100 m Cat5 cable or better.

To configure the VSC8540-04 device in 10BASE-Te mode, set register 17E2.15 to 1 for each port. Additional energy-efficient Ethernet features are controlled through Clause 45 registers. For more information, see Clause 45 Registers to Support Energy-Efficient Ethernet and 802.3bf, page 55.

3.5 Reference Clock

The VSC8540-04 device supports multiple reference clock input options to allow maximum system level flexibility. There are two REFCLK_SEL signals available to allow an end user to select between the various options. The following table shows the functionality and associated reference clock frequency.

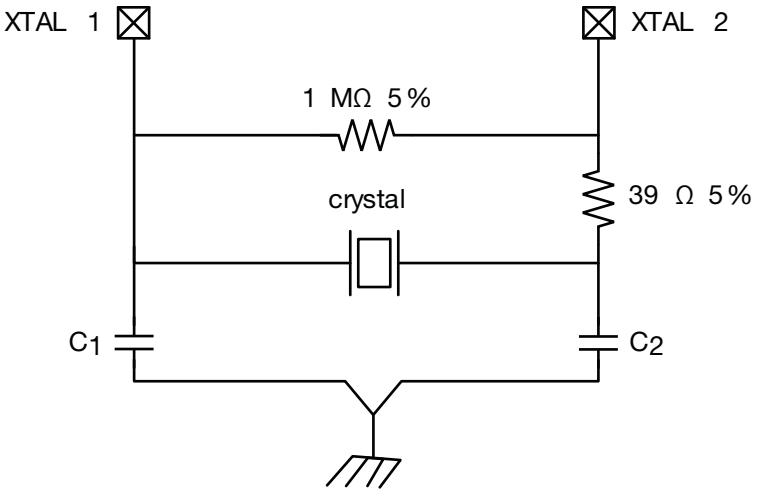
Table 12 • **REFCLK Frequency Selection**

REFCLK_SEL [1:0]	Reference Clock Mode
00	25 MHz, on-chip oscillator ON (XTAL1/2 pins)
01	25 MHz, on-chip oscillator OFF (XTAL1 pin)
10	50 MHz, on-chip oscillator OFF (XTAL1 pin)
11	125 MHz, on-chip oscillator OFF (XTAL1 pin)

The following figure shows a reference tank circuit for a fundamental mode crystal.

Note: For best performance, traces on PCB should be of similar length and Kelvin-connected to ground.

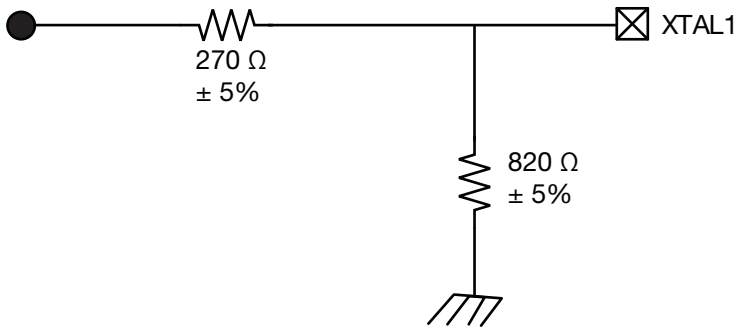
Figure 10 • **XTAL Reference Clock**



with REFCLK_SEL [1:0] = 00

The following figure shows an external 3.3 V reference clock.

Figure 11 • **External 3.3 V Reference Clock**



Note: Reference clock source less than λ/10 from XTAL1, and routing capacitance less than 1 pF.

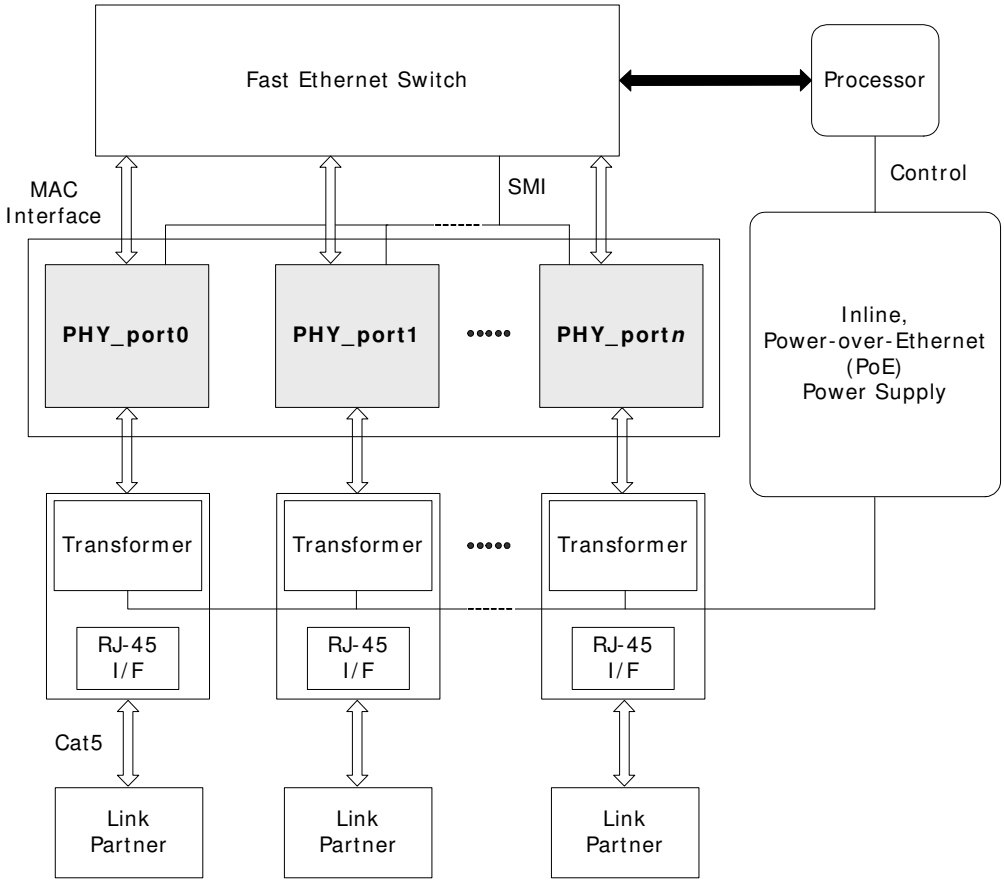
Note: No voltage scaling is required for a 2.5 V external reference.

3.6 Ethernet Inline-Powered Devices

The VSC8540-04 device can detect legacy inline-powered devices in Ethernet network applications. Inline-powered detection capability is useful in systems that enable IP phones and other devices (such as wireless access points) to receive power directly from their Ethernet cable, similar to office digital phones receiving power from a private branch exchange (PBX) office switch over telephone cabling. This type of setup eliminates the need for an external power supply and enables the inline-powered device to remain active during a power outage, assuming that the Ethernet switch is connected to an uninterrupted power supply, battery, back-up power generator, or other uninterruptable power source.

For more information about legacy inline-powered device detection, visit the Cisco website at www.cisco.com. The following illustration shows an example of an inline-powered Ethernet switch application.

Figure 12 • **Inline-Powered Ethernet Switch Diagram**



The following procedure describes the steps that an Ethernet switch must perform to process inline-power requests made by a link partner that is, in turn, capable of receiving inline-power:

1. Enable the inline-powered device detection mode on each VSC8540-04 PHY using its serial management interface. Set register bit 23E1.10 to 1.
2. Ensure that the auto-negotiation enable bit (register 0.12) is also set to 1. In the application, the device sends a special fast link pulse signal to the link partner. Reading register bit 23E1.9:8 returns 00 during the search for devices that require Power-over-Ethernet (PoE).
3. The VSC8540-04 PHY monitors its inputs for the fast link pulse signal looped back by the link partner. A link partner capable of receiving PoE loops back the fast link pulses when the link partner is in a powered down state. This is reported when register bit 23E1.9:8 reads back 01. It can also be verified as an inline-power detection interrupt by reading register bit 26.9, which should be a 1, and which is subsequently cleared and the interrupt de-asserted after the read. When a link partner device does not loop back the fast link pulse after a specific time, register bit 23E1.9:8 automatically resets to 10.
4. If the VSC8540-04 PHY reports that the link partner requires PoE, the Ethernet switch must enable inline-power on this port, independent of the PHY.
5. The PHY automatically disables inline-powered device detection when the register bits 23E1.9:8 automatically reset to 10, and then automatically changes to its normal auto-negotiation process. A link is then autonegotiated and established when the link status bit is set (register bit 1.2 is set to 1).
6. In the event of a link failure (indicated when register bit 1.2 reads 0), it is recommended that the inline-power be disabled to the inline-powered device independent of the PHY. The VSC8540-04 PHY disables its normal auto-negotiation process and re-enables its inline-powered device detection mode.