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VSC8541-01 Datasheet
Single Port Gigabit Ethernet Copper PHY with GMII/RGMII/MII/RMII Interfaces

Microsemi
Power Matters.™

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.0

Revision 4.0 was the first publication of this document.

2 Overview

The VSC8541-01 device is designed for space-constrained 10/100/1000BASE-T applications. It features integrated, line-side termination to conserve board space, lower EMI, and improve system performance. Additionally, integrated RGMII timing compensation eliminates the need for on-board delay lines.

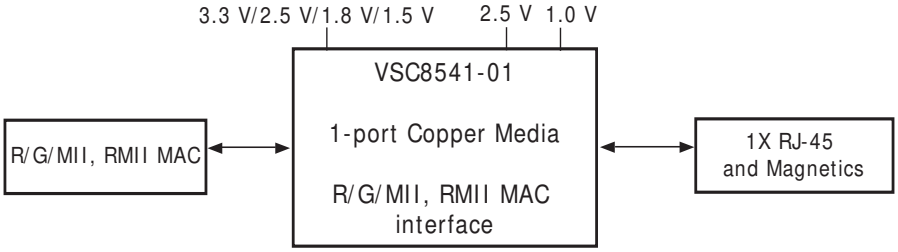
Microsemi's EcoEthernet™ v2.0 technology supports IEEE 802.3az Energy-Efficient Ethernet (EEE) and power-saving features to reduce power based on link state and cable reach. VSC8541-01 optimizes power consumption in all link operating speeds and features a Wake-on-LAN (WoL) power management mechanism for bringing the PHY out of a low-power state using designated magic packets.

Fast link failure (FLF) indication for high availability networks identifies the onset of a link failure in less than 1 ms typical to go beyond the IEEE 802.3 standard requirement of 750 ms ±10 ms (link master). Potential link failure events can be more flexibly monitored using an enhanced FLF2 state machine, which goes beyond FLF indication by enabling signaling of the link potentially going down within 10 µS.

The device includes recovered clock output for Synchronous Ethernet applications. Programmable clock squelch control is included to inhibit undesirable clocks from propagating and to help prevent timing loops. Ring Resiliency allows a PHY port to switch between master and slave timing references with no link drop in 1000BASE-T mode.

The following illustration shows a high-level, general view of a typical VSC8541-01 application.

Figure 1 • **Application Diagram**



2.1 Key Features

This section lists the main features and benefits of the VSC8541-01 device.

2.1.1 Superior PHY and Interface Technology

- Integrated 10/100/1000BASE-T Ethernet copper transceiver (IEEE 802.3ab compliant) with the industry's only non-TDR-based VeriPHY™ cable diagnostics algorithm
- Patented line driver with low EMI voltage mode architecture and integrated line-side termination resistors
- Wake-on-LAN using magic packets
- HP Auto-MDIX and manual MDI/MDIX support
- RGMII/GMII/MII/RMII MAC interface
- Jumbo frame support up to 16 kilobytes with programmable synchronization FIFOs

2.1.2 Synchronous Ethernet and IEEE 1588 Time Stamp Support

- Recovered clock output with programmable clock squelch control for G.8261 Synchronous Ethernet applications
- 1000BASE-T Ring Resiliency feature to switch between master and slave timing without dropping link
- Clock output squelch to inhibit clocks during auto-negotiation and no link status
- Clause 45 registers to support IEEE 802.3bf
- IEEE 1588 Start of Frame (SOF) detection to enhance 1588v2 PTP time stamp accuracy (VSC8541XMV-04 only)

2.1.3 Fast Link Up/Link Drop Modes

- Fast link failure indication (<1 ms typical, programmable down to <10 µS)
- Supports 1000Base-T forced mode for both master and slave end point configurations with constant link self-monitoring and link auto-reset should the link come down

2.1.4 Best-in-Class Power Consumption

- EcoEthernet™ v2.0 green energy efficiency with ActiPHY™, PerfectReach™, and IEEE 802.3az Energy-Efficient Ethernet
- Fully optimized power consumption for all link speeds
- Clause 45 registers to support Energy-Efficient Ethernet

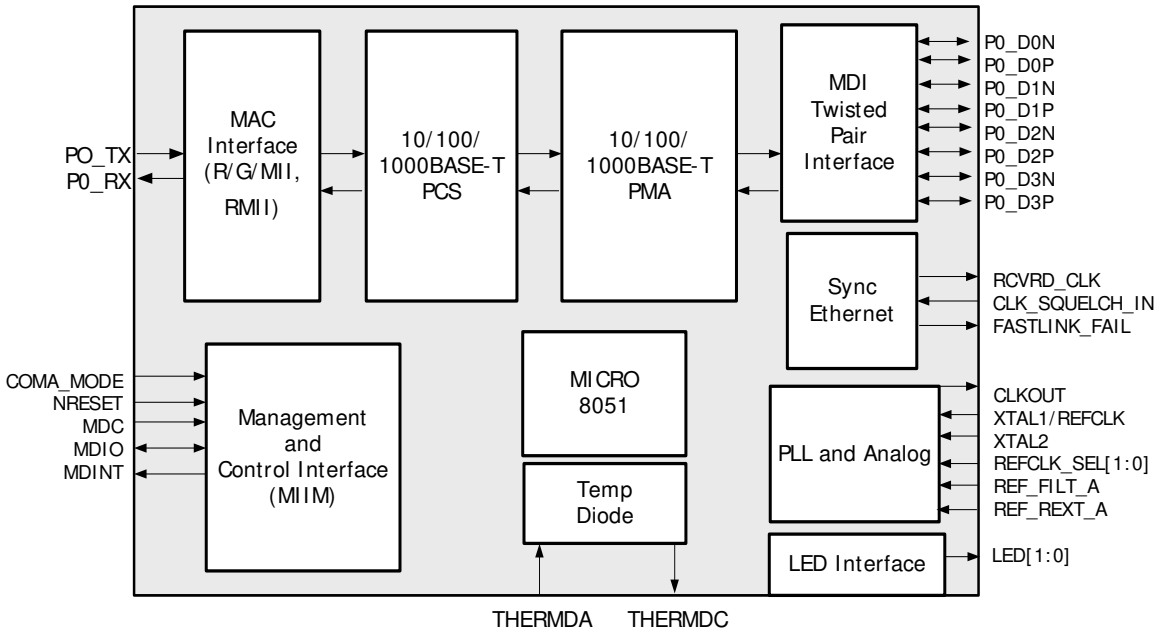
2.1.5 Key Specifications

- Compliant with IEEE 802.3 (10BASE-T, 100BASE-TX, and 1000BASE-T) specifications
- Supports R/G/MII
- Supports 1.5 V, 1.8 V, 2.5 V, and 3.3 V CMOS for RGMII versions 1.3 and 2.0 (without HSTL support), GMII/MII as well as RMII version 1.2
- Supports a variety of clock sources: 25 MHz Xtal, 25 MHz OSC, 50 MHz OSC, 125 MHz OSC
- Supports programmable output frequencies of 25 MHz, 50 MHz, or 125 MHz, regardless of chosen Xtal or OSC frequencies
- Supports a wide array of stand-alone hardware configuration options
- Supports all 5 bits of MDIO/MDC addressing possible for managed mode designs using pull-up/pull-down resistors
- Low alpha mold compound enables 80 SER FIT (VSC8541XMV-04 only)
- Devices support operating temperatures of –40 °C ambient to 125 °C junction or 0 °C ambient to 125 °C junction
- Optionally reports if a link partner is requesting inline Power-over-Ethernet (PoE and PoE+)
- Available in 8 mm x 8 mm, 68-pin QFN package

2.2 Block Diagram

The following illustration shows the primary functional blocks of the VSC8541-01 device.

Figure 2 • **Block Diagram**



3 Functional Descriptions

This section describes the functional aspects of the VSC8541-01 device, including available configurations, operational features, and testing functionality. It also defines the device setup parameters that configure the device for a particular application.

3.1 Operating Modes

The following table lists the operating modes of the VSC8541-01 device.

Table 1 • **Operating Modes**

Operating Mode	Supported Media
RGMII-Cat5	10/100/1000BASE-T
GMII-Cat5	10/100/1000BASE-T
RMII-Cat5	10/100BASE-T

3.2 MAC Interface

The VSC8541-01 device supports RMII version 1.2, RGMII versions 1.3 and 2.0, and GMII/MII MAC interfaces at 1.5 V, 1.8 V, 2.5 V, and 3.3 V operating voltages. In order to help reduce EMI, the VSC8541-01 device also includes edge rate programmability for the MAC interface signals through register 27E2.7:5.

The recommended values for R_S (as shown in Figure 3, page 5, Figure 4, page 5, Figure 6, page 7, and Figure 7, page 7) are listed in the following table.

Table 2 • **Recommended Values for R_S (± 5%)**

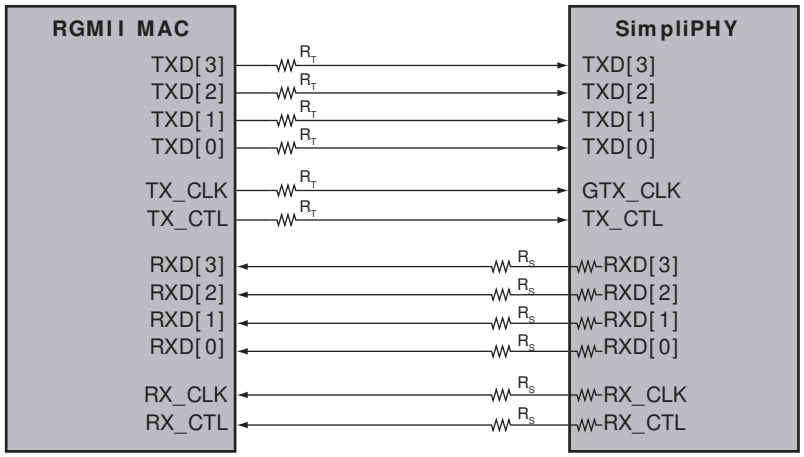
VDDMAC Value	R_S Value
1.5 V	27 Ω
1.8 V	33 Ω
2.5 V	39 Ω
3.3 V	39 Ω

Refer to the MAC datasheet for the value to use for R_T.

3.2.1 RGMII MAC Interface Mode

The VSC8541-01 device supports RGMII versions 1.3 and 2.0 (without HSTL modes). The RGMII interface supports all three speeds (10 Mbps, 100 Mbps, and 1000 Mbps) and is used as an interface to a RGMII-compatible MAC. The device is compliant with the RGMII interface specification when VDDMAC is operating at 2.5 V. While the RGMII specification only specifies operation at 2.5 V, the device can also support the RGMII interface at 1.5 V, 1.8 V, and 3.3 V.

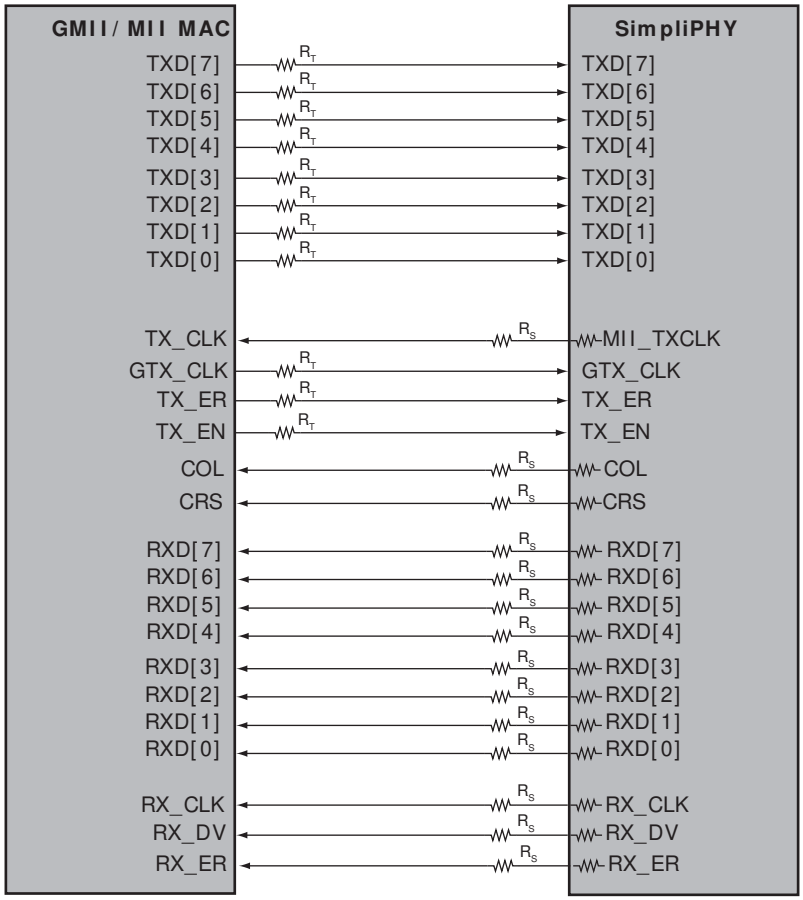
Figure 3 • **RGMII MAC Interface**



3.2.2 GMII/MII Interface Mode

The GMII/MII interface supports all three speeds (10 Mbps, 100 Mbps, and 1000 Mbps), and is used as an interface to a GMII/MII-compatible MAC. The device is compliant with the GMII/MII interface specification when VDDMAC is operating at 3.3 V. While the GMII/MII specification only specifies operation at 3.3 V, the device can also support the GMII/MII interface at 1.5 V, 1.8 V, and 2.5 V.

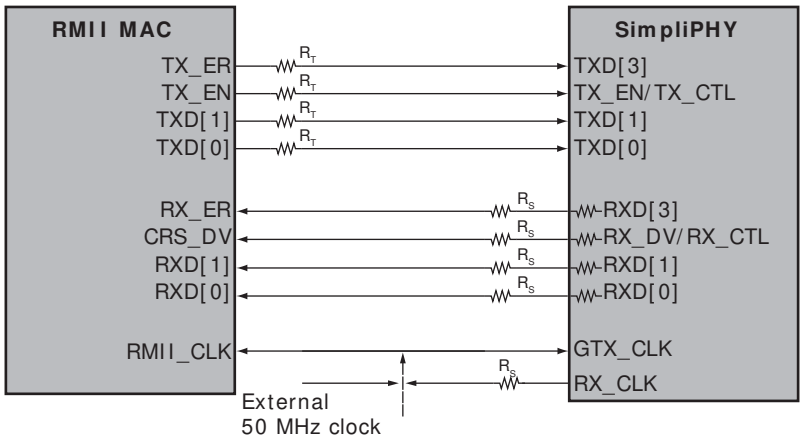
Figure 4 • **GMII/MII MAC Interface**



3.2.3 RMII Mode

The RMII interface supports 10 Mbps and 100 Mbps speeds, and is used as an interface to a RMII-compatible MAC. The device is compliant with the RMII interface specification when VDDMAC is operating at 3.3 V. While the RMII specification only specifies operation at 3.3 V, the device can also support the RMII interface at 1.5 V, 1.8 V, and 2.5 V.

Figure 5 • **RMII MAC Interface**



3.2.3.1 RMII Pin Allocation

The following table lists the chip pins used for RMII signaling in RMII mode.

Table 3 • **RMII Pin Allocation**

Chip Pin	RMII Signal
GTX_CLK	RMII_CLKIN
RX_CLK	RMII_CLKOUT
TXD3	TX_ER (to support 802.3az)
TXD1	TXD1
TXD0	TXD0
TX_EN/TX_CTL	TX_EN
RXD1	RXD1
RXD0	RXD0
RXD3	RX_ER
RX_DV/RX_CTL	CRS_DV

Even though the RMII specification does not call for the use of TX_ER signal, it is required in order to support Energy-Efficient Ethernet (802.3az).

3.2.3.2 RMII Clocking Overview

When the device is in RMII mode, the clock inputs to the device need to support the various modes in which RMII devices can operate. There are two basic modes of operation in RMII mode:

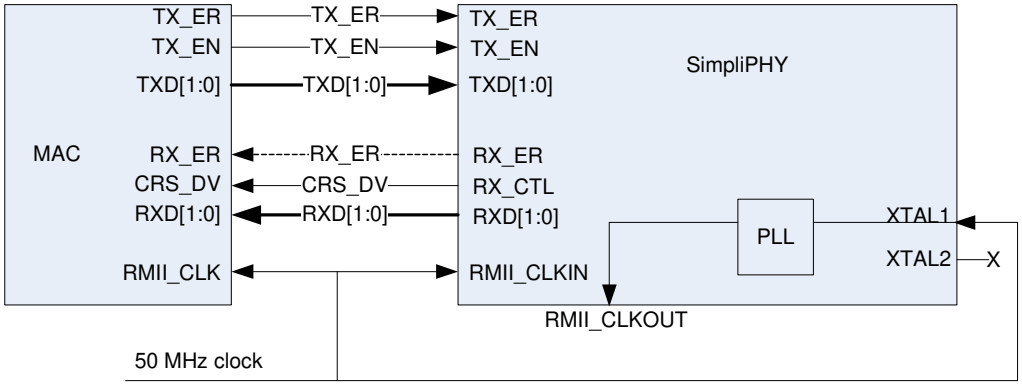
- Mode 1—system provides a 50 MHz clock that is used to clock the RMII interface and must be used as the chip reference clock.
- Mode 2—PHY operates from a 25 MHz or 125 MHz reference clock, and sources the 50 MHz clock used for the RMII interface.

These two modes of operation and the clocking schemes are described in the following sections.

3.2.3.2.1 Mode 1

In this mode of operation, an external source is used to provide a 50 MHz clock through the RMII_CLKIN and the XTAL1 pin. This 50 MHz clock is used as the main clock for the RMII interface, and must be used as the reference clock for the PHY connected to the XTAL1 pin. In this mode, the RMII_CLKOUT signal from the PHY is not used. The RMII_CLKOUT is enabled by default and that clock output should be disabled through register 27E2.4. The following figure illustrates RMII signal connections at the system level.

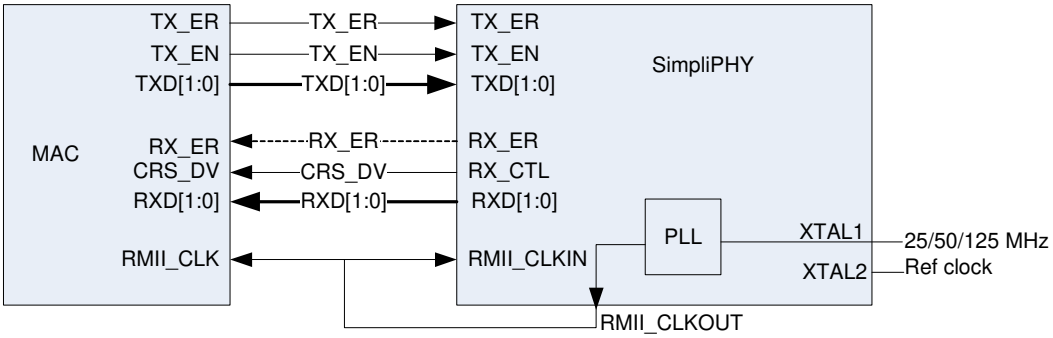
Figure 6 • **Mode 1**



3.2.3.2.2 Mode 2

In this mode of operation, the PHY operates from a 25 MHz crystal (XTAL1 and XTAL2) or 25 MHz/125 MHz single-ended external clock (XTAL1), and sources the 50 MHz clock required for the RMII interface. This 50 MHz clock is output from the PHY on the RMII_CLKOUT pin and then connected to the MAC and PHY RMII_CLKIN signals. In this mode, the PHY generates a 50 MHz clock for the system and that clock output is enabled. The following figure illustrates RMII signal connections at the system level.

Figure 7 • **Mode 2**



3.2.4 MAC Interface Edge Rate Control

The VSC8541-01 device includes programmable control of the rise/fall times for the MAC interface signals. The default setting will select the fastest rise/fall times. However, the fast edge rate will result in higher power consumption on the MAC interface and may result in higher EMI.

It is recommended that the user select the appropriate edge rate setting based on the VDDMAC supply voltage, as shown in the following table.

Table 4 • **Recommended Edge Rate Settings**

VDDMAC Voltage	Edge Rate Setting
3.3 V	100

Table 4 • **Recommended Edge Rate Settings *(continued)***

VDDMAC Voltage	Edge Rate Setting
2.5 V	100
1.8 V	111
1.5 V	111

In order to further reduce power consumption and EMI, the user may elect to choose a slower edge rate than recommended if the end application supports it.

The MAC interface signal rise/fall times can be changed by writing to register bits 27E2.7:5. The typical change in edge rate for each setting at various VDDMAC voltages is shown in the following table.

Table 5 • **MAC Interface Edge Rate Control**

	Edge Rate Change (VDDMAC)			
Register Setting	**3.3 V**	**2.5 V**	**1.8 V**	**1.5 V**
111 (fastest)	Default	Default	Default (recommended)	Default (recommended)
110	–2%	–3%	–5%	–6%
101	–4%	–6%	–9%	–14%
100	–7% (recommended)	–10% (recommended)	–16%	–21%
011	–10%	–14%	–23%	–29%
010	–17%	–23%	–35%	–42%
001	–29%	–37%	–52%	–58%
000 (slowest)	–53%	–63%	–76%	–77%

These values are based on measurements performed on typical silicon at nominal supply and room temperature settings.

3.3 Hardware Mode Strapping and PHY Addressing

The VSC8541-01 device provides hardware-configured modes of operation that are achieved by sampling output pins on the rising edge of reset and externally pulling the pin to a logic HIGH or LOW (based on the desired configuration). These output pins are required by the device as inputs while NRESET is asserted and the logic state of the pin is latched in the device upon de-assertion of NRESET. To ensure correct operation of the hardware strapping function, any other device connected to these pins must not actively drive a signal onto them.

The following table describes the pins used for this purpose and their respective modes.

Table 6 • **Hardware Mode Strapping and PHY Addressing**

Pin(s)	Operation Mode
CLKOUT	Enable/disable CLKOUT signal
RX_CLK	Managed or unmanaged mode
RXD0	Signal A
RXD1	Signal B
RXD2	Signal C
RXD3	Signal D

Table 6 • **Hardware Mode Strapping and PHY Addressing *(continued)***

Pin(s)	Operation Mode
RX_DV/RX_CTL	Signal E
MII_TXCLK	Select GMII/MII or RGMII/RMII MAC interface mode
RXD4	PHY address bit 0 in unmanaged mode
RXD5	PHY address bit 1 in unmanaged mode
RXD6	CLKOUT frequency selection bit 0
RXD7	CLKOUT frequency selection bit 1
RX_ER	Enable Forced 1000BT mode
COL	Force MASTER/SLAVE when Forced 1000BT mode is selected
CRS	Force MDI/MDIX when Forced 1000BT mode is selected

3.3.1 CLKOUT Signal Configuration

When the CLKOUT signal is pulled LOW and the state of that signal is latched to logic 0 on the rising edge of reset, the CLKOUT output is disabled and the device will drive a logic low level on that pin after reset de-assertion. When the CLKOUT signal is pulled HIGH externally and the state of that signal is latched to logic 1, the CLKOUT output is enabled. This behavior can also be controlled through register 13G.15.

The CLKOUT signal is frequency-locked to the reference clock signal input through XTAL1/XTAL2 pins. The frequency of CLKOUT can be programed to the following values through register 13G.14:13:

- 25 MHz
- 50 MHz
- 125 MHz

3.3.2 Managed Mode

When RX_CLK pin is pulled LOW and the state of that signal is latched to logic 0 on the rising edge of reset, the device operates in a managed mode. In managed mode, the remaining 5 signals (A–E) are used to set the PHY address, allowing up to 32 devices to reside on the shared MDIO bus. In this mode, the device can be configured using register access and no additional hardware configurability is provided. The following table lists the assigned PHY address values in managed mode.

Table 7 • **Managed Mode**

Signal	PHY Address Values
Signal A	PHY address bit 0
Signal B	PHY address bit 1
Signal C	PHY address bit 2
Signal D	PHY address bit 3
Signal E	PHY address bit 4

3.3.3 Unmanaged Mode

When RX_CLK is pulled HIGH externally and the state of that signal is latched to logic 1 on the rising edge of reset, the device operates in an unmanaged mode. The signals A–E are used to set default chip configurations, as described in the following sections.

Note: Operating the device in unmanaged mode requires that the NRESET pin is asserted twice during device configuration (for more information, see Configuration, page 27).

Note: The default values for the following registers depend on the chosen hardware strapping options.

- 0.13, 0.6—Forced speed selection
- 0.12—Enable autonegotiation
- 0.8—Duplex
- 0.9:8—1000BASE-T capability
- 23.12:11—MAC interface selection
- 19E1.3:2—Force MDI crossover
- 20E2.6:4—RX_CLK delay
- 20E2.2:0—TX_CLK delay

Additionally, the following registers are set to 1 by default in unmanaged mode.

- 28.6—ActiPHY enable
- 20E1.4—Link speed autodownshift enable

3.3.3.1 Signals A and B

Signals A and B are used to set the RGMII RX_CLK and TX_CLK (GTX_CLK) delay settings (as defined in register 20E2), as per the following table.

Table 8 • **Signals A and B**

Signals A, B	RX_CLK and TX_CLK Delay Setting
0, 0	000 - 0.2 ns
0, 1	010 - 1.1 ns
1, 0	100 - 2.0 ns
1, 1	110 - 2.6 ns

3.3.3.2 Signals C and D

Signals C and D are used to select the link advertisement settings, as defined in the following table.

Table 9 • **Signals C and D**

Signals C, D	Link Advertisement
0, 0	Default mode of operation, 10/100/1000 FDX/HDX, autoneg ON
0, 1	10/100 FDX/HDX, autoneg ON (disable 1000BT advertisements)
1, 0	100BTX, HDX forced mode, autoneg OFF
1, 1	10BT, HDX forced mode, autoneg OFF

3.3.3.3 Signal E

Signal E is used to select between RMII and RGMII MAC interface modes. When the state of Signal E is latched to logic 0 on the rising edge of reset, the device operates in RGMII mode. When the state of Signal E is latched to logic 1 on the rising edge of reset, the device operates in RMII mode.

Note: RMII only supports 10/100 Mbps speeds. When RMII mode is selected, the link advertisement selection must also be changed to either 01, 10, or 11 settings, as defined in Table 9, page 10.

Note: Correct configuration of the device is an end user responsibility, and no attempt is made in the device to disallow incorrect configurations.

Additionally, in unmanaged mode, the following settings are changed from their default values:

- Enable link speed downshift (register 20E1.4 set to 1)
- Enable ActiPHY (register 28.6 set to 1)

3.3.3.4 PHY Address Bit 0/1 Selection in Unmanaged Mode

The RXD4 and RXD5 pins can be pulled LOW or HIGH externally to set the bit 0 and bit 1 of the device PHY address. The upper 3 bits of the PHY address are always set to 0, and the lower 2 bits can be set to

one of 4 possible combinations through this external strapping option to provide a total of 4 PHY addresses in unmanaged operation.

3.3.4 GMII/MII or RGMII/RMII MAC Interface Mode

When MII_TXCLK pin is pulled LOW externally and the state of that signal is latched to logic 0 on the rising edge of reset, the device operates in a RGMII mode. When MII_TXCLK pin is pulled HIGH externally and the state of that signal is latched to logic 1 on the rising edge of reset, the device operates in GMII/MII mode (depending on link speed). This signal is bonded out to a package pin.

Note: If unmanaged mode is selected and Signal E is latched as a logic 1 (indicating RMII mode), the device will default to RMII mode regardless of the latched state of the MII_TXCLK.

3.3.5 CLKOUT Frequency Selection

The RXD6 and RXD7 pins can be pulled LOW or HIGH externally to set the bit 0 and bit 1 default values of the CLKOUT frequency selection register 13G.14:13. The following table describes the allowed default CLKOUT frequency settings.

Table 10 • **CLKOUT Frequency Selection**

CLKOUT Frequency Selection	CLKOUT Frequency
00	25 MHz
01	50 MHz
10	125 MHz
11	Reserved

The CLKOUT frequency can be changed from the default setting to any of the other settings on any device variant by modifying the register bits through the SMI interface.

3.3.6 Forced 1000BASE-T Mode

When RX_ER pin is pulled high externally and the state of that signal is latched to logic 1 on the rising edge of reset, the device operates in a Forced 1000BT mode. When this mode is enabled, the state of pins COL and CRS are latched on the rising edge of reset to configure Master/Slave and MDI/MDI-X, respectively. The latched state of the COL pin configures the device in Master mode when it is logic 1, and in Slave mode when it is logic 0. The latched state of the CRS pin configures the device in MDI mode when it is logic 0 and in MDI-X mode when it is logic 1.

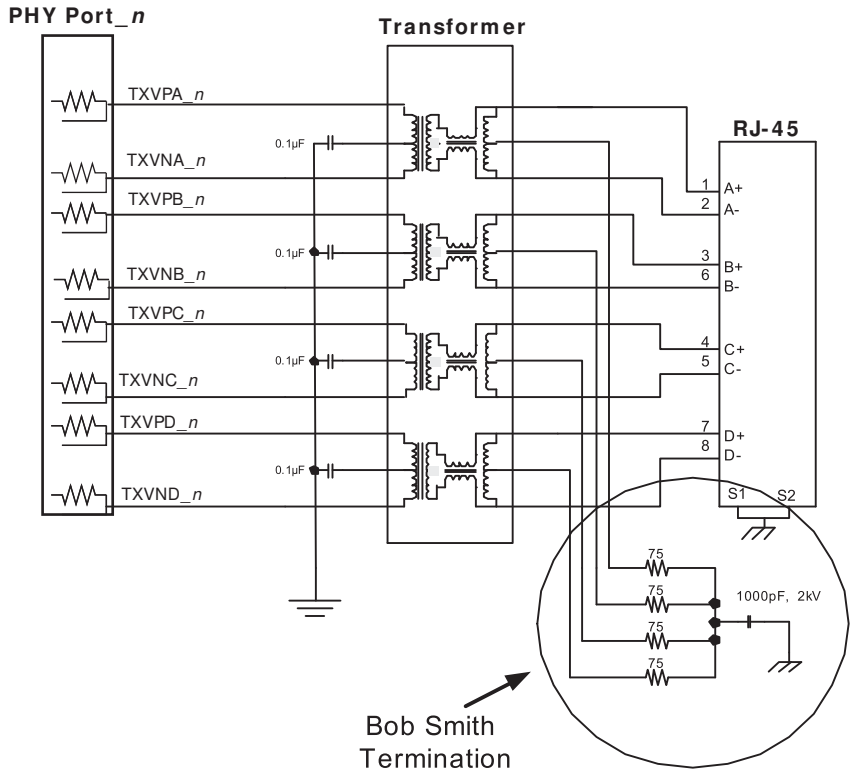
3.4 Cat5 Twisted Pair Media Interface

The twisted pair interface is compliant with IEEE 802.3-2008 and the IEEE 802.3az-2010 standard for Energy-Efficient Ethernet.

3.4.1 Voltage Mode Line Driver

The VSC8541-01 device uses a patented voltage mode line driver that allows it to fully integrate the series termination resistors that are required to connect the PHY's Cat5 interface to an external 1:1 transformer. The interface does not require the user to place an external voltage on the center tap of the magnetic. The following figure illustrates the connections.

Figure 8 • **Cat5 Media Interface**



3.4.2 Cat5 Auto-Negotiation and Parallel Detection

The VSC8541-01 device supports twisted pair auto-negotiation, as defined by IEEE 802.3-2008 Clause 28 and IEEE 802.3az-2010. The auto-negotiation process evaluates the advertised capabilities of the local PHY and its link partner to determine the best possible operating mode. In particular, auto-negotiation can determine speed, duplex configuration, and master or slave operating modes for 1000BASE-TX. Auto-negotiation also enables a connected MAC to communicate with its link partner MAC through the VSC8541-01 device using optional next pages to set attributes that may not otherwise be defined by the IEEE standard.

If the Category 5 (Cat5) link partner does not support auto-negotiation, the VSC8541-01 device automatically uses parallel detection to select the appropriate link speed.

Auto-negotiation is disabled by clearing register 0, bit 12. When auto-negotiation is disabled, the state of register bits 0.6, 0.13, and 0.8 determine the device operating speed and duplex mode.

Note: While 10BASE-T and 100BASE-TX do not require auto-negotiation, IEEE 802.3-2008 Clause 40 has defined 1000BASE-T to require auto-negotiation.

3.4.3 Automatic Crossover and Polarity Detection

For trouble-free configuration and management of Ethernet links, the VSC8541-01 device includes a robust automatic crossover detection feature for all three speeds on the twisted pair interface (10BASE-T, 100BASE-T, and 1000BASE-T). Known as HP Auto-MDIX, the function is fully compliant with Clause 40 of IEEE 802.3-2008.

Additionally, the device detects and corrects polarity errors on all MDI pairs—a useful capability that exceeds the requirements of the standard.

Both HP Auto-MDIX detection and polarity correction are enabled in the device by default. Default settings can be changed using device register bits 18.5:4. Status bits for each of these functions are located in register 28.

Note: The VSC8541-01 device can be configured to perform HP Auto-MDIX, even when auto-negotiation is disabled and the link is forced into 10/100 speeds. To enable this feature, set register 18.7 to 0. To use the feature, also set register 0.12 to 0.

The HP Auto-MDIX algorithm successfully detects, corrects, and operates with any of the MDI wiring pair combinations listed in the following table, which shows that twisted pair A (of four twisted pairs A, B, C, and D) is connected to the RJ45 connector 1, 2 in normal MDI mode.

Table 11 • **Supported MDI Pair Combinations**

RJ45 Connections				
1, 2	**3, 6**	**4, 5**	**7, 8**	**Mode**
A	B	C	D	Normal MDI
B	A	D	C	Normal MDI-X
A	B	D	C	Normal MDI with pair swap on C and D pair
B	A	C	D	Normal MDI-X with pair swap on C and D pair

3.4.4 Manual MDI/MDIX Setting

As an alternative to HP Auto-MDIX detection, the PHY can be forced to be MDI or MDI-X using register 19E1, bits 3:2. Setting these bits to 10 forces MDI and setting 11 forces MDI-X. Leaving the bits 00 enables the HP Auto-MDIX setting to be based on register 18, bits 7 and 5.

3.4.5 Link Speed Downshift

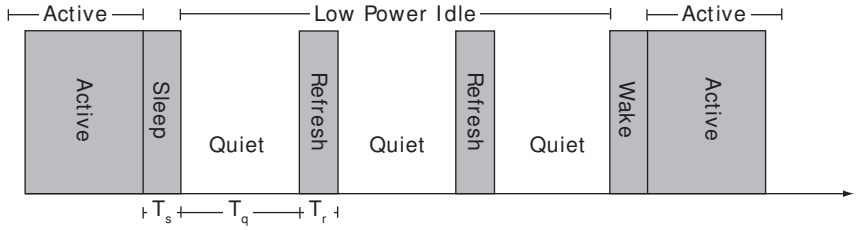
For operation in cabling environments that are incompatible with 1000BASE-T, the VSC8541-01 device provides an automatic link speed downshift option. When enabled, the device automatically changes its 1000BASE-T auto-negotiation advertisement to the next slower speed after a set number of failed attempts at 1000BASE-T. No reset is required to get out of this state when a subsequent link partner with 1000BASE-T support is connected. This feature is useful in setting up in networks using older cable installations that include only pairs A and B, and not pairs C and D.

To configure and monitor link speed downshifting, set register 20E1, bits 4:1.

3.4.6 Energy-Efficient Ethernet

The VSC8541-01 device supports the IEEE 802.3az-2010 Energy-Efficient Ethernet standard to provide a method for reducing power consumption on an Ethernet link during times of low utilization. It uses low power idles (LPI) to achieve this objective.

Figure 9 • **Low Power Idle Operation**



Using LPI, the usage model for the link is to transmit data as fast as possible and then return to a low power idle state. Energy is saved on the link by cycling between active and low power idle states. During LPI, power is reduced by turning off unused circuits and using this method, energy use scales with bandwidth utilization. The VSC8541-01 device uses LPI to optimize power dissipation in 100BASE-TX and 1000BASE-T modes of operation.

In addition, the IEEE 802.3az-2010 standard defines a 10BASE-Te mode that reduces transmit signal amplitude from 5 V peak-to-peak to approximately 3.3 V peak-to-peak. This mode reduces power consumption in 10 Mbps link speed and fully interoperates with legacy 10BASE-T-compliant PHYs over 100 m Cat5 cable or better.

To configure the VSC8541-01 device in 10BASE-Te mode, set register 17E2.15 to 1 for each port. Additional energy-efficient Ethernet features are controlled through Clause 45 registers. For more information, see Clause 45 Registers to Support Energy-Efficient Ethernet and 802.3bf, page 62.

3.4.7 Ring Resiliency

Ring resiliency changes the timing reference between the master and slave PHYs without altering the master/slave configuration in 1000BASE-T mode. The master PHY transmitter sends data based on the local clock and initiates timing recovery in the receiver. The slave PHY instructs nodes to switch the local timing reference to the recovered clock from other PHYs in the box, freezes timing recovery, and locks clock frequency for the transmitter. The master PHY makes a smooth transition to transmission from local clock to recovered clock after timing lock is achieved.

Ring resiliency can be used in synchronous Ethernet systems because the local clocks in each node are synchronized to a grandmaster clock.

Note: For ring resiliency to successfully exchange master/slave timing over 1000BASE-T, the link partner must also support ring resiliency.

3.5 Reference Clock

The VSC8541-01 device supports multiple reference clock input options to allow maximum system level flexibility. There are two REFCLK_SEL signals available to allow an end user to select between the various options. The following table shows the functionality and associated reference clock frequency.

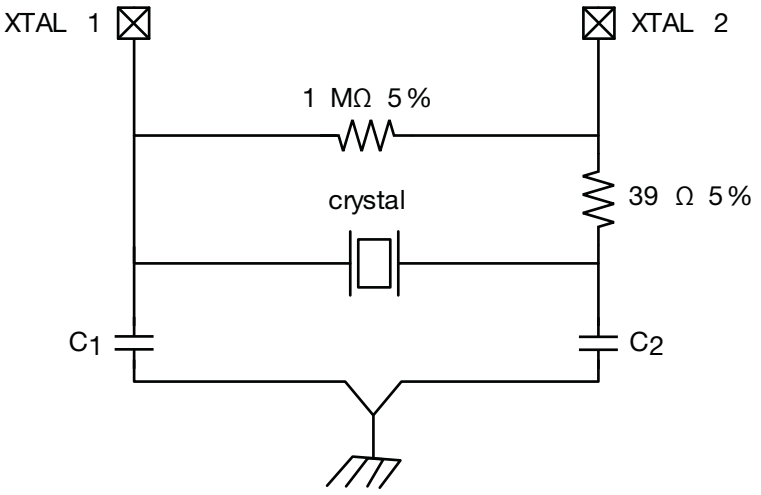
Table 12 • **REFCLK Frequency Selection**

REFCLK_SEL [1:0]	Reference Clock Mode
00	25 MHz, on-chip oscillator ON (XTAL1/2 pins)
01	25 MHz, on-chip oscillator OFF (XTAL1 pin)
10	50 MHz, on-chip oscillator OFF (XTAL1 pin)
11	125 MHz, on-chip oscillator OFF (XTAL1 pin)

The following figure shows a reference tank circuit for a fundamental mode crystal.

Note: For best performance, traces on PCB should be of similar length and Kelvin-connected to ground.

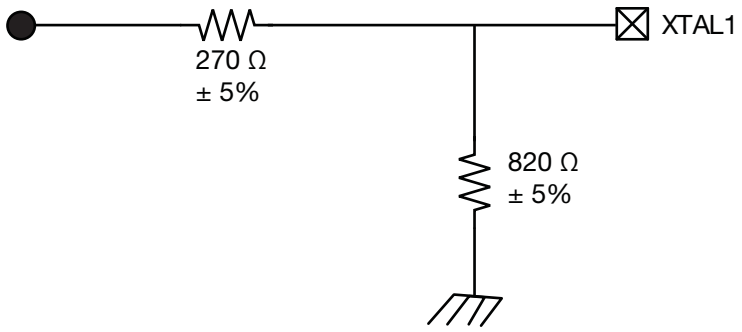
Figure 10 • **XTAL Reference Clock**



with REFCLK_SEL [1:0] = 00

The following figure shows an external 3.3 V reference clock.

Figure 11 • **External 3.3 V Reference Clock**



Note: Reference clock source less than λ/10 from XTAL1, and routing capacitance less than 1 pF.

Note: No voltage scaling is required for a 2.5 V external reference.

3.6 Ethernet Inline-Powered Devices

The VSC8541-01 device can detect legacy inline-powered devices in Ethernet network applications. Inline-powered detection capability is useful in systems that enable IP phones and other devices (such as wireless access points) to receive power directly from their Ethernet cable, similar to office digital phones receiving power from a private branch exchange (PBX) office switch over telephone cabling. This type of setup eliminates the need for an external power supply and enables the inline-powered device to remain active during a power outage, assuming that the Ethernet switch is connected to an uninterrupted power supply, battery, back-up power generator, or other uninterruptable power source.

For more information about legacy inline-powered device detection, visit the Cisco website at www.cisco.com. The following illustration shows an example of an inline-powered Ethernet switch application.