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NVMe PCIe SSD M.2 Manual

NVMe PCIe SSD is a non-volatile, solid-state storage device delivering uncompromising performance, reliability and ruggedness for environmentally challenging applications.

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Revision History

Date	Revision	Description	Checked By
3/16/17	A	Initial Release based on PSFNP7xxxxWxxx and update PN table. Add VSFNP7480GWCHVSM	

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Ordering Information: M.2 110mm PCIe SSD Solid-State Drive

Part Number	Interface	Application	User Capacity (GB)	NAND	Temperature (C)	NAND
VSFNP7960GWCFWSM	PCIe/NVMe	Enterprise PM963	960	TLC	(0 to +70'c)	Samsung VNAND
VSFNP71T92WCGWSM	PCIe/NVMe	Enterprise PM963	1920	TLC	(0 to +70'c)	Samsung VNAND

Notes:

1. Usable capacity based on a level of over-provisioning applied to wear leveling, bad sectors, index tables etc.
2. SSD's ship unformatted from the factory unless otherwise requested.
3. 1 GB = 1,000,000,000 Byte
4. One Sector = 512 Byte.

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1 Introduction

This document describes the specification of Viking SSD which uses PCIe interface. The Viking SSD is fully consist of semiconductor device and using NAND Flash Memory which has a high reliability and a high technology in a small form factor for using a SSD and supporting Peripheral Component Interconnect Express (PCIe) 3.0 interface standard up to 4 lanes shows much faster performance than previous SATA SSDs It could also provide rugged features with an extreme environment with a high MTBF.

1.1 Features

The SSD delivers the following features:

- Native-PCIe SSD for enterprise application
- PCI Express Gen3: Single port X4 lanes
- Compliant with PCI Express Base Specification Rev. 3.0
- Compliant with NVM Express Specification Rev.1.2
- Static and Dynamic Wear Leveling and Bad Block Management
- RoHS / Halogen-Free Compliant
- Support up to queue depth 64K
- Support Power Management: ASPM/PCI-PM L0s, L1, L1.1 and L1.2
- Support SMART and TRIM commands
- Support 48-bit addressing mode
- Firmware update

1.2 PCIE Interface

- PCI Express Gen3: Single port X4 lanes, 8Gb/s
- Compliant with PCI Express Base Specification Rev. 3.0
- Compliant with NVM Express Specification Rev.1.2

For a list of supported commands and other specifics, please see Chapter 5.

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2 Product Specifications

2.1 Capacity and LBA count

Raw Capacity (GB)	User Capacity (GB)	LBA Count
1024	960	1,875,385,008
2000	1920	3,750,748,848

Notes:

- Per www.idema.org, LBA1-03 spec,
LBA counts = (97,696,368) + (1,953,504 * (Advertised Capacity in GBytes – 50))
- GB capacities based on power of 10, GiB capacities are based on powers of 2

2.2 Performance

Access Type	960GB	1920GB
Sequential Read, 128K, MB/s	Up to 1900	Up to 2000
Sequential Write, 128K, MB/s	Up to 980	Up to 1200

Notes:

- Based on PCI Express Gen3 x4, Random performance measured using FIO 2.1.3 in Linux RHEL 6.5(Kernel 2.6.32) with queue depth 32 by 4 workers and Sequential performance with queue depth 32 by 1 worker. Actual performance may vary depending on use conditions and environment.

Table 2-1: Maximum Random Read / Write Input/Output Operations per Second (IOPS)

Access Type	960GB	1920GB
Read, 4K, IOPS	Up to 380K	Up to 450K
Write, 4K, IOPS	Up to 31K	Up to 40K

Notes:

1. Based on PCI Express Gen3 x4, Random performance measured using FIO 2.1.3 in Linux RHEL 6.5(Kernel 2.6.32) with queue depth 32 by 4 workers and Sequential performance with queue depth 32 by 1 worker. Actual performance may vary depending on use conditions and environment.

2.3 Timing / Latency

Table 2-2: Timing Specifications

Type	960GB	1920GB
Random Read/Write Latency	85/50 us	85/50 us
Sequential Read/Write Latency	15/15 us	15/15 us
Power On Ready (POR), Drive Ready Time	10 sec	10 sec

Notes:

1. The random latency is measured by using FIO 2.1.3 in Linux RHEL 6.5(Kernel 2.6.32) and 4KB transfer size with queue depth 1 by 1 worker
2. The sequential latency is measured by using FIO 2.1.3 in Linux RHEL 6.5(Kernel 2.6.32) and 4KB transfer size with queue depth 1 by 1 worker

2.4 Quality of Service (QoS)

Quality of Service (99%)	Unit	QD=1	QD=32
Read(4KB)	ms	0.1	0.4
Write(4KB)	ms	0.06	1.8

Quality of Service (99.99%)	Unit	QD=1	QD=32
Read(4KB)	ms	0.2	0.8
Write(4KB)	ms	0.08	2

Notes:

1. QoS is measured using Fio 2.1.3 (99 and 99.99%) in Linux RHEL 6.5 (Kernel 2.6.32) with queue depth 1, 32 on 4KB random read and write.
2. QoS is measured as the maximum round-trip time taken for 99 and 99.99% of commands to host

2.5 Electrical Characteristics

2.5.1 Absolute Maximum Ratings

Values shown are stress ratings only. Functional operation outside normal operating values is not implied. Extended exposure to absolute maximum ratings may affect reliability.

Table 2-3: Absolute Maximum Ratings

Description	Min	Max	Unit
Maximum Voltage Range for Vin	-0.2	3.6	V
Maximum Temperature Range	-40	85	c

2.5.2 Supply Voltage

The operating voltage is 3.3V

Table 2-4: Operating Voltage

Description	Min	Max	Unit
Operating Voltage for 3.3 V (+/- 5%)	3.135	3.465	V

2.5.3 Power Consumption

Table 2-5: Power Consumption

Description	960 GB	1920 GB	Unit
Active	8	8	W
Idle	2.5	2.5	W

2.6 Environmental Conditions

2.6.1 Temperature and Altitude

Table 2-6: Temperature and Altitude Related Specifications

Conditions	Operating	Shipping	Storage
Commercial Temperature- Case ¹	0 to 70°C	-40 to 85°C	-40 to 85°C
Humidity (non-condensing)	90% under 40C	93% under 40C	93% under 40C

Notes:

1. Tc is measured at the surface of NAND Flash package

2.6.2 Shock and Vibration

SSD products are tested in accordance with environmental specification for shock and vibration

Table 2-7: Shock and Vibration Specifications

Stimulus	Description
Shock(non-operating)	1500G (0.5ms duration x,y,z with 1/2 sine wave)
Vibration (non-operating)	(60min /axis on 3 axes) Displacement: 1.52mm (20 ~ 80 Hz) Acceleration: 20G (80 ~ 2,000 Hz)

2.6.3 Electromagnetic Immunity

M.2 is an embedded product for host systems and is designed not to impair with system functionality or hinder system EMI/FCC compliance.

2.7 Reliability

Table 2-8: Reliability Specifications

Parameter	Description	
ECC	Correct up to 120 bits error in 2K Byte data	
UBER	1 sector per 10^{17} bits read	
MTBF	2,000,000 hours	
Write Endurance	Capacity	TBW
	960GB	1366 (1.3 DWPD)
	1920GB	2733 (1.3 DWPD)
Data retention	> 90 days at NAND expiration	

Notes:

1. The reliability specification follows JEDEC standards JESD218A and JESD219A
2. Average Minimum Program/Erase cycles (TLC, tbd)
3. $TBW = (GB \text{ capacity} \times DWPD \times 365 \times \text{years}) / 1000$

2.8 Data Security

2.8.1 Power Loss Protection

By using internal back-up power technology, the Viking SSD supports power loss protection feature to guarantee the reliability of data requested by the host system. When power is unpredictably lost, the SSD can detect automatically this abnormal situation and transfer all user data and meta-data cached in DRAM into the Flash media during any SSD operations.

2.8.2 Sudden Power Off and Recovery

If power interruption is detected, the SSD dumps all cached user data and meta data to NAND Flash. The SSD could protect even the user data in DRAM from sudden power off while SSD is used with cache on. Commonly, data is protected all of the operation period.

2.8.2.1 Time to Ready Sequence

In normal power-off recovery status, the SSD needs less than 11 seconds to reach operating mode where SSD works perfectly with cache-on state. SSD is ready to respond identify Device command during FTL OPEN. When the sudden power-off occurs, the user data in DRAM will be dumped into the NAND Flash using the stored power in the capacitor. In sudden power-off recovery condition, mapping data will be loaded or the FTL meta data be rebuilt perfectly for initial max. 30 seconds in case of 960GB. During this period, Identify Device command is still supported. This is called Sudden Power Off and Recovery.

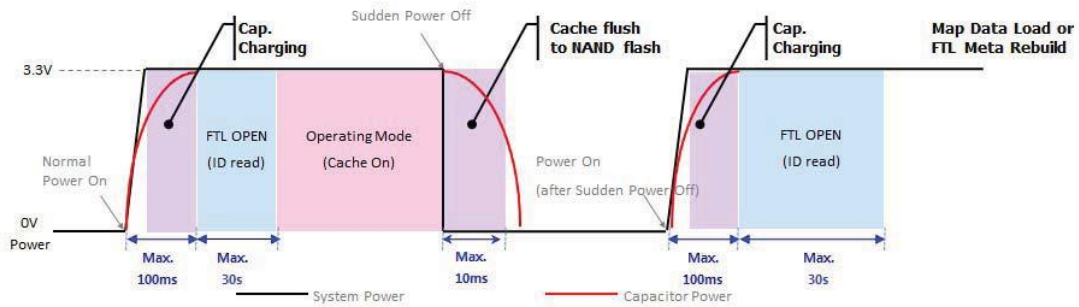


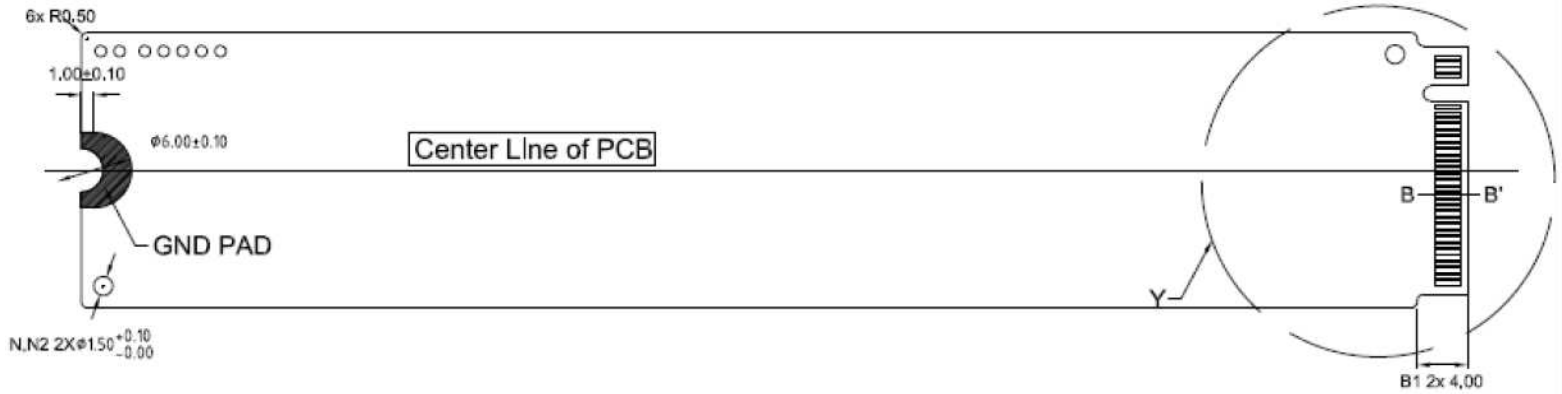
Figure 2-1: Sudden Power on-off operation

FTL Open time

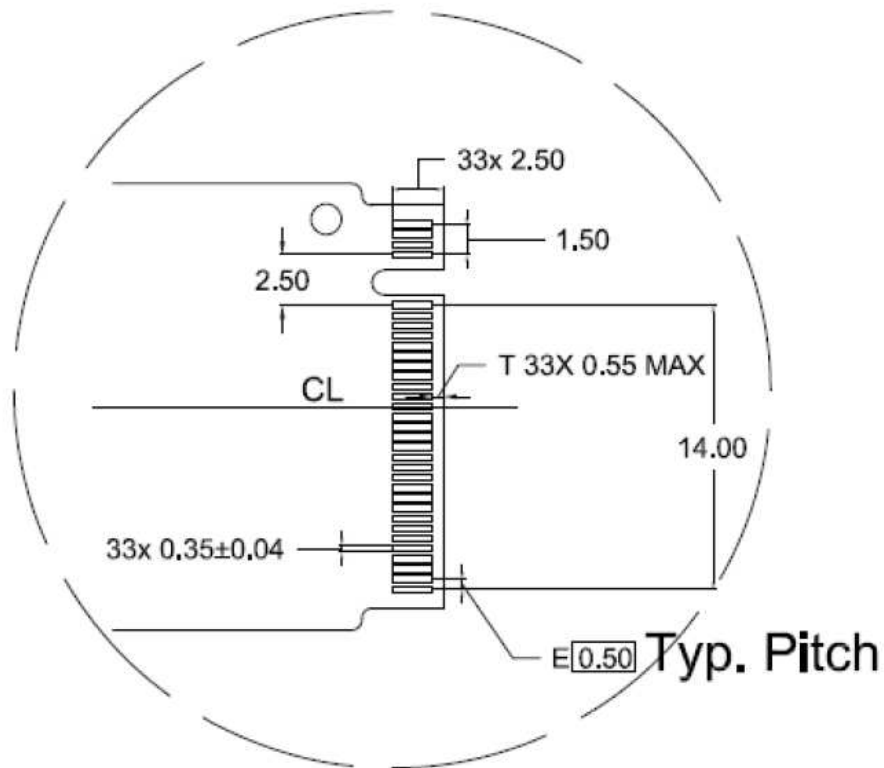
	960GB
<i>FTL open (ID read)</i>	30 sec

Figure 3-3: Dimension Details for M.2 card edge (Bottom View)

Bottom View



Detail Y



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3.3 M.2 SSD Weight

Table 3-1: M.2 SSD weight

Length	Weight	Unit of measure
110 mm	Up to 15	Grams

4 Pin and Signal Descriptions

4.1 Signal and Power Description Tables

Table 4-1: M.2 PCIE Connector Pinouts

Pin #	Assignment	Description	Pin #	Assignment	Description
1	GND	Return current path	2	3.3V	3.3V source
3	GND	Return current path	4	3.3V	3.3V source
5	PETn3	PCle TX	6	N/C	N/C
7	PETp3	PCle TX	8	N/C	N/C
9	GND	Return current path	10	LED1#	Device Active Signal
11	PERn3	PCle Rx	12	3.3V	3.3V source
13	PERp3	PCle Rx	14	3.3V	3.3V source
15	GND	Return current path	16	3.3V	3.3V source
17	PETn2	PCle TX	18	3.3V	3.3V source
19	PETp2	PCle TX	20	N/C	N/C
21	GND	Return current path	22	N/C	N/C
23	PERn2	PCle Rx	24	N/C	N/C
25	PERp2	PCle Rx	26	N/C	N/C
27	GND	Return current path	28	N/C	N/C
29	PETn1	PCle TX	30	N/C	N/C
31	PETp1	PCle TX	32	N/C	N/C
33	GND	Return current path	34	N/C	N/C
35	PERn1	PCle Rx	36	N/C	N/C
37	PERp1	PCle Rx	38	N/C	N/C
39	GND	Return current path	40	N/C	N/C
41	PETn0	PCle TX	42	N/C	N/C
43	PETp0	PCle TX	44	N/C	N/C
45	GND	Return current path	46	N/C	N/C
47	PERn0	PCle Rx	48	N/C	N/C
49	PERp0	PCle Rx	50	PERST#	PCle Reset
51	GND	Return current path	52	CLKREQ#	PCle Device Clock Request
53	REFCLKN	PCle Reference Clock	54	PEWake#	N/C
55	REFCLKP	PCle Reference Clock	56	N/C	N/C
57	GND	Return current path	58	N/C	N/C
67	N/C	N/C	68	SUSCLK	N/C
69	PEDET	N/C	70	3.3V	3.3V source
71	GND	Return current path	72	3.3V	3.3V source
73	GND	Return current path	74	3.3V	3.3V source
75	GND	Return current path			

5 PCIe and NVM Express Registers

5.1 PCI Express Registers

5.1.1 PCI Register Summary

Table 5-1: PCI Register Summary

Start Address	End Address	Name	Type
00h	3Fh	PCI Header	PCI Capability
40h	47h	PCI Power Management Capability	PCI Capability
50h	67h	MSI Capability	PCI Capability
70h	A3h	PCI Express Capability	PCI Capability
B0h	BBh	MSI-X Capability	PCI Capability
100h	12Bh	Advanced Error Reporting Capability	PCI Capability
148h	157h	Device Serial No Capability	PCI Capability
158h	167h	Power Budgeting Capability	PCI Capability
168h	17Bh	Secondary PCI Express Header	PCI Capability
188h	18Fh	Latency Tolerance Reporting (LTR)	PCI Capability
190h	19Fh	L1 Substates Capability Register	PCI Capability

5.1.2 PCI Header Registers

Table 5-2: PCI Header Register Summary

Start Address	End Address	Symbol	Description
00h	03h	ID	Identifiers
04h	05h	CMD	Command Register
06h	07h	STS	Device Status
08h	08h	RID	Revision ID
09h	0Bh	CC	Class Codes
0Ch	0Ch	CLS	Cache Line Size
0Dh	0Dh	MLT	Master Latency Timer
0Eh	0Eh	HTYPE	Header Type
0Fh	0Fh	BIST	Built in Self Test
10h	13h	MLBAR (BAR0)	Memory Register Base Address (lower 32-bit)

Start Address	End Address	Symbol	Description
14h	17h	MUBAR (BAR1)	Memory Register Base Address (upper 32-bit)
18h	1Bh	IDBAR (BAR2)	Index/Data Pair Register Base Address
1Ch	1Fh	BAR3	Reserved
20h	23h	BAR4	Reserved
24h	27h	BAR5	Reserved
28h	2Bh	CCPTR	CardBus CIS Pointer
2Ch	2Fh	SS	Subsystem Identifiers
30h	33h	EROM	Expansion ROM Base Address
34h	34h	CAP	Capabilities Pointer
35h	3Bh	R	Reserved
3Ch	3Dh	INTR	Interrupt Information
3Eh	3Eh	MGNT	Minimum Grant
3Fh	3Fh	MLAT	Maximum Latency

Table 5-3: Identifier Register

Bits	Type	Default Value	Description
31:16	RO	tbd	Device ID
0:15	RO	tbd	Vendor ID

Table 5-4: Command Register

Bits	Type	Default Value	Description
15:11	RO	0	Reserved
10	RW	0	Interrupt Disable
9	RO	0	Fast Back-to-Back Enable (N/A)
8	RW	0	SERR# Enable (N/A)
7	RO	0	Zero value
6	RW	0	Parity Error Response Enable
5	RO	0	VGA Palette Snooping Enable (N/A)
4	RO	0	Memory Write and Invalidate Enable (N/A)
3	RO	0	Special Cycle Enable (N/A)
2	RW	0	Bus Master Enable
1	RW	0	Memory Space Enable
0	RW	0	I/O Space Enable

Table 5-5: Device Status Register

Bits	Type	Default Value	Description
15	RW1C	0	Detected Parity Error
14	RW1C	0	N/A
13	RW1C	0	Received Master Abort
12	RW1C	0	Received Target Abort
11	RW1C	0	Signaled Target Abort
10:9	RO	0	N/A
8	RW1C	0	Master Data Parity Error Detected
7	RO	0	N/A
6	RO	0	Reserved
5	RO	0	N/A
4	RO	tbd	Capabilities List
3	RO	0	INTx Status
2:0	RO	0	Reserved

Table 5-6: Revision ID Register

Bits	Type	Default Value	Description
7:00	RO	tbd	Controller Hardware Revision ID

Table 5-7: Class Code Register

Bits	Type	Default Value	Description
23:16	RO	tbd	Base Class Code
15:08	RO	tbd	Sub Class Code
7:00	RO	tbd	Programming Interface

Table 5-8: Cache Line Size Register

Bits	Type	Default Value	Description
7:0	RW	0h	N/A

Table 5-9: Master Latency Timer Register

Bits	Type	Default Value	Description
7:00	RO	0	N/A

Table 5-10: Header Type Register

Bits	Type	Default Value	Description
7:00	RO	0	N/A

Table 5-11: Built-in Self Test Register

Bits	Type	Default Value	Description
7:00	RO	0	N/A

Table 5-12: Memory Register Base Address Lower 32-bits (BAR0) Register

Bits	Type	Default Value	Description
31:04	RW	0	Base Address
3	RO	0	Pre-Fetchable
2:1	RO	tbd	Address Type (64-bit)
0	RO	0	Memory Space Indicator (MEMSI)

Table 5-13: Memory Register Base Address Upper 32-bits (BAR1) Register

Bits	Type	Default Value	Description
31:0	RO	0	Base Address

Table 5-14: Index/Data Pair Register Base Address (BAR2) Register

Bits	Type	Default Value	Description
31:0	RO	0	Base Address

Table 5-15: BAR3 Register

Bits	Type	Default Value	Description
31:0	RO	0	Base Address