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Datasheet for:

SDHC/SDXC UHS104 SD Cards

VTSD3xxxxCxxxxxC

SD Cards for Client Applications

Legal Information

Revision History

Date	Revision	Description	Checked by
2/21/17	A	Initial release.	
3/31/17	B	Revised format	

Ordering Information for the SDHC/SDXC UHS104 SD Cards

VikingPart#	Interface	Temp	GB	Client/Ent	NAND
VTSD3032GCCBMTLC	SD Card	(0to+70'c)	32GB (SDHC)	Client	TSB 15nm MLC
VTSD3064GCCAMTLC	SD Card	(0to+70'c)	64GB (SDXC)	Client	TSB 15nm MLC
VTSD3128GCCZMTLC	SD Card	(0to+70'c)	128GB (SDXC)	Client	TSB 15nm MLC

Notes:
1. Contact Viking for availability date
2. The lowercase letters x,y and z are wildcard characters that indicate product or customer specific information
3. Refer to the Viking part number coversheet or PN decoder for details.

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1 Introduction

This data sheet describes the specifications of the SDHC/SDXC Standard Card with UHS104 SD Bus mode. The SDHC/SDXC Cards are a Memory Card of Small and Thin with SDMI compliant Security method. (SDMI: Secure Digital Music Initiative) Contents in the Card can be protected by CPRM based security. This contents security can be accomplished by SDHC/SDXC Card, host, and security application software combinations.

1.1 FEATURES

Table 1-1: Features

Media Format	
SD Memory Card Standard	Compliant with the SD Memory Card Standard Ver. 4.20, UHS104
Security Functions	SD Security Specification Ver.3.00 Compliant (CPRM Based) *CPRM: Contents Protection for Recording Media Specification
Logical Format	SD File System Specification Ver.3.00 Compliant SDHC Card = FAT32, SDXC Card = exFAT
Electrical Features	
Operating Voltage	VDD = 2.7V(min), 3.3V(Typ), 3.6V(max)
Operating Current	SDR104 Write : 140mA(max) SDR104 Read : 150mA(max)
SD Interface	DS : Signaling Voltage = 3.3V(Typ), SDCLK = 25MHz HS : Signaling Voltage = 3.3V(Typ), SDCLK = 50MHz
UHS-I Interface	UHS104 : Signaling Voltage = 1.8V(Typ), SDCLK = 208MHz UHS50 : Signaling Voltage = 1.8V(Typ), SDCLK = 100MHz@SDR100 / 50MHz@DDR50 Supported UHS-I bus modes are SDR104, SDR50, DDR50, SDR25, SDR12.
Physical Features	
Physical Package size /Mass	L: 32, W: 24, T: 2.1 (mm), Weight: 1.8g (typ.) SD Physical Layer Specification Ver.4.10 Compliant
Durability	Compliant with SD Physical Layer Specification Ver.4.10 and Standard Size SD Card Mechanical Addendum Version 4.10.
RoHS	Compliant with RoHS regulations (DIRECTIVE 2011/65/EU)
Performance Features	
Maximum access speed	Sequential Write = 75 MB/s Sequential Read = 95 MB/s
Speed Class	UHS Speed Class = U3 SD Speed Class = C10

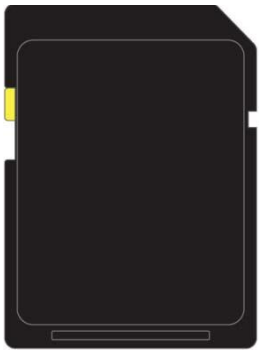

Figure 1-1: Top View

2 SD Card Standards Compatibility

This SD Memory Card Specification is compliant with:

- PHYSICAL LAYER SPECIFICATION Ver.4.20 (Part1)
  (Except for Mechanical Specification)
- FILE SYSTEM SPECIFICATION Ver.3.00. (Part2)
- SECURITY SPECIFICATION Ver.3.00. (Part3)
- Standard Size SD Card Mechanical Addendum Version 4.10

3 Physical Characteristics

3.1 Environmental Characteristics

The standard Operation Conditions are:

- Absolute Maximum Temperature Range — Ta = -25 to +85°C
- Humidity less than RH = 95 %, Non condensed — Ta = 25°C

The standard Storage Conditions are:

- Maximum Temperature Range: — Tstg = -40 to +85°C
- Humidity less than RH = 93%, Non condensed — Ta = 40°C

3.2 Physical Characteristics

Mechanical Write Protect Switch

A mechanical sliding tab on the side of the card can be used as a write protect switch. The host system shall be responsible for this function.

The card is in a “Write Protected” status when the tab is located on the “Lock “ position. The host system shall not write nor format the card in this status.

The card is in “Write Enabled” status when the tab is moved to the opposite position (Un-Lock). (Please refer the figures below for the tab polarity.)

Please slide the tab until a dead end (stopped position). The tab is set on the “Write Enabled” position when it is shipped.

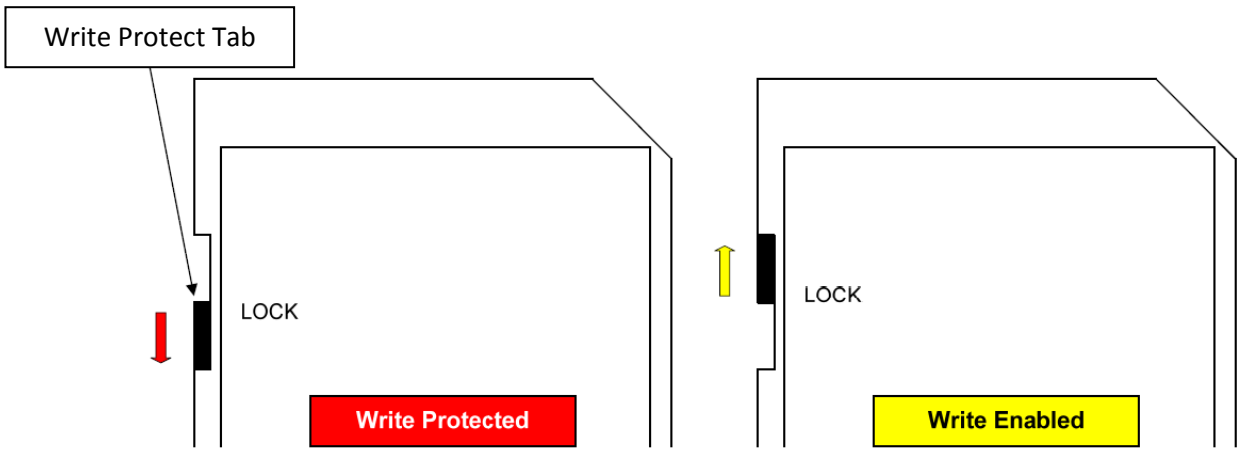

Figure 3-1: Write Protect Tab Polarity (Front View)

4 Electrical Interface

4.1 Pin Assignment

The table below describes the pin assignment of the SD card. The following figure describes the pin assignment of the SD card. Please refer the detail descriptions by SD Card Physical Layer Specification.

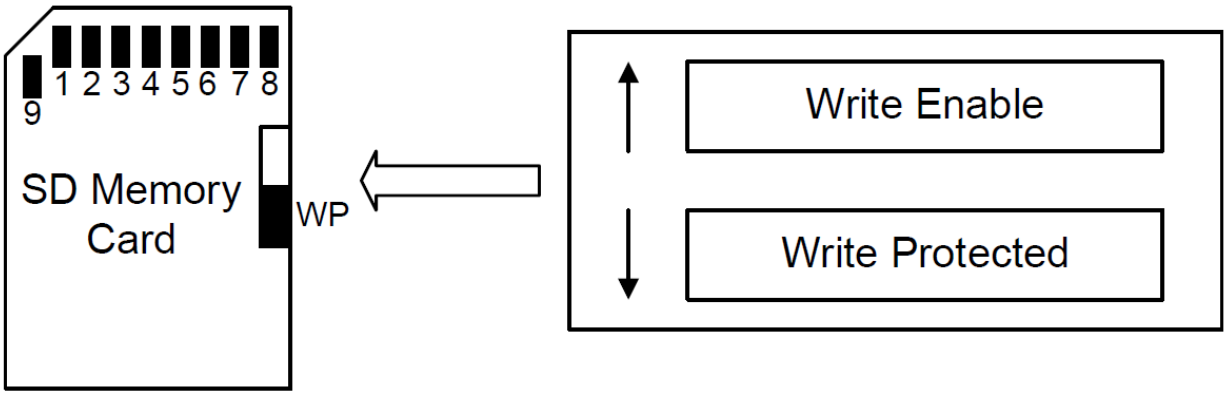

Figure 4-1: SD Card Pin Assignment (Back view of the Card)

Table 4-1: SD Card Pin Assignment

	SD Mode			SPI Mode		
Pin	**Name**	**IO Type**	**Description**	**Name**	**IO Type**	**Description**
1	CD/ DAT3	I/O/ PP	Card Detect/ Data Line[Bit3]	CS	I	Chip Select (Negative True)
2	CMD	PP	Command/Response	DI	I	Data In
3	V_{SS1}	S	Ground	V_{SS}	S	Ground
4	V_{DD}	S	Supply Voltage	V_{DD}	S	Supply Voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS2}	S	Ground	V_{SS2}	S	Ground
7	DAT0	I/O/PP	Data Line[Bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line[Bit1]	RSV	–	Reserved(*)
9	DAT2	I/O/PP	Data Line[Bit2]	RSV	–	Reserved(*)

Notes:
S: Power Supply
I: Input
O: Output using push-pull drivers
PP: I/O using push-pull drivers
(*) These signals should be pulled up by host side with 10-100k ohm resistance in the SPI Mode.

4.2 SD Card Bus Topology

The device supports two alternative communication protocols: SD and SPI Bus Mode. It is as same as standard SD memory card. Host System can choose either one of modes. Same Data of the device can read and write by both modes. SD Mode allows the 4-bit high performance data transfer. SPI Mode allows easy and common interface for SPI channel. The disadvantage of this mode is loss of performance, relatively to the SD mode.

4.2.1 SD Bus Mode protocol

The SD bus allows the dynamic configuration of the number of data line from 1 to 4 Bi-directional data signal. After power up by default, the Device will use only DAT0. After initialization, host can change the bus width. Multiplied SD cards connections are available to the host. Common VDD, VSS and CLK signal connections are available in the multiple connections. However, Command, Respond and Data lined (DAT0-DAT3) shall be divided for each card from host. This feature allows easy tradeoff between hardware cost and system performance. Communication over the SD bus is based on command and data bit stream initiated by a start bit and terminated by stop bit.

Command:

Commands are transferred serially on the CMD line. A command is a token to starts an operation from host to the card. Commands are sent to an addressed single card (addressed Command) or to all connected cards (Broad cast command).

Response:

Responses are transferred serially on the CMD line. A response is a token to answer to a previous received command. Responses are sent from an addressed single card or from all connected cards.

Data:

Data can be transfer from the card to the host or vice versa. Data is transferred via the data lines.

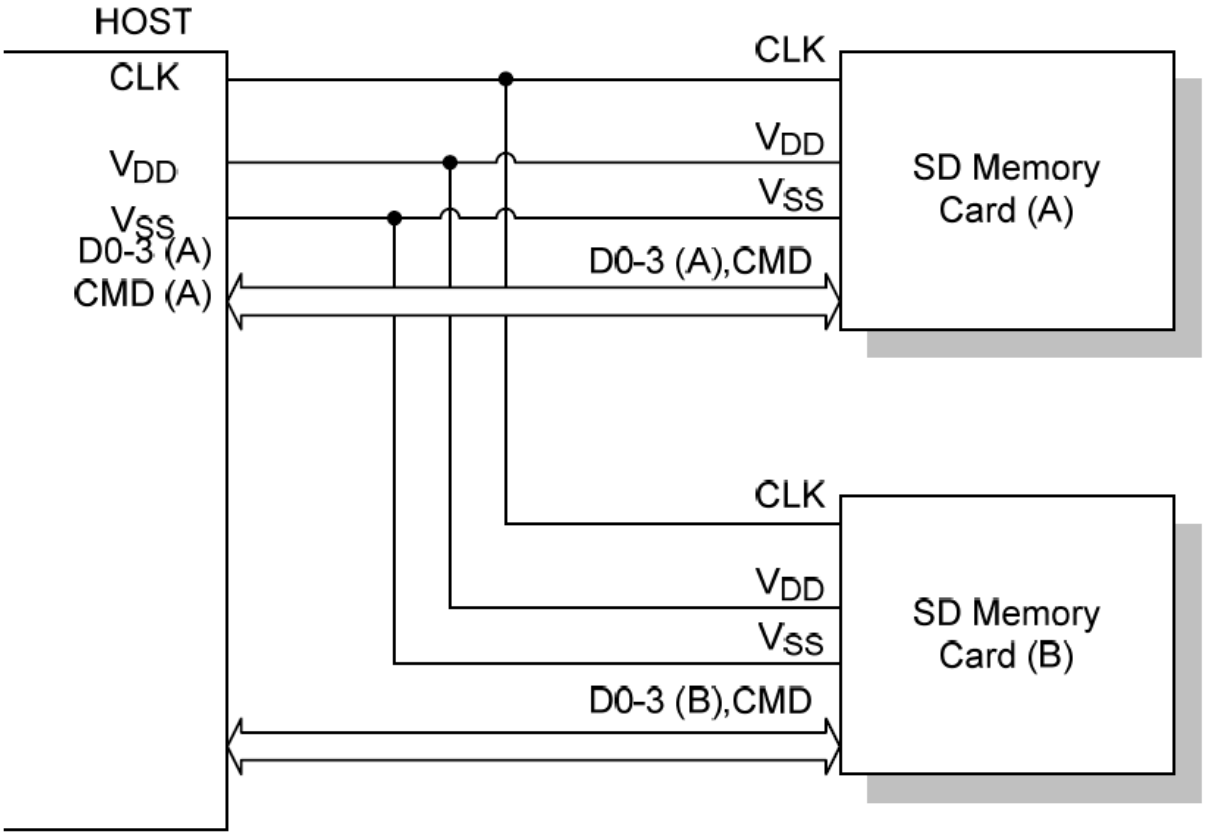

Figure 4-2: Bus Connection Diagram (SD Mode)

CLK	Host card Clock signal
CMD	Bi-directional Command/ Response Signal
DAT0 - DAT3	4 Bi-directional data signal
VDD	Power supply
VSS	GND

Table 4-2: SD Mode Command Set (+ = Implemented, - = Not Implemented)

CMD Index	Abbreviation	Implementation	Note
CMD0	GO_IDLE_STATE	+	
CMD2	ALL_SEND_CID	+	
CMD3	SEND_RELATIVE_ADDR	+	
CMD4	SET_DSR	-	DSR Register is not implemented.
CMD6	SWITCH_FUNC	+	
CMD7	SELECT/DESELECT_CARD	+	
CMD8	SEND_IF_COND	+	
CMD9	SEND_CSD	+	
CMD10	SEND_CID	+	
CMD11	VOLTAGE_SWITCH	+	UHS-I mode

CMD Index	Abbreviation	Implementation	Note
CMD12	STOP_TRANSMISSION	+	
CMD13	SEND_STATUS	+	
CMD15	GO_INACTIVE_STATE	+	
CMD16	SET_BLOCKLEN	+	
CMD17	READ_SINGLE_BLOCK	+	
CMD18	READ_MULTIPLE_BLOCK	+	
CMD19	SEND_TUNING_PATTERN	+	UHS-I mode
CMD20	SPEED_CLASS_CONTROL	+	
CMD23	SET_BLOCK_COUNT	+	
CMD24	WRITE_BLOCK	+	
CMD25	WRITE_MULTIPLE_BLOCK	+	
CMD26	Reserved for Manufacturer	+	
CMD27	PROGRAM_CSD	+	
CMD28	SET_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD29	CLR_WRITE_PROT	-	
CMD30	SEND_WRITE_PROT	-	
CMD32	ERASE_WR_BLK_START	+	
CMD33	ERASE_WR_BLK_END	+	
CMD38	ERASE	+	
CMD42	LOCK_UNLOCK	+	
CMD55	APP_CMD	+	
CMD56	GEN_CMD	+	This command is not specified.
CMD60	Reserved for Manufacturer	+	
CMD61	Reserved for Manufacturer	+	
CMD62	Reserved for Manufacturer	+	
ACMD6	SET_BUS_WIDTH	+	
ACMD13	SD_STATUS	+	
ACMD22	SEND_NUM_WR_BLOCKS	+	
ACMD23	SET_WR_BLK_ERASE_COUNT	+	
ACMD41	SD_SEND_OP_COND	+	1.8V Signaling and XPC (SDXC Power Control) support
ACMD42	SET_CLR_CARD_DETECT	+	
ACMD51	SEND_SCR	+	
ACMD18	SECURE_READ_MULTI_BLOCK	+	
ACMD25	SECURE_WRITE_MULTI_BLOCK	+	
ACMD26	SECURE_WRITE_MKB	+	
ACMD38	SECURE_ERASE	+	
ACMD43	GET_MKB	+	
ACMD44	GET_MID	+	
ACMD45	SET_CER_RN1	+	
ACMD46	GET_CER_RN2	+	
ACMD47	SET_CER_RES2	+	
ACMD48	GET_CER_RES1	+	
ACMD49	CHANGE_SECURE_AREA	-	

Notes:

- CMD28, 29 and CMD30 are optional commands.
- CMD4 is not implemented because DSR register (Optional Register) is not implemented.
- CMD56 is a vender specific command which is not defined in the standard card.

6.2.2 SPI Bus mode Protocol

The SPI bus allows 1 bit Data line by 2-chanel (Data In and Out). The SPI compatible mode allows the MMC Host systems to use SD card with little change. The SPI bus mode protocol is byte transfers. All the data token are multiples of the bytes (8-bit) and always byte aligned to the CS signal.

The advantage of the SPI mode is reducing the host design effort. Especially, the MMC host can be modified with little change. The disadvantage of the SPI mode is the loss of performance versus SD mode.

Caution: Please use SD Card Specification. DO NOT use MMC Specification. (For example, initialization is achieved by ACMD41, and be careful to Register. Register definition is different, especially CSD Register.)

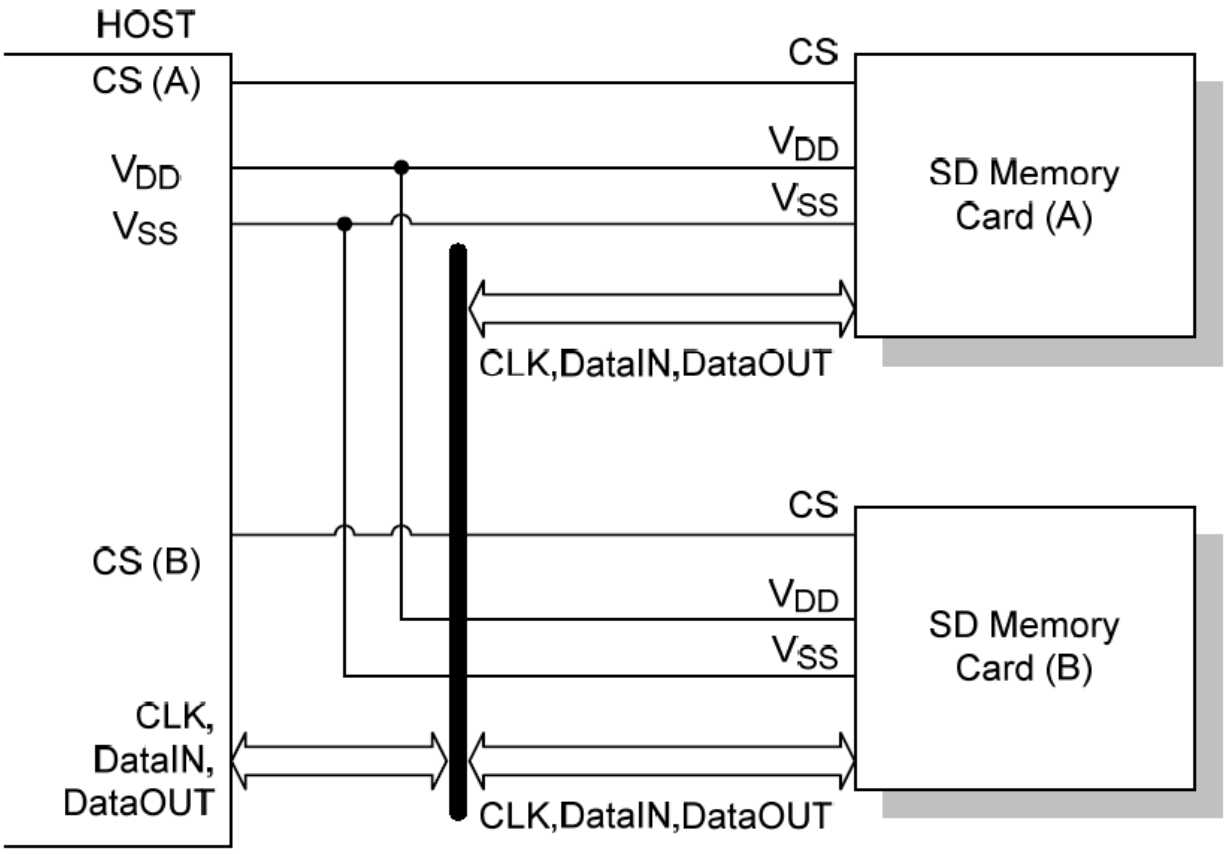

Figure 4-3: Bus Connection Diagram (SPI Mode)

CS	Card Select Signal
CLK	Host card Clock signal
CMD	Bi-directional Command/ Response Signal
DataIN	Host to card data line
DataOUT	Host to card data line
VDD	Power supply
VSS	GND

Table 4-3: SPI Mode Command Set (+ = Implemented, - = Not Implemented)

CMD Index	Abbreviation	Implementation	Note
CMD0	GO_IDLE_STATE	+	
CMD1	SEND_OP_COND	+	
CMD6	SWITCH_FUNC	+	
CMD8	SEND_IF_COND	+	
CMD9	SEND_CSD	+	
CMD10	SEND_CID	+	
CMD12	STOP_TRANSMISSION	+	
CMD13	SEND_STATUS	+	
CMD16	SET_BLOCKLEN	+	

CMD Index	Abbreviation	Implementation	Note
CMD17	READ_SINGLE_BLOCK	+	
CMD18	READ_MULTIPLE_BLOCK	+	
CMD24	WRITE_BLOCK	+	
CMD25	WRITE_MULTIPLE_BLOCK	+	
CMD26	Reserved for Manufacturer	+	
CMD27	PROGRAM_CSD	+	
CMD28	SET_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD29	CLR_WRITE_PROT	-	
CMD30	SEND_WRITE_PROT	-	
CMD32	ERASE_WR_BLK_START	+	
CMD33	ERASE_WR_BLK_END	+	
CMD38	ERASE	+	
CMD42	LOCK_UNLOCK	+	
CMD55	APP_CMD	+	
CMD56	GEN_CMD	+	This command is not specified.
CMD58	READ_OCR	+	
CMD59	CRC_ON_OFF	+	
CMD60	Reserved for Manufacturer	+	
ACMD13	SD_STATUS	+	
ACMD22	SEND_NUM_WR_BLOCKS	+	
ACMD23	SET_WR_BLK_ERASE_COUNT	+	
ACMD41	SD_SEND_OP_COND	+	
ACMD42	SET_CLR_CARD_DETECT	+	
ACMD51	SEND_SCR	+	
ACMD18	SECURE_READ_MULTI_BLOCK	+	
ACMD25	SECURE_WRITE_MULTI_BLOCK	+	
ACMD26	SECURE_WRITE_MKB	+	
ACMD38	SECURE_ERASE	+	
ACMD43	GET_MKB	+	
ACMD44	GET_MID	+	
ACMD45	SET_CER_RN1	+	
ACMD46	GET_CER_RN2	+	
ACMD47	SET_CER_RES2	+	
ACMD48	GET_CER_RES1	+	

Notes:

- CMD28, 29 and CMD30 are optional commands.
- CMD56 is a vender specific command which is not defined in the standard card.

4.3 Initialization

The following figures show the initialization flow chart for UHS-I hosts and the sequence of commands to perform a signal voltage switch. Red and yellow boxes are new procedures to initialize the UHS-I card.

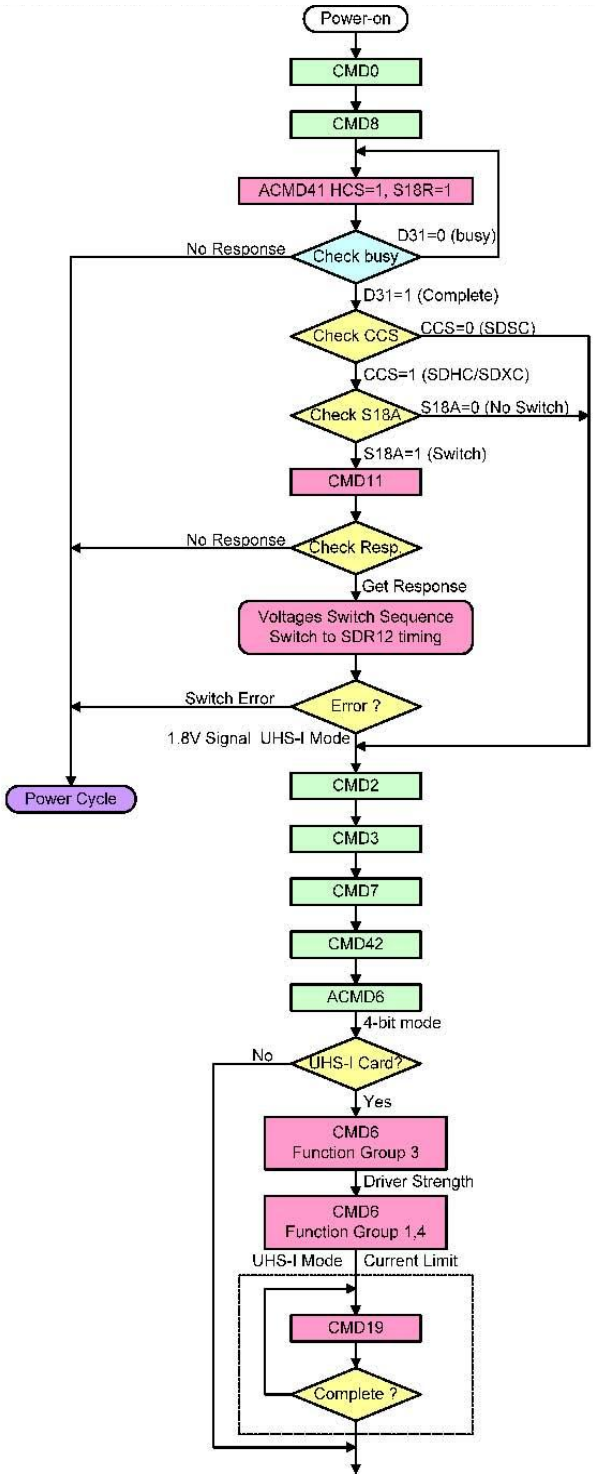

Figure 4-4: UHS-I Host Initialization Flow Chart

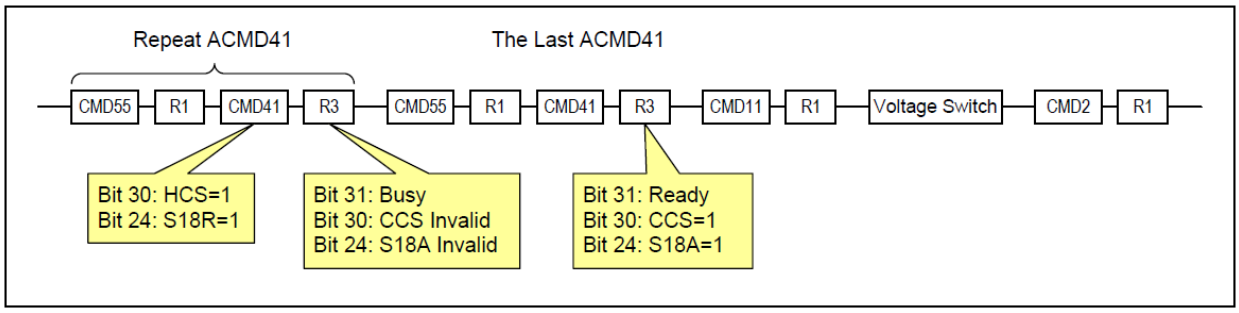

Figure 4-5: ACMD41 Timing Followed by Signal Voltage Switch Sequence

1) POWER ON: Supply Voltage for initialization.

Host System applies the perating Voltage to the card. Apply more than 74 cycles of Dummy-clock to the SD card.

2) Select operation mode (SD mode or SPI mode)

In the case of SPI mode operation, the host should drive pin 1 (CD/DAT3) of the SD Card I/F to a “Low” level. Then, issue CMD0. In the case of SD mode operation, the host should drive or detect pin 1 of the SD Card I/F (Pull up register of pin 1 is pull up to “High” normally). The card maintains selected operation mode except re-issue of CMD0 or power on below is SD mode initialization procedure.

3) Send Interface condition command (CMD8).

When the card is in the Idle state, the host shall issue CMD8 before ACMD41. In the argument, 'voltage supplied' is set to the host supply voltage and 'check pattern' is set to any 8-bit pattern. The card that accepted the supplied voltage returns R7 response. In the response, the card echoes back both the voltage range and check pattern set in the argument. If the card does not support the host supply voltage, it shall not return response and stays in the Idle state.

4) Send initialization command (ACMD41).

When the signaling level is 3.3V, the host repeats an issue ACMD41 with HCS=1 and S18R=1 until the response indicates ready. The argument (HCS and S18R) of the first ACMD41 is effective but the all the following ACMD41 should be issued with the same argument. If Bit 31 indicates ready, the host needs to check CCS and S18A. The card indicates S18A=0, which means that the voltage switch is not allowed and the host needs to use the current signaling level.

Table 4-4:S18R and S18A Combinations

Current Signaling Level	18R	S18A	Comment
3.3V	0	0	1.8V signaling is not requested
	1	0	The card does not support 1.8V signaling
	1	1	Start signal voltage switch sequence
1.8V	X	0	Already switched to 1.8V

5) Send voltage switch command (CMD11)

S18A=1 means that the voltage switch is allowed and host issues CMD11 to invoke voltage switch sequence. By receiving CMD11, the card returns R1 response and start voltage switch sequence. No response of CMD11 means that S18A was 0 and therefore the host should not have sent CMD11. Completion of voltage switch sequence is checked by high level of DAT[3:0]. Any bit of DAT[3:0] can be checked depends on ability of the host. The card enters UHS-I mode and card input and output timings are changed (SDR12 in default) when the voltage switch sequence is completed successfully.

6) Send ALL_SEND_CID command (CMD2) and get the Card ID (CID)

7) Send SEND_RELATIVE_ADDR (CMD3) and get the RCA.
RCA value is randomly changed by access, not equal zero.

8) Send SELECT / DESELECT_CARD command (CMD7) and move to the transfer state.
When entering tran state, CARD_IS_LOCKED status in the R1 response should be checked (it is indicated in the response of CMD7). If the CARD_IS_LOCKED status is set to 1 in the response of CMD7, CMD42 is required before ACMD6 tounlock the card. (If the card is locked, CMD42 is required to unlock the card.) If the card is unlocked, CMD42 can be skipped.

9) Send SET_BUS_WIDTH command (ACMD6).
UHS-I supports only 4-bit mode. Host shall select 4-bit mode by ACMD6. If the card is locked, host needs to unlock the card by CMD42 in 1-bit mode and then needs to issue ACMD6 to change 4-bit bus mode. Operating in 1-bit mode is not assured.

10) Set driver strength.
CMD6 mode 0 is used to query which functions the card supports, and to identify the maximum current consumption of the card under the selected functions. In case of UHS-I card, appropriate driver strength (default is Type-B buffer) is selected by CMD6 Function Group 3.

11) Set UHS-I mode current limit.
UHS-I modes (Bus Speed Mode) is selected by CMD6 Function Group 1. Current limit is selected by CMD6 Function Group 4.

Maximum access settings: SDR104 = (CMD6 Function Group 1 = 3-h, CMD6 Function Group 4 = 0-h(*)) SDR50 = (CMD6 Function Group 1 = 2-h, CMD6 Function Group 4 = 0-h(*)) DDR50 = (CMD6 Function Group 1 = 4-h, CMD6 Function Group 4 = 0-h(*)) (*) The Current Limit is default value (200mA).

Note:

Function Group 4 is defined as Current Limit switch for SDR50, SDR104. The Current Limit does not act on the card in SDR12 and SDR25. The default value of the Current Limit is 200mA (minimum setting). Then after selecting one of SDR50, SDR104 mode by Function Group 1, host needs to change the Current Limit to enable the card to operate in higher performance. This value is determined by a host power supply capability to the card, heat release method taken by a host and the maximum current of a connector.

12) Tuning of sampling point

CMD19 sends a tuning block to the host to determine sampling point. In SDR50 and SDR104 modes, if tuning of sampling point is required, CMD19 is repeatedly issued until tuning is completed. Then the Host can access the Data between the SD card as a storage device.

Application Notes:

1.The host shall set ACMD41 timeout to more than 1 second to abort repeat of issuing ACMD41 when the card does not indicate ready. The timeout count starts from the first ACMD41 which is set voltage window in the argument.

2.Once the signal voltage is switched to 1.8V, the card continues 1.8V signaling regardless of CMD0. Power cycle resets the signal voltage to 3.3V. After switching 1.8V singling, the card cannot be changed to SPI mode.

3.Timing to Switch Signal Voltage To change signaling level at the same time between host and card, signal voltage switch sequence is invoked by CMD11 as shown in the figure below. CMD11 is issued only when S18A=1 in the response of ACMD41.

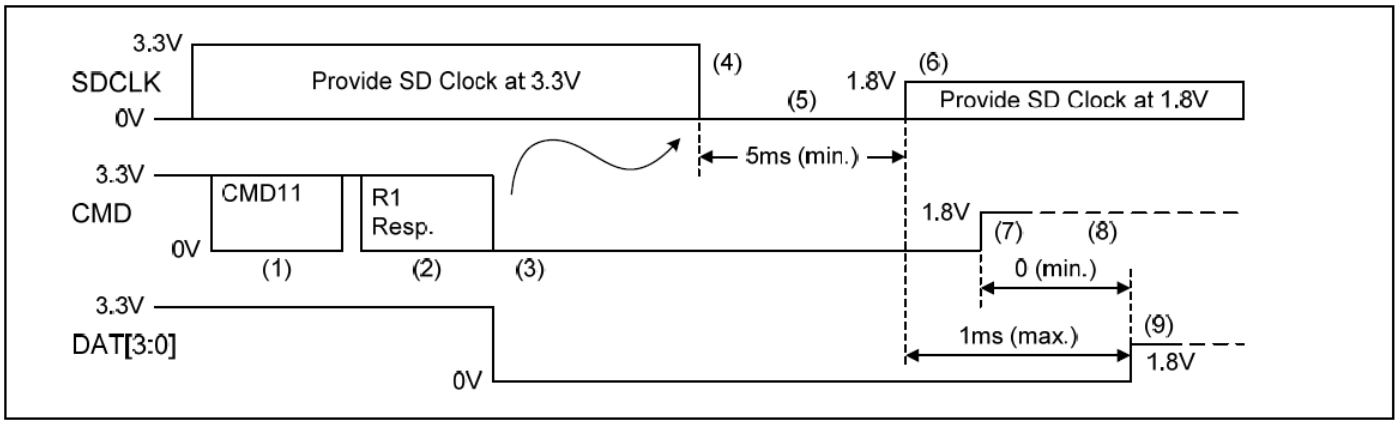

Figure 4-6: Signal Voltage Switch Sequence

Steps that the host takes to start a voltage switch sequence.

1. The host issues CMD11 to start voltage switch sequence.
2. The card returns R1 response.
3. The card drives CMD and DAT[3:0] to “low” immediately after the response.
4. The host stops supplying SDCLK. The card shall start switching voltage after host stops SDCLK. The time to stop SDCLK is not specified. The host can detect whether the sequence starts by checking signal level of either one of CMD, DAT[3:0]. What signal should be checked will depend on the ability of the host. If low level is not detected, the host should abort the sequence and execute power cycle.

5. 1.8V output of voltage regulator in card shall be stable within 5ms.The Host keeps SDCLK low at least 5ms. This means that 5ms is the maximum for the card and the minimum for the host.
6. After 5ms from (step 4) and host voltage regulator is stable, the host starts providing SDCLK at 1.8V. The card can check whether SDCLK voltage is 1.8V.
7. By detecting SDCLK, the card drives CMD to high at 1.8V for at least one clock and then stops driving (tri-state). CMD is triggered by rising edge of SDCLK (SDR timing).
8. The card can check whether host drives CMD to 1.8V through the host pull-up resister.
9. If switching to 1.8V signaling is completed successfully, the card drives DAT[3:0] to high at 1.8V at least one clock and then stop driving (tri-state). DAT[3:0] is triggered by rising edge of SDCLK (SDR timing). DAT[3:0] shall be high within 1ms from start of providing SDCLK. Host check whether DAT[3:0] is high after 1ms from supplying SDCLK. This means that 1ms is the maximum for the card and the minimum for the host.

4.4 Electrical Characteristics

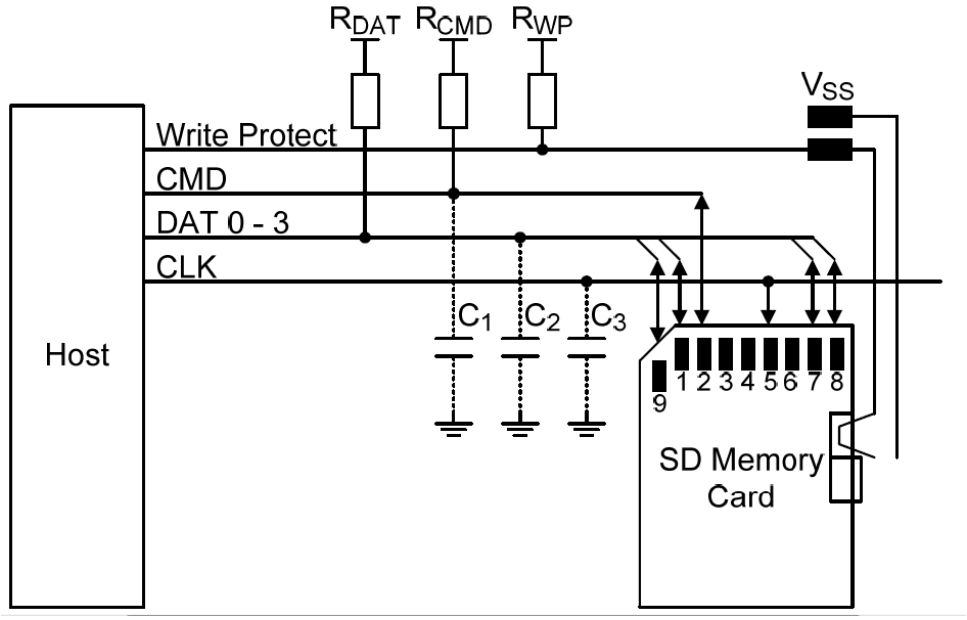

Figure 4-7: SD Card Connection Diagram

4.4.1 Absolute Maximum Conditions

Table 4-5: Absolute Maximum Conditions

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to 3.9	V
Input Voltage	V_{IN}	-0.3 to V_{DD}+0.3 (≤3.9)	V

4.4.2 DC Characteristics

Table 4-6: DC Characteristics

Item	Symbol	Condition	MIN.	Typ.	MAX.	Unit	Note
Supply Voltage	V_{DD}	-	2.7	-	3.6	V	

Item			Symbol	Condition	MIN.	Typ.	MAX.	Unit	Note
3.3V Signaling	Input Voltage	High Level	V_{IH}		V_{DD}*0.625	-	-	V	
		Low Level	V_{IL}		-	-	V_{DD}*0.25	V	
	Output Voltage	High Level	V_{OH}	I_{OH} = -2mA	V_{DD}*0.75	-	-	V	
		Low Level	V_{OL}	I_{OL} = 2mA	-	-	V_{DD}*0.125	V	
1.8V Signaling	Input Voltage	High Level	V_{IH}	-	1.27		2	V	
		Low Level	V_{IL}		-	-	0.58	V	
	Output Voltage	High Level	V_{OH}	I_{OH} = -2mA	1.4	-	-	V	
		Low Level	V_{OL}	I_{OL} = 2mA	-	-	0.45	V	
Standby Current		32GB	I_{CCS}	V_{DD} = 3.6V Clock Stop	-	-	400	uA	Ta=25℃
		64GB			-	-	450		
		128GB			-	-	650		
Operation Read Current (peak)		32GB 64GB 128GB	I_{CCOP11}	SDR104 Current Limit = 200mA, 400mA V_{DD}= 3.6V	-	-	170	mA	Ta=25℃
				SDR50 Current Limit = 200mA, 400mA V_{DD} = 3.6V	-	-	155		
				DDR50 Current Limit = 200mA, 400mA V_{DD} = 3.6V	-	-	155		
				SDR25, HS V_{DD} = 3.6V	-	-	135		
				SDR12, DS V_{DD} = 3.6V	-	-	125		

Item			Symbol	Condition	MIN.	Typ.	MAX.	Unit	Note
Operation Write Current (peak)		32GB 64GB 128GB	$I_{CCOP1\ 1}$	SDR104 Current Limit = 200mA, 400mA V_{DD}= 3.6V	-	-	220	mA	Ta=25℃
				SDR50 Current Limit = 200mA, 400mA V_{DD} = 3.6V	-	-	205		
				DDR50 Current Limit = 200mA, 400mA V_{DD} = 3.6V	-	-	205		
				SDR25, HS V_{DD} = 3.6V	-	-	145		
				SDR12, DS V_{DD} = 3.6V	-	-	140		
Operation Read Current (average)	32GB 64GB 128GB		$I_{CCOP2\ 2}$	SDR104 Current Limit = 200mA, 400mA V_{DD}= 3.6V	-	-	130	mA	Ta=25℃
				SDR50 Current Limit = 200mA, 400mA V_{DD} = 3.6V	-	-	100		
				DDR50 Current Limit = 200mA, 400mA V_{DD} = 3.6V	-	-	95		
				SDR25, HS V_{DD} = 3.6V	-	-	80		
				SDR12, DS V_{DD} = 3.6V	-	-	70		

Item			Symbol	Condition	MIN.	Typ.	MAX.	Unit	Note
				SDR104 Current Limit = 200mA, 400mA V_{DD}= 3.6V	-	-	145	mA	Ta=25℃
				SDR50 Current Limit = 200mA, 400mA V_{DD} = 3.6V	-	-	115		
				DDR50 Current Limit = 200mA, 400mA V_{DD} = 3.6V	-	-	110		
				SDR25, HS V_{DD} = 3.6V	-	-	90		
Operation Write Current (average)	32GB 64GB 128GB		$I_{CCOP2\ 2}$	SDR12, DS V_{DD} = 3.6V	-	-	75		

Notes: Peak Current RMS value over a 10usec period. 2) Average Current value over 1second period.

Table 4-7: Bus Operating Conditions - Signal Line's Load

Parameter	Symbol	Min.	Max.	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	kΩ	To prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card C_{HOST}+C_{BUS} shall not exceed 30 pF
Card capacitance for each signal pin	C_{CARD}		10	pF	
Maximum signal line inductance			16	nH	
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	kΩ	May be used for card detection
Capacity Connected to Power Line	C_C		5	uF	To prevent inrush current